Improving radiation tolerance in e2v CCD sensors

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ABSTRACT

e2v have been developing new approaches to mitigate against the effects of radiation damage in CCD sensors. The first of these is our "rad-hard" device technology, primarily developed to reduce the flat-band voltage shift following ionising radiation. With this technology a very significant improvement has been demonstrated, the flat-band shift reducing from typically 100-200 mV/kRad(Si) with standard devices to only 6 mV/kRad(Si), plus an associated reduction in the increase in surface dark signal. The rad-hard process thereby allows devices to be operated in environments with at least 500kRad total dose and/or with reduced shielding.

Developments aimed at reducing the impact of proton radiation have included the manufacture of p-channel devices. Our initial data indicates that at -50°C the increase in charge transfer inefficiency is reduced by a factor of two times for parallel transfer and five times for serial transfer.

Keywords: CCD, Radiation damage, Flat-band shift, Process improvement, p-channel

1. INTRODUCTION

The charge-coupled device (CCD) is vulnerable to radiation-induced performance changes. These may be divided as follows.

- Those due to the total ionising dose, primarily from charged particles, X-rays and γ–rays, causing charging of the gate dielectric and a build-up on interface states.
- Displacement damage, largely arising from heavy particles such as protons and neutrons, causing defects in the crystal lattice with consequent build-up of bulk traps.

These effects are discussed separately.

2. IONISING DAMAGE

Ionising radiation generates electron-hole pairs in the gate dielectric between the electrodes and the underlying silicon. For radiation having an adsorption length of more than a few microns the generation can be considered uniform per unit depth.

2.1 Charge build-up

The consequences of this generation regarding charge build-up are shown in Figure 1 for an oxide dielectric under positive and negative gate bias [1].

Under positive bias the electrons are highly mobile and move towards and through the gate material and are lost to the system. The holes are less mobile and move away from the gate eventually becoming trapped close to the Si-SiO_2 interface (somehow the atomic structure does not allow further motion into the silicon). If the trapped holes are represented as a sheet of charge Q C/cm^2, then the change of flat-band voltage

change is given by $\Delta V_{fb} = -Qx/\varepsilon$, where x is the distance from the gate electrode and ε is the dielectric constant. Since the quantity of charge Q is also dependent on the thickness x, ΔV_{fb} is therefore dependent on x^2. Thin dielectrics therefore show least change.

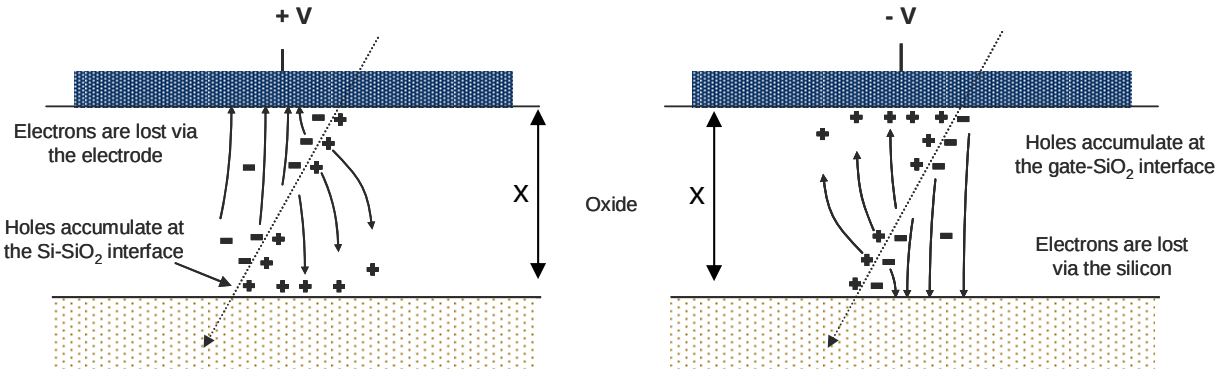

Fig 1: Effect of bias on movement of radiation-induced charge in oxide-only MOS

Under negative bias the electrons now move towards and into the silicon and are again lost from the system. The holes move towards the gate and become trapped in a layer close to the electrode. However, as the distance x is now small, the ΔV_{fb} change is also small, much smaller than for positive bias.

Many CCD manufacturers used a mixed gate dielectric with a layer of silicon nitride on top of the oxide as this facilitates maintaining the same overall thickness when fabricating the multiple layers of polysilicon used for the electrodes. The consequences for ionisation-generated electron-hole pairs [1] are shown in Figure 2.

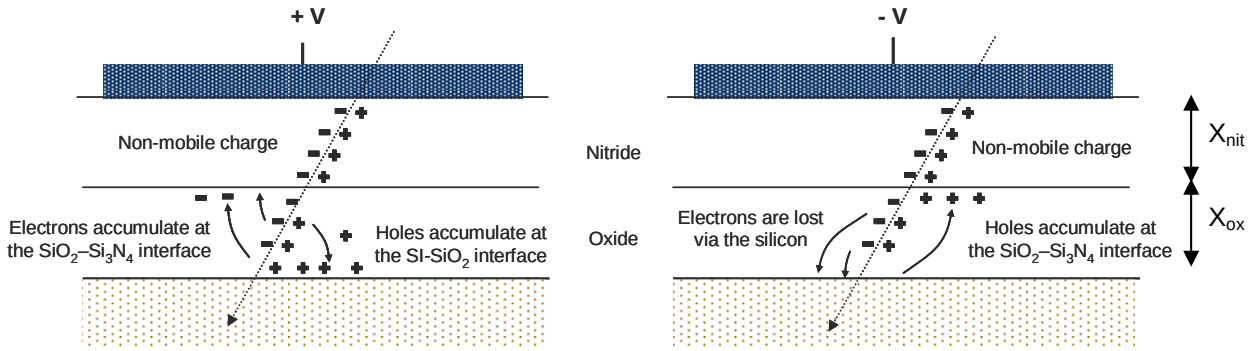

Fig 2: Effect of bias on movement of radiation-induced charge in oxide-nitride MOS

Within the nitride layer the mobilities of electrons and holes are relatively low and much of the charge is likely to recombine.

Under positive bias the holes generated in the oxide layer move towards the Si-SiO_2 interface and become trapped. The corresponding electrons move towards the oxide-nitride interface and also become trapped. The situation at this interface is however complex and some of the electrons may be able to tunnel into the nitride and recombine with holes. It is therefore difficult to predict the resulting flat-band voltage shift.

Under negative bias the electrons generated in the oxide layer now move towards the Si-SiO_2 interface and are lost. The corresponding holes move towards the oxide-nitride interface and become trapped. Thus the shift is $\Delta V_{fb} = -Qx_{nit}/\varepsilon_{nit}$. Since the quantity of charge Q will be dependent on the oxide thickness x_{ox}, ΔV_{fb} should be proportional to the product ($x_{ox}.x_{nit}$), and of a value higher than that obtained under equivalent positive bias.

Actual flat-band voltage shifts measured for e2v devices with standard gate dielectrics are shown in Figure 3, together with values obtained with an equivalent oxide-only dielectric. It may be noted that with the oxide-nitride layer the shift under positive bias is a little lower than under negative bias, as suggested above, but to a good approximation it can be assumed that the shifts are roughly equal. This is not the case with the oxide-only dielectric; the shift under negative bias is smaller than oxide-nitride, whereas that under positive bias is much higher. In either case the shift under zero bias is always relatively small as most of the generated carriers are likely to recombine.

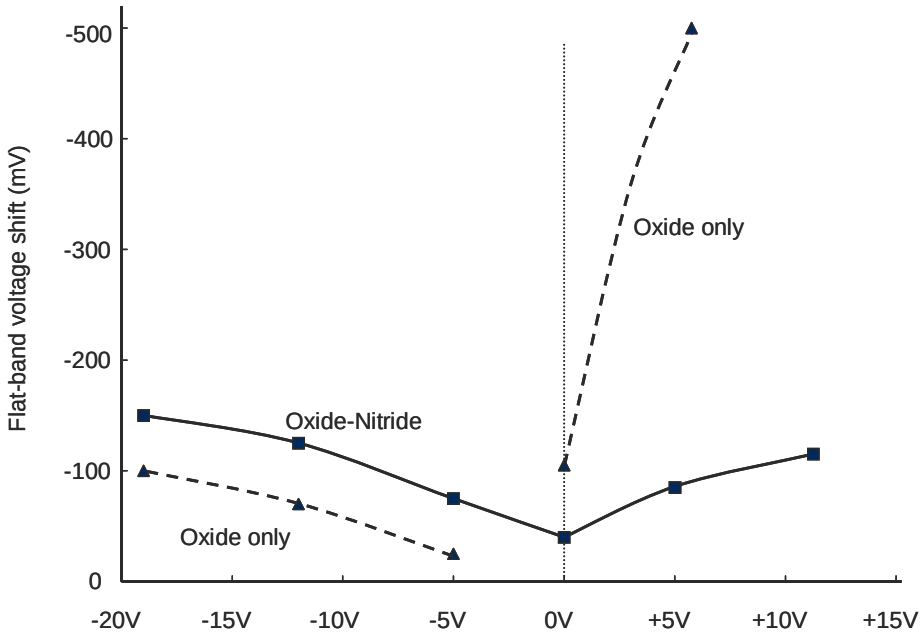

Fig 3: Flat-band shift of a standard dielectric compared with oxide-only equivalent

Note that in the case of an n-channel CCD, even though an electrode may be biased at a positive voltage with respect to the substrate, the gate is actually at a negative voltage with respect to the potential maximum in the underlying channel. However, the gate can be at a positive voltage with respect to isolation regions, e.g. p-type channel stops. The polarities are of course reversed in the case of a p-channel CCD. Note also that with the standard MOS sign convention, a flat-band voltage shift given as $-\Delta V_{fb}$ volts is equivalent in effect to the gate voltage having being changed by $+\Delta V_{fb}$ volts. For convenience the ΔV_{fb} values are given in this paper as only the magnitudes, but the shifts are actually all negative voltages (as is shown in Figure 3).

2.2 Interface trapping-state build-up

A generation-recombination centre, usually described as a “trap” or “trapping state”, is a result of any imperfection within the silicon that reduces the binding energy of an electron to below that in the regular lattice. Surface or interface traps are due to the inherent atomic mismatch between silicon and silicon dioxide. The mismatch results in unpaired electrons, described as “dangling bonds”. The binding energy of

these electrons is below that of the lattice, thus the sites behave as traps with energy levels that are distributed right across the band gap. In normal device operation the silicon surface is depleted and the traps cause the generation of dark signal, with those at about mid-band being most active.

In the early days of MOS technology using polysilicon gates (early 1970s), it was found that the transistors were less stable than earlier devices using aluminium gates, but that stability could be improved if the final stage of device manufacture is an anneal in hydrogen gas at a temperature of ~ 400°C – generally termed "passivation". In the CCD the same step is found to reduce the surface component of dark current by a large factor. Various studies [e.g. 2, 3] have now shown that the H_2 dissociates and hydrogen atoms attach to some of the dangling bonds rendering them inactive, as shown schematically in Figure 4, thereby giving the reduction in the dark current. It appears that not all the dangling bonds are passivated, with the result that the reduction of dark current is not complete. It is also apparent that the generation of hydrogen occurs automatically if aluminium is present over the structure, possibly through reaction with residual moisture.

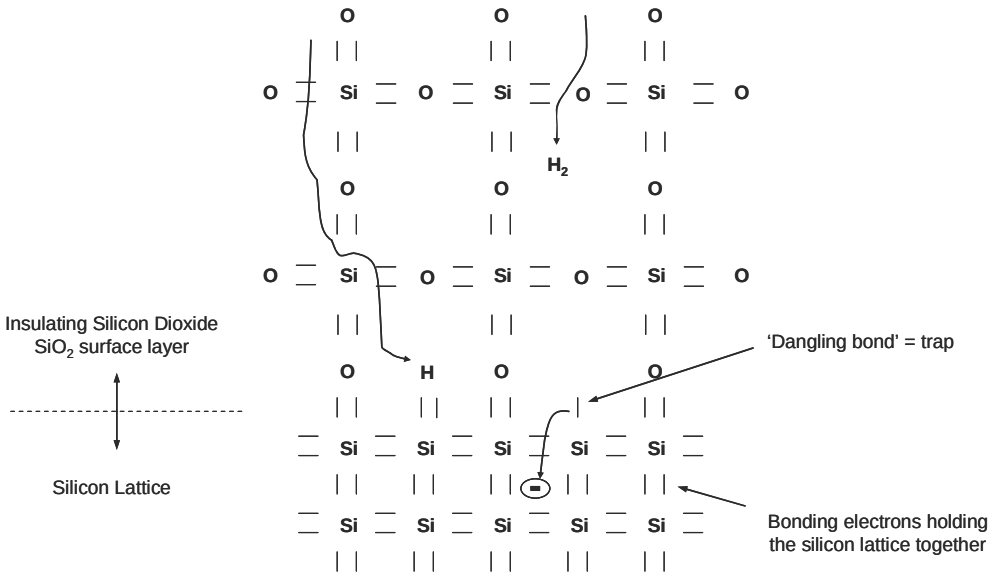

Fig 4: Passivation of the silicon surface with a high temperature hydrogen anneal

Ionising radiation is often said to "damage" the Si-SiO_2 interface, but what actually happens is that the passivation is reversed [3] leaving the surface in the pre-passivated state with a higher density of traps. The mechanism for the reversal involves the radiation-induced holes liberating protons (H^+) within the dielectric that diffuse down to the interface to combine with the H atoms attached to the dangling bonds, thereby increasing the trap density and forming gaseous H_2 that is no longer active (which probably diffuses out of the device). Experience at e2v suggests that H^+ can also be liberated in the regions *above* the electrodes, e.g. in the protective oxide layers, and diffuse down into the active regions to add to the de-passivation. Thus devices with thicker protective layers are found to show a greater increase of dark current.

Note that the movement of hydrogen can continue *after* irradiation and a stabilising anneal at about 100-200°C is generally given before measurements are taken.

However, having said all this, the exact mechanism for the de-passivation is not at all clear. The classic description assumes a positive gate bias that attracts H^+ to the Si-SiO_2 interface, but in reality the same increase in dark signal is found with negative bias. A possible suggestion is that the active species is H^o,

which would give this bias-independence, but it appears that H^+ is the only stable charge state capable of existing at the interface and reacting with the bound hydrogen [3].

Support for the basic hydrogen-related mechanism comes from the fact that devices often show increased dark current in the outermost pixels and that a pattern is sometimes seen that relates to peripheral layout features. The fact that the peripheral regions are generally fabricated with a much thicker oxide (to reduce parasitic capacitance for the tracks) means that far more H^+ is likely to be generated. It is reported that there is an easy path for lateral diffusion along the Si-SiO_2 interface [3], with the result that spreading by diffusion is likely towards the lower concentrations in the thinner oxide regions. Any peripheral structures which can hinder this diffusion can thereby impart a pattern. The fact that this diffusion can occur means that the peripheral dump columns or drains must be sufficiently wide to contain any likely spread. Note that any light emission from the output circuit will cause a localised increase in the dark current and this contribution could increase with radiation through changes in the transistor parameters.

2.2 Device hardening

It is clear from the description of charge build-up that the change of flat-band voltage can be minimised using thinner oxides. Some of the considerations are as follows.

CCD fabrication technology was developed during the late 1970s and early 1980s using the then-current mainstream MOS technology with gate oxide thicknesses in the region of 100 nm, resulting in devices being clocked with typically 10V pulses. Now, nearly 30 years later, whilst the mainstream technology has seen ever decreasing oxide thicknesses (now a few nm with modern CMOS, giving negligible flat-band shifts), the CCD manufacturers have tended to stay with the original thicknesses. One reason is that the thicker dielectric has a very high yield, which therefore makes possible the very large area devices that are seen today, e.g. e2v CCD230-84 with 36 cm² active area. Also, whereas it is possible to reduce the thickness and so reduce the operating voltages, it is also found that the inter-electrode potential distribution becomes more difficult to control with potential bumps and pockets often formed and causing charge transfer problems. Very thin dielectrics are therefore not generally used.

Various experimentations have been carried out at e2v over the last 10 years to determine the best approach for achieving devices that are less susceptible to ionising radiation. The standard process uses equal thickness of oxide and nitride and, under normal bias levels, achieves flat-band voltage shifts typically 100-200 mV per kRad(Si). Recently, CCD47-20 devices (a scientific-type frame-transfer array with 1000 x 1000 pixels, each 13 µm square) have been fabricated with a slightly thinner nitride layer and the oxide reduced to that just thick enough to avoid tunnelling into the nitride from the silicon. From the analysis given earlier, the factor of improvement should be about an order of magnitude. Results after Co^{60} γ-irradiation under normal bias are shown for some front-face devices in Figure 5 and back-face in Figure 6 (results for 500 kRad(Si) are not yet available). These all plot the dark current as a function of the substrate bias, V_{SS}.

For each curve the point of inflection is where the electrodes at 0V clock low level form a layer of holes at the Si-SiO_2 interface and become “pinned”, with their surface component of dark current then suppressed. The change in this point with γ-radiation dose is a measure of the flat-band voltage shift, and the earlier part of the curve gives the corresponding increase in the dark current. Results are quite impressive with the flat-band shift now down to about 6 mV per kRad(Si) for both front and back-illuminated devices. The dark current at 20°C increases at about 20 pA/cm^2 per kRad(Si) for front-illuminated devices. The figure for back-illuminated devices is higher at about 40 pA/cm^2 per kRad(Si), which is attributed to the fact that extra hydrogen is likely to be liberated from the thicker dielectric that is used over the electrodes to give added protection when mounting the silicon on support material prior to back-thinning.

It may be noted that the reduction in the flat-band shift is somewhat larger than the order of magnitude anticipated. From this and other work it would appear that the reduction tends to be proportional to the oxide thickness squared (i.e. not the nitride), for reasons that have not been determined.

Complete suppression of the surface component of dark current is possible using devices of the inverted-mode type (MPP) but note that, to maintain full pinning with increasing radiation dose, the bias levels will need to be adjusted to compensate for the flat-band voltage shift.

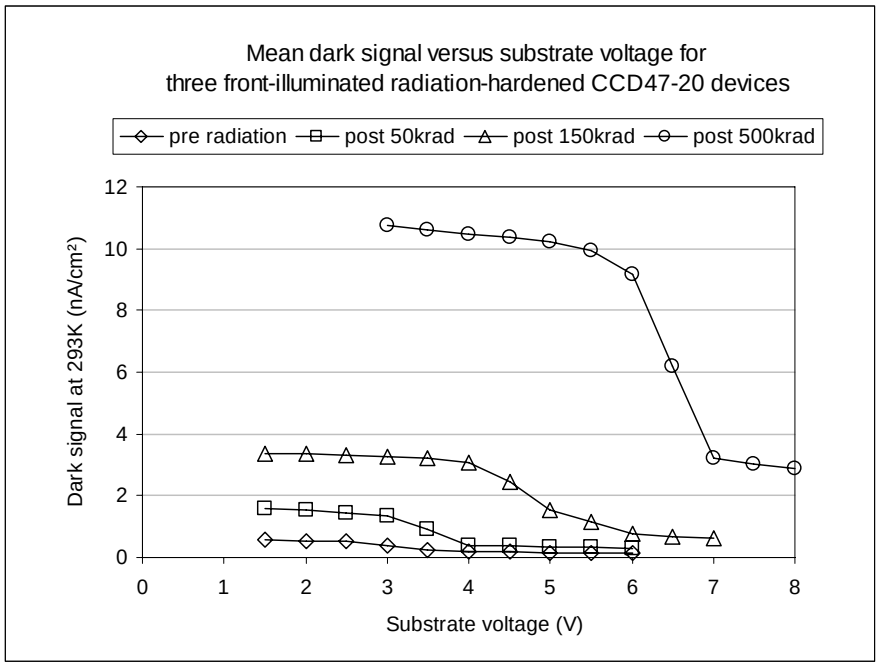

Figure 5: Results for front-illuminated devices

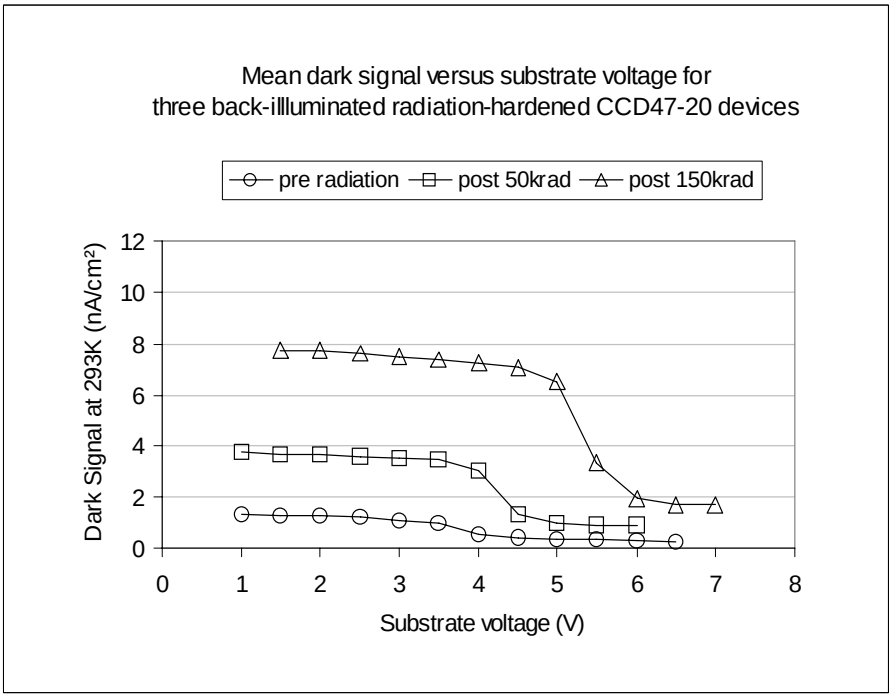

Figure 6: Results for back-illuminated devices

3. DISPLACEMENT DAMAGE

As stated previously, a “trap” is a result of any imperfection within the silicon that reduces the bonding energy of an electron to below that of the regular lattice. The concentration of such traps in the bulk silicon tends to be far lower than that at the surface. Although considered to be ultra-pure, the various methods of silicon production do generally result in a relatively high concentration of the impurities oxygen and carbon, plus crystal irregularities in the form of vacancies, dislocations and interstitials. Most of these features reside in an inert state within the silicon, but certain combinations can create active traps influencing CCD performance, and the number of these can increase with high-energy particle irradiation.

High-energy particles can collide with the silicon lattice and cause “displacement damage”, with formation of vacancies and interstitials, as shown schematically in Figure 7. The vacancies are fairly mobile and can move through the lattice. Stable combinations are however formed in association with an oxygen atom or a phosphorus atom and each of these gives rise to an electron trap. The energy levels of these traps measured from the conduction band edge are about 0.17 eV for the former (the O-V or A-centre) and about 0.44 eV for the latter (the P-V or E-centre).

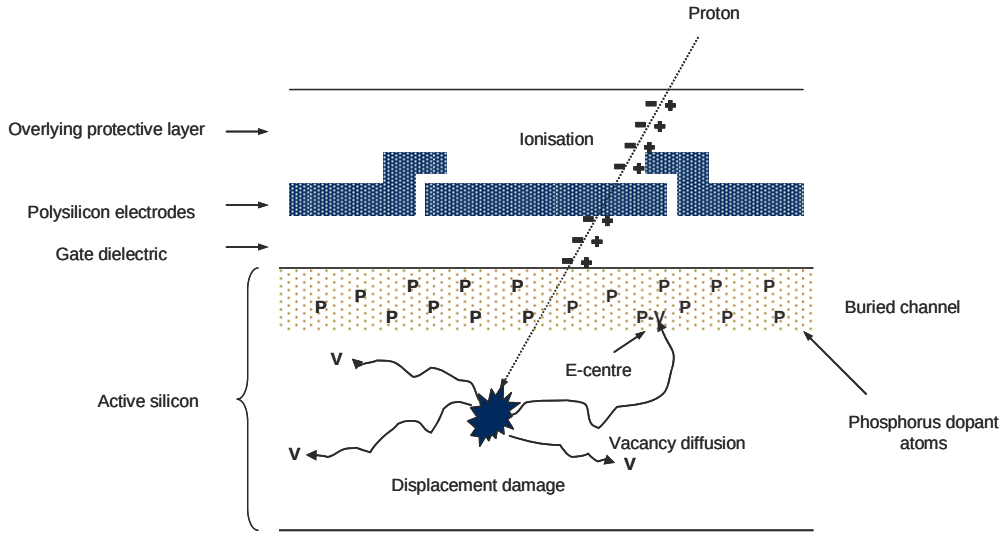

Fig 7: Displacement damage in an n-channel CCD

The major CCD parameter for which such traps are of importance is that of charge transfer efficiency (CTE). Traps take charge from any charge packet and release it at later times. Since the release time is proportional to exp(E/kT), where E is the trap energy, k is Boltzmann’s constant and T is absolute temperature, measurement of the released signals as a function of time and temperature can give a good indication of the traps that are present in any device. This has been done for e2v devices [4] and, pre-irradiation, the dominant traps are found to be the A-centre and an electron trap with an energy level of about 0.30 eV, the origin of which is as yet unknown, but is possibly vacancy-related. Post proton-irradiation the concentrations of these traps are found to increase, but the largest concentration is now the E-centre. This last trap is highly likely in the n-channel CCD because phosphorus doping forms the channel, as is shown in Figure 7. The dopant could of course be arsenic, but the properties of an As-V centre are not known.

Note that if the emission time of a trap is short in comparison with the clock period, then the released charge adds back to the main charge packet and the CTE remains high. On the other hand, if the emission time of a trap is long in comparison with the clock period, then the trap is likely to remain filled as the next charge

packet arrives and the CTE again remains high. Thus, at the cryogenic temperatures typical of scientific imaging applications, because of the varying energy levels of the different traps, the A-centre tends to be of importance at only register speeds, the 0.30 eV trap at register and fast frame-rate speeds and the E-centre at only frame rates. The CTE values for the different sections of a device can therefore vary, and the values will vary with change of speed and temperature, making comparisons between different devices difficult.

The increase in the trap concentrations cause the bulk dark current to increase. There is also an increase in the number of bi-stable traps giving random telegraph signal (RTS) effects, i.e. a localised source of dark signal switching randomly between two levels. The actual trap type responsible for this behaviour has not yet been identified.

3.1 Device hardening

Since the device degradation through displacement damage is very much at the mercy of fundamental processes in silicon, there is less that can be done to improve performance.

3.1.1 p-channel

One possibility that has received considerable attention of late is to fabricate opposite polarity p-channel devices. The channel is now formed from boron doping, thereby avoiding the P-V centres. The underlying substrate is n-type, but the concentration is at a very low level. The performance of these devices is less well documented than n-channel, especially information about which traps are dominant. Possible candidates [5] are the divacancy (V-V), carbon interstitial (C_i) and carbon interstitial-oxygen interstitial pair (C_i-O_i), with energies above the valence band of 0.20 eV, 0.28 eV and 0.36 eV, respectively.

Various p-channel devices have been fabricated at e2v, the most recent being CCD47-20 devices produced under an ESTEC contract [6]. A standard gate dielectric was used. Assessment of front-face devices in comparison with n-channel equivalents at temperatures over a range 0°C to –50°C showed marginally inferior CTE performance pre-irradiation, but superior performance post proton irradiation by a factor of about 5 serial (1 MHz) and a factor 2 parallel (1 ms line time). Note that different values are likely to be found at lower temperatures because different traps will be active.

It should be noted that p-channel will not be suitable for all applications. The fact that the ionisation rate of holes is lower than that of electrons means that achieving gain via avalanche multiplication is likely to be impracticable because of the need for much higher voltages. Inverted-mode operation and indeed any pinned operation are also impracticable because the clock-induced charge (caused by electron multiplication at the surface) is now much too high.

3.1.2 Shaped channels

The charge transfer efficiency naturally decreases as the signal size gets smaller. The now classic method to minimise this loss with the smaller signals is to use a “supplementary channel” or “notch” [7], as shown schematically in Figure 8. With this structure the small charges are constrained to transfer through a small volume of silicon (i.e. much smaller than that of the whole pixel) and therefore encounter fewer traps. It may be noted that the e2v type CCD43 device employed in the WFC3 camera of the latest Hubble upgrade uses such a structure.

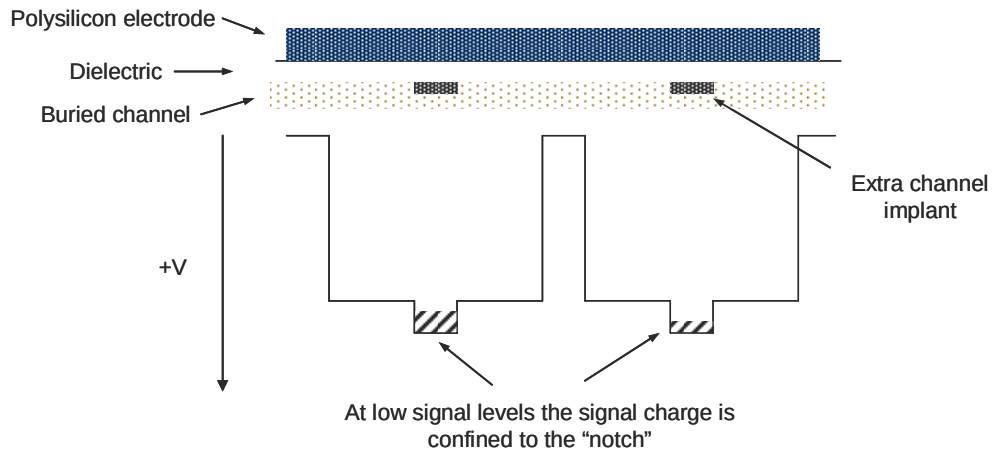

Fig 8: Supplementary channel or “notch”

Another possibility for large pixels transferring only small signals is to use a tapered finger between phases, as shown in Figure 9. A widening electrode has a potential in the underlying channel that increases along the length, thus the taper gives a field to speed the electron transfer and the probability of interacting with a trap is small. This structure also provides a 2-dimensional constraint on charge position between transfers, further reducing the probability of interaction with traps.

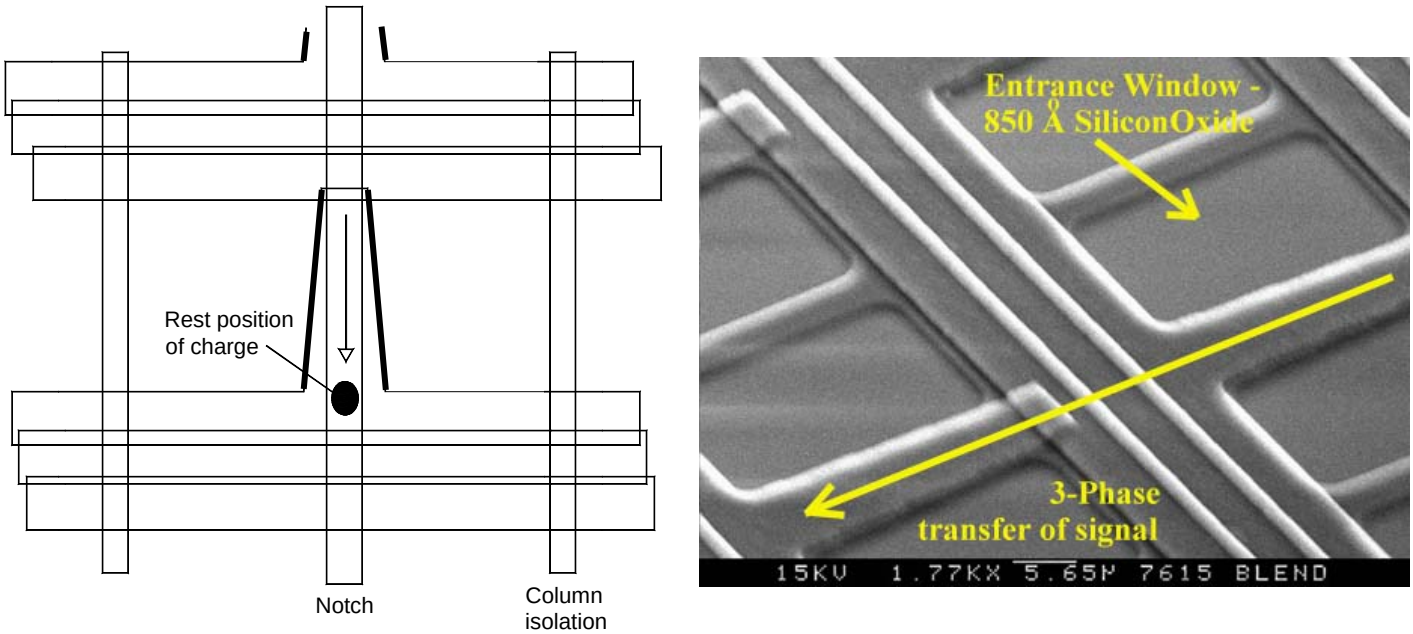

Fig 9: Tapered-electrode pixel

The areas adjacent to the taper can either be covered with another electrode or left open (with p+ channel stop) to increase the front-face quantum efficiency. This latter approach is used with the e2v CCD22 MOS-EPIC X-ray imaging devices in the highly successful XMM-Newton satellite, which is now approaching 10 years of operation with minimal reduction of energy resolution.

4. CONCLUSIONS

The newly-developed “rad hard” process has shown a significant reduction in the flat-band voltage shift that results from ionising radiation, down from typically 100-200 mV per kRad(Si) with standard processing to about 6 mV per kRad(Si), plus a reduction in the associated increase of dark current.

Developments aimed at reducing the impact of proton radiation have included the manufacture of p-channel devices. Our initial data indicates that at -50°C the increase in charge transfer inefficiency is reduced by a factor of two times for parallel transfer and five times for serial transfer. However, due to the fact that electrons and holes have different ionisation rates, the technology is not suitable for implementing gain via avalanche multiplication nor for device operation with electrodes pinned (inverted mode).

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