Improving Receiver Close-in Blocker Tolerance by Base-band $G_m - C$ Notch-Filtering

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***Abstract*—This paper presents a receiver front-end with improved blocker handling implemented in a 65 nm CMOS technology. Since close-in blockers are challenging to reject at RF, the receiver features a base-band notch-filter, which effectively sinks close-in blocker current directly from the output of an LNTA and passive mixer structure. The notch-filter frequency can be tuned to match the blocker offset frequency, and measurements indicate a significant improvement in the overall front-end interference robustness, while sensitivity remains unaffected. To optimize notch performance the base-band impedance is analyzed in detail. The front-end RF range is 750 MHz to 3 GHz with an RF channel bandwidth of 20 MHz corresponding to 10 MHz base-band bandwidth. The notch frequency is programmable from 16 MHz, which is less than one octave from the channel edge, up to 160 MHz. The gain-compression improvement is upto 9 dB, while IIP2 can be increased by more than 26 dB without calibration and IIP3 is 1 dBm. The current overhead for the notch function is between 7.5 mA and 30 mA, but it only exists under strong blocker conditions as the notch-filter can be switched off if strong blockers are absent. The total front-end current consumption excluding the notch-filter varies with LO frequency from 31 mA to 44 mA from a 1.2 V supply.**

***Keywords*—Interference robustness, blocker rejection, Notch filter, compression point, linearity, Gm-C filter,CMOS technology, linearization.**

I. Introduction

Interference robustness of radio receivers is an increasing worry, as the amount of wireless devices increases and strong interference is more likely to occur. Furthermore, communication standards such as LTE-advanced push for ever higher data rates [1], [2], leading to reduced guard bands for filtering. Higher data rates necessitate channel bandwidth increase, while the blocker frequency offsets do not increase. Introducing carrier aggregation increases the bandwidth even further. All these trends make blocker handling more tough.

Extensive research efforts have been made to improve receiver front-end blocker handling, and even realize SAW-less CMOS receivers, e.g. [3]–[5]. The focus in these works was on improving the RF part, while the base-band (BB) bandwidth is considerably smaller than the blocker offset. It is then easier to perform BB filtering, and the key bottleneck is linearity of the RF part, However, with the expansion of channel bandwidth, the blocker signals are less rejected at the BB filter output, as the ratio of blocker offset frequency and BB bandwidth is reduced, leading to less filter attenuation for the same filter order (see Fig. 1). As the residual blocker signal at BB is stronger now, BB output gain compression becomes a bottleneck. For example in LTE for frequency division duplex (FDD) systems, an important scenario of the handset is at the cell edge where a very weak signal should be received while the transmitter is at full power. Due to the limited duplexer isolation, the self-interference at the front-end input could be as large as -20 dBm and as close as 30 MHz from the desired received signal with a maximum of 20 MHz RF-channel bandwidth (10 MHz BB bandwidth) [1]. To illustrate the problem, assume a 50 dB of front-end gain and a 10 MHz BB first order low-pass filter, which would amplify a -20 dBm blocker signal at 100 MHz offset by 30 dB. Assuming 50 Ω, 63 mVpk-pk is amplified to 2 Vpk-pk at the output, which would be hard-clipped by the amplifier to a typical 1.2 V supply. Moreover, although the low frequency second order intermodulation (IM2) caused by the low noise amplifier (LNA) is filtered by the DC blocking capacitors, mismatch in the mixer and BB low-pass filter devices still pose a limit on the second order intercept point (IIP2) of the front-end. The

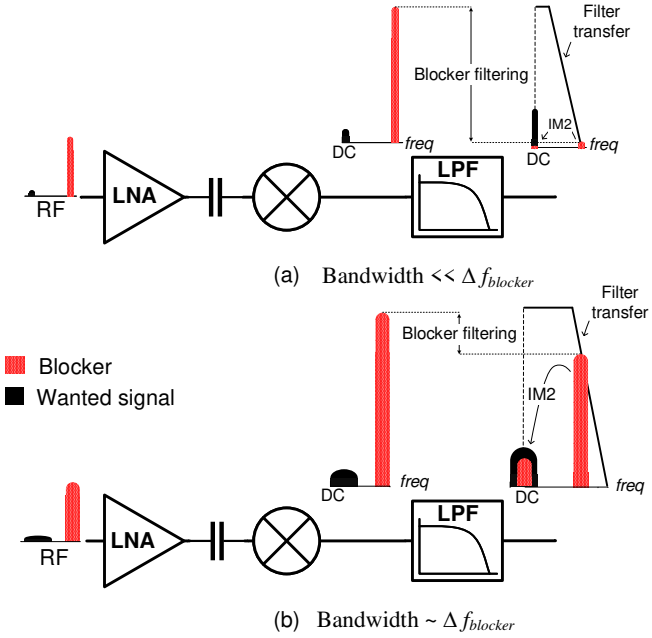

Fig. 1: Signal Spectrum before and after the Low Pass Filter (LPF) of (a) a traditional narrow BB bandwidth receiver and (b) a wide BB bandwidth receiver with small frequency offset to blocker.

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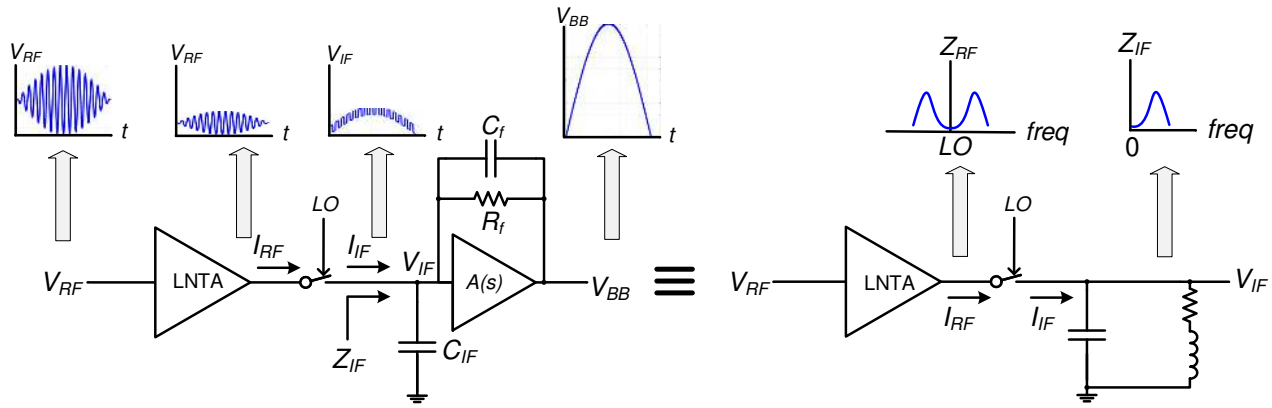


Fig. 2: (a) A signal path in a current mode receiver front-end. (b) An equivalent model of the base-band input behaviour.

effect of IM2 due to a modulated blocker is shown in Fig. 1. Suppression of close-in blockers is then very much wanted. In particular, Tx leakage is a major concern in such systems and this work will therefore target suppression of the Tx signal in the receiver after the frequency down-conversion.

A low noise transconductance amplifier (LNTA) is a key part in many receiver front-ends, not only for noise, but also since it provides isolation from the LO to the RF port. Attempts to remove the LNTA, taking a mixer-first approach, result in superior linearity, [6]–[10], but suffer from increased LO leakage and worse noise figure (NF). An LNTA was therefore used for its superior NF and LO leakage, while still achieving an IIP3 in the order of 0 dBm, which is often sufficient for FDD front-ends [11]. The BB linearity and compression bottlenecks are addressed by the notch filtering to be described.

Current mode receiver front-ends are attractive, compared to a voltage-mode LNA, since the signal information is conveyed as current to avoid large RF-voltage swings [12], [13], [14], [3]. BB I-V conversion in a trans-impednace amplifier (TIA) is then combined with channel filtering to achieve overall good linearity. The LNTA should be linear enough (in our case around 0dBm IIP3) as it defines out-of-band linearity (see Fig. 2a) [14], [12].

A BB amplifier with high voltage gain is needed to ensure that the TIA achieves both low input impedance and high loop gain. This is important for BB linearity and is required at all frequencies where desired signals or blockers are located. However, due to the speed limitation of the amplifier, impedance peaking occurs at BB leading to degraded linearity and ultimately BB compression. This peaking can actually be modeled as an RLC circuit, as shown in Fig. 2b, where the inductor models the increase of TIA input impedance due to gain roll-off, assuming $A(s)$ in Fig. 2a has a single dominant pole. As the passive mixer is bidirectional, the BB impedance shape Z_{IF} seen by the mixer is up-converted to Z_{RF} in Fig. 2b around the LO frequency at the RF-input of the mixer [12], [14]–[16].

It is possible to shunt the RF-current of the LNTA to ground via a notch filter, as proposed by Khatri *et al.* [17]. This filter exploits impedance frequency up-conversion via a passive mixer followed by an auxiliary TIA. As its input impedance is similar to that of the main TIA, notch depth is limited and only a moderate IIP2 improvement of 7 dB was achieved. Higher improvement can be achieved by providing a notch filter with an impedance significantly smaller than the main path impedance, but this requires low-ohmic switches and a large baseband-Gm. In contrast, this work exploits the already present BB-impedance peaking

This work targets >20 dB notch suppression in BB. We propose a BB current sink that counteracts the BB-impedance peaking to reject blockers very close to the pass-band, see Fig. 3. The notch filter sinks the blocker current before entering the TIA, hence mitigating TIA distortion and compression. *While impedance peaking is normally a disadvantage, it is exploited here to improve the efficiency of the notch filtering. Due to the peaking the blocker current can be more efficiently diverted by the notch filter, so that less blocker current enters the TIA. The distortion (cross-modulation, intermodulation, compression) of the TIA caused by the blocker current is then reduced, leading to an overall improved linearity.*

This paper presents and analyzes the concept and demonstrates feasibility. The filter concept is introduced and analyzed in section II. First, the front-end architecture is presented in subsection II-A, and frequency behaviour is analyzed and optimized in subsection II-B. Measurement results on a 65 nm prototype chip and a comparison to state-of-the-art are shown in section III. Finally, conclusions are drawn in section IV.

II. Wide bandwidth Receiver with Notch Filter

The proposed front-end architecture is shown in Fig. 4. If $A(s)$ would be ideal ($=\infty$), the impedance at node (X) is 0Ω and the notch would not be effective. However, finite $A(s)$ can be exploited to benefit, as will be shown later in this paper. However, first we will briefly describe the overall system architecture. To achieve wide RF bandwidth and power matching, a complementary common source stage with resistive shunt feedback followed by a transconductance stage (G_m) was used as an LNTA [18]. Noise canceling [14], [19]–[21] was also used to achieve sub-3 dB NF. The LNTA is AC-coupled to the mixer to remove low-frequency IM2 products. The RF is down-converted to BB using a current-mode quadrature passive mixer. The 25% duty cycle quadrature LO signals are generated by a current-mode logic divide-by-2 circuit followed

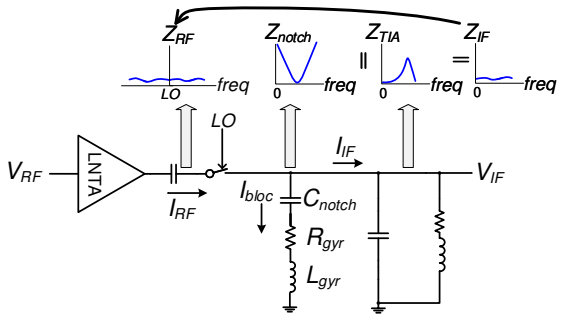


Fig. 3: Front-end with a notch filter.

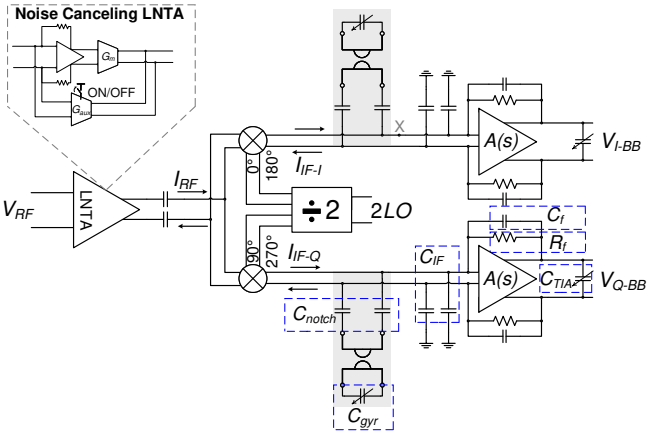


Fig. 4: Architecture of the proposed receiver front-end.

by AND gates. The notch filter is implemented using a tunable differential active inductor (gyrator and tunable capacitor) in series with capacitors. The TIA used in this work is similar to the one proposed in [18]. The notch frequency is tuned based on knowledge of the blocker. In FDD systems the TX leakage offset is known and therefore the settings to tune notch frequency can be easily applied for highest blocker rejection.

A. Notch filter implementation

Around the notch frequency, a down-converted blocker is shunted to ground. As the blocker current is directed into the notch filter, rather than the TIA, this helps overcome the fundamental voltage headroom limitation in advanced CMOS processes. This enables higher in-band gain and increased out-of-band blocker resilience. This is in contrast to increasing the low pass filter order in the BB, which would result in tough linearity requirements to avoid filter internal node clipping, as the filter would then need to handle large signal current levels and at the same time have increased quality factors of the poles. Moreover, the in-band and band-edge linearity remains similar as the gain from increased filter order results in limited filtering at such small frequency offsets.

The active inductor schematic is shown in Fig. 5. Digitally switched transconductance cells allow for tuning the effective overall inductance. Each cell has $G_{m-unit} = g_m$, as shown in Fig. 5b. The number of transconductance cells to be activated depends on the level of blocker current, which is to be sunk by G_{m2}. The inductance (L_{gyr}), series resistance (R_{gyr}) and the notch frequency (ω_{gyr}) in Fig. 4 are given by

$$L_{gyr} \approx \frac{C_{gyr}}{G_{m1}G_{m2}} \tag{1}$$

$$R_{gyr} \approx 2\frac{G_{o1}+G_{o2}}{G_{m1}G_{m2}} \tag{2}$$

$$\omega_{gyr} \approx \sqrt{\frac{G_{m1}G_{m2}}{C_{gyr}C_{notch}}} \tag{3}$$

where G_{o1} and G_{o2} are the output conductances of the G_{m1} and G_{m2} stages in the gyrator. The current coming from the LNTA takes the most low-ohmic path, which means that the sunk blocker current is maximized when the TIA is high-ohmic (peak in Z_{IF}) at the blocker frequency, while the notch filter is low-ohmic (at its resonance frequency ω_{gyr}). The maximum notch depth thus occurs when the peaking frequency (ω_{IFmax}) of the TIA and ω_{gyr} in (3) are equal, which can be achieved by e.g. scaling C_{gyr} and C_{notch}. The notch depth can then be approximated as the ratio of BB peak impedance Z_{IFmax} (17) and R_{gyr} (2):

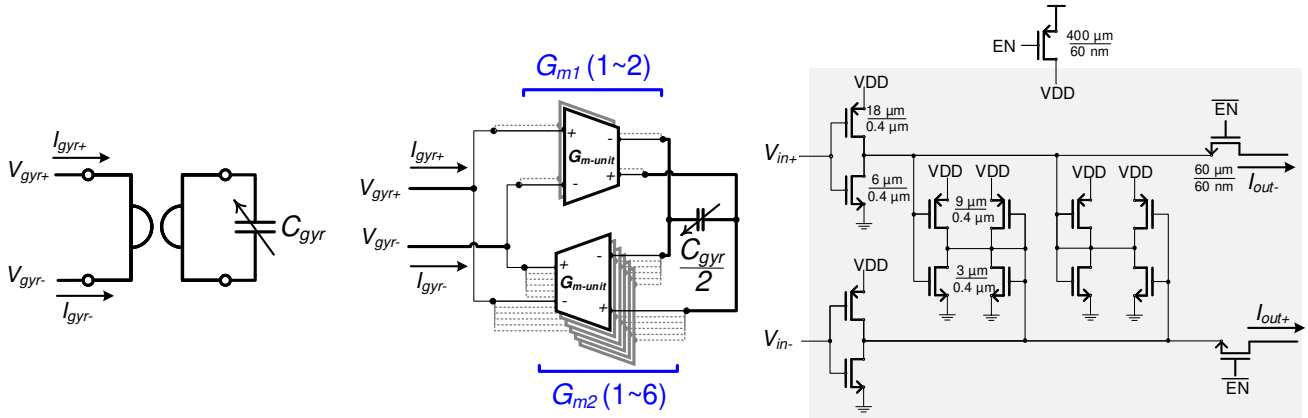
$$Notch\ depth_{max} \approx \left(Z_{IFmax}\right)_{TIA} \times \left(\frac{G_{m1}G_{m2}}{2(G_{o1}+G_{o2})}\right)_{gyr}$$

if

$$\left(\omega_{IFmax}\right)_{TIA} \approx \left(\frac{G_{m1}G_{m2}}{C_{gyr}C_{notch}}\right)_{gyr} \tag{4}$$

As seen in (4), to improve the notch depth, G_o^{gyr} must be reduced, which will reduce the gyrator series resistance R_{gyr}. The operational transconductance amplifier (OTA) of choice is the Nauta cell [22] (see Fig. 5c). This choice is more fundamentally motivated in [23], where the inverter is shown to belong to a class of circuits that achieves maximum normalized signal to noise ratio, which can be related to spurious free dynamic range per power. To reduce G_o^{gyr} the inverter devices are made approximately seven times longer than the minimum allowed feature size of the technology. The notch frequency is controlled by C_{gyr}, while the increasing of G_{m2}^{gyr} is needed only to sink large blocker current. The notch depth can also be increased if Z_{IFmax} is at the notch frequency. The TIA is therefore loaded with a tunable capacitor (C_{TIA}) for Z_{IF} peak tuning, see Fig. 4. A practical approach could be to tune Z_{IF} by means of the OTA bias current. In this work, however, we avoided tuning the bias current and instead loaded the TIA with a programmable capacitor. In this way we could maintain a high performance TIA also when the notch was turned off, to perform a more fair performance comparison. Tuning the impedance using the load capacitance results in reduced loop gain, but the linearity performance is still improved since the increased notch depth diverts more blocker current from the main path.

For an optimal design of the front-end, the input impedance ratio of the TIA and the notch filter needs to be evaluated, see (4). In subsection II-B detailed analysis of the input impedance



(a) Active inductor (b) Digitally tunable inductor (c) Nauta g_m cell

Fig. 5: Tunable active inductor realization.

is therefore presented together with guidelines on improving the notch depth.

B. BB Impedance Peaking and Notch Filter Optimization

The widely used feedback-based TIA comprised of a two-stage OTA is studied in this section. The results, however, can be used for simpler single-stage OTA implementations as well. Detailed analysis and approximate expressions are presented to provide more insight on both BB design in general and the selection of TIA design parameters.

A capacitor C_{IF} is often connected from the TIA input to ground, forcing Z_{IF} to be low at higher frequencies. While this looks good at first, it is of limited use for close-in blockers and for linearity at frequencies in-band, at the band-edge and close out-of-band. The reason is that a larger capacitor value heavily limits the loop gain of the TIA at these frequencies, and therefore the linearity at the band-edge and out-of-band is compromised. Moreover, the chip area of such capacitors increases cost. Even if a large value of C_{IF} is acceptable, it still introduces a rather limited filter attenuation. Furthermore, during the design phase, careful simulations are required to choose safe C_{IF} values for TIA stability. In the transition band of the low-pass BB filter, blockers will still experience high gain or cause distortion and even clipping at the output.

The behaviour in the transition band can be modelled with the peaking of Z_{IF} (see Fig. 2b). A two stage OTA is frequently used in the TIA to ensure low in-band Z_{IF} and high linearity. The OTA can then be modeled by two g_m stages, each loaded with a resistor (r_o) in parallel with a capacitor (c_o), see the model in Fig. 6. Typically, $c_{o1} >> c_{o2}$, modeling the pole separation realized by the implemented frequency compensation such as Miller, feed forward or any other compensation technique used. The TIA is designed such that the dominant open loop pole $(c_{o1}r_{o1})^{-1}$ is approximately equal to or higher than the TIA closed-loop pole $(C_f R_f)^{-1}$ realized by the feedback network (10 MHz in this case), to ensure flat Z_{IF} in-band. To ensure high linearity and avoid high voltage swings at the BB input and the LNTA output, the peak value of Z_{IF} and its frequency is of interest for design

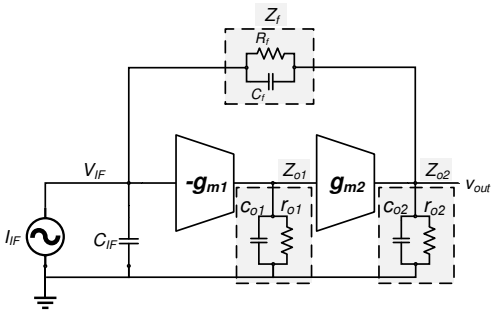


Fig. 6: A model of the TIA using a two-stage OTA.

insight. From the TIA model in Fig. 6, Z_{IF} is calculated as

$$Z_{IF} = \frac{Z_{C_{IF}}(Z_f + Z_{o2})}{Z_f + Z_{o2} + Z_{C_{IF}}(1 + g_{m1}g_{m2}Z_{o1}Z_{o2})} \tag{5}$$

First the behaviour of Z_{IF} at low frequency is investigated. Considering only resistive impedances, the value of Z_{IF} at low frequencies can be approximated to that at DC (assuming $Z_{o1} = r_{o1}$, $Z_{o2} = r_{o2}$ and $g_{m1}g_{m2}r_{o1}r_{o2} >> 1$):

$$Z_{IFDC} \approx \frac{R_f + r_{o2}}{g_{m1}g_{m2}r_{o1}r_{o2}} \tag{6}$$

As can be seen in (6) the low frequency in-band impedance Z_{IFDC} is inversely proportional to the OTA voltage gain. Therefore maximizing the voltage gain is required to ensure low impedance. In this work the targeted TIA DC input impedance is 6.5Ω.

The high frequency behaviour of Z_{IF} is then investigated assuming a large C_{IF}. As can be seen in (5), as $Z_{C_{IF}}$ becomes small at very high frequencies ($C_{IF} >> c_{o1}, c_{o2}, C_f$) then Z_{IF} reduces to $Z_{C_{IF}}$. Z_{IF} is thus low both at low frequencies (6) and at high frequencies $Z_{IF} \approx Z_{C_{IF}}$. At increasing intermediate frequencies, however, Z_{IF} first increases as the loop gain rolls off due to limited amplifier bandwidth, but at higher frequencies $Z_{C_{IF}}$ starts dominating causing Z_{IF} to decay again, see Fig. 2b. A study of Z_{IF} at the intermediate frequencies is necessary, since blockers are not much attenuated there and are hence most problematic.

TABLE I: TIA model parameters

Parameter	Value	Unit
C_{IF}	1 to 100	pF
R_f	5000	Ω
C_f	3	pF
r_{o1}	1600	Ω
r_{o2}	1600	Ω
c_{o1}	5	pF
c_{o2}	0.1 to 100	pF
g_{m1}	20	mS
g_{m2}	20	mS

TABLE II: Notch filter model parameters

Parameter	Value	Unit
C_{notch}	40	pF
C_{gyr}	4 to 40	pF
G_{m-unit}	4	mS
G_{o-unit}	0.092	mS
G_{m1}	G_{m-unit} to $2G_{m-unit}$	mS
G_{m2}	G_{m-unit} to $6G_{m-unit}$	mS

Analyzing (5) in detail, poles and zero frequencies were derived. The zero frequencies are given by

$$Z_{1,Z_{IF}} = -\frac{1}{r_{o1}c_{o1}} \tag{7}$$

$$Z_{2,Z_{IF}} = -\frac{1}{R_f \| r_{o2}(C_f + c_{o2})} \tag{8}$$

The first pole frequency is given by

$$P_{1,Z_{IF}} \approx -\frac{1}{R_f C_f} \tag{9}$$

and the next two complex conjugate poles frequencies are

$$P_{2\&3,Z_{IF}} \approx -\frac{1}{2R_f C_f} - \frac{1}{2r_{o2}C_f} - \frac{1}{2r_{o2}C_{IF}} - \frac{1}{2r_{o1}c_{o1}} \pm i\frac{\sqrt{A_v}}{\sqrt{r_{o1}r_{o2}c_{o1}C_{IF}}} \tag{10}$$

where A_v is the DC voltage gain of the OTA, given by

$$A_v = g_{m1}g_{m2}r_{o1}r_{o2} \tag{11}$$

A pole in Z_{IF} results in impedance roll off and therefore helps to reduce the impedance at higher frequencies while a zero in Z_{IF} instead causes an increase in the impedance magnitude. It can be seen in (7-11) that the first zero frequency (9) is at the OTA's open loop dominant pole frequency, which indicates that the 3dB bandwidth of the OTA should be maximized for a flat in-band impedance if $Z_{2,Z_{IF}} \geqslant P_{1,Z_{IF}}$. This condition is becoming increasingly difficult to meet for new wide-band communication standards, but in general it is beneficial to minimize the distance between (7) and (9), which can be achieved using a more efficient frequency compensation (e.g. [24], [25]).

As a case study, the TIA modeled in Fig. 6 is assumed to have the parameters provided in TABLE I. Those values are based on the OTA implemented in this front-end, with inverter based first and second stages. It is important to note, however, that the technique is not limited to that particular design, and that designs with other OTA characteristics could equally well be used. The effect of C_{IF} was investigated by sweeping its value and studying Z_{IF}. Fig. 7 shows the pole-zero map with C_{IF} swept from 1pF to 100 pF. As expected the zero frequencies in (7) and (8) as well as the pole frequency in (9) remain unchanged, while the complex conjugate poles in (10) are reduced as C_{IF} increases. The Q-factor of the poles also decreases, indicating reduction in peak magnitude of Z_{IF} as C_{IF} increases. This is verified in Fig. 8a where the magnitude of Z_{IF} is plotted, where C_{IF} is swept from 20 pF to 100 pF while c_{o2} =0.1 pF and other parameters are according to TABLE I.

The peak magnitude of Z_{IF} (Z_{IFmax}) and its frequency (ω_{IFmax}) in Fig. 8a reduce as C_{IF} increases. This behaviour is often exploited to reduce the blocker voltage, but this has disadvantages like reduced loop gain in the TIA (degrading its distortion) and the required very high capacitance. In out example, the size of C_{IF} needed for 16 dB blocker gain reduction without using the notch at 50 MHz offset would be 3.2 nF, which takes $800\,\mu\text{m} \times 800\,\mu\text{m}$ chip area in the technology in use. Instead, we propose here to exploit the peaking in Z_{IF} to improve notch filter efficiency. To tune the frequency of Z_{IFmax}, we will exploit c_{o1} or c_{o2} to imitate a slower OTA, as illustrated in Fig. 8b. The minimum frequency difference results in maximum notch depth at such frequency given that $Z_{IFmax} >> R_{gyr}$. The value of c_{o2} is chosen to maintain the pole-zero pairing in (7) and (9) and achieve high impedance peaking at lower frequency offset as shown in Fig. 8b.

The notch filter design parameters used in this work are shown in TABLE II. To evaluate the effectiveness of the notch filter, Z_{IF} of the TIA is simulated. Setting C_{IF} =40 pF and c_{o2} =10 pF, while for the notch filter all g_m cells are activated and C_{gyr} =10 pF results in a notch frequency as well as a peaking frequency of 110 MHz. The frequency response of the modeled TIA with and without the notch filter are plotted in Fig. 9a, while the input impedance is shown in Fig. 9b. The difference in impedance is 29.5 dB, which is similar to the notch depth in the overall TIA response, confirming that the impedance ratio is indeed relevant.

In order to improve the notch depth, and achieve an optimal notch-TIA co-design, an estimation of the peak frequency and impedance levels is needed. Therefore, further investigations of Z_{IF} behaviour at different frequency offsets are performed. The second zero frequency in (8) causes further peaking in Z_{IF}. The complex conjugate poles in (10) limit the peaking and force the impedance to roll off again. Looking at (7) and (8), peak Z_{IF} tuning can also be performed through c_{o1} and c_{o2}. To increase the notch depth such tuning should also move Z_{IFmax} to lower frequency offsets. Hence it is useful to evaluate the effect of different Z_{IF} tuning possibilities.

Finding accurate yet simple approximations for Z_{IFmax} and ω_{IFmax} is desirable to effectively co-design the notch filter and the TIA. Attempts in finding equations for Z_{IFmax} and the peaking frequency ω_{IFmax} unfortunately resulted in excessively large expressions providing very limited insight. An intuitive approach is therefore used instead. Assuming by design that the pole frequency in (9) is close to that of the zero in (7), this pole-zero cancelation results in constant impedance

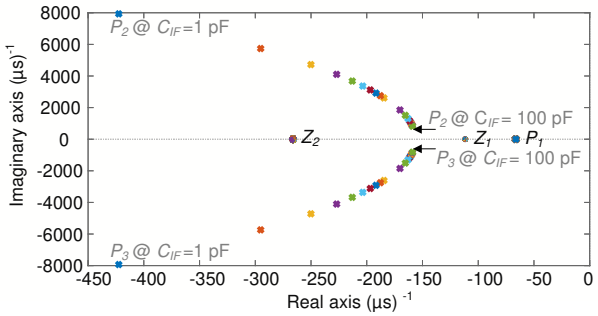


Fig. 7: Pole-zero map of Z_{IF} for different values of C_{IF}.

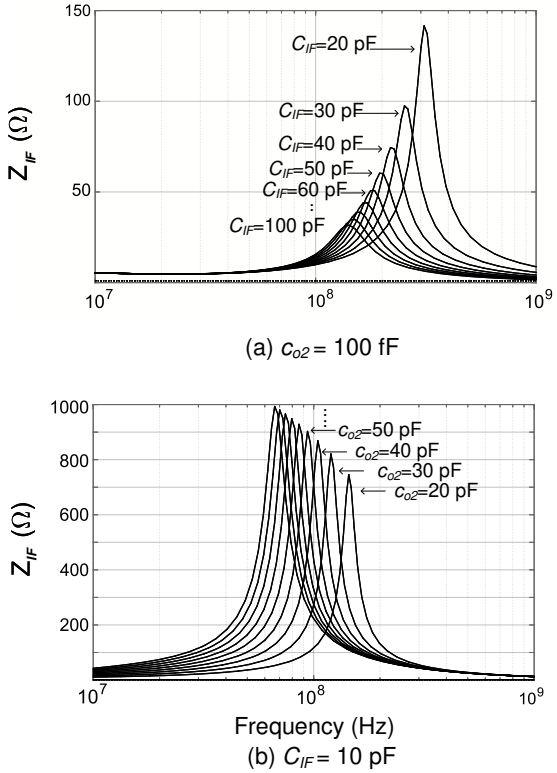


Fig. 8: Z_{IF} peaking for different values of (a) C_{IF} and (b) c_{o2} (notch filter is not applied).

in-band. What is left are the complex conjugate poles given by (10) and the zero given by (8). From the modeled TIA pole-zero map in Fig. 7, the peaking frequency ω_{IFmax} can be estimated. Noticing the Y-axis scale in Fig. 7, the two complex conjugate poles have a high Q, suggesting a large magnitude of Z_{IFmax}. If the effect of the first pole-zero pair in (9, 7) can be safely neglected (i.e. by design they have small frequency offset), Z_{IF} is approximated to have the form

$$Z_{IFapprox} \approx K \frac{s+\omega_z}{s^2+\frac{\omega_o}{Q}s+\omega_o^2} \tag{12}$$

where ω_z is the zero frequency given by (8), Q and ω_o are the quality factor and frequency of the poles in (10) and K is a scaling factor. The approximation of Z_{IF} in (12) can also

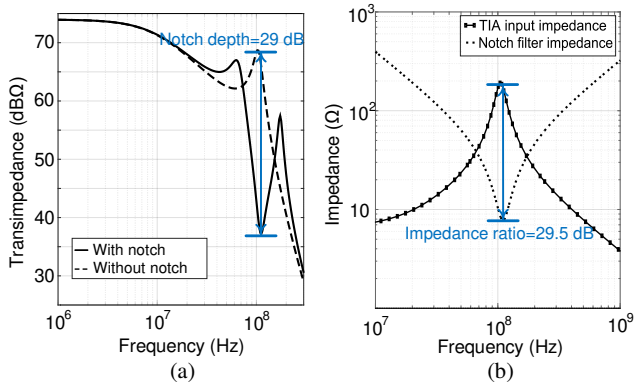


Fig. 9: Demonstration of the beneficial effect of the notch filter and its relation to impedance ratio: (a) overall transfer function; (b) BB impedances; the impedance ratio correlates with notch depth.

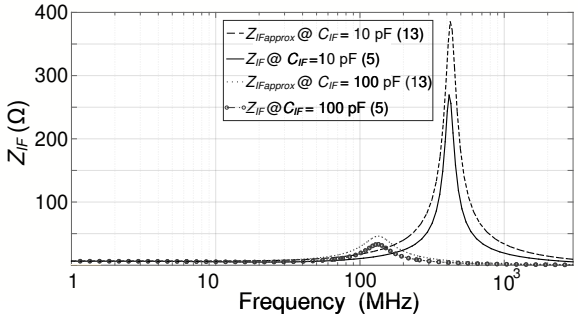


Fig. 10: Z_{IF} Full model (5) vs. approximation (13) for two C_{IF} settings.

be rewritten as

$$Z_{IFapprox} \approx K \frac{s+Z_2^{Z_{IF}}}{s^2+(P_2^{Z_{IF}}+P_3^{Z_{IF}})s+(P_2^{Z_{IF}}P_3^{Z_{IF}})} \tag{13}$$

The accuracy of $Z_{IFapprox}$ was compared to (5) for the modeled TIA, for C_{IF} =10 pF and C_{IF} =100 pF, see Fig. 10. As can be seen, the approximation predicts ω_{IFmax}. The deviation of the magnitude from Z_{IFmax} is due to neglecting the effect of the low frequency pole-zero pair. The approximation of ω_{IFmax} becomes

$$\omega_{IFmax} \approx \sqrt{(-\frac{1}{2R_fC_f}-\frac{1}{2r_{o2}C_f}-\frac{1}{2r_{o2}C_{IF}}-\frac{1}{2r_{o1}c_{o1}})^2+\frac{g_{m1}g_{m2}}{c_{o1}C_{IF}}} \tag{14}$$

for values of g_{m1} and g_{m2} much larger than $1/r_{o1}$ and $1/r_{o2}$, (14) is further simplified to

$$\omega_{IFmax} \approx \sqrt{\frac{g_{m1}g_{m2}}{c_{o1}C_{IF}}} \tag{15}$$

Decreasing the Q of $P_2^{Z_{IF}}$ and $P_3^{Z_{IF}}$, i.e. the ratio of the imaginary and real part, results in reduced Z_{IF} peaking. As can be seen in (10) this can be accomplished by increasing C_{IF} or decreasing the output resistances r_o of the OTA stages. This is shown in Fig. 7, where C_{IF} is varied from 1 pF to 100 pF. Reducing r_o directly impacts the performance of the OTA and is therefore not desirable. Increased g_m helps restoring

the impedance at the cost of increased current consumption. In this work, however, increased peaking aids the notch filter efficiency and increasing g_m is not necessary.

The accurate expression of Z_{IFmax} is rather complex and gives little insight into the design trade-offs, but a more intuitive estimate can be made. Using (6) the magnitude of Z_{IFDC} can be found. The complex conjugate poles in (10) will then cause the impedance at ω_{IFmax} to increase from Z_{IFDC} by a factor approximately equal to their Q-factor [26]. The effect of the zero in (10) is a further increase in impedance by the ratio ($\frac{\omega_o}{\omega_z}$). Therefore Z_{IFmax} can be approximated by

$$Z_{IFmax} \approx \frac{\omega_o}{\omega_z} Z_{IFDC} Q \tag{16}$$

where Q is calculated as the ratio of the imaginary and real part of (10). The expressions for Z_{IFmax} and its frequency ω_{IFmax} are given by (17)

To verify validity of the approximations, the TIA's Z_{IFmax} given by (5) is compared to the approximation (17) in Fig. 11. The trend fits well and the error seen is mainly due to the non-perfect pole-zero pair cancellation, and due to the approximation of the peaking being equal to the Q-factor of the poles in (10). The fit is within 20% when the low frequency pole-zero pair are matched in frequency. The notch depth given in (4) is valid if (18) holds. The equation helps in designing the TIA and selecting the design parameters for the expected scenario.

To summarize the findings in this section, the BB impedance behaves as an RLC network with considerable impedance peaking that may lead to front-end compression. It can be seen in (17) and Fig. 10 that in a typical design increasing C_{IF} helps reducing Z_{IFmax} and its frequency. Unfortunately, large C_{IF} also heavily reduces the TIA loop gain. This is seen in Fig. 12, where loop gain versus C_{IF} at 50 MHz and 100 MHz frequency offsets are shown. Reduced loop gain results in worse linearity, and it is therefore desirable to avoid increasing C_{IF} and use notch filter instead. Counteracting the impedance peaking without using large C_{IF}, and reducing the blocker gain without affecting the in-band gain.

The presented analysis in this section is for two-stage OTAs. However, also single stage implementations of the TIA could be used. Fortunately the input impedance of such TIAs is more straight-forward to analyze and can be derived from the presented analysis. Even though impedance peaking is not a major concern in such implementations, the input impedance of single stage TIAs is considerably higher, since the input impedance is increased by approximately a factor of $g_m r_o$, i.e. the voltage gain of one stage. Therefore the input impedance to notch impedance ratio is still high, resulting in a high notch depth. Attempts to implement a single stage TIA with impedance similar to that of a two stage TIA would result in very high power consumption, making the proposed solution attractive also for single stage TIAs. Moreover, the presented notch filter technique is effective whether an LNTA is used or a mixer first receiver architecture is adopted.

III. Measurement Results

A test circuit was designed and fabricated in a low power 65 nm CMOS process with a core area of 0.3 mm x 0.7 mm (see Fig. 13). The supply voltage used for the RF, LO and BB parts was 1.2 V, while a 1.4 V supply was used for the serial to parallel interface (SPI) and the digital switches. The chips were wire bonded to FR-4 PCBs, and PCB losses were measured with a network analyzer and carefully de-embedded from the presented results. Three samples were fully measured with similar results, however, the IIP2 measurements showed difference between I and Q channels and therefore only worst case measurement results are reported in this paper including IIP2 measurements. The LNTA and TIA in this work are similar to the ones proposed in [18].

The small signal front-end gain measurements are shown in Fig. 15, 16, to be compared to the thin curve where the notch filter is disabled. In Fig. 15, G_{m2} was swept from $6 \times G_{m-unit}$ to G_{m-unit}, reducing the notch frequency from 40 MHz to 16 MHz (less than one octave from the band-edge). The notch depth increases with frequency thanks to TIA impedance peaking. Note that this peaking is normally a disadvantage, but it is turned into an advantage here as blocker current is directed towards the notch when Z_{IF} is increased due to peaking. We predicted in the previous section that a slower TIA improves the notch depth. To verify this the TIAs were loaded with a variable differential capacitance C_{TIA} tuned from 1.5 pF to 22.5 pF (see Fig. 4). As can be seen in Fig. 16a increasing C_{TIA} (slower OTA) increases the notch depth by almost 10 dB since the frequency difference between the impedance peak and the notch decreases. Added to that also the notch bandwidth increases, which is desirable to reject realistic modulated blockers. In Fig. 16b, C_{gyr} was swept instead and it can be seen that the notch frequency is tuned from 160 MHz down to 54 MHz offset. This is attractive since depending on the blocker level one can activate the required number of G_{m-unit} cells to sink the current and then use C_{gyr} to program the frequency.

The front-end is operational for an RF frequency range of 750 MHz to 3 GHz, and the presented measurements are for an LO frequency of 2 GHz. The LO generation circuit including the buffers to drive the mixers consumes 9 mA at 750 MHz, and 22 mA at 3 GHz effective LO frequency. The BB bandwidth is fixed to 10 MHz (20 MHz RF bandwidth) and the measured small signal front-end gain is 49.5 dB with an LNTA transconductance of 60 mS and a BB transimpedance of 5 kΩ. The OTAs used in the TIAs consume only 6 mA in total. The measured input power match S_{11} is better than -10 dB over the whole RF range.

To compare the front-end performance with and without notch filter, the gyrator was turned off and C_{TIA} was set to 0 to maintain high loop gain when the notch was disabled. A performance summary of the front-end with and without notch filter (where all gyrator cells are on) is found in TABLE III. Clearly, IIP2 and compression are significantly improved. Each G_{m-unit} cell consumes 3.75 mA of supply current, and turning all the cells on is only needed to sink high blocker currents. The value of C_{gyr} is used to tune the notch frequency. The IIP3 is dominated by the LNTA, since a first stage with voltage gain and shunt feedback was chosen to achieve wide-band power match and low NF. Linearity can be traded for NF by using a different LNTA configuration, such as the common

$$Z_{IFmax} \approx \frac{R_f(C_f + c_{o2})}{C_{IF}c_{o1}r_{o1}((R_fC_f)^{-1} + (C_fr_{o2})^{-1} + (C_{IF}r_{o2})^{-1} + (c_{o1}r_{o1})^{-1})} \quad @ \quad \omega_{IFmax} \approx \sqrt{\frac{g_{m1}g_{m2}}{c_{o1}C_{IF}}} \tag{17}$$

$$Notch\ depth_{max} \approx \left(Z_{IFmax}\right)_{TIA} \times \left(\frac{G_{m1}G_{m2}}{G_{o1}+G_{o2}}\right)_{gyr} \quad if \quad \left(\frac{G_{m1}G_{m2}}{C_{gyr}C_{notch}}\right)_{gyr} \approx \left(\frac{g_{m1}g_{m2}}{c_{o1}C_{IF}}\right)_{TIA} \tag{18}$$

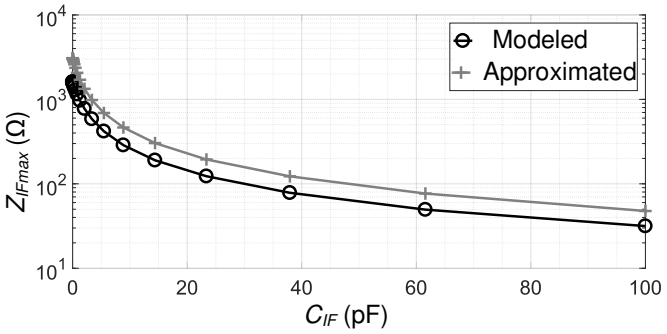


Fig. 11: Modeled and approximated Z_{IFmax} vs. C_{IF}.

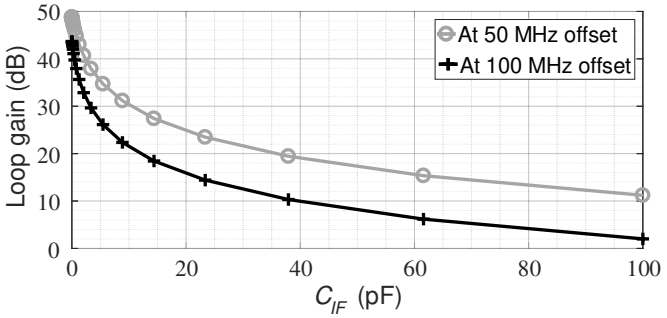


Fig. 12: TIA loop gain vs. C_{IF} at 50 MHz and 100 MHz frequency offsets.

gate. The measured IIP3 is, however, inline with state-of-the-art considering the high front-end gain. The simulation of the stand alone TIA is shown in Fig. 14. The two tone test simulation was performed for each notch frequency setting where one of the tones was placed at the notch frequency and the IM3 frequency is kept at 1 MHz. The simulation shows an improvement of more than 20 dB suggesting that the technique indeed improves IIP3 of the BB. It can be seen in TABLE III that the IIP2 improvement is more than 26 dB compared to only an improvement of 7 dB in [17], which also has a BB notch filter, and the P_{1dB} improvement exceeds 6 dB since BB compresses before the LNTA. This explains why the improvement in P_{1dB} is more than the IIP3 improvement. Extensive measurements of IIP2 on both I and Q channels of three samples show that the improvement is at least equal to that of the notch depth, regardless of how many G_{m-unit} cells are active.

To investigate the effectiveness of the proposed technique, a 5 MHz bandwidth blocker with QPSK modulation was used to test P_{1dB} and NF, see Fig. 17. As can be seen P_{1dB} improves by 6 dB and 9 dB for offsets of 100 MHz and 54 MHz respectively, so that P_{1dB} becomes mainly limited by the

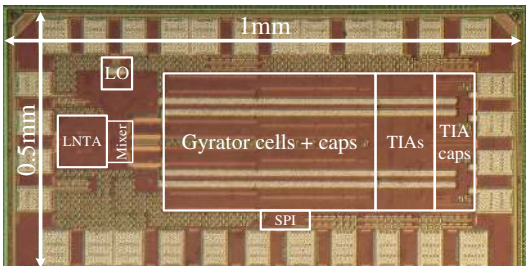


Fig. 13: Chip micro-graph.

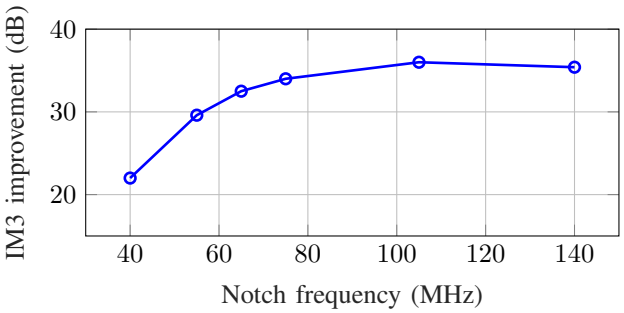


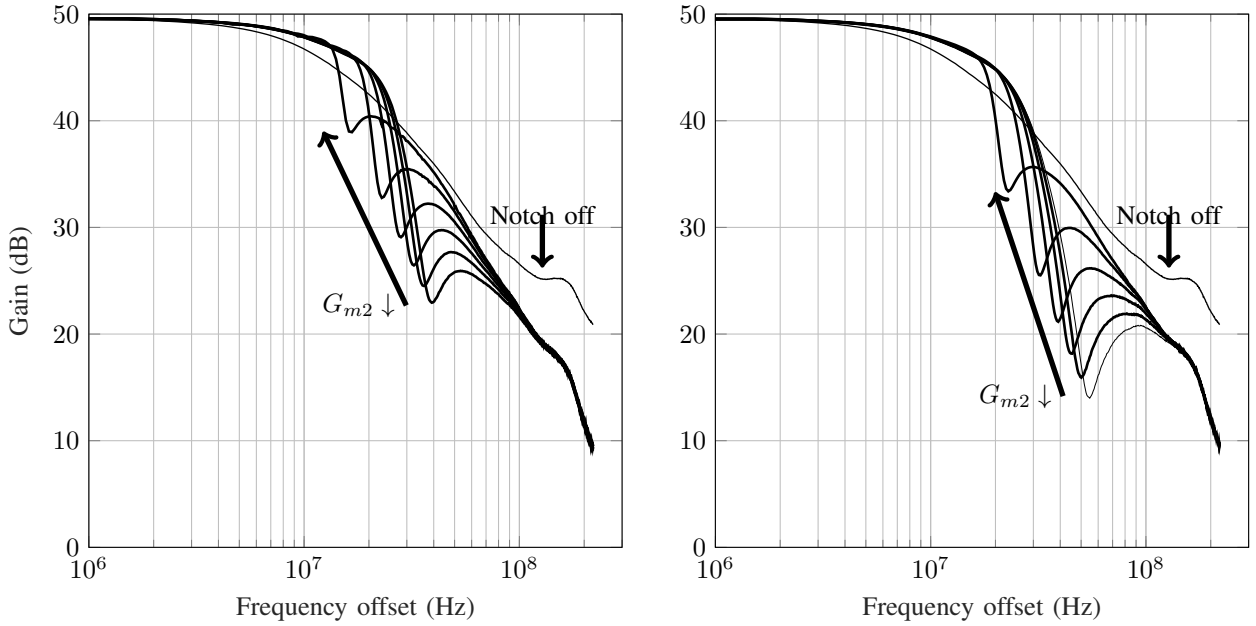
Fig. 14: Simulation of the improvement in IM3 for a stand-alone TIA when the notch filter is added. The notch frequency was swept using C_{gyr}.

TABLE III: Measured front-end performance summary

	w/o notch	w/ notch	Unit
System gain	49.5		dB
RF range	0.75-3		GHz
NF DSB	2.3		dB
S_{11}	< -10		dB
Supply	1.2		V
I_{DC} **LNTA**	16		mA
I_{DC} **LO**	9-22		mA
I_{DC} **TIA**	6		mA
BB bandwidth	10		MHz
Notch frequency	–	16-160	MHz
Notch depth	–	6-30	dB
I_{DC} **notch**	0	7.5-30	mA
IIP3	0	1	dBm
IIP2$^{(1)}$	39	65	dBm
$P_{1dB}{}^{(2,3)}$	-21.3	-14.6	dBm
$P_{1dB}{}^{(2,4)}$	-25.5	-16.5	dBm

(1) Measured worst case in both channels of three samples while improvement is remains similar in all samples.
(2) Blocker is a 5MHz QPSK modulated blocker.
(3) Blocker center frequency is 100MHz.
(4) Blocker center frequency is 54MHz.

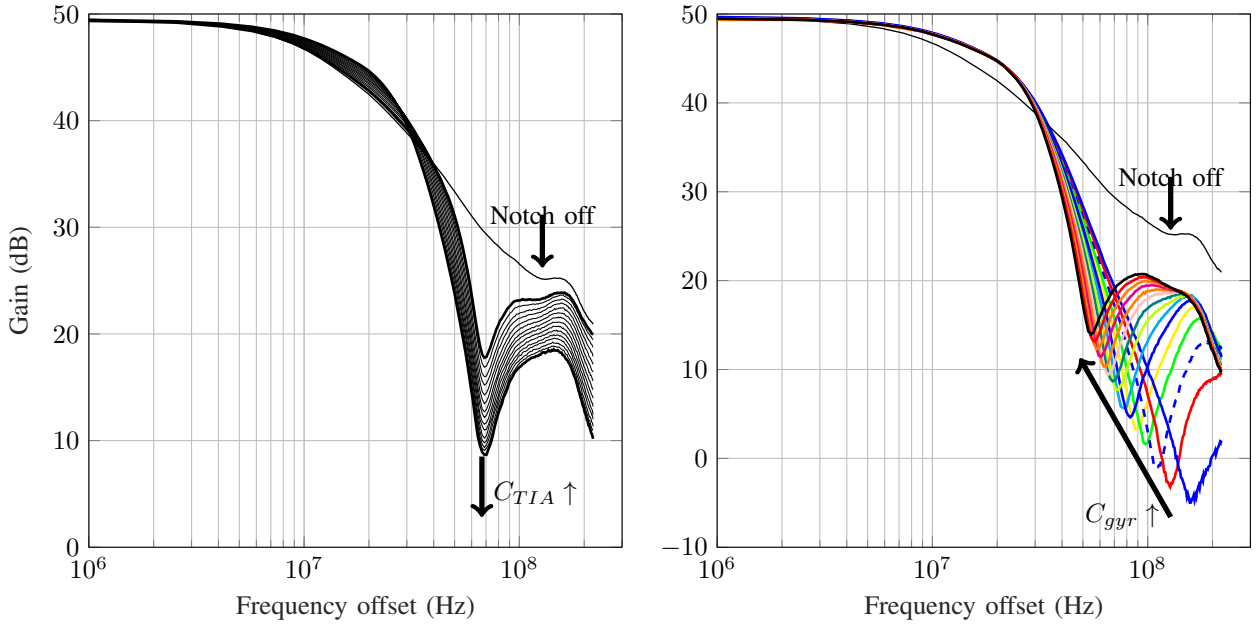
LNTA. To measure NF versus blocker power, a commercial SAW filter (EPCOS/LP75J) was used to filter the signal



(a) Setting $G_{m1} = G_{m-unit}$.

(b) Setting $G_{m1} = 2 \times G_{m-unit}$.

Fig. 15: System frequency response when G_{m2} is swept from $6 \times G_{m-unit}$ to $1 \times G_{m-unit}$.



(a) Notch depth vs. C_{TIA} sweep.

(b) Notch frequency vs. C_{gyr} sweep.

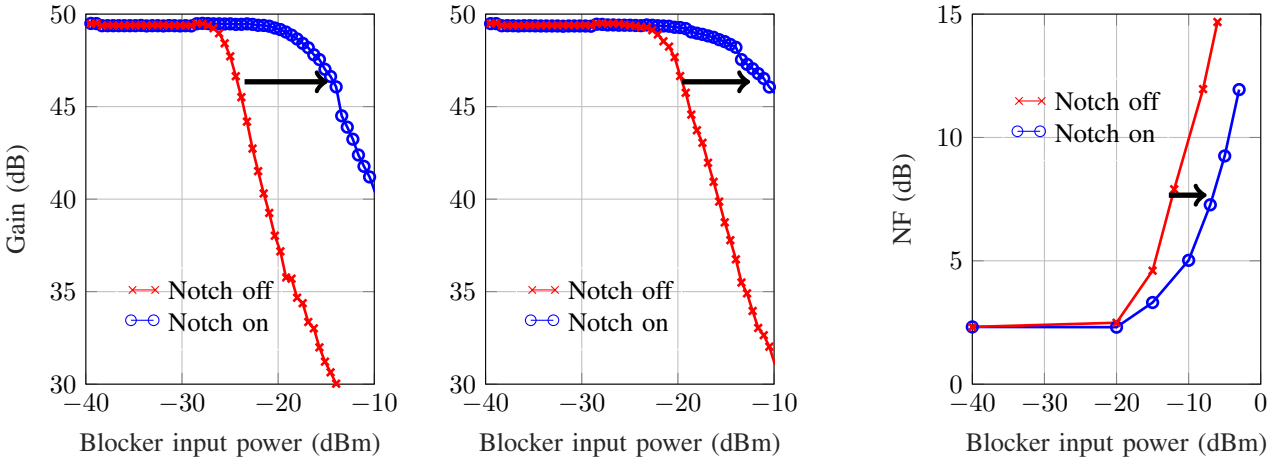
Fig. 16: The effect of C_{TIA} and C_{gyr} when $G_{m2} = 6 \times G_{m-unit}$ and $G_{m1} = 2 \times G_{m-unit}$.

generator noise. The blocker offset from LO was set to 120 MHz to fit into the pass band of the SAW filter. As can be seen in Fig. 17c, blocker NF crosses 10 dB at -4.5 dBm interference, compared to -10 dBm when the notch is deactivated.

The front-end is compared to state-of-the-art in TABLE IV. As can be seen this work achieves better than state-of-the-art IIP2 without any calibration of the mixer devices, if the system gain, which includes LNTA transconductance, mixer down-conversion loss and TIA trans-impedance, is taken into account. It has competitive overall performance and very small chip area.

IV. Conclusions

A receiver front-end with improved blocker resilience is presented. A programmable notch filter at the mixer output effectively sinks blocker currents without affecting the passband characteristics including the NF. The notch filter transfer function is analyzed and appears to interact with the frequency dependent input impedance of the TIA due to TIA bandwidth limitation. It is shown that the TIA input impedance peaking, which is normally a problem, can now be exploited to optimize notch filter efficiency. The notch frequency can be placed less than an octave away from the channel band-edge



(a) IGC with blocker at 54 MHz offset. (b) P_{1dB} with blocker at 100 MHz offset. (c) NF vs. OB blocker at 120 MHz to match the SAW filter stop band.

Fig. 17: Front-end P_{1dB} and NF with a 5 MHz wide QPSK blocker at different offset frequencies.

TABLE IV: Measured front-end performance summary

	This work		**JSSC'2010 [17]**	**ISSCC'2016 [27]**	**TMTT'2014 [28]**	**JSSC'2015 [29]**
Technique	LNTA with baseband notch filter		LNTA with active Tx leakage suppression	Filtering by aliasing	RF N-path filtering	Noise canceling and blocker filtering
Technology [nm]	65		180	65	40	40
RF range [GHz]	0.75 - 3		1.96	0.1-1	2.5	0.1 - 2.8
Gain [dB]	**49.5**		45	18.9	38.7	50
BB rejection [dB]	**54**	**11**	NA	36	NA	40
Δf**/BW**	**16**	**1.6**	128	3.5	12	20
IIP2 [dBm]	**>65**(1)		46	60	>46	50
OIP2(4) **[dBm]**	**>114**(1)		91	79	>85	100
Core area [mm^2]	**0.21**		2.5	2	0.75	0.8
IIP3 [dBm]	1		-4.8	17	>3	5
OIP3(4) **[dBm]**	50.5		40	36	>42	55
NF [dB]	2.3		4.9	6.5	3.5	1.8
P_{1dB} **[dBm]**	-14.6(2)		NA	8	-14	NA
Power [mW]	39 - 72 (3)		144	56 - 62	53	27 - 40

(1) Measured worst case in both channels of three samples while improvement is remains similar in all samples.
(2) Blocker is a 5MHz QPSK modulated blocker.
(3) Including LO current increase with frequency.
(4) Output referred intercept point.

without degrading the in-band gain. It is tunable from 16 MHz up to 160 MHz, for 10 MHz base-band channel bandwidth. Measurements demonstrate improvements in P_{1dB} by more than 6 dB at 54 MHz offset and in IIP2 by more than 26 dB at 100 MHz offset. The proposed technique reduces the burden of reduced supply voltages by diverting the blocker signal current away from the BB-voltage signal path.

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