

 Open access • Journal Article • DOI:10.1109/LED.2007.907267

Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate — [Source link](#)

[Chenming Hu](#), [YewChung Sermon Wu](#), [Chi-Ching Lin](#)

Institutions: [National Chiao Tung University](#)

Published on: 29 Oct 2007 - [IEEE Electron Device Letters](#) (IEEE)

Topics: [Amorphous silicon](#), [Substrate \(electronics\)](#), [Thin-film transistor](#) and [Silicon](#)

Related papers:

- [Polysilicon TFT technology for active matrix OLED displays](#)
- [An investigation of laser annealed and metal-induced crystallized polycrystalline silicon thin-film transistors](#)
- [Development and electrical properties of undoped polycrystalline silicon thin-film transistors](#)
- [Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization](#)
- [Gettering of Ni from Ni-metal induced lateral crystallization polycrystalline silicon films using a gettering substrate](#)

Share this paper:    

View more about this paper here: <https://typeset.io/papers/improving-the-electrical-properties-of-nilc-poly-si-films-2hmnktf95z>

Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate

Chen-Ming Hu, YewChung Sermon Wu, and Chi-Ching Lin

Abstract—Ni-metal-induced lateral crystallization (NILC) of amorphous silicon (α -Si) has been employed to fabricate polycrystalline silicon (poly-Si) thin-film transistors. However, current crystallization technology often leads to Ni and NiSi₂ precipitates being trapped, thus degrading the performance of the device. We proposed using α -Si-coated wafers as Ni-gettering substrates. After bonding the getting substrate with the NILC poly-Si film, both the Ni-metal impurity within the NILC poly-Si film and the leakage current were greatly reduced, thus increasing the ON/OFF current ratio.

Index Terms—Gettering, Ni-metal-induced lateral crystallization (NILC), thin-film transistors (TFTs).

I. INTRODUCTION

LOW-TEMPERATURE polycrystalline silicon thin-film transistors (TFTs) have attracted considerable interest for their use in active-matrix liquid crystal displays since they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates [1], [2]. Since poly-Si TFTs require glass substrates, intensive studies have been carried out, aiming to reduce the crystallization temperature of amorphous silicon (α -Si) films.

Ni-metal-induced lateral crystallization (NILC) is one of the achievements resulting from these efforts. In NILC, Ni islands are selectively deposited on top of α -Si films and allowed to crystallize at a temperature that is below 600 °C [3], [4]. Unfortunately, the poly-Si grain boundaries trap Ni and NiSi₂ precipitates, which increase the leakage current and shift the threshold voltage [5]–[9]. Therefore, Ni contamination should be reduced to enhance the performance of the device. Several metal-gettering methods have been utilized to reduce the amount of undesired metal impurity [10]–[14]. These processes are complicated and require high process temperatures. In this letter, an α -Si-coated Si wafer was utilized as Ni-gettering substrate. Through a specialized wafer-bonding technique [15], both the Ni contamination and the leakage current of NILC poly-Si film were significantly reduced.

II. EXPERIMENT

Two types of poly-Si films were investigated in this letter. The samples were designated as 1) “NILC-POLY,” which were

Manuscript received June 19, 2007; revised August 17, 2007. This work was supported by the National Science Council of Taiwan, R.O.C., under Grant NSC94-2216-E009-015 and NSC95-2622-E007-011. The review of this letter was arranged by Editor J. Sin.

The authors are with the Department of Material Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: sermonwu@stanfordalumni.org).

Digital Object Identifier 10.1109/LED.2007.907267

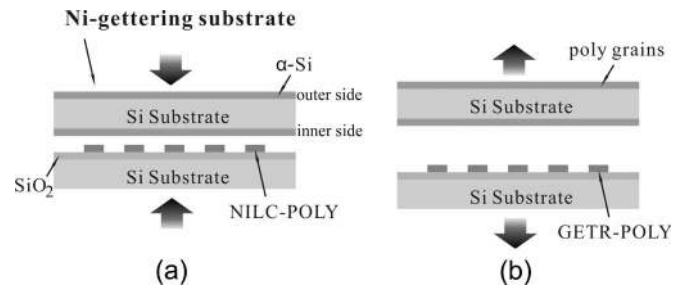


Fig. 1. Schematic of getting process. (a) NILC-POLY was bonded to the Ni-gettering substrate. They were then annealed at 550 °C for 12 h to carry out the getting process. (b) Separation of the two substrates.

poly-Si films that were fabricated by traditional NILC method, and 2) “GETR-POLY,” which were poly-Si films that were fabricated by the same traditional NILC method with an additional Ni-gettering process. The basic NILC fabrication process of both poly-Si films began with 4-in Si(100) wafer substrates, where wet oxide films of 500 nm were grown using a H₂/O₂ mixture. Silane-based α -Si films with a thickness of 1000 Å were deposited using low-pressure chemical vapor deposition (LPCVD). The photoresist was patterned to form the desired Ni lines, and a 20-Å-thick Ni film was deposited on the α -Si. The samples were then dipped into acetone for 5 min to remove the photoresist and subsequently annealed at 550 °C for 12 h to form the NILC poly-Si film. To reduce Ni contamination, the unreacted Ni metal was removed by chemical etching. Reactive ion etching was employed to form islands of poly-Si regions on the wafers.

For the Ni-gettering substrate, 1000-Å-thick α -Si films were directly deposited onto both sides of the Si substrate using LPCVD, as shown in Fig. 1. To form GETR-POLY, NILC-POLY was bonded to the Ni-gettering substrate [16] and then annealed at 550 °C for an additional 12 h. Following the getting process, the Ni-gettering substrate was separated by razor blade.

III. RESULTS AND DISCUSSION

It was found that NILC poly-Si was composed of needle-like Si grains. After the samples were dipped into a silicide-etching solution (HNO₃ : NH₄F : H₂O = 4:1:50), numerous holes were observed at the boundaries where two NILC poly-Si fronts intersected, as shown in Fig. 2. These holes were residues of the Ni silicides that had been etched away by the silicide-etching solution.

After the getting process, no silicide-etched holes were found on GETR-POLY, indicating that a substantial number

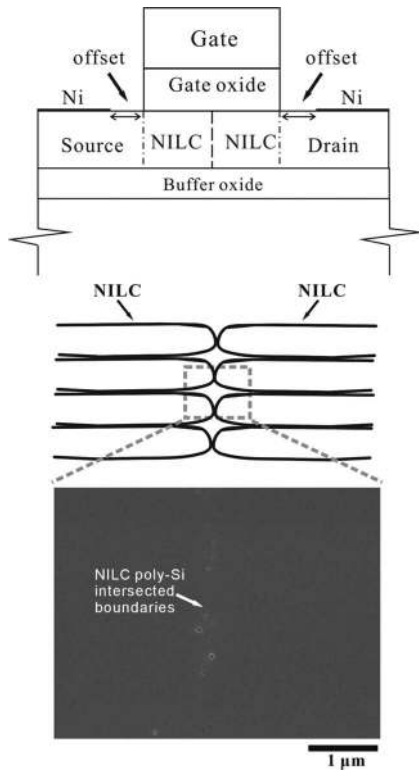


Fig. 2. Schematic of the TFT device structure and a scanning electron microscopy image of NILC poly-Si front region (after etching by silicidetching solution).

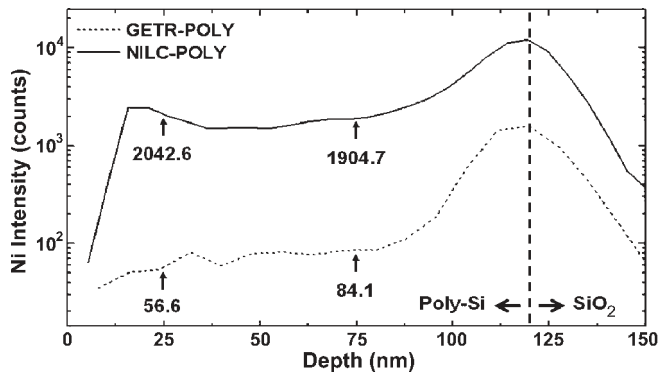


Fig. 3. SIMS depth profile of nickel in the poly-Si film.

of Ni atoms had diffused into the Ni-gettering substrate. Secondary-ion mass spectroscopy (SIMS) analysis also revealed that the Ni concentration in GETR-POLY had been reduced to 1/30, compared with that in NILC-POLY, as shown in Fig. 3.

Examining the Ni-gettering substrate revealed that most of the inner and outer Si films were composed of NILC poly-Si. In other words, during the gettering process, Ni atoms diffused from NILC-POLY to the gettering substrate due to a concentration gradient. When Ni atoms reached the inner α -Si film, α -Si was transformed into needlelike poly-Si grains. Then, Ni atoms were allowed to diffuse through the Si wafer. The diffusion time can be estimated by the following equation: $\sqrt{Dt} = l$, where D is the Ni diffusivity [17] and l is the

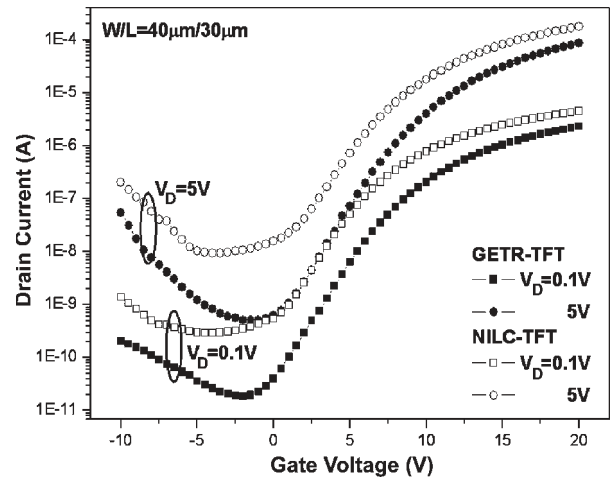


Fig. 4. Transfer characteristics (I_D - V_G curves) of GETR-TFT and NILC-TFT.

TABLE I
DEVICE CHARACTERISTICS OF GETR-TFT AND
NILC-TFT (12 DEVICES WERE MEASURED)

$W/L=40 \mu\text{m}/30 \mu\text{m}$	GETR TFT	NILC TFT
Mobility ($\text{cm}^2/\text{V}\cdot\text{s}$) @ $V_d=0.1\text{V}$	52.3 ± 7.3	80.3 ± 6.2
Subthreshold slope (V/dec) @ $V_d=0.1\text{V}$	1.13 ± 0.12	1.02 ± 0.05
Threshold voltage (V) @ $V_d=0.1\text{V}$	7.5 ± 1.4	2.9 ± 0.7
on/off ratio current (10^5) @ $V_d=5\text{V}$	1.11 ± 0.26	0.13 ± 0.07
Minimum leakage current / channel width ($\text{pA}/\mu\text{m}$) @ $V_d=5\text{V}$	13.9 ± 2.9	473.9 ± 243.9

thickness of the Si wafer ($= 500 \mu\text{m}$). Therefore, it takes only 15 min for Ni atoms to pass through the Si wafer. When Ni atoms reached the outer α -Si films, α -Si was again transformed into needlelike poly-Si grains. Since Ni atoms could pass through the Si wafer in just 15 min, most of the outer α -Si films were transformed into poly-Si after the 12-h gettering process.

The performance of TFT devices was evaluated by examining the quality of poly-Si films. As shown in Fig. 2, numerous Ni residues were located at the boundaries where two NILC poly-Si fronts intersected. These boundary regions were definitely less suitable for fabricating TFT devices. However, these regions were quite sensitive to whether the Ni residues had been reduced and were therefore ideal for elucidating the effect of “Ni gettering” on the performance of TFTs.

Fig. 4 shows the transfer characteristics (I_D - V_G curves) of TFTs that were measured at two different drain voltages ($V_{DS} = 0.1$ and 5 V). The measured as well as extracted key device parameters are summarized in Table I. The ON/OFF current ratio I_{ON}/I_{OFF} and the minimum leakage current were measured at a drain voltage of $V_{DS} = 5$ V. Threshold voltage V_{TH} and the subthreshold swing were measured at $V_{DS} = 0.1$ V. Field-effect mobility μ_{FE} was extracted from the maximum value of transconductance at $V_{DS} = 0.1$ V.

As shown in Table I, the device transfer characteristics of GETR-TFT showed an 8.5-fold increase in the ON/OFF current ratio and a 34.1-fold decrease in the minimum leakage

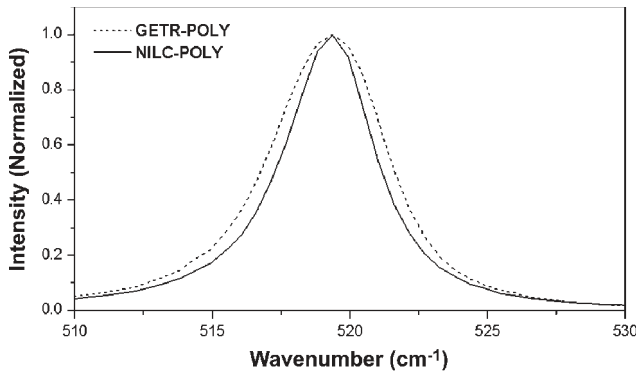


Fig. 5. Raman spectra of GETR-POLY and NILC-POLY.

current compared with those of NILC-TFT. These improvements were attributed to the reduction in Ni concentration in the GETR-POLY film. In the poly-Si film, Ni residues serve as deep-level traps, which promote thermionic emission-dominated leakage current in the low-gate and drain-voltage region [18], [19]. With the reduction in Ni concentration, the minimum leakage current was reduced, thus increasing the ON/OFF current ratio.

Since the amount of Ni residues in GETR-TFT was much less than that in NILC-TFT, the defects (caused by Ni residues) in the channel of GETR-TFT were expected to be less than those of NILC-TFT. In other words, the mobility of GETR-TFT should be higher than that of NILC-TFT. However, as shown in Table I, the mobility of GETR-TFT ($52.3 \text{ cm}^2/\text{V} \cdot \text{s}$) was not as good as that of NILC-TFT ($80.3 \text{ cm}^2/\text{V} \cdot \text{s}$). It seemed that the crystal quality of GETR-POLY was poorer than that of NILC-POLY.

Laser Raman spectroscopy was employed to study the quality of the poly-Si film. As shown in Fig. 5, NILC-POLY had a slightly smaller full-width at half-maximum value. In other words, the crystallinity of NILC-POLY was slightly better than that of GETR-POLY. This might be because the gettering of Ni in GETR-POLY results in less complete crystallization with smaller grains.

Moreover, as shown in Table I, the V_{TH} of GETR-TFT was 7.5 V, whereas that of NILC-TFT was 2.9 V. Compared with that of NILC-TFT, the I_D - V_G curve of GETR-TFT showed a positive shift. These results are similar to the findings of Lee *et al.* [20] on the performance of NILC p-channel poly-Si TFTs, in which two different thicknesses (5 and 60 Å) of Ni seed layers were employed to fabricate p-channel TFTs. They found that the 60-Å Ni seed layer led to a more negative V_{TH} than the 5-Å one, implying that the 60-Å seed layer could leave more nickel residues within the Si film. These Ni residues could cause a high density of positive charge at the oxide/poly-Si interface. The negative shift of V_{TH} was due to the presence of these positive charges and nickel-related donorlike defects in the 60-Å NILC poly-Si film.

In our studies, compared with GETR-POLY, NILC-POLY had more nickel residues within the poly-Si film, particularly, at the boundaries where two NILC poly-Si fronts intersected (Fig. 3). As a result, the V_{TH} and the I_D - V_G curve of GETR-TFT had positive shifts.

IV. CONCLUSION

An investigation of the relationship between Ni-gettering substrates and the performance of NILC poly-Si (NILC-POLY) TFTs had led to the development of an effective Ni-gettering process for NILC poly-Si films. Ni-gettering substrates were fabricated by coating α -Si films on both sides of Si wafers. It was found that the silicide-etched holes at NILC-POLY grain boundaries were greatly reduced after the Ni-gettering process. The Ni concentration within NILC-POLY was reduced to 1/30. The device transfer characteristics of GETR-TFT showed an 8.5-fold increase in the ON/OFF current ratio and a 34.1-fold decrease in the minimum leakage current compared with those of NILC-TFT.

ACKNOWLEDGMENT

The authors would like to thank the National Nano Device Laboratory of the National Science Council and the Nano Facility Center of National Chiao Tung University for their technical support.

REFERENCES

- [1] M. Stewart, R. S. Howell, L. Pires, and M. K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 845–851, May 2001.
- [2] W.-K. Chen, *Linear Networks and Systems*. Belmont, CA: Wadsworth, 1993, pp. 123–135.
- [3] S. W. Lee and S. K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 17, no. 4, pp. 160–162, Apr. 1996.
- [4] Z. Meng, M. Wang, and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," *IEEE Trans. Electron Devices*, vol. 47, no. 2, pp. 404–409, Feb. 2000.
- [5] P. J. van der Zaag, M. A. Verheijen, S. Y. Yoon, and N. D. Young, "Explanation for the leakage current in polycrystalline-silicon thin-film transistors made by Ni-silicide mediated crystallization," *Appl. Phys. Lett.*, vol. 81, no. 18, pp. 3404–3406, Oct. 2002.
- [6] G. A. Bhat, Z. Jin, H. S. Kwok, and M. Wong, "Effects of longitudinal grain boundaries on the performance of MILC-TFTs," *IEEE Electron Device Lett.*, vol. 20, no. 2, pp. 97–99, Feb. 1999.
- [7] Z. Jin, K. Moulding, H. S. Kwok, and M. Wong, "Performance of thin-film transistors with ultrathin Ni-MILC polycrystalline silicon channel layers," *IEEE Electron Device Lett.*, vol. 20, no. 4, pp. 167–169, Apr. 1999.
- [8] G. A. Bhat, H. S. Kwok, and M. Wong, "Behavior of the drain leakage current in metal-induced laterally crystallized thin film transistors," *Solid State Electron.*, vol. 44, no. 7, pp. 1321–1324, Jul. 2000.
- [9] D. Murley, N. Young, M. Trainor, and D. McCulloch, "An investigation of laser annealed and metal-induced crystallized polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 48, no. 6, pp. 1145–1151, Jun. 2001.
- [10] B. Mohadjeri, J. S. Williams, and J. W. Leung, "Gettering of nickel to cavities in silicon introduced by hydrogen implantation," *Appl. Phys. Lett.*, vol. 66, no. 15, pp. 1889–1891, Apr. 1995.
- [11] M. Zhang, X. Zeng, P. K. Chu, R. Scholz, and C. Lin, "Nickel precipitation at nanocavities in separation by implantation of oxygen," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 18, no. 5, pp. 2249–2253, Sep. 2000.
- [12] R. Hoelzl, K. J. Range, L. Fabry, J. Hage, and V. Raineri, "Gettering efficiencies of polysilicon-, stacking fault- and He-implanted backsides for Cu and Ni," *Mater. Sci. Eng. B*, vol. 73, no. 1, pp. 95–98, Apr. 2000.
- [13] S. Martinuzzi, I. Perichaud, and J. J. Simon, "External gettering by aluminum-silicon alloying observed from carrier recombination at dislocations in float zone silicon wafers," *Appl. Phys. Lett.*, vol. 70, no. 20, pp. 2744–2746, May 1997.
- [14] S. Martinuzzi, N. G. Henquinet, I. Périchaud, G. Mathieu, and F. Torregrossa, "Efficiency of cavity gettering in single and in multicrystalline silicon wafers," *Mater. Sci. Eng. B*, vol. 71, no. 1, pp. 229–232, Feb. 2000.

- [15] P. C. Liu, C. Y. Hou, and Y. S. Wu, "Wafer bonding for high-brightness light-emitting diodes via indium tin oxide intermediate layers," *Thin Solid Films*, vol. 478, no. 1/2, pp. 280–285, May 2005.
- [16] C. P. Chao, Y. S. Wu, T. L. Lee, and Y. H. Wang, "Wafer bonding by Ni-induced crystallization of amorphous silicon," *Jpn. J. Appl. Phys.*, vol. 42, no. 9A, pp. 5527–5530, Sep. 2003.
- [17] A. M. Myasnik, M. C. Poon, P. C. Chan, K. L. Ng, M. S. Chan, W. Y. Chan, S. Singla, and C. Y. Yuen, "On mechanism of nickel diffusion during metal induced lateral crystallization of amorphous silicon," *Mater. Res. Soc. Symp. Proc.*, vol. 715, pp. A22.11.1–A22.11.4, 2002.
- [18] K. R. Olasupo and M. K. Hatalis, "Leakage current mechanism in sub-micron polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1218–1223, Aug. 1996.
- [19] M. Yazaki, S. Takenaka, and H. Ohshima, "Conduction mechanism of leakage current observed in metal–oxide–semiconductor transistors and poly-Si thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 31, no. 2A, pp. 206–209, Feb. 1992.
- [20] Y. Lee, S. Bae, and S. J. Fonash, "High-performance nonhydrogenated nickel-induced laterally crystallized P-channel poly-Si TFTs," *IEEE Electron Device Lett.*, vol. 26, no. 12, pp. 900–902, Dec. 2005.