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Improving the Linearity and Efficiency of RF Power Amplifiers

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This article describes improvements in device technology and design techniques that will enable power amplifiers with higher efficiency and better linearity performance — at higher frequencies

A growing number of semiconductor technologies are being applied to RF power transistor applications. These technologies include Si LDMOS FET, SiGe HBT, InGaP HBT, GaAs MESFET, AlGaAs pHEMT, SiC MESFET and AlGaN/GaN HEMT. The dependencies of linearity and efficiency of such technologies are often common, such as transconductance derivatives, capacitance variations, breakdown effects and parasitic resistances. This article overviews the work that has been achieved to date to maximize linearity and efficiency in the most promising technologies, as related specifically to infrastructure applications. The article also addresses the increasing number of device and circuit level techniques that are being used to enhance these two important parameters as required for IM3, ACPR and ACLR suppression in 3G systems such as W-CDMA/UMTS.

This article focuses on high power (that is greater than 10 watt) RF transistor technologies where digital modulation techniques are demanding higher and higher peak-to-average ratios (PARs) and thus higher peak powers. Peak and average DC-to-RF efficiencies have become critical parameters, and much attention is being focused in decreasing multi-carrier intermodulation distortion, adjacent channel power ratios (ACPRs) and adjacent channel leakage ratios (ACLRs). Unfortunately, improving transistor linearity often leads to decreased efficiency which directly affects overall system efficiency, heat removal, size and cost.

Competing Technologies

The generation of solid state RF power has been in existence since the late 1960s when silicon bipolar transistors were introduced by such companies as TRW and RCA (ref. 1). Today there are a range of technologies available, including silicon bipolar, silicon LDMOS FET, GaAs MESFET, GaAs pHEMT, AlGaAs/InGaAs HFET, GaAs, InP, InGaP and SiGe HBT as well as wide bandgap transistors such as SiC MESFET and AlGaN/GaN

Technology	Price/Watt	Power Density	Supply Voltage	Linearity	Frequency	PAE
Si BJT	Low Cost	Medium	26 V	Poor	<2 GHz	Low
SiGe BJT	Low Cost	Medium	<20 V	Good	>2 GHz	High
Si LDMOS	Low Cost	Low	26 V	Very Good	<3 GHz	Medium
GaAs MESFET	Competitive	Medium	12 V	Good	>2 GHz	Medium
GaAs pHEMT	Medium	Medium	8 V to 12 V	Very Good	>2 GHz	High
GaAs HBT	Competitive	High	8 V to 26 V	Good	>2 GHz	High
SiC MESFET	Competitive	Very High	48 V	Good	>4 GHz	Medium
GaN HEMT	N/A	Very High	48 V	Promising	>12 GHz	High

Table 1 · Overview of competing solid-state RF power transistor technologies.

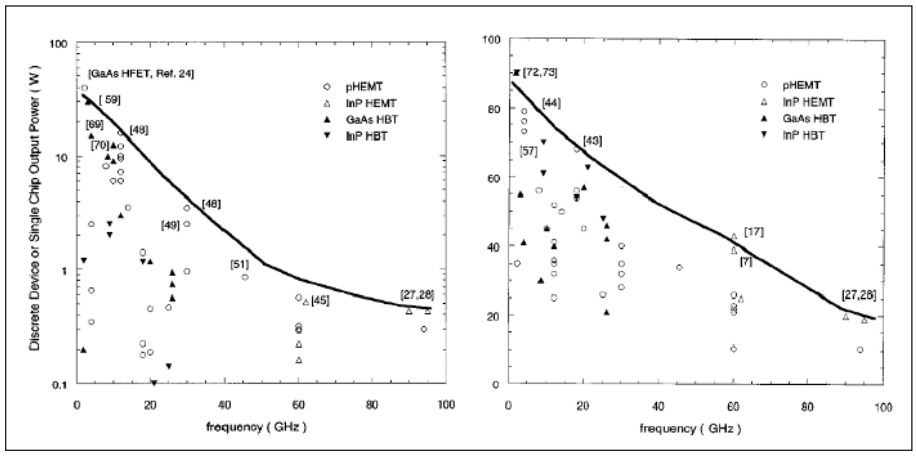

Figure 1 · Discrete device output powers and efficiencies versus frequency (after Nguyen and Micovic, ref. 2).

HEMT. Table 1 presents a brief comparative overview of some of these technologies. Figure 1 shows the trends in discrete transistor output powers and efficiencies as a function of frequency for HEMTs and HBTs. Single die peak powers for Si LDMOS FETs have reached greater than 60 watts at 2 GHz.

Of particular interest today are wide bandgap transistors such as silicon carbide (SiC) MESFETs and gallium nitride (GaN) HEMTs. Such transistors exhibit very high RF power densities (watts per mm of gate width) compared to any other technologies (by a factor of 10 over GaAs MESFET for example) (ref. 3 and 4).

Wide band-gap transistors fabricated from 4H-SiC and AlGaN/GaN offer superior RF performance, particularly at elevated temperatures, compared to comparable components fabricated from GaAs or Si. RF output powers on the order of 4 to 7 W/mm and 10-12 W/mm are achievable from SiC MESFETs and AlGaN/GaN HFETs respectively.

Achievement of higher power densities is a priority for RF power technologies as it reduces size, which is important in both fixed and mobile platforms. It also provides higher working impedances, which are important for wider bandwidth operation, simpler circuits and easier manufacture.

Figure 2 shows a comparison of the input and output impedances of a 20 mm GaN HEMT delivering greater than 100 watts CW peak power with a commercially available Si LDMOS FET of similar power capability. Clearly, the GaN HEMT has much more convenient impedance levels which can also result in easier packaging whereby no internal pre-matching is needed (Figure 3). The higher gain of the GaN device requires lower drive drive. Initial linearity measurements show similar performance for the two device technologies.

Both SiC MESFETs and GaN HEMTs show promising efficiencies and linearities. For example, Figure 4 shows the peak efficiencies of a GaN HEMT as a function of drain-to-source voltage over a range of 10 to 40 volts. Note that the drain efficiency remains almost constant at greater than 60 percent over the complete voltage range which enables efficiencies to be optimized at reasonable back-off powers (e.g. up to 10 dB). Figure 5 shows an example of the promising linearity that can be obtained from such wide bandgap transistors. The figure shows a comparison between a 1.2 mm gate width GaAs pHEMT and a 1 mm gate width AlGaN HEMT. Although these transistors have comparable gate widths the AlGaN HEMT provides >10 dBm more output power with improved third order intermodulation distortion.

	Modeled GaN 20 mm HEMT	Motorola MRF18090B
P_{out}	100 Watts	100 Watts
Z_{in}	25 +j49 Ω	2 +j8 Ω
Z_{out}	3.8 +j0.8 Ω	1.3+j2.2 Ω
Gain	>25 dB	>13 dB

- Similar packages assumed—matching capacitor included for GaN input
- No output matching for GaN device
- V_{ds} = 35 V GaN, 26 V for LDMOS

Figure 2 · High power GaN HEMT in a cellular base station application.

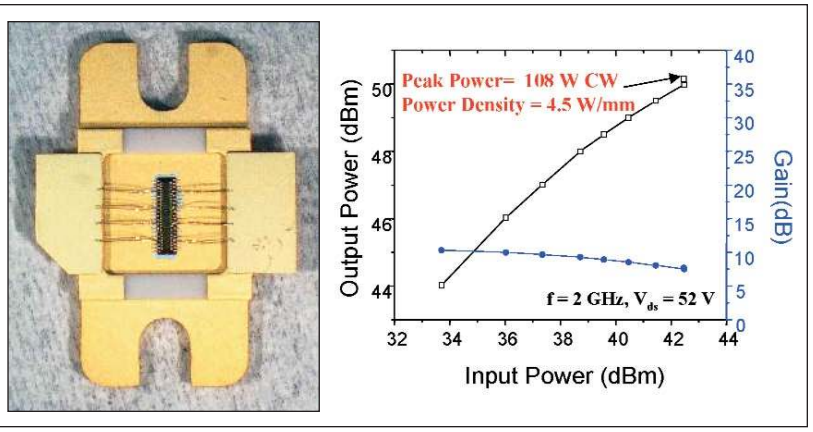

Figure 3 · Example of a packaged 100 watt GaN HEMT (ref. 20). P_{out} is >100 W and peak drain efficiency is 54 percent.

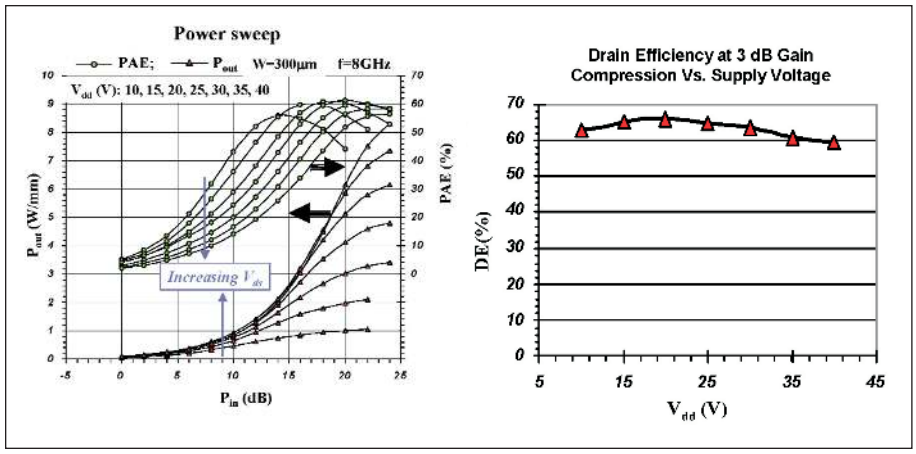

Figure 4 · Characterization of AlGaN/GaN HEMTs using a fixed load at varying supply voltages (ref. 21).

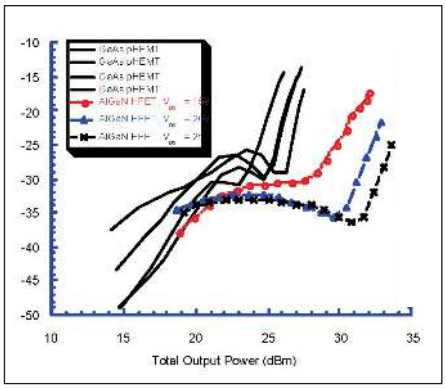

Figure 5 · Intermodulation performance of AlGaN HEMT compared to GaAs pHEMT of comparable gate periphery.

Ways of improving Efficiency and Linearity

There are basically three ways to improve the efficiency and linearity of RF power transistors:

- Intrinsic technology improvements
- Device/circuit level improvements
- Circuit/sub-system level improvements

This article concentrates on the first two methods and does not include sub-system linearization techniques such as feedforward and pre-distortion. These are covered well by authors such as Cripps (ref. 5) and Pothercary (ref. 6).

There are many common factors in the determination of linearity in various RF power transistor technologies. These include changing impedance levels (both input and output) as a function of RF signal level; changing transconductance and its derivatives as a function of DC bias and RF signal levels (which is a primary determinant of multi-tone intermodulation characteristics); changing capacitances and their derivatives as a function of DC bias and RF signal levels; breakdown and substrate conduction effects; and, of course, class of operation commonly Class A through E.

There are a number of ways in which basic transistor linearity can be improved:

- By increasing the transconductance or beta of the device and its rate of increase from threshold. Examples of this are the linearity improvements provided by pHEMTs in comparison to MESFETs as well as the ability to engineer channel and drain improvements in HBTs and LDMOS FETs
- By increasing working voltage, which tends to decrease the capacitance of the transistor per watt of RF power
- By decreasing odd order transconductance derivatives
- By reducing capacitance variations with voltage, e.g. CBC in HBTs
- By increasing breakdown voltage, for example, using a double gate recess versus a single gate recess in a MESFET
- By reducing surface trapped charge

A common expression for the relationship between drain current and gate voltage in a FET is given by Equation (1), where I_D is the large-signal drain current and V_G and i_D are incremental gate voltage and drain current around the quiescent bias point I_D ($V_{G,0}$) respectively. In a two-tone test with frequencies ω_1 and ω_2, third order intermodulation products with frequencies of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are generated by the third term in Equation (1).

The third term in Equation (1) is directly related to the rate of change of transconductance with applied gate voltage. Hence, if the field-effect transistor can be engineered with as constant a change in transconductance as possible as it comes out of threshold and before it enters saturation then the linearity of the device will be improved.

An example of the optimization of the epitaxial layer structure and gate recess that provides high and steep transconductance change close to threshold is shown in Figure 6 from work reported by Takenaka et al in 2000 (ref. 7). In this example, third order intermodulation distortion was decreased by greater than 10 dBc over a wide range of output power levels.

Transistor efficiency can be

$$i_D = dI_D/dV_{G|V=VG,0}\, V_G + d^2I_D/2dV_G{}^2{}_{|V=VG,0}\, V_G{}^2 + d^3I_D/6dV_G{}^3{}_{|V=VG,0}\, V_G{}^3 = g_1V_G + g_2V_G{}^2 + g_3V_G{}^3$$

Equation 1 · The relationship between drain current and gate voltage.

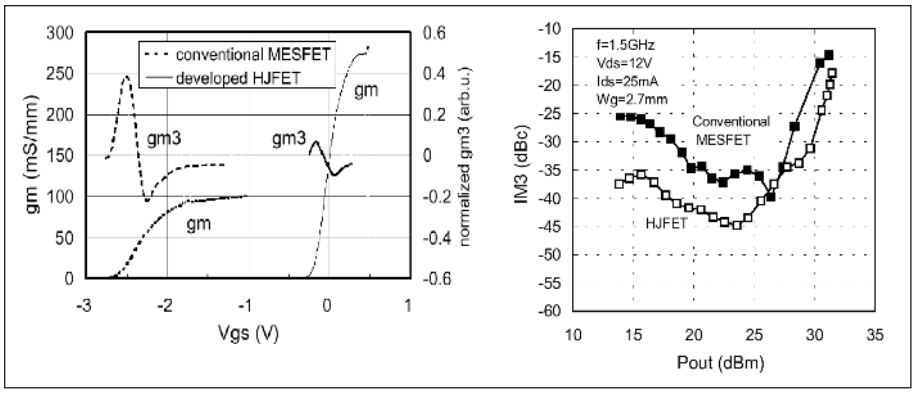

Figure 6 · Optimization of transconductance and reduction in transconductance derivative.

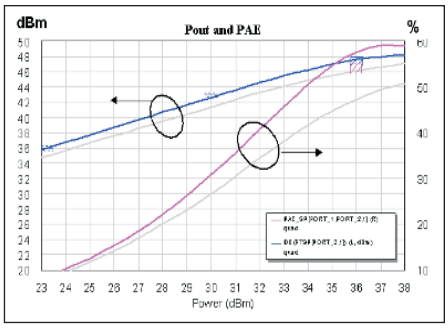

Figure 7 · Output Power and Power-Added Efficiency as a function of RDSON for a Si LDMOS FET power amplifier operating at 2.14 GHz.

improved in a number of ways:

- By reducing parasitic resistances such as R_D and R_{DSON} in LDMOS FETs
- By optimizing die layout
- By reducing thermal resistance which decreases device self heating
- By optimizing various properties such as substrate materials and thicknesses

Figure 7 shows an example of the effect that R_{DSON} can have on the output power and power added efficiency of a 60 watt hybrid amplifier consisting of two, 30 watt LDMOS FETs operating between quadrature hybrids. R_{DSON} is the total resistance of the device when it is operating (as a "switch") at the extreme of its load-line (between drain and source but excluding parasitic drain resistance). In this example R_{DSON} is changed from 0.13 to 0.26 ohms resulting in 9 percent degradation in peak efficiency and over 1.5 dBm reduction in output power.

At the device/circuit level there are a number of ways to improve both efficiency and linearity.

- By employing harmonic terminations (refs. 8, 9);
- By employing Doherty amplifier configurations (refs. 10, 11, 12)
- By employing derivative superposition approaches and transconductance compensation (refs. 13, 14, 15, 16 and 17)
- By employing novel Class AB-C approaches (ref. 18)
- By employing dynamic power supply approaches (ref. 19)

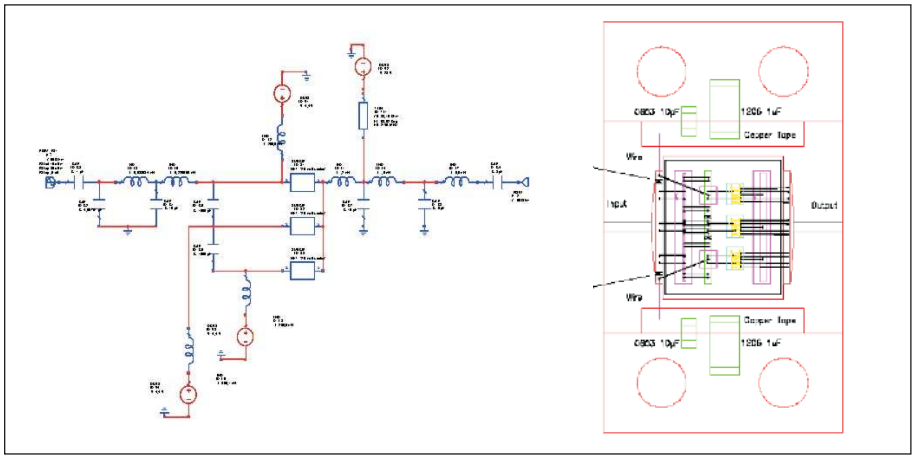

Figure 8(a) · Circuit diagram of Transconductance Derivative Superposition applied to a 15 watt LDMOS FET power amplifier, with a hybrid circuit implementation (right).

This article concentrates on one aspect of device/circuit level improvement—so-called derivative superposition. Webster et al (ref. 13) originally described this concept. In the approach a number of transistors are connected in parallel such that the negative d^3I_D/dV_G^3 (see Equation 1) of one transistor cancels the positive d^3I_D/dV_G^3 of another transistor which is biased at a different gate drive. The positive and negative characteristics of d^3I_D/dV_G^3 are not symmetrical so "flat compensated IM3 regions" can be extended by using more transistors with different gate widths.

Figure 8(a) shows a circuit diagram of such a scheme where 5 watt LDMOS FET die have been used in a mini-hybrid approach. In this case each FET had the same gate width but the gate voltage applied to each FET was different resulting in 7 to 10 dBc improvement in IM3 over the 8 to 13 dB back-off range (Figure 8(b)).

By using different gate width devices and increasing the number of FETs, IM3 improvements can be increased. Figure 9 shows an example of four LDMOS FETs being used where the total output power at 1 dB compression is 48 dBm.

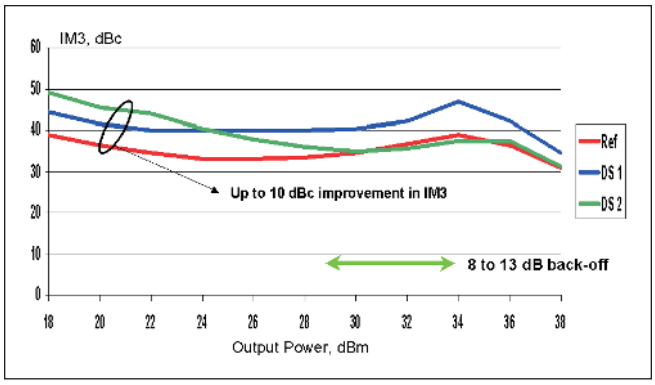

Figure 8(b) · Improvement in IM3 for a 3 FET transconductance derivative superposition circuit.

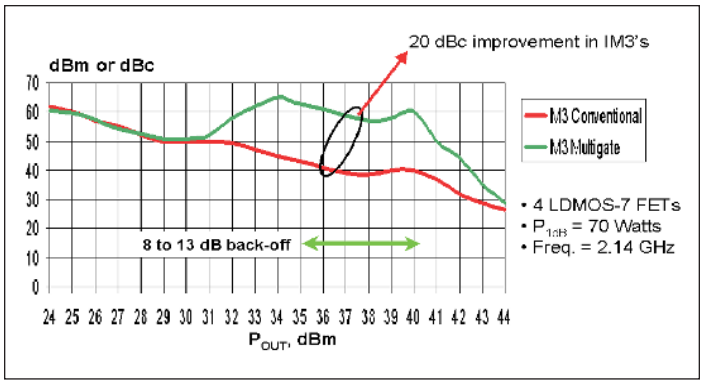

Figure 9 · Example of IM3 improvement for a 4 FET transconductance derivative superposition arrangement.

Table 2 shows a comparison of some of the device/circuit level linearization/efficiency improvement techniques that can be applied to a range of transistor technologies. The emphasis today is to develop methods that can replace feedforward and other techniques to reduce complexity and cost.

The use of a limited combination of approaches such as derivative superposition to improve linearity and Doherty amplification to improve efficiency can provide solutions which can then be incorporated into sub-system approaches such as predistortion, dynamic power supplies etc.. The challenge is to implement these new schemes in a cost-effective manner.

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Technique	Pros	Cons
Device Selection, e.g. HEMT versus LDMOS-FET (see Table 1)	Intrinsic solution offering batch manufacturing	Process maturity
Device Optimization	Intrinsic solution offering batch manufacturing	Process maturity
Derivative Superposition	Relatively simple; Discrete or IC solution	Requires reproducible threshold voltage
Harmonic Terminations	Relatively simple	Limited improvements
Doherty	Well proven	Can be complex for higher order Doherty
Dynamic Power Supplies	Relatively complex	Needs high operating voltage for optimum performance. Wide bandgap is a good candidate

Table 2 · Comparison of various device/circuit level techniques to improve transistor efficiency and linearity.

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