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Improving the performance of amorphous and crystalline silicon heterojunction solar cells by monitoring surface passivation

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ABSTRACT

The influence of thermal annealing on the crystalline silicon surface passivating properties of selected amorphous silicon containing layer stacks (including intrinsic and doped films), as well as the correlation with silicon heterojunction solar cell performance has been investigated. All samples have been isochronally annealed for 1 h in an N_2 ambient at temperatures between 150 °C and 300 °C in incremental steps of 15 °C. For intrinsic films and intrinsic/n-type stacks, an improvement in passivation quality is observed up to 255 °C and 270 °C, respectively, and a deterioration at higher temperatures. For intrinsic/n-type a-Si:H layer stacks, a maximum minority carrier lifetime of 13.3 ms at an injection level of 10^{15} cm^{-3} has been measured. In contrast, for intrinsic/p-type a-Si:H layer stacks, a deterioration in passivation is observed upon annealing over the whole temperature range. Comparing the lifetime values and trends for the different layer stacks to the performance of the corresponding cells, it is inferred that the intrinsic/p-layer stack is limiting device performance. Furthermore, thermal annealing of p-type layers should be avoided entirely. We therefore propose an adapted processing sequence, leading to a substantial improvement in efficiency to 16.7%, well above the efficiency of 15.8% obtained with the 'standard' processing sequence.

1. Introduction

Silicon heterojunction (SHJ) solar cells consisting of hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si) form a potentially inexpensive alternative to standard p–n homojunction c-Si solar cells [1–4]. In conventional c-Si solar cells, the p–n junction is formed by a thermal diffusion for which temperatures around 900 °C are required. In case of a-Si:H/c-Si based heterojunction solar cell processing, temperatures below 200 °C are typically used, as the p–n junction is formed by depositing a thin doped a-Si:H layer on a c-Si wafer. This lower temperature processing (i) decreases the thermal budget of the production process, (ii) limits thermal degradation of the c-Si wafer quality, and (iii) enables the use of thinner wafers (<100 μm), avoiding warpage issues associated with traditional high temperature processing.

Surface passivation of c-Si is a key requirement in optimizing the performance of SHJ solar cells. The design of SHJ solar cells allows for the deposition of a surface passivating thin intrinsic layer consisting of a-Si:H before depositing the doped emitter and back surface field (BSF) layers, which can increase the open circuit voltage (V_{OC}) of these solar cell structures to values exceeding 720 mV [2,3]. Sanyo [1] has introduced this concept in 1992 and due to their excellent results, inspired many other groups worldwide to focus on this concept as well.

The passivating properties of intrinsic a-Si:H have been widely studied [5–9]. In SHJ cells, however, the influence of the doped layers is also very crucial. The BSF creates additional field effect passivation, repelling minority charge carriers from the a-Si:H/c-Si interface at the back side, thereby further reducing recombination losses. At the emitter side, minority carriers are passing through the a-Si:H/c-Si interface region in the front side, which enhances recombination losses. Furthermore, doped a-Si:H contains high levels of defect density, as the formation enthalpy for defects counteracting the active dopants is reduced when the Fermi level approaches one of the band edges [10–12].

In this contribution, the influence of post-deposition annealing temperature on the passivation properties of layer stacks consisting of intrinsic and doped (both n- and p-type) a-Si:H is investigated. Furthermore, SHJ solar cell performance for the used annealing temperatures is evaluated, and correlated with the passivation properties of the different a-Si:H containing layer stacks. Based on the findings described in this contribution, a modified processing sequence for SHJ solar cell fabrication is proposed and an improvement compared to the standard deposition order is demonstrated.

2. Experimental details

Four different types of samples were studied: First of all, n-type c-Si wafers which are passivated on both sides by deposited intrinsic a-

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Si:H films with a device-relevant thickness of 10 nm (Type 1). Secondly, we have deposited our standard BSF on both sides of c-Si wafers, consisting of intrinsic (5 nm) and an n-type (20 nm) a-Si:H films (Type 2). Thirdly, we made a sample for which we deposited our standard BSF on one side of the c-Si wafer, and on the other side our standard emitter, consisting of intrinsic (5 nm) and p-type (20 nm) a-Si:H films (Type 3). Finally, we made an entire SHJ solar cell, based on the insight gained on the previously described layer stacks by subsequent Indium Tin Oxide (ITO) deposition and contact formation (Type 4).

For all the samples, we use ~275 μm thick n-type <111> oriented double sided polished (DSP) float zone (FZ) c-Si wafers (2–5 Ω cm). Prior to a-Si:H deposition, the wafers are dipped in HF (1% diluted in H_2O) for 3 minutes. The a-Si:H layers are made by rf PECVD (radio frequency plasma enhanced chemical vapor deposition) at a plasma excitation frequency of 13.56 MHz in a high vacuum multi-chamber system, called PASTA [13]. For each type of a-Si:H layer, a different process chamber is used to avoid cross-contamination. The intrinsic a-Si:H films are deposited from pure SiH_4 at a process pressure of 1.08 mbar, a power density of 30 mW/cm^2 and a substrate temperature of 130 °C. The n-type a-Si:H films are fabricated using a gas mixture consisting of SiH_4, H_2, and PH_3 at gas flow ratio of 4:1:0.02, a power density of 21 mW/cm^2 and a substrate temperature of 195 °C. The p-type a-Si:H films are fabricated using a gas mixture consisting of SiH_4, H_2 and $B(CH_3)_3$ (also called TMB) at gas flow ratios of 1:10:0.28, a power density of 35 mW/cm^2 and a substrate temperature of 150 °C. The ITO layers are deposited by rf magnetron sputtering from a ceramic target consisting of In_2O_3:Sn_2O_3 (10%) without additional heating in the SALSA system through custom masks defining solar cell size of 1 cm^2, more elaborately described in [14]. Solar cell contacts are formed by Ag evaporation.

Sample types 1–3 are characterized by Quasi Steady State Photoconductance measurements [15], using the quasi-transient mode and the generalized mode [16]. From these measurements, the injection level dependent minority carrier lifetime and the implied V_{OC} can be determined. The implied V_{OC} is calculated from the quasi-Fermi level splitting at a light intensity of 1 Sun (1000 W/m^2) [15].

The finished solar cells (Sample type 4) are characterized by means of current density versus voltage (J–V) measurements under AM1.5 illumination [17], using a dual beam solar simulator. In the solar simulator, a reference photodiode is mounted to accurately control and correct for the illumination intensity.

All four samples were isochronally annealed at stepwise increased temperatures, in 11 steps, starting at 150 °C and ending at 300 °C, with 15 °C increments, each step lasting for 1 h in an N_2 ambient. The accuracy of the temperature control during annealing is estimated to be ± 5 °C. The influence of annealing temperature on passivation quality (Sample types 1–3), as well as solar cell performance (Sample type 4) were determined after each step.

3. Results

3.1. Surface passivation

The as-deposited minority carrier lifetimes at an injection level of 10^{15} cm^{-3} of the different samples are shown in Table 1: The as-deposited minority carrier lifetime of c-Si passivated by the intrinsic a-Si:H films with only device-relevant thickness is very low (only 42 μs).

In Fig. 1, the minority carrier lifetimes at an injection level of 10^{15} cm^{-3} of the different samples versus annealing temperature is shown. For sample 1, a drastic improvement in passivation quality can be observed up to T = 270 °C and thereafter a decrease.

For c-Si passivated with layer stacks consisting of i/n a-Si:H (Sample type 2), a similar trend in passivation quality versus annealing temperature can be observed as for the surface passivating intrinsic a-Si:H films only (Sample type 1). The decrease in passivation quality, however, starts at a somewhat lower temperature; T = 255 °C. At annealing temperatures between 210 °C and 270 °C, excellent minority carrier lifetimes in excess of 10 ms at an injection level of 10^{15} cm^{-3} are obtained, peaking at an annealing temperature of 255 °C. The minority carrier lifetime at this temperature is equal to τ_{eff} = 13.3 ms; so far the highest value reported in literature for c-Si passivated by a-Si:H [18]. At lower injection levels, we have measured even higher minority carrier lifetime values (exceeding 15 ms for injection levels below 1.5×10^{14} cm^{-3}). At higher injection levels, the minority carrier lifetime is limited by Auger recombination [19]. The injection level dependent minority carrier lifetime of this sample is shown in Fig. 2.

For c-Si passivated on one side by i/n a-Si:H and on the other side by i/p a-Si:H (Sample type 3), however, a monotonous decrease in minority carrier lifetime is observed over the whole investigated temperature range, indicating that thermal annealing is already detrimental at moderate temperatures when p-type a-Si:H layers are involved. The minority carrier lifetime values of such samples strongly imply that the p-type a-Si:H film limits the passivation quality and is thus expected to be limiting the device performance.

Table 1
As-deposited as well as best minority carrier lifetimes at injection level of 10^{15} cm^{-3} for Types 1–3.

Sample no.	Description	As dep τ_{eff} (ms)	Best τ_{eff} (ms)	T_{best} (°C)
1	i/c-Si/i	$(4.2\pm0.1)\ 10^{-2}$	4.1 ± 0.1	270 ± 5
2	ni/c-Si/in	4.7 ± 0.1	13.3 ± 0.1	255 ± 5
3	ni/c-Si/ip	1.4	1.4	As dep

3.2. Solar cell performance

The results shown in section 3.1 have several implications for device fabrication. It has been observed that annealing at temperatures up to 255 °C is beneficial for the passivation properties of intrinsic a-Si:H layers only, as well as for intrinsic/n-type a-Si:H stacks. For intrinsic/p-type a-Si:H layer stacks, on the other hand, post-deposition temperatures above 150 °C are detrimental for device performance and should therefore be avoided. Based on these findings, we fabricated our SHJ solar cells (Sample type 4) in the following manner: After the HF dip, we first deposit the entire BSF structure. Subsequently, we flip the wafer in air without performing an additional HF dip and thereafter deposit a passivating intrinsic a-Si:H layer at the emitter side of the wafer. Then, the sample is annealed at 200 °C in vacuum for 16 h to induce improved passivation properties [8] and finally the p-type a-Si:H layer is deposited at

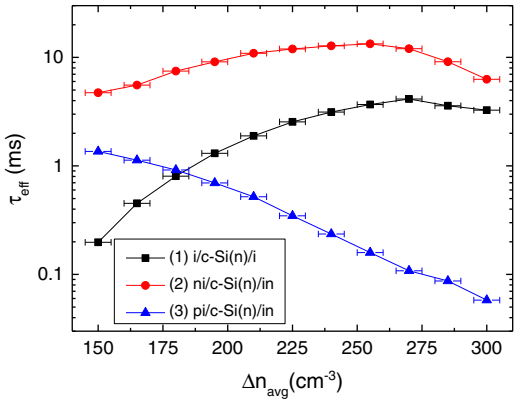

Fig. 1. Minority carrier lifetime at an injection level of 10^{15} cm^{-3} for Sample types 1–3 for different annealing temperatures.

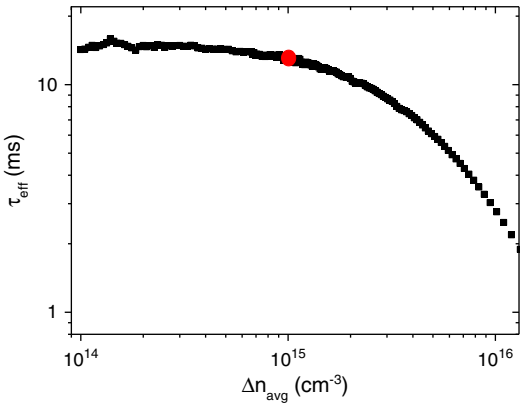

Fig. 2. Injection level dependent minority carrier lifetime of Sample type 2 after annealing at T = 255 °C.

150 °C. This way, the intrinsic and n-type a-Si:H films are exposed to a higher temperature, whereas the p-type a-Si:H films are not post-annealed. We chose an annealing temperature of 200 °C instead of 255 °C to maintain the advantages of low T processing, as described in the introduction.

The SHJ solar cell, fabricated as described above, showed an as-deposited conversion efficiency of 16.7% (V_{OC} = 681 mV). A reference SHJ solar cell, in which the emitter side was first fabricated, and thereafter the BSF side, showed an efficiency of 15.8% (V_{OC} = 659 mV). The J–V curves of the both solar cells (as-deposited) are shown in Fig. 3. The solar cell parameters (V_{OC}, J_{SC}, FF, η) of both cells are depicted in Table 2.

Subsequent annealing at T > 150 °C leads to a decrease in V_{OC} over the entire temperature range, in agreement with the decrease in implied V_{OC} of the passivation sample (see Fig. 4).

4. Discussion

4.1. Intrinsic a-Si:H films

The obtained results can be explained as follows: Low T intrinsic a-Si:H growth results in defective material, as the hydrogen is not properly equilibrated during deposition due to its low diffusion coefficient [10,20]. For this reason, a-Si:H films that are deposited at relatively low temperatures typically possess a higher void density, porosity and fraction of hydrogen that is bonded as multihydrides ($Si–H_{n>1}$) [6,20,21], leading to higher defect densities and reduced passivation of such films [21,22]. This effect has been observed to be stronger if these multi-hydrides are present close to the a-Si:H/c-Si interface [21]. Prolonged thermal annealing at temperatures higher than the deposition temperature enables the hydrogen to become mobile [10,20], diffuse towards the interface and equilibrate bulk and surface defect densities [7,10,20]. It has been demonstrated that this mechanism strongly reduces the defect density at the a-Si:H/c-Si interface, thereby improving surface passivation [6–9]. If the temperature is too high (T ~ 270 °C–300 °C), the passivation quality again decreases due to hydrogen effusing out of the intrinsic a-Si:H film [9,12, 23–25].

Table 2
As-deposited solar cell parameters of both cells (standard order and reversed order).

Parameter	Reversed order SHJ cell	Standard order SHJ cell
V_{OC} (mV)	681 ± 5	659 ± 5
J_{SC} (mA/cm^2)	33.5 ± 0.5	33.4 ± 0.5
FF (%)	73.1 ± 0.2	71.8 ± 0.2
η (%)	16.7 ± 0.3	15.8 ± 0.3

4.2. Doped a-Si:H films

For the a-Si:H containing stacks involving doped layers, the passivation quality already decreases at lower temperatures compared to the case of intrinsic films. This phenomenon can be explained by Fermi energy dependent Si–H bond rupture in a-Si:H [12,23]. In doped semiconductors (either n-type or p-type), an increased amount of doping will shift the Fermi level towards one of the band edges. This will reduce the formation enthalpy in the material for defects compensating the doping [10–12]. In a-Si:H, this asymmetry leads to a lower defect formation enthalpy as a function of Fermi level shift for p-type than for n-type films. This causes a higher defect density and reduced passivation quality for p-type than for n-type films [12,23]. This defect formation enthalpy can be associated with the energy which is needed to break two Si–H bonds and subsequently form an H_2 molecule [23].

We may also hypothesize another model for the annealing behavior. In an intrinsic/p-type a-Si:H stack, the hydrogen concentration gradient across the stack might play a role in its inferior performance with respect to annealing. Boron doped a-Si:H layers have a lower hydrogen concentration compared to intrinsic layers [26], attributed to the scavenging effect of boron. In the present case, the difference in deposition temperatures of the intrinsic and p-type a-Si:H layers also contributes to the hydrogen concentration difference. This concentration gradient will allow the hydrogen to diffuse out of the passivating intrinsic a-Si:H layer to the p-type layer and this process is more pronounced at higher annealing temperatures when more hydrogen effuses out of the p-type layer. This process increases the hydrogen concentration gradient between the intrinsic and p-type a-Si:H film. Hydrogen effusion experiments

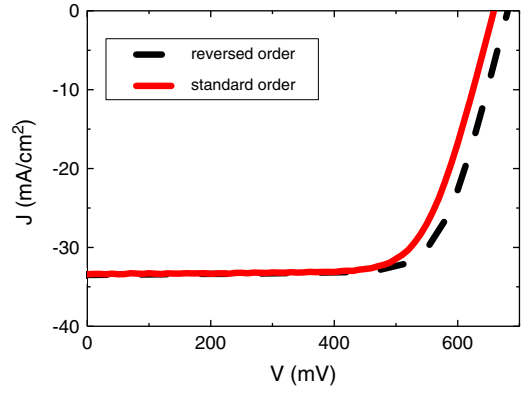

Fig. 3. J–V curve under AM1.5 illumination of SHJ solar cell fabricated in modified process order compared to the standard order (as-deposited).

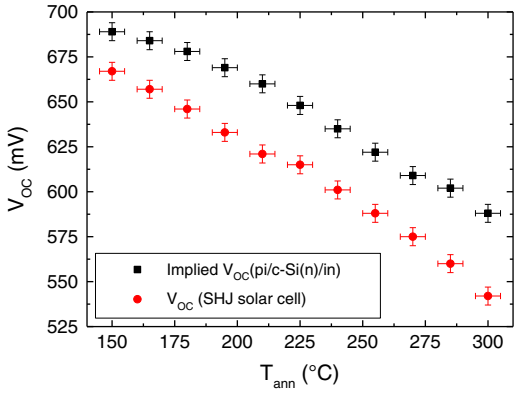

Fig. 4. Implied V_{OC} (Sample type 3) and solar cell V_{OC} (Sample type 4) after different anneal temperatures.

performed by different laboratories [12,23,24] have indeed indicated that the Si–H bond rupture associated with doping takes place at the lowest temperatures for p-type a-Si:H films (effusion peaking at 200 °C–250 °C), followed by n-type a-Si:H films (peaking slightly above 300 °C), and at intrinsic a-Si:H (peaking at 350 °C–400 °C). In case of an intrinsic/n-type a-Si:H stack, the hydrogen concentration difference between the i and n layers is much less pronounced and moreover, the hydrogen effusion from the n-type a-Si:H film is lower at the temperatures used in this experiment compared to the p-type film [23]. This explains the difference between the intrinsic/p-type and the intrinsic/n-type a-Si:H stacks in the annealing characteristics. All dependencies of minority carrier lifetime on annealing temperature as shown in Fig. 1 are in qualitative agreement with these temperature dependent effusion results.

4.3. Solar cell results

The difference in implied V_{OC} for Sample type 3 and directly measured V_{OC} in finished solar cells (Sample type 4) can mostly be ascribed to electrical losses in the TCO layers and contacts, as well as in the p-type a-Si:H layer. As mentioned earlier, the decrease in V_{OC} is related to the reduced passivation quality of the respective a-Si:H based layers. The ITO layers are deposited without any heating, which means that the temperature during ITO deposition does not have any detrimental influence on the passivation quality. The effect of ITO deposition on surface passivation for our films has elaborately been described elsewhere [27].

5. Conclusions

The influence of annealing temperature on the surface passivating properties of different types of a-Si:H based layer stacks has been investigated and can very well be correlated to the observed trends in SHJ solar cell performance as a result of post-annealing. For intrinsic a-Si:H films and for intrinsic/n-doped a-Si:H layer stacks, we observe a significant improvement in passivation quality after annealing at temperatures up to 255 °C and 270 °C, respectively. For c-Si wafers passivated by intrinsic/n-doped a-Si:H layer stacks, we obtained an excellent minority carrier lifetime of 13.3 ms at an injection level of $10^{15}\,cm^{-3}$ after annealing at 255 °C for 1 h, superior to lifetime values found in the literature for a-Si:H passivation layers on c-Si. For intrinsic/p-type a-Si:H layer stacks, however, we already observe a decrease in passivation quality for temperatures higher than 150 °C. This is attributed to Fermi-level dependent Si–H bond rupture, and hydrogen diffusion from the intrinsic towards the doped a-Si:H layers, which is known to be more pronounced in p-type than in n-type a-Si:H. Based on these findings, we fabricated SHJ solar cells in a specific order, leading to an efficiency of 16.7% on flat c-Si wafers, without light scattering enhancement by texturization, which is a considerable improvement to the 'standard' order ($\eta = 15.8\%$). The excellent passivation properties of our intrinsic a-Si:H films and our BSF structure suggest that further improvement in device performance should be obtained by modifying the p-type a-Si:H as well as the TCOs and electrical contacts.

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