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In-Band Phase Noise Reduction Techniques for Phase-Locked Loops in Advanced CMOS Technologies

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Abbreviations

AC-SS	Alias-Cancelling Subsampling
ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Controller
BJT	Bipolar Junction Transistor
CML	Current-Mode Logic
CMOS	Complementary Metal–Oxide–Semiconductor
DCO	Digitally Controlled Oscillator
DSM	Delta-Sigma Modulator
DSP	Digital Signal Processing
DTC	Digital-to-Time Converter
ENOB	Effective Number of Bits
FET	Field-Effect Transistor
FFT	Fast Fourier transform
FLL	Frequency-Locked Loop
FoM	Figure of Merit
GaAs	Gallium Arsenide
GMSK	Gaussian Minimum Shift Keying
GRO	Gated Ring Oscillator
IC	Integrated Circuit
ILFD	Injection-Locked Frequency Divider

IoT	Internet of Things
IP	Intellectual Property
IRO	Inverted Ring Oscillator
LDO	Low-Dropout
LO	Local Oscillator
LPF	Low-Pass Filter
LSB	Least Significant Bit
MPW	Multi-Project Wafer
MUX	Multiplexer
NRE	Non-Recurring Engineering
PCB	Printed Circuit Board
PDK	Process Design Kit
PLL	Phase-Locked Loop
PNRR	Phase Noise Rejection Ratio
PSD	Power Spectral Density
PSK	Phase-Shift Keying
PSRR	Power Supply Rejection Ratio
PS-SS	Phase-Switching Subsampling
PVT	Process, supply Voltage, and Temperature
QAM	Quadrature Amplitude Modulation
R&D	Research and Development
RBW	Resolution Bandwidth

RDL	Redistribution Layer
REF	Reference
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RS-SS	Rerefence-Shifting Subsampling
SiGe	Silicon-Germanium
SiP	System in Package
SNR	Signal-to-Noise Ratio
SoC	System on a Chip
SPI	Serial Peripheral Interface
SRO	Switched Ring Oscillator
SSCP	Subsampling Charge Pump
SSPD	Subsampling Phase Detector
SSPLL	Subsampling Phase-Locked Loop
SWT	Sweep Time
TDC	Time-to-Digital Converter
TSV	Through-Silicon Via
VCO	Voltage-Controlled Oscillator

Summary

Phase-locked loops (PLLs) have been successfully used as frequency synthesizers for decades in complementary metal–oxide–semiconductor (CMOS) transceivers for wireless communications. However, modern developments in communications require PLLs with wider loop bandwidth and lower in-band phase noise. High in-band phase noise leads to serious consequences in communications, such as degraded signal-to-noise ratio (SNR) and constellation diagram, resulting in low communication quality. Therefore, low PLL in-band phase noise is crucial to the overall transceiver performance, especially in future high-speed high-quality wireless communications. Unfortunately, frequency synthesizers based on conventional PLL structures are facing challenges because their in-band phase noise is often limited by the phase detectors and charge pumps. Noises from these components are amplified due to the structure of the conventional PLLs. Furthermore, PLL often needs to achieve short settling time for some communication standards, and has to provide multi-phase output in some transceiver architectures. Inspired by these requirements, this thesis aims to enhance PLL in-band phase noise performance while meeting other important requirements of future wireless communications in the multi-GHz band.

As the background of this research, conceptual PLL fundamentals related to phase noise will be briefly discussed. According to these fundamentals, the in-band phase noise is usually limited by the phase detector and charge pump in analog PLLs, and by the time-to-digital converter (TDC) in digital PLLs. Therefore, the objective of this research is specifically to reduce the adverse impact from these components. When choosing an analog or a digital PLL structure, characteristics of the adopted fabrication technology have to be considered. As the CMOS technology development is facing physical and economic limitations, two promising future CMOS technologies have been predicted, i.e., the *more-than-Moore* technology and the *more-Moore* technology. In regard to PLL implementation, the *more-than-Moore* technology permits the use of CMOS with larger feature size so that high-performance analog PLLs can be designed with mature methods,

while the *more-Moore* technology keeps using the finer processes in which digital PLLs may be more suitable due to their promising performance with technology scaling. Both PLL types will be important in future advanced CMOS technologies. Therefore, this research investigates in-band phase noise reduction techniques for both analog and digital PLLs.

Firstly, in-band phase noise reduction technique for analog PLLs is investigated. With mature design and verification methods, analog PLLs have evolved and achieved low power consumption in the past years. However, conventional analog PLLs suffer from the high in-band noise from the phase detector and charge pump because noises from these components are amplified. To reduce such adverse impact, one of the most attractive structures is the fractional-*N* subsampling phase-locked loop (SSPLL) that can remove this amplification. It has enabled promising in-band performance and fine tuning steps for wireless systems. However, prior arts of fractional-*N* SSPLLs need long time for calibrations (~20 ms), which is much longer than PLL settling time (normally less than 200 μs). So these prior arts are not suitable for wireless communications requiring short settling time, such as Bluetooth. To extend the SSPLL applications, we explore the fractional-*N* SSPLL with a calibration-free manner and propose a phase-switching subsampling (PS-SS) technique. Fabricated in a 65 nm CMOS technology, a 2.6-3.4 GHz fractional-*N* 8-phase SSPLL prototype using the proposed technique totally eliminates the need for calibration and achieves a low in-band phase noise of -100.3 dBc/Hz at 100 kHz offset. Under calibration-less measurement condition, this prototype achieves the best jitter performance and figure of merit (FoM) among fractional-*N* SSPLLs. By using the proposed PS-SS technique, a low in-band phase noise in future analog PLLs can be expected without the need for long calibration time.

Secondly, in-band phase noise reduction technique for digital PLLs is investigated. For CMOS processes with small feature size, digital PLL has been proposed as a promising substitution of analog PLL due to many aspects. In these processes, in contrast to relying on the degraded transistor analog characteristics, digital PLLs take advantages of the improved digital characteristics and time resolution. Therefore, performance of digital PLLs can be improved with technology scaling. In addition, digital PLLs can also

benefit from the automated digital design tools with shorter design cycle. However, in-band noise performance of digital PLLs is generally limited by the TDC noise. Among various TDC types, TDCs based on controlled oscillators have been reported to achieve low noise, hence low PLL in-band noise. Nevertheless, there is still a lot of headroom in such TDCs towards even lower noise. Besides, the operations of these TDCs draw different supply current at different time, leading to disturbance to power supply and to other circuitries when applied in a digital PLL. This can also affect the phase noise of the digital PLL. In this thesis, we investigate the controlled oscillator-based TDC family and propose an inverted ring oscillator (IRO) technique to further reduce TDC noise. A noise model is also proposed for noise prediction and design optimization for the controlled oscillator-based TDC family. An IRO-TDC prototype achieves an integrated noise of 196 fs_{rms} in a 3 MHz bandwidth at 200 MS/s rate, showing lower in-band noise compared with state-of-the-art works. Moreover, a unique coherent phase noise cancellation (up to 36.4 dB cancellation ratio measured) and a constant TDC power dissipation were demonstrated, which can reduce the digital PLL in-band noise caused by coherent noises.

In summary, this thesis proposes techniques and methods to improve PLL in-band phase noise in advanced CMOS technologies. The proposed techniques, models, and methods can be extended to more complicated designs in future researches and products.

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1 Introduction

1.1 CMOS PLLs in RFIC

In most radio frequency integrated circuit (RFIC) for wireless communications, frequency synthesizers are used to generate local oscillator (LO) signals for other blocks. As shown in Figure 1-1, a common wireless transceiver comprises three main modules, including the receiver, the transmitter, and the frequency synthesizer. A PLL technique is usually adopted as the core of the frequency synthesizer to regulate the LO signals. The LO signals determine the frequency at which the transceiver communicates with other devices. Therefore, the PLLs have critical importance to the communication quality.

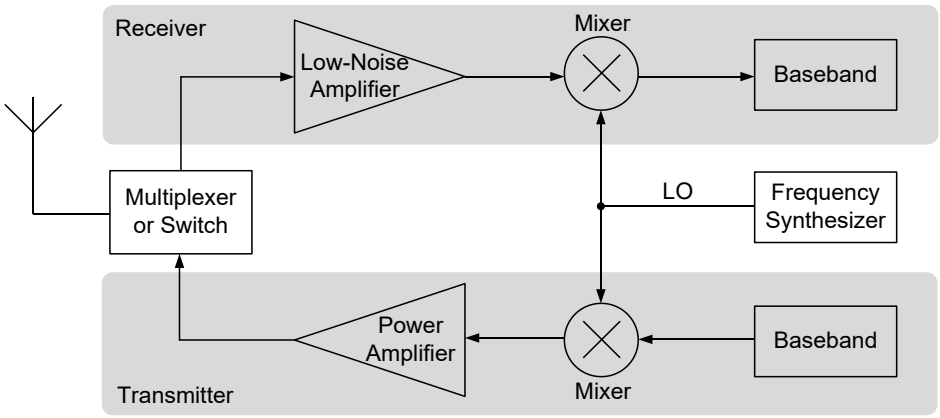
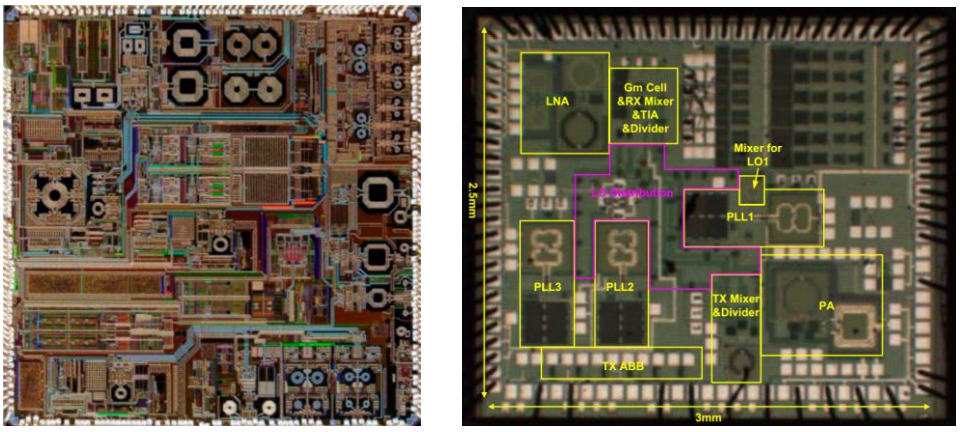


Figure 1-1 A general architecture of a wireless transceiver.

In traditional IC technologies, the RF front-end circuits were implemented using processes such as bipolar junction transistors (BJTs), gallium arsenide (GaAs), silicon-germanium (SiGe), while the digital signal processing (DSP) circuits and analog circuits were implemented in complementary metal–oxide–semiconductor (CMOS) technologies. It was the time when designers faced many challenges when fabricating RF circuits on CMOS process. However, many of these challenges have been resolved, such as high-quality on-chip inductors [1]-[4], wide-band CMOS oscillators [5]-[7], CMOS low-noise amplifiers [8]-[10], etc. Moreover, due to the surge of consumer electronics such

as smartphones and entertainment electronics, wireless applications evolve towards low power, small dimensions, higher yield, and higher level of integration owing to its low cost. Driven by these incentives, efforts have been made to combine RF modules and baseband circuits in a single CMOS chip. Figure 1-2 shows two RFIC arts. Figure 1-2(a) is a micrograph of an RF transceiver chip from Qualcomm, equipping frequency synthesizers for GSM, WCDMA, and GPS with about 1/4 of its total area and power consumption [11]. Figure 1-2(b) shows a prototype of one of the author's projects for IEEE 802.11 WLAN application. This prototype includes three PLL frequency synthesizers and a buffer network for LO clock delivery [12]. In fact, CMOS PLL frequency synthesizers are commonly considered as the most complicated blocks in an RFIC, and usually determine the design cycle of a RFIC product [13].



(a) (b)

Figure 1-2 (a) An RF transceiver from Qualcomm [11], and (b) a 802.11 WLAN RF front-end [12].

1.2 CMOS PLLs Challenges in Future Communications

In general, for PLLs adopted in RF frequency synthesizers, designers have to consider at least three specifications. Firstly, the frequency has to be tuned accurately with small steps, so that the transceiver can communicate precisely at the target frequency. Secondly, the LO signals should be clean in spectrum with low phase noise. Thirdly, the synthesizer should settle and generate the LO signals within a specified time. For example, in GSM applications, the frequency has to settle within 200 μs.

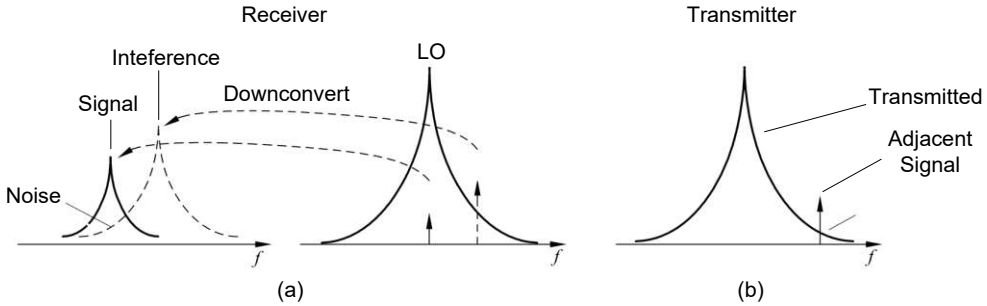


Figure 1-3 Phase noise impact on (a) receiver and (b) transmitter [13].

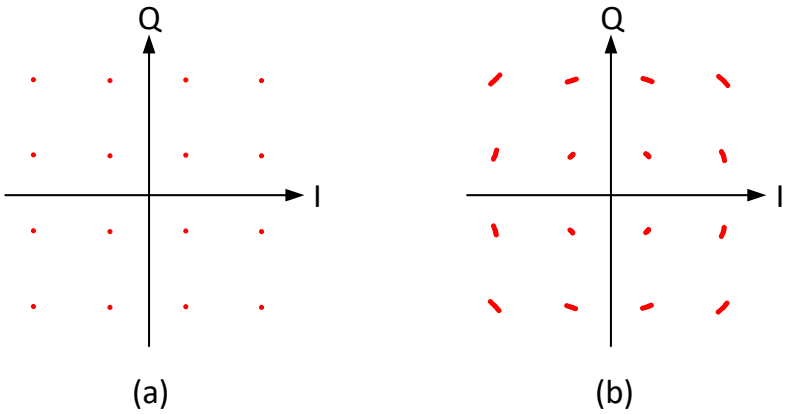


Figure 1-4 Constellation diagram with (a) no phase noise and (b) large phase noise.

A poor phase noise performance can lead to many serious consequences to wireless communication. Figure 1-3 illustrates these impacts. For receivers, an LO with poor phase noise makes the mixer convert not only the wanted RF signal but also some adjacent interferences down to baseband, degrading the SNR of the signal, as shown in Figure 1-3(a). In transmitters, a poor LO phase noise is emitted by the power amplifier and contaminates other channels nearby, as shown in Figure 1-3(b). Some modern wireless standards utilize phase information to transmit data, such as Gaussian minimum shift keying (GMSK) and phase-shift keying (PSK) in phase modulated GSM/EDGE. The in-band phase noise can introduce rotation and degradation to the constellation diagram, as shown in Figure 1-4.

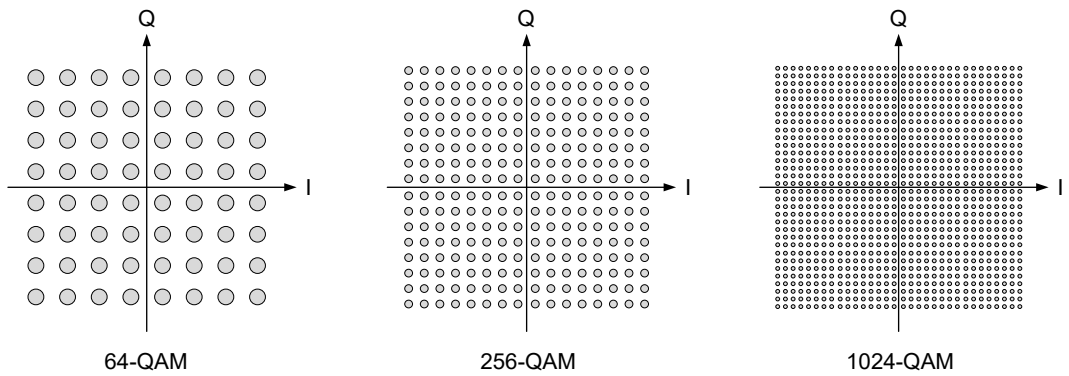


Figure 1-5 Constellation diagrams of 64-, 256-, and 1024-QAM.

As wireless communication standards are becoming more complicated, the specifications for frequency synthesizers are also more stringent than that in the older generations.

One important challenge in future is that the modulation scheme is becoming more complicated and requiring better phase noise performance from the PLLs. For example, in 802.11n standard, the most complicated modulation is 64-quadrature amplitude modulation (-QAM). The later 802.11ac requires a more sophisticated 256-QAM, and the latest 802.11ax even requires a 1024-QAM modulation for higher data rate. In terms of the constellation diagram, this leads to a more congest pattern, as shown in Figure 1-5. As phase noise cause rotation to the constellation diagram and degrades the communication quality, the PLL phase noise performance becomes increasingly important in future [14]-[17].

Another challenge is that a wide bandwidth is preferred and sometimes required. As PLL is essentially a control loop, it has an own loop bandwidth which determines the major characteristics. A wide PLL bandwidth is desirable as it results in [18]-[23]:

- Improved data modulation bandwidth for higher data throughput
- Larger suppression of oscillator phase noise, which helps to reduce power consumption (will be explained in Chapter 2)
- Faster settling time to meet specified requirement
- Reduced oscillator pulling to enhance robustness

Due to the increased loop bandwidth and lower phase noise, the in-band phase noise performance is becoming increasingly important in future.

To summarize, the challenge for the PLLs in future is the reduction of the phase noise, especially the in-band phase noise, without scarifying other important features such as fast settling time.

However, conventional analog PLL structures fail to satisfy this requirement because the noise of their phase detector and charge pump is amplified and dominates the in-band phase noise. Fractional-*N* SSPLL has been proposed to eliminate this amplification and has achieved low in-band phase noise. However, these SSPLLs require time-consuming calibrations. In order to apply these SSPLLs into communications requiring short settling time, such calibration time has to be reduced or totally eliminated.

On the other hand, a digital PLL architecture has been reported to take advantages of the future CMOS processes with finer feature size. Phase detector and charge pump do not exist in such architecture. In-band phase noise of these digital PLLs is dominated by the noise from their TDCs. Designers have made great effort to reduce the TDC noise using different TDC structures. One of the promising approaches is utilizing noise shaping by employing controlled oscillator-based TDCs due to their low in-band noise. Yet, the in-band noise of these TDCs is dominated by the internal oscillator phase noise. And there is no prior technique to further reduce such noise. In addition, prior arts of these TDCs draw varying supply current, introducing disturbance to the power supply and hence to other circuitries in a digital PLL, leading to other phase noises.

In order to overcome these challenges, the goal of this thesis is to investigate and propose techniques to reduce in-band phase noise of both analog and digital PLLs.

1.3 Major Contributions of the Thesis

As the background of this research, we review the current limitations of *Moore's Law* and two promising advanced CMOS technologies, including a function-oriented *more-than-Moore* technology (i.e., system in package (SiP) technology) and a

cost-oriented *more-Moore* technology (i.e., system on a chip (SoC) technology). In regard to PLL implementation, the SiP technology permits the use of CMOS with larger feature size in which analog PLLs can be designed and verified with mature methods, while the SoC technology keeps following *Moore's Law* and tries to use finer processes in which digital PLLs may be more suitable due to their promising performance that can be improved by technology scaling. Therefore, this thesis tries to achieve in-band noise reduction in both PLL types. Accordingly, contributions in this research can be divided into two parts.

The first part focuses on analog PLL in-band phase noise. In-band phase noise of a conventional analog PLL is usually limited by the noise amplification of phase detector and charge pump. Fractional-*N* SSPLLs can be used to reduce this noise amplification. However, prior arts of such PLLs require time-consuming calibrations. Contributions in this part are listed below.

- Prior arts in low-noise fractional-*N* SSPLL have been investigated. Their needs for the time-consuming calibrations are explained.
- A novel PS-SS technique that can eliminate the need for calibrations is introduced. This PS-SS technique utilizes the phase information from the voltage-controlled oscillator (VCO) output rather than a calibrated digital-to-time converter (DTC). Hence, the phase is inherently related to the VCO phase without any calibration.
- A phase model for PS-SSPLL analysis is proposed. This phase model can be used for output phase noise prediction and design optimization not only in this research, but also in future designs with similar operation.
- A prototype fractional-*N* PS-SSPLL is designed, fabricated, and measured to verify the proposed PS-SS technique. An 8-phase output at 2.6-3.4 GHz is available in this structure. The prototype achieves an in-band phase noise of -100.3 dBc/Hz and an FoM of -234.3 dB. Under a calibration-less condition, this

prototype achieves the best jitter performance and FoM among the fractional-*N* SSPLLs.

- Conclusions and design suggestions for similar future designs are provided. The core idea of PS-SS technique is to obtain phase shifting steps from the VCO phase rather than a calibrated circuit. This idea can drive other implementations of calibration-free designs.

The second part focuses on digital PLL in-band phase noise, which is usually limited by the TDC noise. Prior arts have been achieved low TDC in-band noise through noise shaping by using controlled oscillators, but there is still headroom towards lower in-band noise. Therefore, in this part, the major focus is to further reduce the TDC in-band noise. Contributions in this part are listed below.

- A noise model is proposed to analyze the noise characteristics of the controlled oscillator-based TDC family. In this model, operation of these TDCs is generalized as transformation from time domain to phase domain and digital domain. By analyzing the noises in these transformations, the TDC noise can be predicted in order to help with design and optimization. This model can also conduce to future TDC designs with more complicated controlled oscillators.
- A novel IRO technique that can reduce the TDC in-band noise is introduced. This IRO can invert its oscillation direction with unchanged frequency. By doing this, a potentially larger gain can be expected, and the noise performance can be improved. In addition, due to the constant oscillator frequency, the supply current is kept constant, leading to a reduced disturbance to the power supply and other circuitries when applied in a digital PLL.
- A prototype IRO-TDC is designed, fabricated, and measured to verify the proposed IRO technique. With a sampling rate of 200 MS/s and a wide signal bandwidth of 3 MHz, the IRO-TDC prototype achieves a low in-band noise of 196 fs_{rms}, outperforming state-of-the-art works. To our knowledge, this is the first

demonstration of utilizing oscillation inversion to reduce the impact of oscillator phase noise and achieve coherent noise cancellation.

- A unique coherent oscillator phase noise cancellation in the proposed IRO is predicted by the noise model and verified through measurement results. A cancellation ratio of up to 36.4 dB is achieved in measurement. This unique noise cancellation protects the TDC from the coherent noise sources such as power supply noise and substrate noise.
- Conclusions and design suggestions for similar future designs are provided. The proposed IRO utilizes oscillation inversion to achieve noise reduction, coherent noise cancellation, and low disturbance to power supply at the same time. As an extension, the proposed idea suggests future converters to utilize polarity of a parameter, rather than its amplitude, to achieve similar properties.

Together, these contributions demonstrate helpful techniques that can enhance the noise performance of the analog and digital CMOS PLLs in future advanced CMOS technologies.

1.4 Organization of the Thesis

The rest of this thesis is organized as follows.

Chapter 2 provides the background of this research. To begin with, PLL principle and noise characteristics are briefly introduced to identify the contributors of in-band phase noise. Detailed analysis of in-band noise depends on the actual PLL implementation in different CMOS technologies. Therefore, the development of CMOS technologies is also reviewed. This chapter summarizes the implementation considerations of PLLs in different applications and technologies, and serves as a guidance of this research. Our conclusion in this chapter is that advanced CMOS technologies will follow both an SiP technology where analog PLLs may be preferable, and an SoC technology where digital PLLs may be more suitable. The following chapters deal with these two PLL types accordingly.

Chapter 3 focuses on in-band noise reduction for analog PLLs. Literature review of divider PLLs and SSPLLs is provided as the basis of our exploration. The reasons and drawbacks of the time-consuming calibration issue are discussed. The proposed PS-SS technique and PS-SSPLL implementation are described in detail, with measurement results provided. At the end of this chapter, we point out some potential drawbacks in this prototype and provide possible solutions.

For a digital PLL, the in-band phase noise is usually limited by the TDC. Therefore, the main focus of Chapter 4 is on low-noise TDCs, which can be applied to reduce in-band phase noise of digital PLLs. Among various TDC types, the controlled oscillator-based TDCs provide attractive noise-shaping characteristics and achieve low in-band noise. Literature review about this TDC family is provided. The proposed IRO and noise model are described in detail. Noise characteristics of gated ring oscillator- (GRO-), switched ring oscillator- (SRO-), and IRO-TDCs are also compared. The unique IRO noise cancellation is predicted using the noise model. Measurement results and calculation results from the model are provided and compared. At the end, we conclude this IRO-TDC work, point out drawbacks of the prototype, and give some possible solutions.

Chapter 5 draws the conclusion of this research and provides recommendations for future work. Core ideas of the proposed techniques are reworded in a physical point of view for future researches. Other possible implementations of the proposed techniques are also mentioned.

2 Background on CMOS PLLs

2.1 PLL Fundamentals

In this chapter, in order to provide the reader a conceptual understanding of PLLs, we will introduce some PLL fundamentals without diving into circuit details. In the later PLL analysis, some fundamentals in this chapter will be extended accordingly.

As suggested by its name, the purpose of a PLL is to adjust an output phase according to an input phase with a given input-output relation. Such a required function dates back to 1930s when researchers were building a direct-conversion receiver, in which the receiver LO was tuned to the desired input frequency and multiplied with the input signal in order to obtain the original modulation information. Since the LO frequency would drift, a feedback control mechanism is needed to correct the LO frequency in order to maintain the phase and frequency of the desired LO signal. The technique was described in [24]-[25] by Henri de Bellescize in 1932.

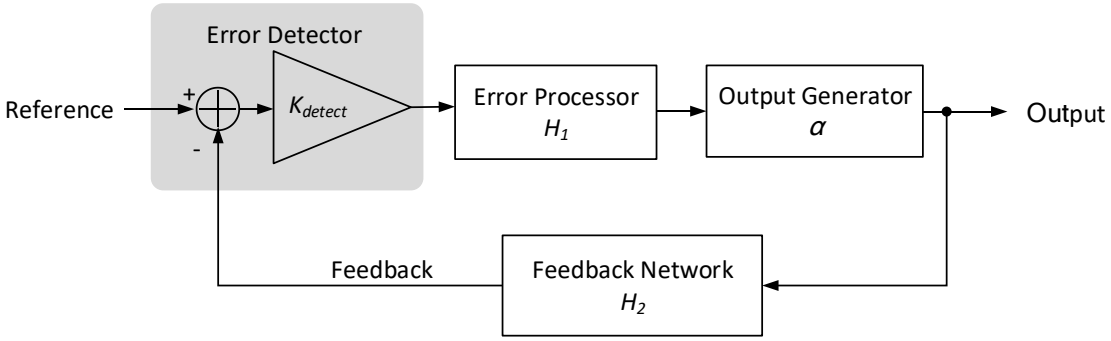


Figure 2-1 Conceptual diagram of a feedback control loop.

2.1.1 Conceptual Architecture

A PLL is essentially a negative feedback loop with high feedforward gain and accurate feedback factor. Figure 2-1 shows the conceptual diagram of a feedback control loop. Such a conceptual diagram can apply to other kinds of control loop circuits such as closed-loop DC-DC converters, low-dropout (LDO) regulators, closed-loop amplifiers, etc. Functions of different blocks are described next.

A controllable output generator is to produce the wanted output signals across a targeted range. In PLL, a controlled oscillator is used to generate the output clock, i.e., the output phase.

An input is applied to the loop as the reference for the output signal. For LDO and DC-DC converters, the parameter to be controlled is the output voltage. A bandgap reference circuit is normally integrated in the IC to provide a constant reference voltage, because the BJTs in IC technologies can provide a voltage with sufficiently small deviation across a wide range of process, supply voltage, and temperature (PVT) variations. Similar to a reference voltage, a reference phase (or a reference clock) can also be generated in the IC itself. However, such an integrated clock in IC has poor frequency stability due to material limitations. This poor frequency stability is unacceptable for most RF transceivers. As a matter of fact, for a common PLL for RF transceivers, the reference clock is generally from an external clock source with much more stable frequencies, such as a crystal oscillator.

In order to maintain a certain relation between the output and input parameters, a feedback network, an error detector and an error processor are used. In this thesis, we term a set of components an "error detector" if their function is to detector the difference between the reference and the feedback signal and to generate a signal representing this difference. For conventional analog PLLs, the error detector comprises a phase detector and a charge pump. For digital PLLs (which will be introduced later), the error detector is usually a TDC. The error detector usually has its own gain, which is denoted as K_{detect}. Generally, a high feedforward gain ($K_{detect}H_1\alpha \gg 1$) and an accurate feedback gain (H_2) are adopted, and the open-loop gain is usually high ($K_{detect}H_1\alpha H_2 \gg 1$). The output signal of the error detector represents the error between the input reference and the feedback information. An error processor takes this signal and generate a control signal to regulate the output generator. This error processor is usually a low-pass filter, and thus called a "loop filter" in PLL researches. The closed-loop gain of this control loop can be expressed as

$$A_{cl} = \frac{K_{detect}H_1\alpha}{1 + K_{detect}H_1\alpha H_2} \approx \frac{1}{H_2}. \quad (2\text{-}1)$$

If the feedforward gain is changed by $\Delta(K_{detect}H_1\alpha)$, the variation of the loop gain is

$$\left.\frac{\Delta A_{cl}}{A_{cl}}\right|_{H_2} = \frac{1}{1 + K_{detect}H_1\alpha H_2} \cdot \frac{\Delta(K_{detect}H_1\alpha)}{K_{detect}H_1\alpha} \approx 0. \quad (2\text{-}2)$$

This implies that for normal PLLs ($K_{detect}H_1\alpha H_2 \gg 1$), the loop gain is not sensitive to the feedforward gain. Similarly, if the feedback gain is changed by ΔH_2, loop gain variation is

$$\left.\frac{\Delta A_{cl}}{A_{cl}}\right|_{K_{detect}H_1\alpha} = \frac{-K_{detect}H_1\alpha H_2}{1 + K_{detect}H_1\alpha H_2} \cdot \frac{\Delta H_2}{H_2} \approx -\frac{\Delta H_2}{H_2}. \quad (2\text{-}3)$$

In contrast, this implies that the PLLs are sensitive to the feedback gain. Thus, an accurate and linear feedback gain has to be guaranteed. In fact, the feedback network determines the input-output relation of the target parameter.

The above discussion reveals that the feedforward path requires a high gain and the feedback network requires sufficient accuracy and linearity.

Note that this PLL concept is not limited to circuit implementations. All the above blocks may be embodied in software (software PLL), neurons (neuronal PLL), natural phenomena, and even human activities.

2.1.2 Noise Contributors

Using the conceptual structure, we can obtain a simplified analysis of the PLL noise performance. As a PLL is used to provide phase information, when considering the noise from the PLL, a concept of phase noise is usually adopted since the amplitude noise seldom affects the transceiver performance. The phase noise is defined by the deviation from the ideal phase to the actual phase, as shown in Figure 2-2. A common expression of phase noise is the single-sided power spectral density (PSD) of the stochastic instantaneous phase error, $\delta\varphi$. The unit of this PSD is *dBc/Hz*, where character *c* refers to *carrier frequency*. The unit *dBc/Hz* is the logarithmic of rad^2/Hz. The expression of phase noise can be better understood through an analogy with the single-sided PSD of a voltage noise, where the unit

is V^2/Hz. The instantaneous phase error, $\delta\varphi$, can also be converted into a time domain jitter in some analysis.

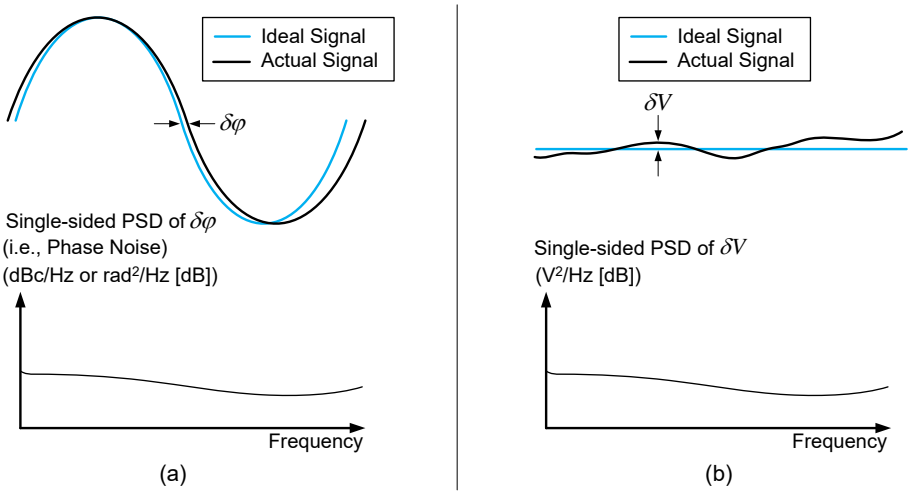


Figure 2-2 Comparison between concepts of (a) phase noise and (b) voltage noise.

Each sub-circuit in a PLL, as well as the input reference signal, generates its own noise. These noises may be transformed into phase domain by the PLL, and thus contributes to the output phase noise. Figure 2-3 shows a noise model of a general PLL. Parameters $\Phi_{REF,n}$, $\Phi_{FB,n}$, n_{detect}, n_{FF}, and $\Phi_{OSC,n}$ represent the input reference phase noise, feedback phase noise, error detector noise, error processor noise, and oscillator phase noise, respectively. K_{OSC} is the control gain of the oscillator. The closed-loop transfer function for each noise source is listed in Table 2-1. As can be seen later in Chapter 3, low in-band phase noise can be guaranteed in the feedback network. Therefore, it has a negligible contribution to the PLL in-band phase noise.

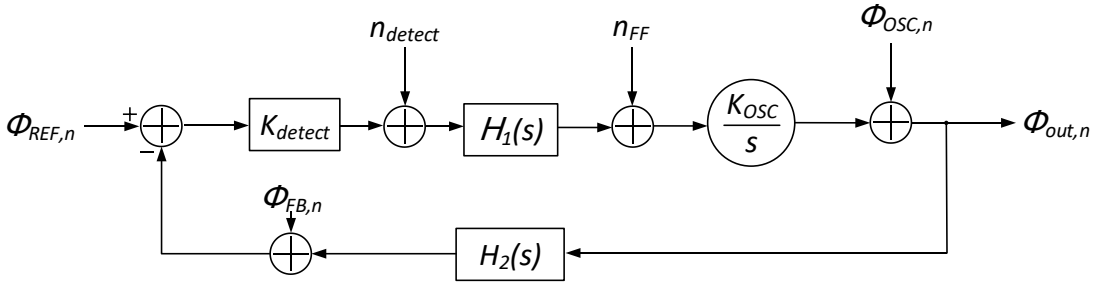


Figure 2-3 Noise model of a general PLL.

Table 2-1 Closed-Loop Transfer Functions from each Noise Source to PLL Output

Noise Source	Transfer Function*	Transfer Function Type
Reference Phase	$\frac{\Phi_{out,n}}{\Phi_{REF,n}}(s) = \frac{1}{H_2(s)} \cdot \frac{G(s)}{1+G(s)}$	Low Pass
Feedback Phase	$\frac{\Phi_{out,n}}{\Phi_{FB,n}}(s) = \frac{-1}{H_2(s)} \cdot \frac{G(s)}{1+G(s)}$	Low Pass
Error Detector	$\frac{\Phi_{out,n}}{n_{detect}}(s) = \frac{1}{K_{detect} \cdot H_2(s)} \cdot \frac{G(s)}{1+G(s)}$	Low Pass
Error Processor	$\frac{\Phi_{out,n}}{n_{FF}}(s) = \frac{K_{OSC}}{s} \cdot \frac{1}{1+G(s)}$	Band Pass
Oscillator Phase	$\frac{\Phi_{out,n}}{\Phi_{OSC,n}}(s) = \frac{1}{1+G(s)}$	High Pass

* Open-loop transfer function $G(s) = K_{detect} \cdot H_1(s) \cdot H_2(s) \cdot K_{OSC}/s$.

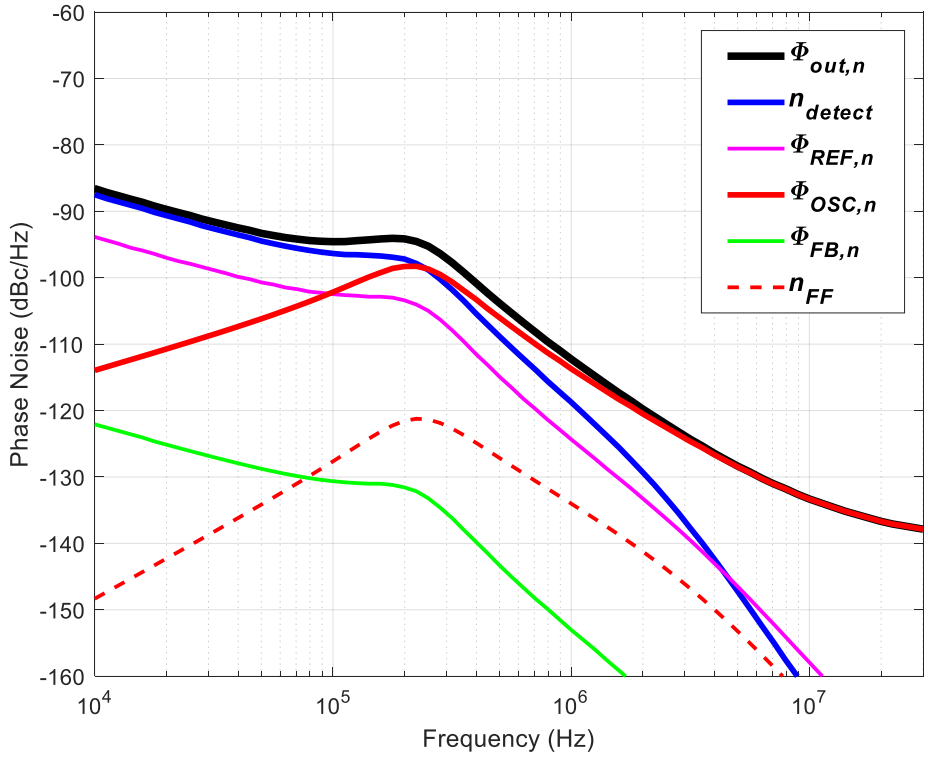


Figure 2-4 An example of noise source contributions to the PLL output phase noise.

As an example, Figure 2-4 plots the phase noise contribution of each in a typical PLL. From the figure and Table 2-1, the PLL in-band phase noise may be dominated by the input reference noise or comparator noise since they follow low-pass transfer function, whereas

the out-of-band phase noise is probably dominated by the oscillator due to its high-pass transfer function.

The high-pass transfer function of the oscillator phase noise implies a suppression of the oscillator phase noise within the PLL bandwidth. This reveals that within the loop bandwidth, the negative feedback mechanism can correct the oscillator output phase according to the input reference phase; while at the frequencies outside the loop bandwidth, the oscillator noise is changing so fast that the loop fails to correct it. This reveals that, with a wider loop bandwidth, more oscillator phase noise can be suppressed, so that a noisy oscillator with lower power consumption can be adopted. Therefore, a wide-bandwidth PLL is preferred in terms of the oscillator noise and power dissipation.

Another consideration for wide bandwidth is the loop transient. With a wider bandwidth, the PLL can lock from one target frequency to another faster, in order to fulfill the requirement of the corresponding standard. Moreover, for some applications the PLL is used not only to provide the LO, but also to modulate the LO signal. Under such a scheme, the modulation input is controlling the target output frequency. Such a modulation follows the same low-pass transfer function. Obviously, a wider loop bandwidth permits a wider modulation bandwidth, hence a wider data bandwidth. However, the phase model in Figure 2-3 is an approximation with the precondition that the loop bandwidth is much smaller than the reference frequency. Consequently, for most PLLs, the loop bandwidth is an order of magnitude lower than the reference frequency.

As PLL bandwidth increases, the integrated in-band phase noise becomes more important to the PLL overall noise. If the reference clock is provided by an external crystal oscillator, its phase noise is usually very low. Therefore, the error detector noise is usually the major contributor to the in-band noise. From a general point of view, the proposed techniques in this thesis aim to reduce noise from the error detectors.

2.2 CMOS Technology Development

Actual implementation of a PLL depends on the process technology. Transistors in various processes have different characteristics, such as leakage and noise performance. Therefore, there is not a single scheme or integration level that is optimized for all IC technologies. In fact, the proposal of PLL technique (Bellescize, 1932) and applications of PLL in television receivers (late 1930s) date back to even well before the invention of the first IC (Jack Kilby, 1958).

Early monolithic PLL ICs (e.g., [37]-[39]) integrated the phase detector and oscillator in a single chip, but without reference clock, loop filter (as the error processor) or feedback network. Users were thus able to configure the loop filter and the frequency division ratio externally. However, bulky passive components for the loop filter made the whole design very large, and interconnections between the IC and the printed circuit board (PCB) also degraded the PLL performance. Current fully integrated PLLs in modern RFICs leave only the reference clock source outside the chip (e.g., [11]-[12]). Crystal oscillators are still commonly used as the reference clock source for modern wireless transceiver PLLs.

The PLLs we will discuss in this thesis are limited to designs fabricated in CMOS technologies. In order to provide a ground for our research and to help future explorations, next, we will review the CMOS technology development that is related to PLL implementation.

2.2.1 Moore's Law and Limitations

The history of IC technology can be represented by one famous observation, the *Moore's Law*, which is named after Gordon Moore. It projected that the number of transistor components per IC area would double after every two years. The chip performance was predicted to improve with the similar pace. The reason of *Moore's Law* is that the semiconductor industry needs an appropriate growth pace to maximize the overall profit. Companies would spend certain amount of their profit to upgrade their technologies, in order to increase their future profit. Figure 2-5 shows this evolution during the past several decades.

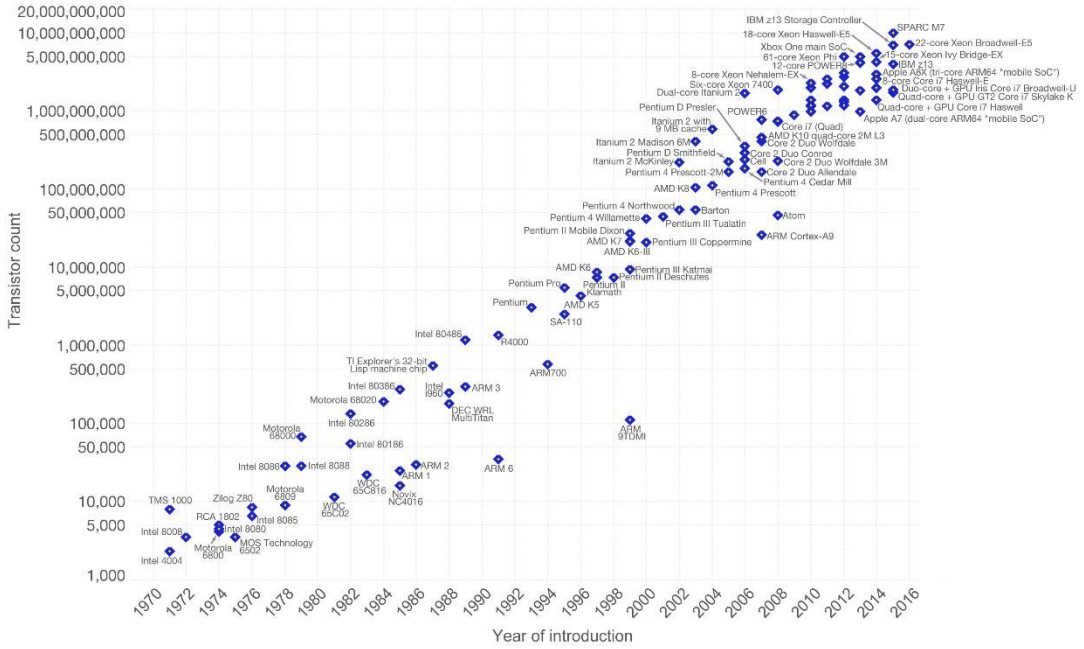


Figure 2-5 Microprocessor transistor counts in 1971-2011 [40].

Along with the size scaling, the IC performance enhanced during the last decades. Due to size shrinking, power consumption was reduced and speed was increased. Chips with higher-performance can be fabricated with same power specification.

Two driving forces for *Moore's Law* include fabrication technology development and economic considerations. At larger feature sizes, scaling seems promising and easy. Lithography masks used to fabricate ICs could be produced with smaller and smaller resolutions. Companies were willing to invest for new technologies in order to improve performance, to reduce cost and to maximize profits. However, physical laws and the size of atoms are not scalable. These facts set a huge barrier against the CMOS feature size scaling. As the feature size approaches the boundary of macrophysics and quantum physics, research and development (R&D) of advanced process technologies is becoming tremendously challenging and expensive.

Physical Limitations

The major physical limitations are quantum effects and lithography accuracy. When the feature size is reduced to 10 nm, quantum effects need to be considered, making the transistor characteristics difficult to control. For example, the quantum tunneling effect

results in serious transistor leakage and degrades the transistor performance dramatically. For mobile applications, this means a high power consumption and short battery life even in a standby mode. Such leakage also degrades the analog/RF circuit performance. Another limitation is the lithography accuracy, which is mainly determined by the wavelength of the light for lithography. In order to obtain smaller resolution, it requires light with extremely small wavelength and the corresponding photoresist. Lack of these tools calls for more researches in the fabrication research.

Economic Limitations

In order to understand the economics of an IC chip, it is important for the IC designer and company to be able to anticipate the cost and time required. For a particular IC product, the total cost includes the following elements:

- Non-recurring engineering (NRE) costs, including cost for manpower (designers, supporting staffs, etc.), tools (computers, software, process design kits (PDKs), intellectual properties (IPs), etc.), and most importantly the prototype fabrication. In addition, NREs tend to increase with longer design cycle.
- Recurring cost, R_{total}, which is spent on each product and thus increases with the number of product. This includes the wafer process cost, packaging cost, and test cost.

The total cost of a product can be expressed as

$$C_{total} = NREs + R_{total} \times N, \tag{2-4}$$

where N denotes the total number of the product. Figure 2-6 illustrates the major costs for the product. $R_{process}$ refers to the wafer process cost for each die. It depends on the cost per wafer (i.e., R_{wafer}), number of dies per wafer (i.e., n), and yield.

Scaling of feature size mainly helps reduce process cost of each die and increase profit. As the transistors and the whole IC can be produced in a smaller size, the wafer process cost for each chip, $R_{process}$, shrunk continuously because they need less materials and area. On the other hand, for processes with smaller feature size, the design tools (such as PDKs

and IPs) and prototype fabrication are more expensive. Hence, NREs increase with smaller feature size.

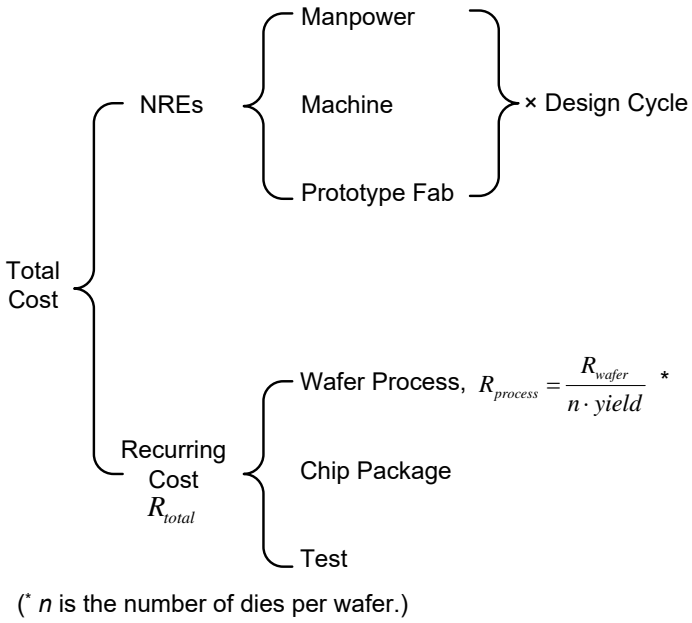


Figure 2-6 Costs of an IC product [41].

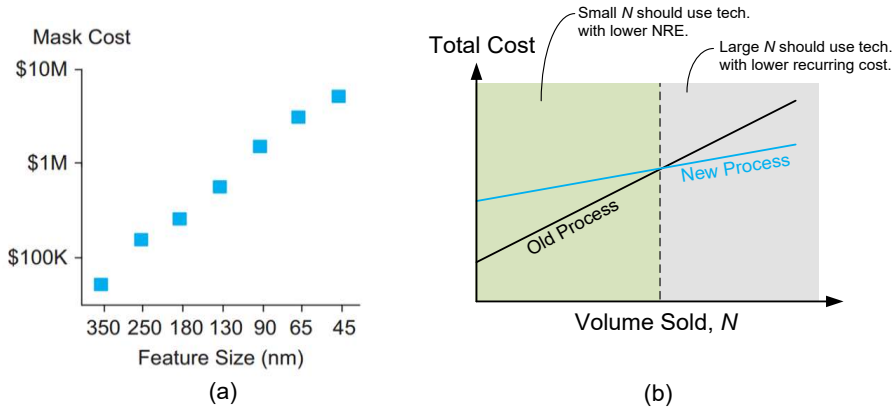


Figure 2-7 (a) Approximate mask set cost [41]. (b) Product total cost in old and new technologies.

Figure 2-7(a) shows the approximate fabrication mask set cost of different technologies. In order to reduce NREs, multi-project wafer (MPW) project can be used for functional verification. However, an MPW project cannot prove the yield and behavior across process variations.

Another consideration of the NRE is the design cycle. For advanced and sophisticated technologies, the design rules are so strict that the designers need to spend longer time on

the design. More prototype runs are probably required to verify the design. This results in even higher NREs. Subsequently, if an advanced technology is used, more chips have to be sold to increase the total profit, as shown in Figure 2-7(b).

Unfortunately, due to the physical challenges of the small resolution, the NRE increases dramatically in the processes with small feature size, such as the 3 nm node announced last year. For products using such expensive technologies, a great amount of product has to be sold. Many companies with small specific markets cannot afford such a costly prototype.

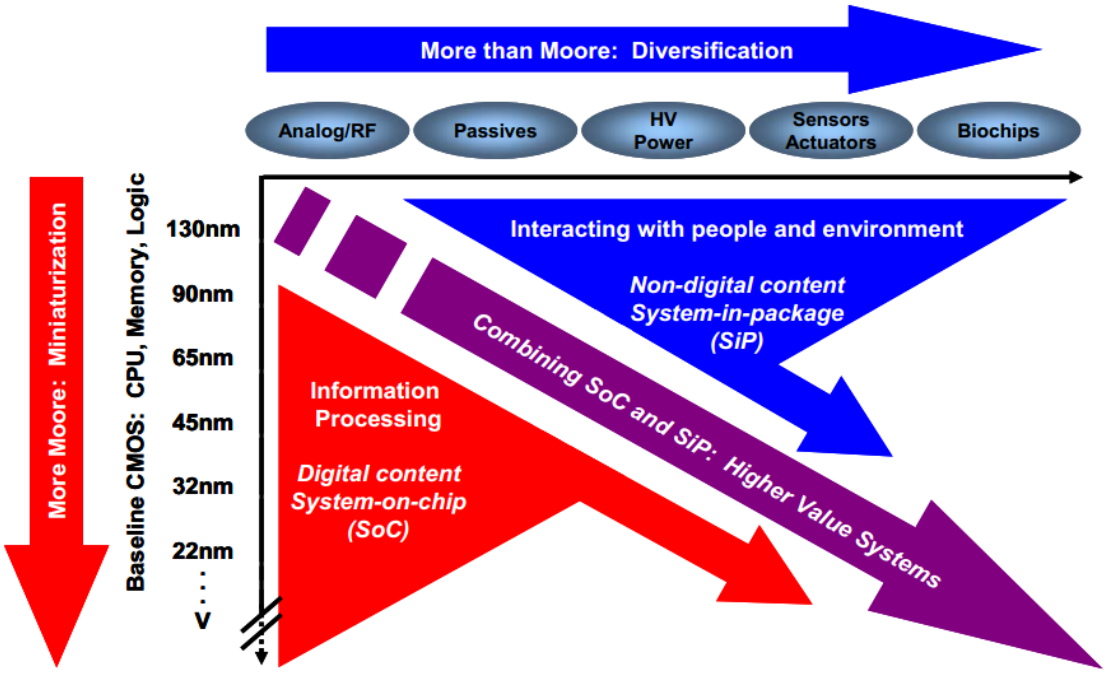


Figure 2-8 *More-Moore* and *more-than-Moore* technologies [42].

2.2.2 Predicted Advanced CMOS Technologies

From the discussions above, the CMOS IC performance and cost cannot be improved by violently shrinking the feature size. However, on the contrary, there are even more demands to be fulfilled by the IC industry. Surging applications such as mobile computing, big data, internet of things (IoT), etc. are requiring better IC performance in many aspects. To fill this gap, two advanced CMOS technologies have been proposed for future industry. Next, we introduce these two technologies, namely *more-than-Moore* technology and *more-Moore* technology, as shown in Figure 2-8.

Table 2-2 Different Technologies Preferred by Various Functional Circuits

Functionality	Preferred Technology Features
DRAM	Deep trench, high capacitance density
Analog	Sufficient VDD and voltage headroom
RF	Thick metal, high-Q inductors
Digital	Small feature size

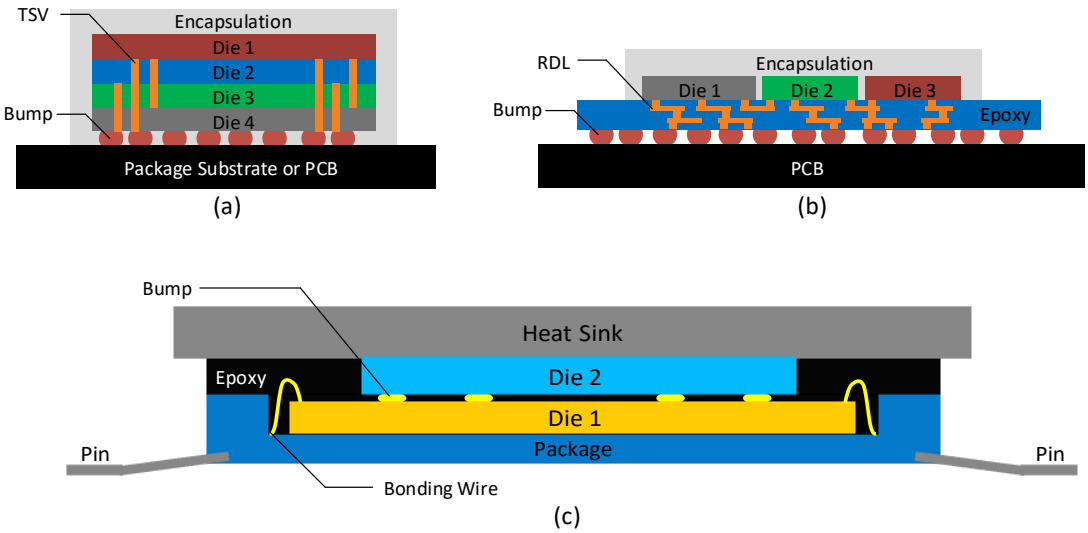


Figure 2-9 Exemplary SiP technologies combining several dies in one package, including (a) TSV, (b) InFO, and (c) dual-die flip-chip packaging.

More than Moore

The concept of *more than Moore* suggests separating the whole versatile system into several dies with different processes. Indeed, various circuits prefer different technologies to better achieve their functions and best performances. With this separation, these circuits can be fabricated with their preferred processes and do not need to struggle in the process with extremely small feature size. Table 2-2 lists some exemplary circuits and their preferable technologies.

Figure 2-9 shows several so-called SiP technologies. Figure 2-9(a) shows the concept of through-silicon via (TSV) technology. It permits stacking of several dies by using TSVs for connections. The advantage is that the total floor space of the whole design is reduced, at the cost of increased height which is acceptable for most applications. However,

fabrication cost of these TSVs is high since it uses some amount of the costly silicon area. One example of lower-cost integrations is the InFO shown in Figure 2-9(b). This technique uses low-cost materials such as epoxy to fasten the dies and grows redistribution layer (RDL) metals for interconnection. It was reported that the iPhone 7 processor, A10, had used InFO technology. Figure 2-9(c) shows another prototype of the author's project that integrates two dies with different processes using a simple flip-chip bonding.

More-than-Moore technology enables the combination of several sections with different processes, so that NREs of each circuit can be reduced by using mature and lower-cost process. For example, RF circuits can be fabricated in the 65 nm CMOS with satisfactory transistor characteristics. Another benefit is that since the process for these dies is not necessarily scaled, many mature designs can be reused, thus no extra design cycle is required for these modules. For example, even though the digital cores upgrade from a 28 nm process to a 10 nm process, a mature design with 180 nm process can still be reused in the future integration. Designers need only to verify the digital modules built with new process.

However, the recurring cost for each chip may not be reduced. In order to align and connect the dies, the packaging complexity and cost are increased compared with the traditional flip chip and wire bonding. Besides, testing has to be performed for each die, leading to higher testing cost for each product compared with the SoC technologies where the whole product is fabricated and tested in the same CMOS process. Since different circuits are allowed to use different preferred processes to achieve their best performance, this technology is function-oriented or performance-oriented.

More Moore

In contrast, the concept of *More Moore* keeps following the Law. The field-effect transistors (FET) can be implemented in new structures such as FinFETs or carbon nanotube FETs, so that the transistor density can still be increased in order to follow *Moore's Law*. Recurring cost can still be shrunk by these techniques. Circuits with mostly digital nature, such as central processing units (CPUs), can still benefit by using these

advanced processes in spite of the higher NREs. Besides, consumer electronics are still cost-oriented owing to their large number of users and short renewal cycle. In order to reduce recurring cost, some analog/RF/mixed-signal circuits may still need to be integrated with the digital cores on the same die for low-cost SoC products.

It should be emphasized that *more-than-Moore* technology is not an alternative or even competitor to the *more-Moore* technology. In fact, *more-than-Moore* technology aims for better functional diversity of an IC product.

2.3 PLL Schemes in Advanced CMOS Technologies

Based on the above review and discussion, we can conclude that the *more-than-Moore* and *more-Moore* technologies aim for different concerns. The function-oriented *more-than-Moore* technology permits different circuits to use preferred processes for better performance in different functions. The cost-oriented *more-Moore* technology suggests the whole design to use the same process to reduce cost. Accordingly, we can anticipate that multi-function electronics, such as future mobile phones, will rely more on *more-than-Moore* technology, while lower-cost electronics with great sales volume, such as simple IoT devices, will rely more on *more-Moore* technology.

For wireless transceivers in both product types, PLLs are still probably necessary. Therefore, PLLs can be fabricated in different types of technologies. According to their implementation, PLLs can be divided into two categories, namely “analog PLLs” and “digital PLLs”.

The term “analog PLL” does not have a consistent definition in various literatures and may refer to different PLL structures when it is used. This is same for “digital PLL”. Therefore, before the introduction, we clarify the definitions of both PLL types that will be used for following discussions.

In this thesis, the classification of digital PLL and analog PLL is based on how the phase error is represented and processed. An “analog PLL” refers to a PLL structure in which the phase error is represented as analog information, such as voltage or current pulse,

and is processed by an analog loop filter. In contrast, a "digital PLL" refers to a PLL structure that transforms the phase error into digital code, which is processed by a digital loop filter. In some literatures, a digital PLL is called "all-digital PLL" [13].

2.3.1 Analog PLL

Figure 2-10 shows the structure of a typical analog PLL. A phase detector and a charge pump (if any) constitute the error detector. An analog loop filter (using passive and maybe active components) acts as the error processor. A VCO is used as the output clock generator. The feedback network may be a frequency divider or other components, depending on different PLL structures. PLL designs using conventional technologies have been continuously developed and optimized to achieve better noise performance and lower power consumption. Many mature PLL designs can be found in both publication and product lists, e.g., [43]-[48].

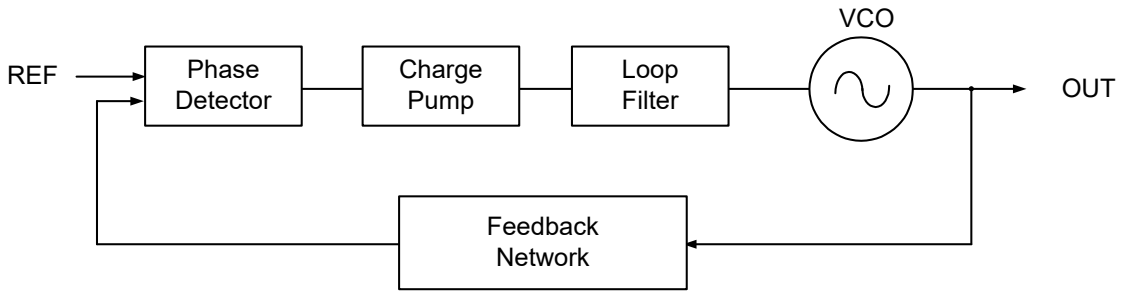


Figure 2-10 Structure of a general analog PLL.

However, due to continuous shrinking of feature size, non-idealities such as leakage and reduced transistor output impedance may degrade the noise performance of each block. Moreover, if an LC-VCO is used, most of the area of a common PLL is occupied by the VCO inductor and the loop filter. Unfortunately, area of these components does not scale with feature size, resulting in an even higher cost in advanced technologies. Hence, analog PLLs do not benefit much from the scaling when the feature size is already very small, such as CMOS with feature size less than 65 nm.

Thanks to the *more-than-Moore* technology, analog PLLs built with older process are still viable even if the more advanced process is used for the digital processors. Research

efforts in high-performance analog PLLs are still very worthwhile. In Chapter 3, we will investigate in-band phase noise reduction techniques in such analog PLLs.

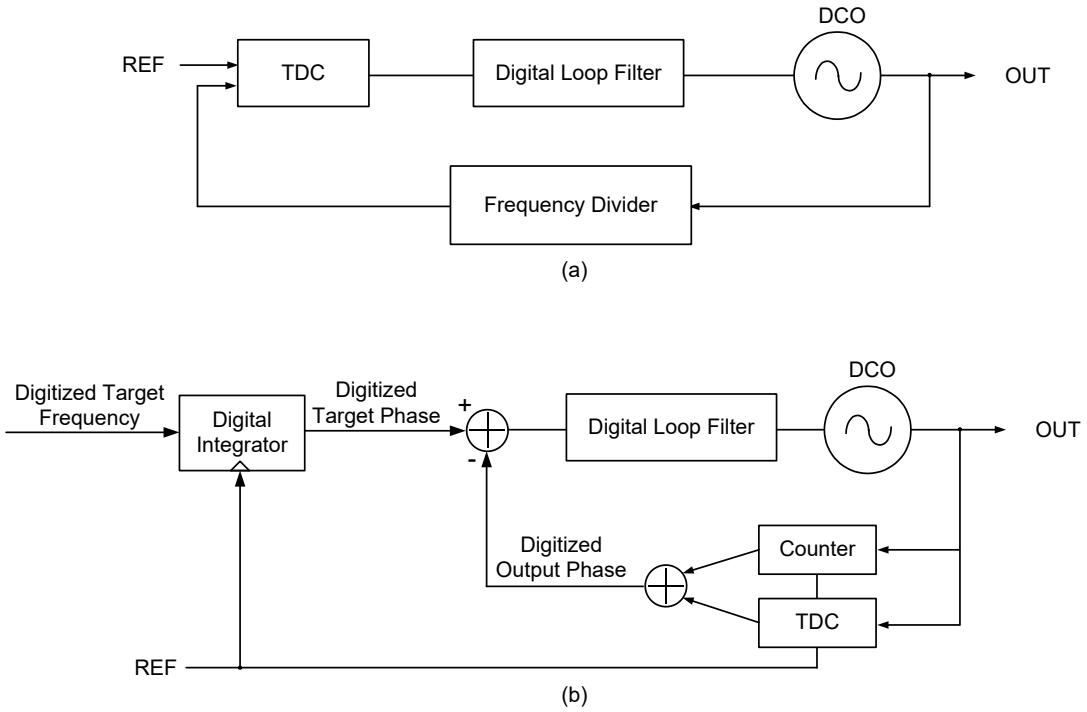


Figure 2-11 Structures of digital PLLs (a) with frequency divider and (b) without frequency divider.

2.3.2 Digital PLL

In order to enhance the PLL performance in scaling feature size, digital PLLs were proposed and developed [49]-[52]. The most important reason for the use of digital PLLs is the degradation of transistor analog characteristics in the technologies with smaller feature size. Figure 2-11 shows two digital PLL structures that are commonly used. The digital PLL in Figure 2-11(a) is a digital analogy of a conventional analog PLL, in which the phase detector and charge pump are replaced with a TDC to transform the phase error (or time error) into digital code. Accordingly, the TDC acts as the error detector and dominates the in-band phase noise in this structure. The TDC output code is fed into a digital loop filter that can be fully synthesized. Compared with an analog filter, a digital filter can be easily configured even during the PLL operation, enabling more sophisticate error processing. Moreover, such digital processing is ideal and noiseless. For CMOS feature size below 45

nm, a digital loop filter tends to be smaller than an analog loop filter with a comparative performance [13]. To connect with the digital loop filter interface, the VCO is replaced with a digitally controlled oscillator (DCO), whose frequency is digitally configured by the input word. Design and implementation of the frequency divider can be the same as in a conventional analog PLL. The divider-less digital PLL in Figure 2-11(b) was proposed by Texas Instruments. Integer and fractional error between the output phase and the reference phase are measured by a counter and a TDC, respectively. The two inputs to the TDC in Figure 2-11(a) usually have the same frequency. In Figure 2-11(b), frequencies of the two TDC inputs may be very different.

In contrast to an analog PLL, the only two physical noises among a digital PLL are the TDC noise and the DCO phase noise, corresponding to the error detector noise and the oscillator noise discussed in Chapter 2, respectively. Accordingly, TDC noise is the major contributor to in-band phase noise, and DCO phase noise dominates out-of-band phase noise. With a clean external reference clock, noise from TDC dominates of the in-band phase noise. TDC noise can be reduced with better TDC resolution. In analog PLLs, noise of the error detector relies on the analog characteristics, which is deteriorated if the feature size keeps scaling. In contrast, time resolution improves with such scaling, and the TDC resolution can be expected to improve in future. Digital PLLs are thus competitive in future finer technologies. Besides scaling, design techniques that can reduce TDC noise can also enhance in-band phase noise of digital PLLs.

In terms of a future IC product, a digital PLL can be fabricated together with the digital processor in the same CMOS technologies in order to reduce recurring cost. Research efforts in high-performance digital PLLs can bring large profit in these products. In Chapter 4, a technique providing low TDC noise will be demonstrated.

Table 2-3 provides a comparison between analog PLLs and digital PLLs. It can be seen that a digital PLL tends to prefer a scaled technology, and that an analog PLL may be a better choice in processes with moderate feature size and satisfactory analog characteristics. Therefore, the PLLs in future IC products may be implemented as analog

PLLs located in the die with larger feature size, or digital PLLs located in the die with finer feature size.

2.4 Summary

In this chapter, we review the PLL phase noise fundamentals and explain that the PLL in-band phase noise is usually limited by error detectors. Two major future PLL architectures are discussed based on future CMOS technologies. As a conclusion, both analog and digital PLLs are important for future industry and products. Analog PLLs are more mature and reliable with SiP technologies, and will not benefit much from the CMOS feature size scaling. In contrast, digital PLL performance and cost can still be improved in finer process. Specifically, we project that analog PLLs will be used in function-oriented applications and will be fabricated in suitable process, while digital PLLs will be integrated in cost-oriented products using CMOS process with smaller feature size.

Table 2-3 Characteristics Comparison between Analog and Digital PLLs in Processes with Moderate and Small Feature Sizes

Scheme	Moderate Feature Size	Small Feature Size
Analog PLL	Low power consumption Mature design and verification	Poor noise Long design cycle High cost Hard to design Hard to verify
Digital PLL	High power consumption Poor TDC noise	Reduced area Reduced noise Automatic design flow Shrinking cost

3 Low In-Band Phase Noise Analog Fractional-*N* SSPLL

In this chapter, we investigate some techniques that can reduce the in-band phase noise of an analog PLL. Specially, SSPLLs have the capability of reducing in-band noise from the error detector. A novel PS-SS technique is proposed in this chapter in order to enhance the in-band phase noise performance of SSPLLs and to broaden their applications in wireless communications by removing the time-consuming calibration. A phase model is proposed for phase noise calculation. A calibration-less PS-SSPLL prototype is fabricated in a 65 nm CMOS technology and measured to verify the low in-band noise in a fractional-*N* operation.

3.1 Literature Review of Divider PLLs and SSPLLs

In this section, we will introduce two important structures of analog PLLs, namely the divider PLLs and SSPLLs, so that the reader can understand our proposed technique more easily. The concept of delta-sigma modulator (DSM) will also be discussed briefly.

In Section 2.1.2, we have introduced the PLL noise characteristics using a general PLL phase model. In this section, this model is extended to compare the in-band noise performance of divider PLLs and SSPLLs.

3.1.1 Integer-*N* Divider PLL

Figure 3-1 shows the structure of a conventional analog divider PLL. The most important feature is that a frequency divider is used as the feedback network, i.e., $H_2(s) = 1/N$. In this thesis, we call this structure a divider PLL in order to distinguish from an SSPLL without feedback dividers. In some literatures, a divider PLL is called charge-pump PLL. When the PLL is locked, the phase error is regulated to around zero, yielding $\Phi_{REF} = \Phi_{out}/N$, thus $f_{out} = f_{REF} \times N$. If *N* is digitally configured, the output frequency is hence

digitally controlled to be a multiplication of the reference frequency. Accordingly, this PLL is called an integer-*N* divider PLL.

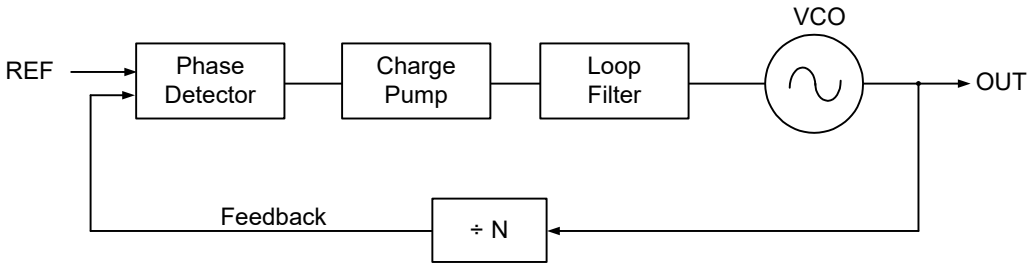


Figure 3-1 Basic structure of an analog divider PLL.

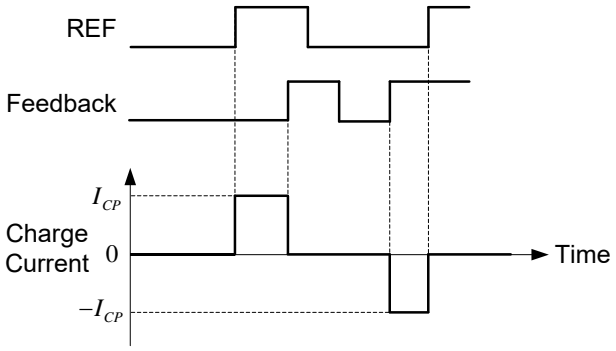


Figure 3-2 Input-output timing diagram of phase detector and charge pump.

A phase detector and a charge pump act as the error detector. The phase detector detects the phase difference between the feedback signal and reference input, and the charge pump generates a current pulse with fixed amplitude (denoted as I_{CP}). The width and polarity of this pulse represents the phase difference between reference clock and feedback clock, as shown in Figure 3-2. The current is positive if the feedback clock lags, while it is negative if the reference clock lags. According to Table 2-1, the in-band noise transfer function of the error detector in such a PLL is

$$\frac{\Phi_{out,n}(s)}{n_{detect}(s)} = \frac{N}{K_{detect}} \cdot \frac{G(s)}{1+G(s)} \approx \frac{N}{K_{detect}}. \tag{3-1}$$

The gain of the error detector is defined as

$$K_{detect} = \frac{\overline{\Delta i}\ over\ one\ cycle}{\Delta\Phi_{in}}, \tag{3-2}$$

which equals to

$$K_{detect} = \frac{I_{CP} \cdot \Delta t / T_{REF}}{2\pi \cdot \frac{\Delta t}{T_{REF}}} = \frac{I_{CP}}{2\pi}. \quad (3\text{-}3)$$

Substituting (3-3) into (3-1), the closed-loop transfer function of the error detector is

$$\frac{\Phi_{out,n}(s)}{n_{detect}(s)} \approx \frac{2\pi N}{I_{CP}}. \quad (3\text{-}4)$$

This reveals the fact that the error detector noise will be amplified by N before contributing to the PLL in-band phase noise.

3.1.2 Fractional-*N* Divider PLL

In the previous PLL, $f_{OUT} = N \times f_{REF}$. The wireless transceiver can change the value of N for different LO frequencies. To achieve a fine frequency tuning step (e.g., several kHz) for common transceivers, a small reference frequency can be adopted. By doing this, however, the loop bandwidth has to be reduced to even smaller, leading to more VCO phase noise as explained in Section 2.1.2.

If a fractional-*N* operation can be achieved, a higher-frequency input reference can be used for a specified output frequency step. Accordingly, the loop bandwidth can be large enough to suppress more VCO phase noise. A common realization of such a fractional-*N* division is using a dynamic division ratio, *N*, which is dithered by a controller, as shown in Figure 3-3.

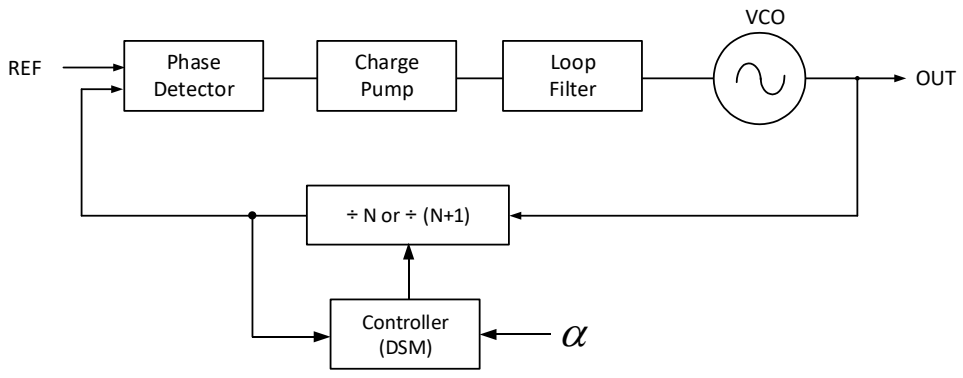


Figure 3-3 Conventional fractional-*N* divider PLL structure.

During its operation, the divider is still performing integer-*N* division at every instance of its output. However, the division ratio is changed after each its output, forming

a fractional average division ratio. Accordingly, a dithering controller can be used to dynamically switch the division ratio. As an example, the divider modulus is *N*+1when the controller outputs '1', whereas the divider modulus is set to *N* when controller outputs '0'. Over a long period of time, the average of controller output is α $(0 < \alpha < 1)$, and the average division ratio is thus $N + \alpha$.

The elegance of this dithering is that it achieves a fine-tuned average ratio even if the hardware supports only coarse steps. From a physical point of view, such a dithering utilizes *time* as an additional parameter along which an averaging can be performed. This concept can be extended to other parameters such as *space*. However, this will introduce issues related to this additional parameter. For a time-based dithering, a dithering noise is introduced.

Since the divider is dithered to obtain the target fractional ratio, any deviation from the target ratio is regarded as noise. This noise arises at the divider and is delivered to the error detector output and to the low-pass loop filter. Therefore, the high-frequency components (outside the loop filter bandwidth) of this dithering noise would be filtered out and should have negligible effect to the PLL phase noise. However, this filtering is helpless to the in-band dithering noise. Accordingly, a DSM is usually adopted owing to its noise-shaping characteristic.

There are several types of DSM that can be used in a fractional-*N* PLL. In this thesis, we only discuss a cascaded MASH 1-1 DSM adopt in our prototype. Figure 3-4 shows the signal flow of this DSM. In actual implementation, the input code, x, is a fine digital word with γ bits, where γ is an integer. The output code, y, is usually a coarse digital word (e.g., a 2-bit word). The quantizer is simply a digital block that extracts the MSB of its input as its output.

From the above signal flow, the output of the first quantizer is

$$y_1 = z^{-1}x + (1 - z^{-1})q_1, \tag{3-5}$$

and the second quantizer output is

$$y_2 = -z^{-1}q_1 + (1 - z^{-1})q_2. \tag{3-6}$$

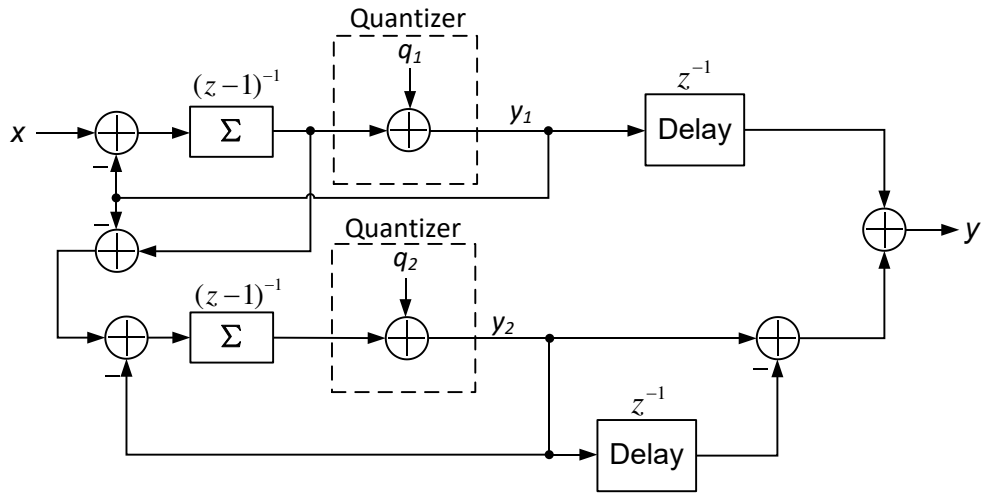


Figure 3-4 MASH 1-1 DSM structure.

After combination, the DSM output can be expressed as

$$y = z^{-1}y_1 + (1 - z^{-1})y_2 = z^{-2}x + (1 - z^{-1})^2 q_2. \tag{3-7}$$

Parameters q_1 and q_2 denote the quantization errors of the quantizer. Note that q_2 is the only quantization noise contributing to the DSM output, y, because q_1 is cancelled out after combination. In common calculations, it can be regarded as a white noise. From (3-7), the transfer function from x to y is z^{-2}, which is simply a two-cycle delay, hence an all-pass transfer function. Therefore, over a long period of time, the average value of y is

$$\bar{y} = x. \tag{3-8}$$

Since x is a fine digital word with γ bits, the tuning step of $\bar{y}$ is accordingly

$$\Delta\bar{y} = \frac{1}{2^{\gamma}}. \tag{3-9}$$

On the other hand, the noise transfer function (NTF) from q_2 to y is

$$\frac{y}{q_2}(\mathrm{z}) = (1 - z^{-1})^2, \tag{3-10}$$

which is a second-order high-pass transfer function. As a result, the DSM output exhibits a noise-shaped profile with reduced noise power at the low frequencies. However, designers need to note that the high-frequency components will be amplified by factor $(1 - z^{-1})$, requiring larger attenuation at the loop filter. A higher-order DSM can be designed to further reduce the low-frequency quantization error, at the cost of larger high-frequency quantization noise and requiring even higher-order attenuation at the loop filter.

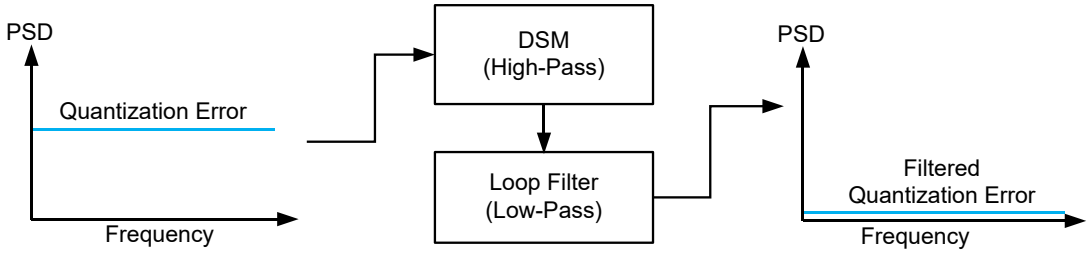


Figure 3-5 Conceptual signal path showing the impact of DSM and loop filter on quantization error.

From the above discussions, the dithering noise will be mitigated by the DSM noise shaping and the loop filter, as shown in Figure 3-5.

In-band phase noise analysis of a fractional-*N* divider PLL is the same with that of an integer-*N* divider PLL. As a matter of fact, due to the strong low-frequency attenuation in a DSM, the in-band phase noise of a divider PLL is hardly affected. Thus, fractional-*N* and integer-*N* divider PLLs have the same level of in-band phase noise.

3.1.3 Integer-*N* SSPLL

As discussed in Section 3.1.1, the noise from error detector is amplified by N times and contributes to the PLL in-band phase noise after a low-pass filtering. Assuming a low reference phase noise, noise from error detector dominates the in-band frequency region and limits the noise performance. To reduce the in-band noise, divider-less SSPLL was proposed [53].

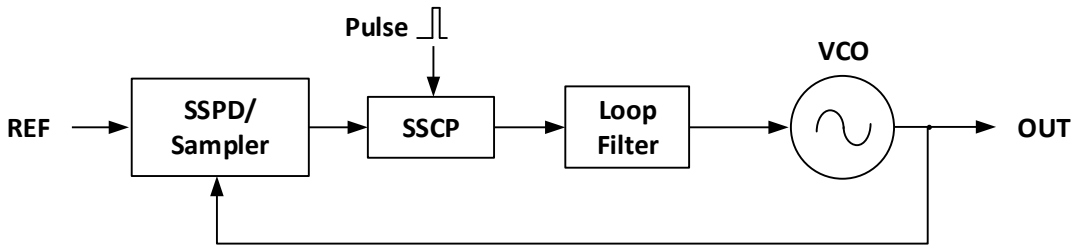


Figure 3-6 Structure of a conventional SSPLL.

Figure 3-6 shows the basic structure of a conventional integer-*N* SSPLL. A sampler is used as the subsampling phase detector (SSPD), and it tracks and holds the voltage directly from the oscillator. The oscillator frequency is *N* times higher than the sampling frequency,

where N is an integer. Upon the reference clock edge, the sampler captures the voltage of the oscillator output and feeds this voltage to a subsampling charge pump (SSCP). The SSCP is actually a G_m cell that transforms this voltage into a current pulse to the loop filter. The SSPD and SSCP constitute the error detector of a SSPLL. In contrast to the error detector in a divider PLL, this current pulse has a constant width while its current amplitude is proportional to the sampled voltage. The loop filter and VCO are the same as in a divider PLL.

During the subsampling operation, the sampling frequency of SSPD is f_{REF} and the sampled signal frequency is f_{OUT}. According to sampling theory, the sampler output is equivalent to a low-frequency alias at frequency

$$f_{alias} = f_{OUT} - Nf_{REF}, \tag{3-11}$$

where N is the largest integer fulfilling $0 < f_{OUT} - Nf_{REF}$. If the PLL output frequency is close to the target frequency (i.e., Nf_{REF}), f_{alias} should be very close to zero. The subsampling nature equivalently inserts an ideal $\times N$ frequency multiplier to the reference signal path before it enters the SSPD. Figure 3-7 shows an equivalent phase model of an SSPLL. After the SSPLL settles, the phase error will be corrected by the loop, yielding

$$f_{OUT} = N \cdot f_{REF}. \tag{3-12}$$

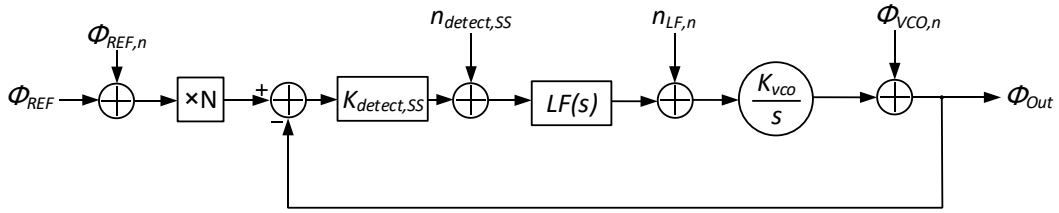


Figure 3-7 Phase model of a conventional SSPLL [53].

According to Table 2-1, the closed-loop transfer function from this error detector to PLL output is

$$\frac{\Phi_{out,n}(s)}{n_{detect,SS}(s)} = \frac{1}{K_{detect,SS}} \cdot \frac{G'(s)}{1+G'(s)} \approx \frac{1}{K_{detect,SS}}, \tag{3-13}$$

where $G'(s)$ is the open-loop transfer function

$$G'(s) = \frac{K_{detect,SS} LF(s) K_{VCO}}{s}, \tag{3-14}$$

and $K_{detect,SS}$ denotes the gain of the error detector (i.e., SSPD and SSCP).

Compared with a divider PLL, the closed-loop transfer function of the error detector is reduced by *N* times, implying that the error detector noise is not amplified by *N*. Moreover, the error detector gain, $K_{comp,SS}$, can be larger than that of a divider PLL, leading to even smaller phase noise contribution. It can be approximated as

$$K_{detect,SS} \approx g_m \cdot A_{VCO} \cdot f_{REF} \cdot t_{ON}, \tag{3-15}$$

where g_m, A_{VCO}, f_{REF}, t_{ON} denote the SSCP gain, VCO output voltage amplitude, reference frequency, and constant current pulse width, respectively.

To be noticed, based on (3-12), a SSPLL may lock at any integer times of reference frequency, as long as that output frequency is within the VCO output range. Besides, an SSPLL has limited frequency acquisition range, meaning that the SSPLL may lose lock if the output frequency is too far away from the target frequency. Thus, a frequency-locked loop (FLL) is commonly used to assist the SSPLL acquisition. When the phase error is small enough, the FLL can be suspended to reduce power consumption, and the SSPLL maintains the phase lock.

3.1.4 Fractional-*N* SSPLL

Due to the nature of subsampling, the above SSPLL can only operate in integer-*N* mode. During a fractional-*N* mode operation, the phase error between reference and oscillator will increase with time and thus the PLL fails to lock, as shown in Figure 3-8. Similar to an integer-*N* divider PLL, this large frequency step limits its application in wireless communications, and a low reference frequency is not practical, either.

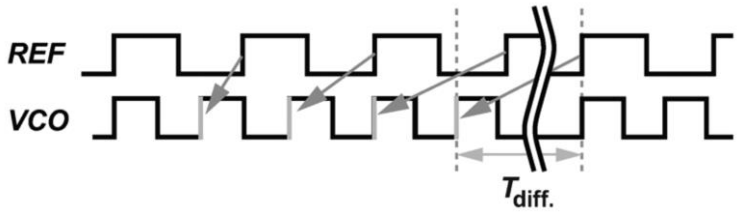


Figure 3-8 Phases fail to align with a fractional frequency ratio [55].

In recent years, two approaches have been reported to achieve fractional-*N* operation SSPLL [54]-[58]. In this thesis, we name these two methods as reference-shifting subsampling (RS-SS) and alias-cancelling subsampling (AC-SS).

Reference-Shifting SSPLL

In order to achieve fractional-*N* mode, an intuitive way is to modify the reference phase so that it can align with the VCO phase, shown as Figure 3-9.

By using a DTC as a controllable delay cell, the reference edge can be deliberately delayed within a certain range of time to align with the fractional-*N* output phase [54]- [57]. This is equivalent to changing the reference frequency to a new f_{REF} by simply shifting each of its edges. The new clock is applied to a traditional integer-*N* SSPLL as its input clock. In other words, the fractional function is realized at the reference clock. Therefore, similar to reference phase noise, any noise from the delay cell will be amplified by *N* to the PLL output. This poses design challenge to the delay cell.

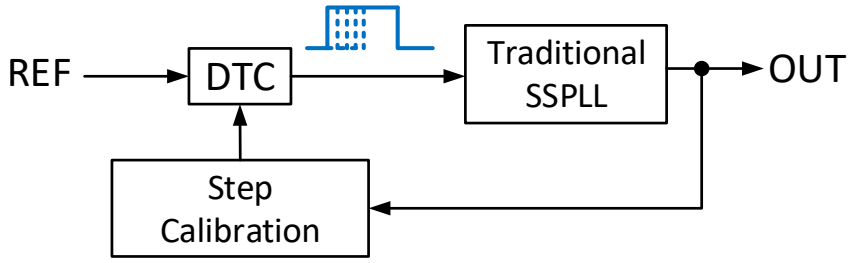


Figure 3-9 Achitecture of a fractional-*N* reference-shifting SSPLL.

The key consideration in this reference-shifting scheme is that, to ensure the perfect shifting of reference, the DTC step, τ_{DTC} has to be related to the oscillator period, T_{VCO}, i.e.,

$$\tau_{DTC} = T_{VCO}/P, \tag{3-16}$$

where P is an integer. With a larger value of P, the reference edge can be shifted more accurately in order to align better with the VCO feedback. However, every time the target frequency is changed, τ_{DTC} has to be calibrated so that (3-16) can be maintained, otherwise this DTC gain error will degrade the in-band phase noise performance. Authors in [54]-[57] paid a great effort in the DTC design and calibration of the DTC step.

Unfortunately, such calibration requires not only sophisticated design but also operation effort and time. A calibration time of about 20 ms was measured [55]. Before the calibration is finished, the in-band phase noise and jitter performance of the PLL output is at poor levels. For applications requiring short settling time or fast frequency modulation, such a time-consuming calibration simply cannot complete.

Alias-Canceling SSPLL

Another approach to fractional-*N* SSPLL is shown in Figure 3-10 [58]. Figure 3-11 shows its operation principle. In contrast, this work did not align the reference phase with the oscillator phase. Instead, it deliberately generates an artificial signal to cancel out the alias, which is generated in a fractional-*N* subsampling. After cancellation, the error detector acts as if there is no phase error. Therefore, the PLL can be locked at a fractional-*N* output.

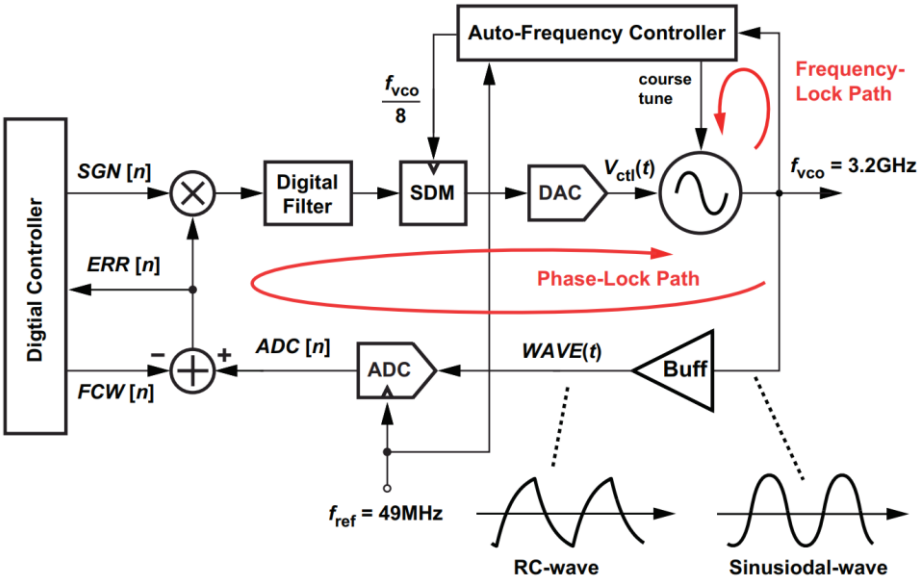


Figure 3-10 Architecture of a fractional-*N* alias-canceling SSPLL [58].

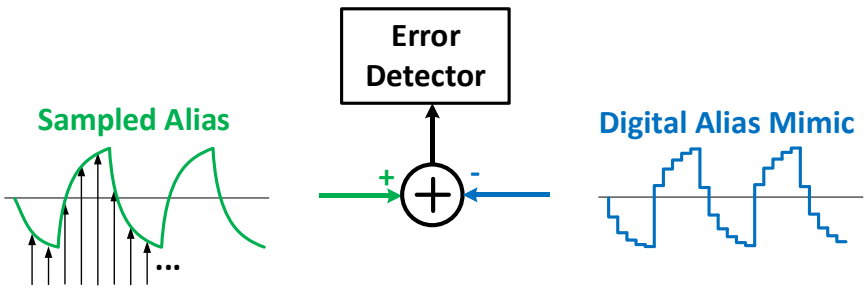


Figure 3-11 Operation of alias canceling.

The critical requirement is to cancel out the alias completely. Due to the nature of the alias, to distinguish a positive frequency deviation from a negative one, the alias waveform being sampled has to be predetermined and asymmetrical. Hence, a sine wave is not suitable due to its symmetrical shape. In this work, a buffer transforms the oscillator output wave into an asymmetrical RC charging/discharging wave. In order to mimic such an RC wave in a digital manner, the alias cancellation is performed in digital domain. During its operation, an analog-to-digital converter (ADC) is used to capture the RC wave, and the artificial RC wave is read from digital memory and to subtract the captured wave. After subtraction, a digital difference representing the phase error is generated for the control loop.

However, there exists some inevitable difference between the digital RC wave and the actual alias wave, resulting in phase noise to the PLL output. Therefore, calibration is also need in this alias-cancelling scheme. With an ADC with higher resolution, such difference can be reduced, at the cost of higher ADC power consumption.

In summary, both existing techniques for fractional-*N* SSPLL require time-consuming calibrations. Long calibration time prevents such SSPLLs in wireless transceivers that require short settling time. In this research, we try to propose a fractional-*N* SSPLL technique that can radically remove these calibrations.

3.2 Proposed PS-SS Technique

From the previous discussion, the calibration stems from the fact that the shifting step must be related to the VCO output period. Each time the SSPLL is set to another target frequency, the VCO period is changed and the shifting step has to be adjusted accordingly by the calibration, resulting in a long calibration time.

If the shifting step is directly from the VCO phase, such a calibration is no longer needed. To realize such a shifting, a PS-SS technique can be used as shown in Figure 3-12. If the VCO contains several phases, a multiplexer (i.e., MUX in the figure) can select one phase to be fed to the sampler. This phase switching equivalently shifts the feedback signal

with a step that is directly related to the VCO period. A phase-switching controller determines which phase to be selected in order to set the target output frequency. By doing so, the integer input-output relation can be changed.

3.2.1 Constant-Step Phase Switching

The non-integer output frequency tuning step can be explained if we take a look at the operation of the phase switching with a constant switching step. Assume the VCO provides a k-phase output. Phase difference of these phases is $2\pi/k$. Figure 3-13 illustrates the corresponding realization. In this example, the VCO provides an eight-phase output (Φ_0 to Φ_7), so k=8.

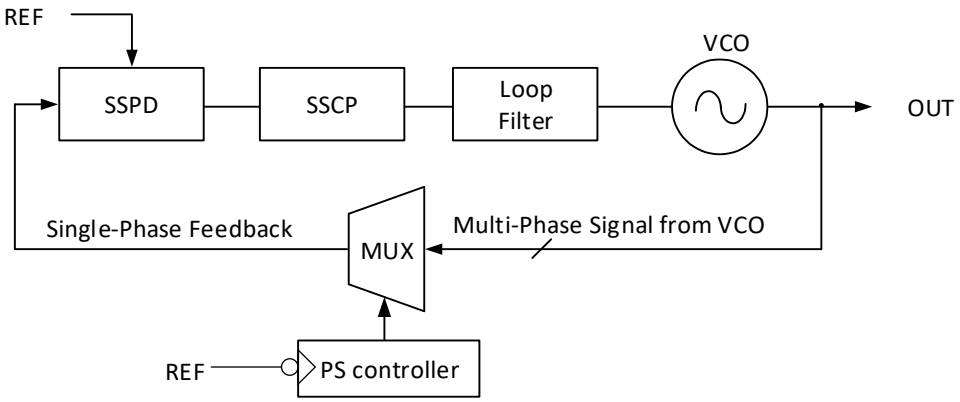


Figure 3-12 Architecture of a PS-SSPLL.

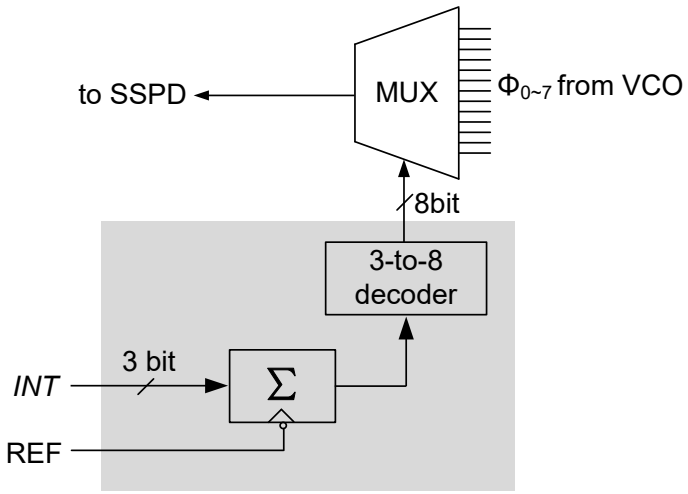


Figure 3-13 Structure of constant-step phase switching.

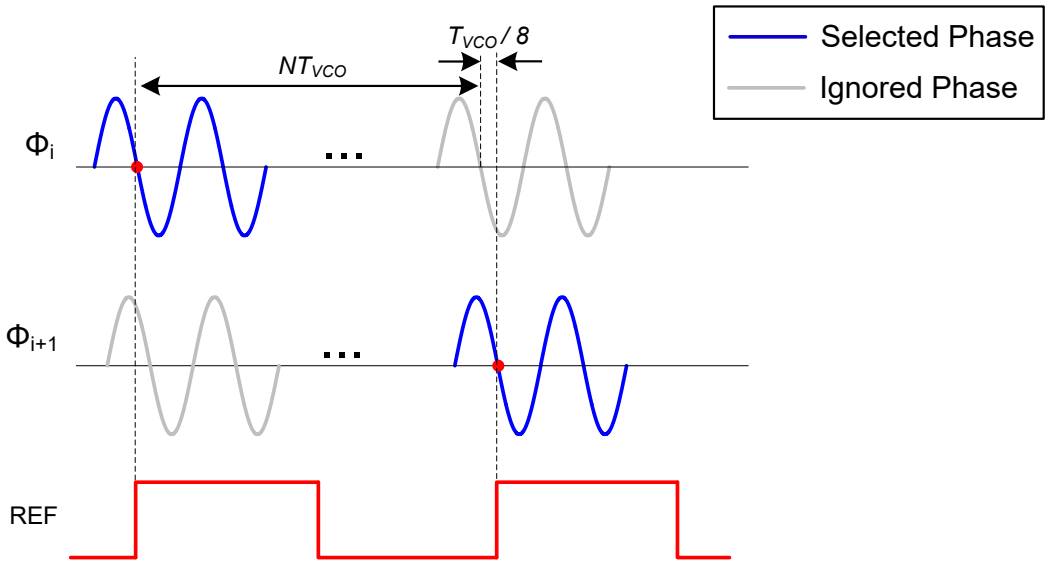


Figure 3-14 Timging diagram of constant-step phase switching ($INT = 1$).

Figure 3-14 shows the timing diagram during its operation. A constant step $INT = 1$ is chosen in this example. At the first sampling, Φ_0 is selected to be sampled. At the next sampling, Φ_1 is selected to be sampled, followed by Φ_2, Φ_3, and etc. Note that after Φ_7 is selected, the controller wraps back and select Φ_0 for the following cycle.

Note that each time the next phase is selected, a phase shift of $2\pi/8$ is equivalently subtracted. According to timing diagram,

$$T_{REF} = \left(N + \frac{1}{8}\right) T_{VCO}. \tag{3-17}$$

Hence,

$$f_{VCO} = \left(N + \frac{1}{8}\right) f_{REF}, \tag{3-18}$$

where N is an integer that $\left(N + \frac{1}{8}\right) f_{REF}$ is within the VCO output range. Equation (3-18) implies a non-integer relation between f_{VCO} and f_{REF}. If the constant step is changed to other values, (3-18) is accordingly modified to

$$f_{VCO} = \left(N + \frac{INT}{8}\right) f_{REF}. \tag{3-19}$$

If the value of INT can be programed externally with a step of $\Delta INT = 1$, this enables an output frequency step of

$$\Delta f_{VCO} = \frac{f_{REF}}{8}. \tag{3-20}$$

More generally, if there are k phases to be selected, the output frequency would be

$$f_{VCO} = \left(N + \frac{INT}{k}\right) f_{REF}, \tag{3-21}$$

and the tuning step would be

$$\Delta f_{VCO} = \frac{f_{REF}}{k}. \tag{3-22}$$

This means that a finer tuning step can be achieved with more phases provided.

3.2.2 DSM-Assisted Phase Switching

For a SSPLL using 40 MHz reference clock, even with an eight-phase VCO, the resolution of f_{VCO} is as large as $40\,MHz/8 = 5\,MHz$, which is still too large for wireless transceivers. Reason for this limitation is that in (3-19), INT is integer. Recall that in a divider PLL where the division ratios cannot be finely tuned, DSM dithering can be applied to the division ratio for a fine tuning step. Similar dithering can be added to INT to build a truly fractional-*N* SSPLL.

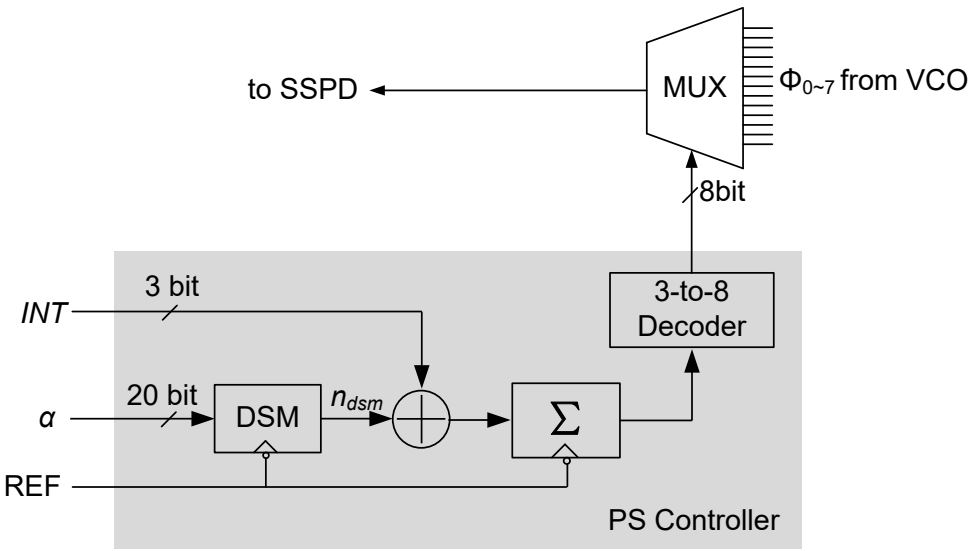


Figure 3-15 Structure of DSM-assisted phase switching.

Phase switching with a DSM can be implemented as shown in Figure 3-15. The DSM generates a dynamic integer, n_{dsm}, according to an accurate digital input, α. Due to the nature of DSM, an average of $\overline{n_{dsm}} = \alpha$ is obtained over a long period of time. The DSM

output is added with INT before entering the integrator. Therefore, the PLL output frequency can be expressed as

$$f_{VCO} = \left(N + \frac{INT + \overline{n_{dsm}}}{8}\right) f_{REF}. \tag{3-23}$$

From the DSM theory, fractional number, $\overline{n_{dsm}}$, can be tuned with a step of $1/2^{\gamma}$, where γ denotes the input bit width of the DSM. Hence, the output frequency tuning step is reduced to

$$\Delta f_{VCO} = \frac{f_{REF}}{8 \times 2^{\gamma}}. \tag{3-24}$$

INT	-	3	3	…	3	…	3	…
n_{dsm}	-	2	1	…	0	…	0	…

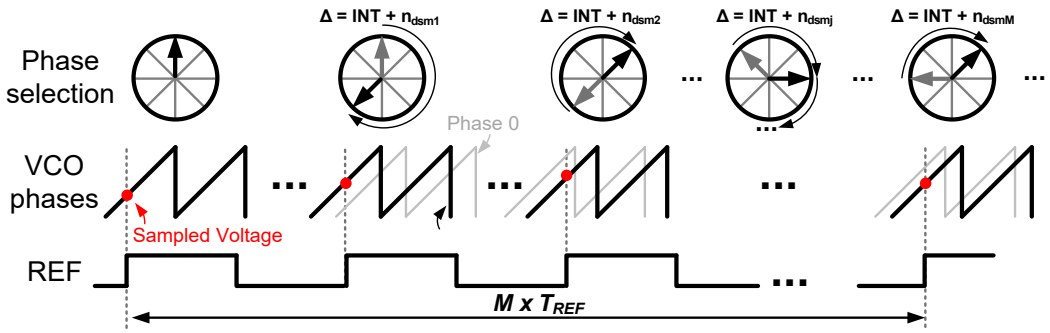


Figure 3-16 Timing diagram of DSM-assisted phase switching.

As an example, if $f_{REF} = 40MHz$ and $\gamma = 20$, an PLL frequency tuning step of $\Delta f_{VCO} \approx 4.8Hz$ is achieved.

An example in Figure 3-16 illustrates the realization of this fractional-N subsampling through DSM dithering. In the figure, $INT = 3$ is a fixed input, and n_{dsm} is the DSM output sequence. Among the VCO phases, the selected phase to be sampled is highlighted as the dark curve, and Φ_0 is also shown for better understanding. After each cycle, the phase is shifted by

$$\frac{2\pi}{8}\left(INT + n_{dsm_j}\right), \tag{3-25}$$

where j denotes the cycle index. During the locked state, over a long period of $M \times T_{REF}$, where M is a large integer, the total phase shifted is

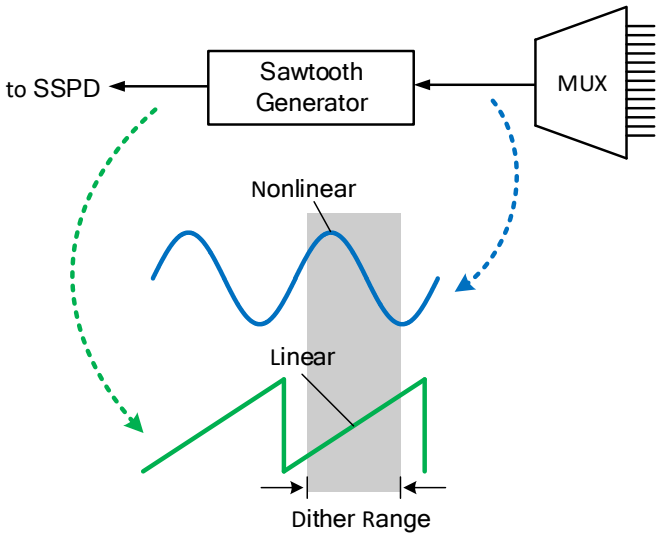


Figure 3-17 Feedback signal can be transformed into a sawtooth wave with a larger linear range for DSM dithering.

$$\sum_{j=1}^{M} \frac{2\pi}{8}\left(INT + n_{dsm_j}\right). \tag{3-26}$$

The average shifted phase number during each T_{REF} is thus

$$\left(\sum_{j=1}^{M} \frac{2\pi}{8}\left(INT + n_{dsm_j}\right)\right)/M \approx \frac{2\pi}{8}(INT + \overline{n_{dsm}}). \tag{3-27}$$

It can be seen in the timing diagram that the sampled voltage is equivalently dithered by the DSM output sequence. According to the DSM theory, this dithering contains high-pass shaped noise, which can be reduced by the loop filter. However, to ensure an effective filtering to DSM noise, the feedback waveform should be linear across the sampled voltage range. Therefore, the feedback waveform can be transformed into sawtooth for a large linear range, as shown in Figure 3-17.

Table 3-1 give a comparison of fractional-*N* PLLs. Since the switching step is directly related to VCO phase, PS-SS technique eliminates the need for calibration radically.

Table 3-1 Comparison among Fractional-*N* Divider PLLs and SSPLLs

PLL Scheme	In-band Phase Noise	Calibration
Divider PLLs	High	Free
RS-SSPLL	Low	Needed
AC-SSPLL	Low	Needed
PS-SSPLL	Low	Free

3.3 Proposed Phase Model

3.3.1 Phase Switching Noise

From the fractional-*N* PS-SSPLL architecture in Figure 3-12, a phase model can be produced as in Figure 3-18. The phase shifting controller determines the amount of shifted (i.e., subtracted) phase in the feedback path. At each cycle, the selected phase index increment is $INT + n_{dsm} = INT + \alpha + Q_{DSM}$, where α denotes the target DSM fractional output and Q_{DSM} denotes the shaped DSM noise. For an 8-phase VCO, the subtracted phase step is $2\pi/8$.

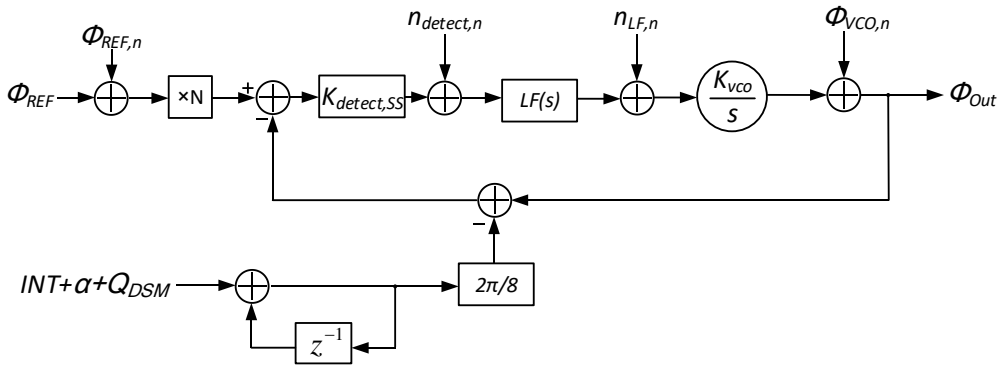


Figure 3-18 Phase model of the proposed PS-SSPLL.

The phase model can be reconstructed for easier analysis. For the index increment in Figure 3-18, $INT + \alpha$ is constant. This means that a constant phase amount of $2\pi(INT + \alpha)/8$ is subtracted after each reference cycle (i.e. each $\frac{\Phi_{REF}}{2\pi}$ cycle). Therefore, as the reference phase increases, this accounts for a total subtracted phase amount of

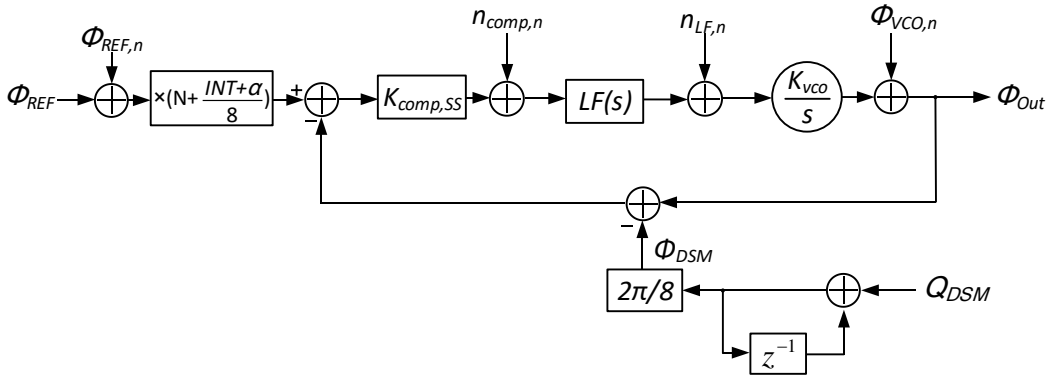


Figure 3-19 Reconstructed phase model of the proposed PS-SSPLL.

$$\frac{2\pi(INT+\alpha)}{8}\cdot\frac{\Phi_{REF}}{2\pi}=\frac{INT+\alpha}{8}\cdot\Phi_{REF}. \tag{3-28}$$

This is a function of Φ_{REF}. Thus, this constant phase subtraction can be merged into the reference signal path. Considering the impact of Φ_{REF} noise, the phase model can be reconstructed as in Figure 3-19. As can be seen, the amplification factor is changed into a fractional value of $N+\frac{INT+\alpha}{8}$. The output frequency is thus

$$f_{OUT}=\left(N+\frac{INT+\alpha}{8}\right)f_{REF}. \tag{3-29}$$

Note that the DSM output noise is shaped according to the DSM theory. Assuming the DSM has a quantization noise transfer function of $NTF(z)$, the DSM output noise is

$$n_{DSM}(z)=q_2\cdot NTF(z), \tag{3-30}$$

where q_2 is the quantization error of the DSM quantizer. According to the model, the inserted phase switching noise is

$$\Phi_{DSM}(z)=\frac{2\pi}{8}\cdot\frac{1}{1-z^{-1}}\cdot n_{DSM}(z). \tag{3-31}$$

Combining (3-30) and (3-31), the inserted phase switching noise is

$$\Phi_{DSM}(z)=\frac{2\pi}{8}\cdot\frac{1}{1-z^{-1}}\cdot q_2\cdot NTF(z). \tag{3-32}$$

The shape of the phase switching noise depends on the DSM noise transfer function. In out prototype, a MASH 1-1 DSM is adopted, thus $NTF(z)=(1-z^{-1})^2$. For a continuous-time analysis, the z-domain $\Phi_{DSM}(z)$ can be transformed into s-domain $\Phi_{DSM}(s)$.

3.3.2 Phase Mismatch

In the previous discussion, we assume no phase mismatch among the VCO phases. This is not true in the real implementation. Effect of such phase mismatch is evaluated in this section. As the average adjacent phase difference is always $2\pi/8$ as long as the output frequencies of the dividers are stable, the average phase mismatch among eight phases should be zero:

$$E(\Phi_{mm})=\frac{1}{8}\sum_{i=0}^{7}\Phi_{mm,i}=0, \tag{3-33}$$

where $\Phi_{mm,i}$ denotes the phase mismatch of the i-th phase, and $E(\Phi_{mm})$ is the expectation of the phase mismatch. Definition of the phase mismatch is

$$\Phi_{mm,i} = \frac{2\pi T_{mm,i}}{T_{FB}}, \tag{3-34}$$

where $T_{mm,i}$ is the time mismatch of the i-th phase, and T_{FB} is the feedback clock period. We set the first phase Φ_0 as a reference without mismatch, thus $\Phi_{mm,0} = 0$. The values of $T_{mm,i}$ can be obtained by post-layout simulation of the multiplexer and the frequency divider chain. Based on (3-34), $\Phi_{mm,i}$ can be determined.

In the real implementation, the mismatch of each phase is mostly because of the layout and fabrication mismatch, such as different routing length or transistor parameters. Mismatch among different outputs of the frequency dividers may also exists due to the similar reasons. An important characteristic of these mismatches is that they do not change with time during the SSPLL operation.

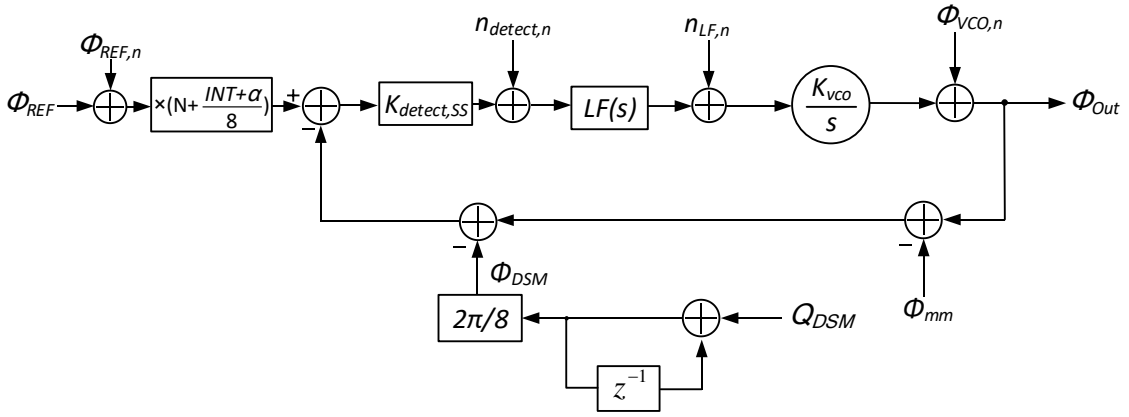


Figure 3-20 Phase model with multi-phase mismatch added.

Under DSM dithering, the phases are randomly selected as the feedback signal. Therefore, the phase mismatch acts as a random phase noise introduced to the feedback path, as shown in the revised phase model in Figure 3-20. Since the phase is selected randomly, the inserted rms phase noise is

$$\Phi_{mm,rms} = \sqrt{\frac{1}{8}\sum_{i=0}^{7} {\Phi_{mm,i}}^2}. \tag{3-35}$$

Table 3-2 Closed-Loop Transfer Functions from each Noise Source to PS-SSPLL Output

Noise Sources	Transfer Function*	Transfer Function Type
Reference Phase	$\frac{\Phi_{out,n}}{\Phi_{REF,n}}(s) = \left(N + \frac{INT+\alpha}{8}\right)\frac{G'(s)}{1+G'(s)}$	Low Pass
Error Detector (i.e., Sampler + SSCP)	$\frac{\Phi_{out,n}}{n_{comp,n}}(s) = \frac{1}{K_{comp,SS}} \cdot \frac{G'(s)}{1+G'(s)}$	Low Pass
Loop Filter	$\frac{\Phi_{out,n}}{n_{LF,n}}(s) = \frac{K_{VCO}}{s} \cdot \frac{1}{1+G'(s)}$	Band Pass
VCO Phase	$\frac{\Phi_{out,n}}{\Phi_{VCO,n}}(s) = \frac{1}{1+G'(s)}$	High Pass
DSM	$\frac{\Phi_{out,n}}{\Phi_{DSM}}(s) = \frac{G'(s)}{1+G'(s)}$	Low Pass
Mismatch	$\frac{\Phi_{out,n}}{\Phi_{mm}}(s) = \frac{G'(s)}{1+G'(s)}$	Low Pass

* Open-loop transfer function $G'(s) = K_{comp,SS} \cdot LF(s) \cdot K_{VCO}/s$.

Under stochastic dithering at frequency of f_{REF}, this phase noise will be spread equally over the frequency range from $-f_{REF}/2$ to $+f_{REF}/2$. The single-sided PSD level of mismatch is thus

$$S_{\Phi_{mm}} = \frac{2 \cdot {\Phi_{mm,rms}}^2}{f_{REF}}. \tag{3-36}$$

Similar to the DSM noise, its noise transfer function to the PLL output is

$$\frac{\Phi_{out,n}}{\Phi_{mm}}(s) = \frac{G'(s)}{1+G'(s)}. \tag{3-37}$$

This is also a low-pass transfer function, implying that a contribution from mismatch to in-band phase noise. Using (3-36) and (3-37), the in-band phase noise contribution of mismatch can be calculated. Assuming a very poor matching of $\Phi_{mm,rms} = 1$ rad and a reference clock of 40 MHz, the in-band phase noise due to mismatch is merely -146 dBc/Hz, which is much lower than other noises. Therefore, for practical implementation, the mismatch should have negligible impact to in-band phase noise.

The closed-loop transfer functions from each noise source to the SSPLL phase noise are listed in Table 3-2.

In contrast to the prior RS-SSPLL where the DTC noise is amplified by N, the noise introduced in the proposed PS-SS technique is not amplified. This reveals a less strict design requirement for the multiplexer and the DSM.

3.4 Fractional-*N* Low-Noise PS-SSPLL Implementation

To begin with, Table 3-3 lists the design specifications of our prototype. Based on the specification of a GSM mask scaled to 2.5 GHz carrier frequency, a phase noise level of -100 dBc/Hz is used as the in-band specification.

Table 3-3 Specifications of the PS-SSPLL Prototype

Characteristics	Values
Reference Frequency	40 MHz
PLL Output Frequency	2.4 to 2.8 GHz
VCO Gain	50 MHz/V
Loop Bandwidth	0.4 MHz
In-band Phase Noise	-100 dBc/Hz
Power Consumption	15 mW

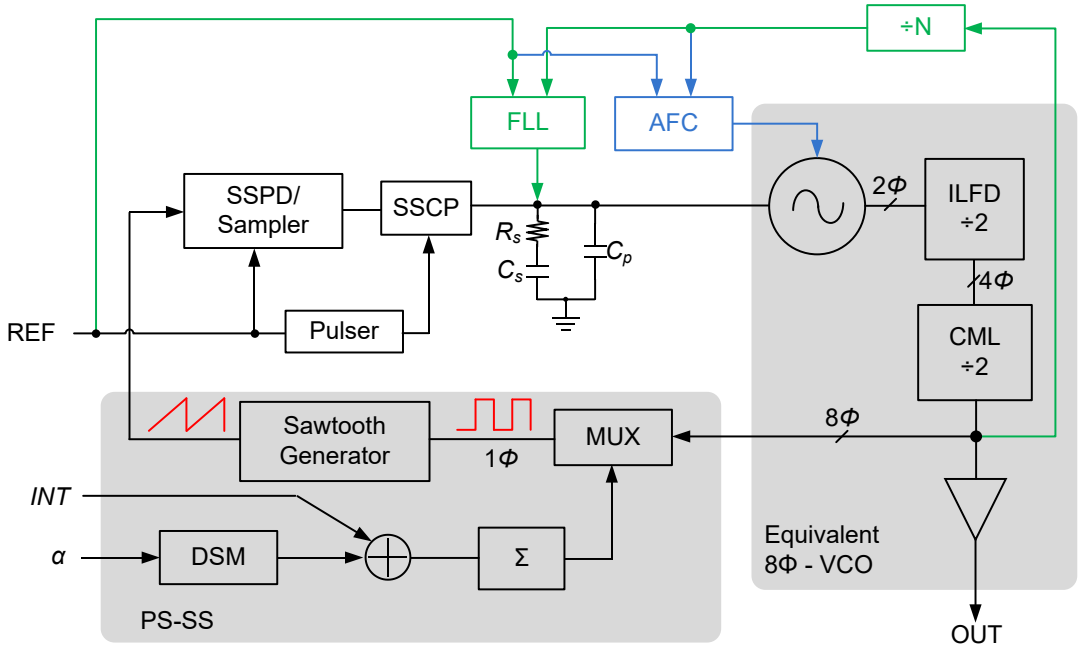


Figure 3-21 Schematic of the PS-SSPLL prototype.

Figure 3-21 shows the schematic of the overall proposed PS-SSPLL. Similar to a conventional integer-*N* SSPLL, an FLL and a digital automatic frequency controller (AFC) are equipped to assist the frequency locking within tens of reference cycles. Compared with a conventional integer-*N* SSPLL, only the phase switching module is inserted.

3.4.1 VCO and 8-Phase Feedback Signal

Realization of the phase switching requires a multi-phase VCO output. In this prototype, a conventional 10 GHz differential-output VCO and two subsequent frequency dividers are adopted and act together as an 8-phase 2.5 GHz VCO.

As a matter of fact, this VCO-divider structure is suitable for our calibration-free requirement. Indeed, techniques such as delay-locked loop or phase interpolation can also be used to generate the multi-phase output. However, these are not suitable because the most important consideration for our design is to generate the 8 phases without calibration. Using frequency dividers are preferable since the dividers take little time to settle. As a side benefit, this scheme provides a quadrature output at 5 GHz and an 8-phase output at 2.5 GHz, covering more frequency bands with more phases for the user applications. The 8-phase output can also be generated by a 5 GHz quadrature VCO and a frequency divider.

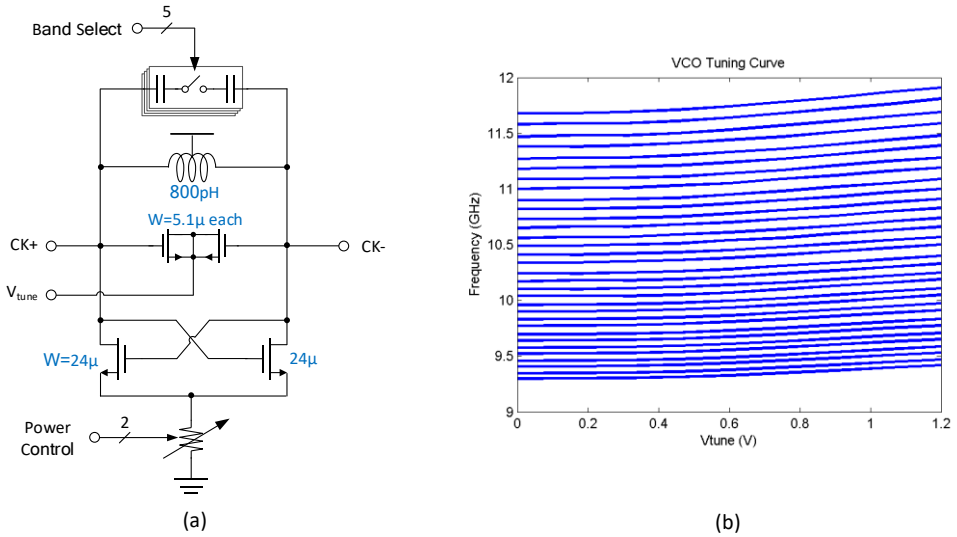


Figure 3-22 (a) VCO schematic and (b) post-layout simulation of its tuning curve.

Figure 3-22(a) shows the schematic of the 10 GHz VCO. The K_{VCO} is about 200 MHz/V. A capacitor array is used for wider frequency coverage, providing totally 32

frequency bands. An AFC is designed to provide the band selection word. The varactor is tuned by V_{tune}, which is the output voltage of the loop filter. Figure 3-22(b) provides the post-layout simulation of the VCO frequency, showing a VCO output range seamlessly from 9.3 to 11.9 GHz. After divided by 4, the output frequency ranges from 2.325 to 2.975 GHz.

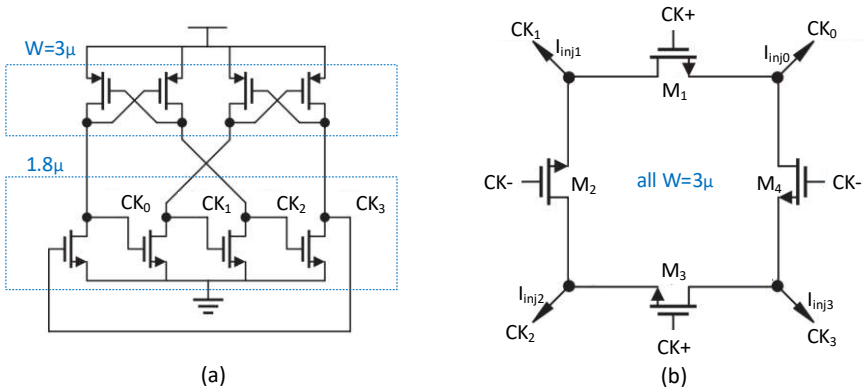


Figure 3-23 Schematic of the adopted ILFD [59].

As shown in Figure 3-21, the VCO is followed by two frequency dividers. The first divider takes the 2-phase VCO output and generates a 4-phase clock at 5 GHz. An injection-locked frequency divider (ILFD) with the same structure as [59] is adopted to take advantage of its higher input frequency and wide locking range. Figure 3-23 shows the schematic of this ILFD. It contains a two-stage differential RC ring oscillator for high free-running frequency and quadrature outputs. Each stage uses a cross-coupled PMOS load. The four NMOS tail transistors are connected as an oscillator (oscillation loop). The drains of these NMOS transistors are connected to another loop (injection loop) formed by transistors $M_{1\text{-}4}$. The differential input clock (i.e., *CK*+ and *CK*-) drives the gates of $M_{1\text{-}4}$. Such a connection guarantees the quadrature relation among the output clock, $CK_{0\sim3}$. In conventional ILFDs, large injection transistors result in larger injection currents and larger locking range. On the other hand, they can damp the ring oscillator and reduces its locking range. This tradeoff is eliminated in this ILFD. The injection loop generates four quadrature currents at nodes $CK_{0\text{-}3}$. These currents inject into the oscillation loop, performing a multi-phase injection. Hence, a larger locking range is achieved. Post-layout

simulation shows its input frequency range from 9 GHz to 14 GHz with less than 1 mA current consumption at a 1.2V supply.

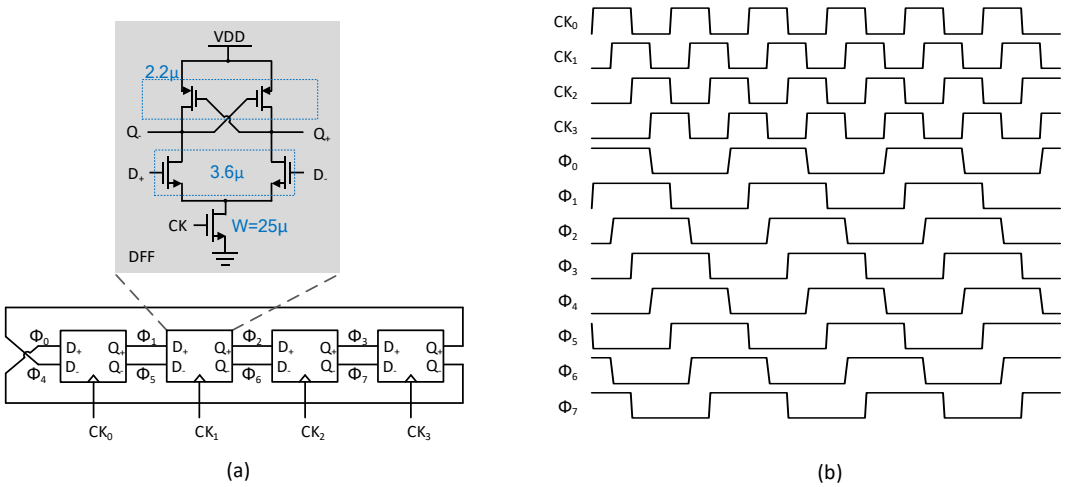


Figure 3-24 (a) Schematic and (b) timing diagram of the adopted 4-input 8-output CML divider.

The other frequency divider takes the 4-phase clock (i.e., $CK_{0\sim3}$) from the ILFD, and generates the 8-phase output to be selected. Figure 3-24(a) shows the schematic of this 4-input 8-output divider. This divider can be regarded as a cascaded DFF chain triggered by $CK_{0\text{-}3}$. Each DFF uses an identical current-mode logic (CML) structure. The differential structure can also reduce the interference from the divider to the power supply. Figure 3-24(b) illustrates the timing diagram during its operation. The eight outputs will be processed by the subsequent phase multiplexer. Post-layout simulation of this divider shows a maximum input frequency of 7 GHz with 2 mA current consumption from a 1.2 V supply.

The above VCO and two dividers constitute the equivalent 8-phase 2.5 GHz VCO in Figure 3-21. Figure 3-25 shows the simulated worst−case phase noise of the 8-phase output clock at 2.9 GHz.

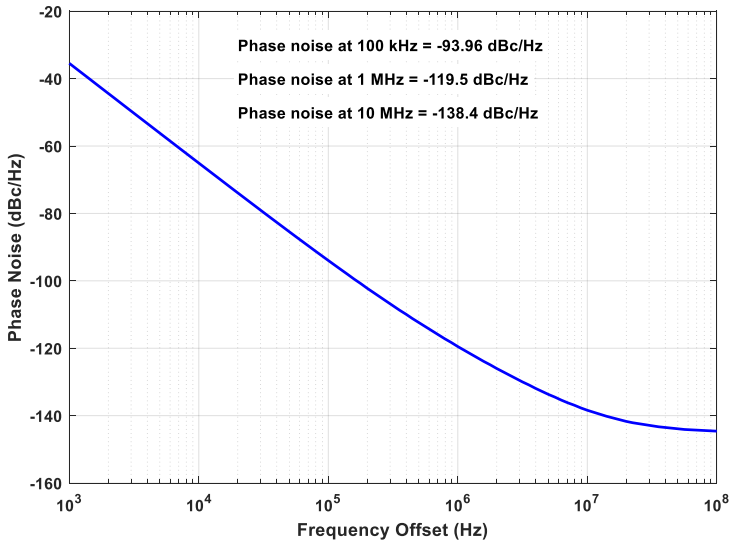


Figure 3-25 Post-layout simulation showing worst case phase nosie of the 8-phase clock.

3.4.2 Multiplexer and Sampler

In this prototype, the multiplexer selects a certain phase from the 8 phases of the 2.5 GHz clock. Figure 3-26 shows the schematic of the multiplexer. Transmission gates are used for each signal path. The 8-bit one-hot selection code $SEL_{0\sim7}$ controls the state of the transmission gates. If a *SEL* bit is high, the corresponding phase is connected to the output node, while the others kept isolated. Note that all the input phases are square wave due to the CML divider logic.

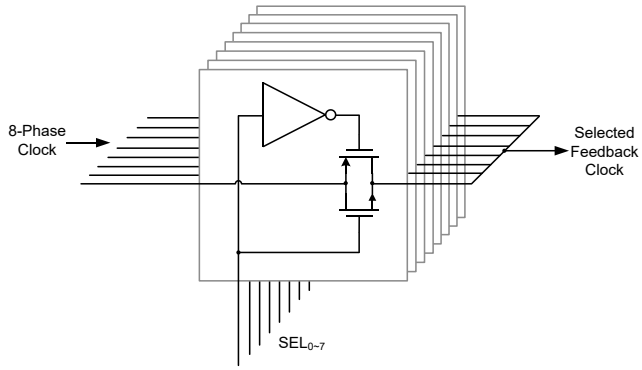
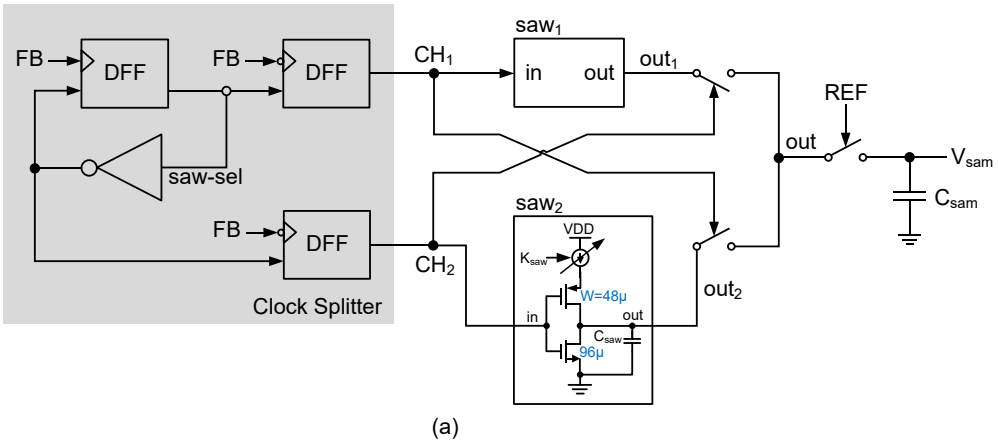
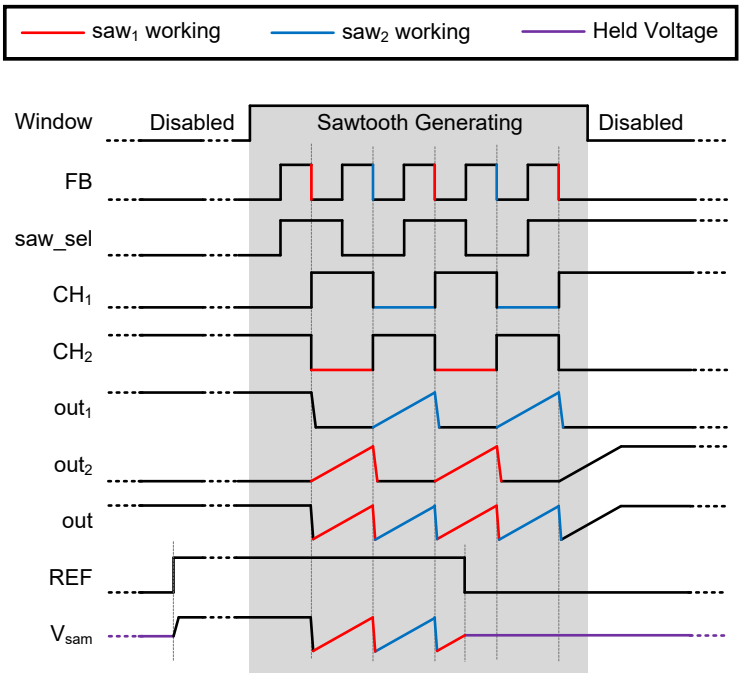


Figure 3-26 Schematic of the multiplexer.



(a)



(b)

Figure 3-27 (a) Schematic and (b) timing diagram of the waveform generator and sampler.

As discussed in Section 3.2.2, a sawtooth waveform is preferred for larger linear dithering range. Figure 3-27 describes the (a) schematic and (b) operation of the sawtooth generator and sampler. The *saw1* and *saw2* are two identical sawtooth generation cells. The input clock *FB* is the output of the multiplexer. The clock splitter divides the input clock and generates the charging/discharging signals (i.e., *CH1* and *CH2*) to control *saw1* and *saw2* alternatively in order to generate the sawtooth wave. In the identical *saw1* and *saw2*, large size is used for NMOS in order to discharge the capacitor quickly. The

charging current can be digitally adjusted during measurement in order to change the sawtooth slop. Outputs of saw_1 and saw_2 (i.e., out_1 and out_2) are alternatively connected to node *out*. Upon the arrival of the reference falling edge, the sampling capacitor, C_{sam}, holds the voltage of *out* as the final output of the sampler. Note that the sawtooth cycle being sampled is the only cycle matters. Other sawtooth cycles that are not sampled do not affect the sampling result but draw supply current. Thus, the sawtooth generators can be disabled by a *Window* signal well before and after each sampling in order to reduce power consumption.

Although the sawtooth waveform is at high frequency of 2.5 GHz, timing requirement for the multiplexer switching is not strict because this phase switching only needs to be stable before the next reference sampling edge (which is at 40 MHz). Moreover, as predicted by the phase model in Section 3.3, the phase noise introduced by the multiplexer and the sawtooth generator will not be amplified by *N*. This simplifies the design of the multiplexer.

Post-layout simulation shows that the phase noise introduced by the multiplexer and sampler is less than -115 dBc/Hz at 1 kHz offset and less than -120 dBc/Hz at 10 kHz offset. This imposes a negligible impact to the in-band phase noise performance.

3.4.3 SSCP

The SSCP in this prototype uses the same structure as in [60], as shown in Figure 3-28. The SSCP converts the voltage difference between V_B and V_{sam} into a current pulse output, where V_{sam} is the output voltage of the sampler and V_B is a bias voltage that can be adjusted externally for measurement purpose. A dummy capacitor is added as a current dumping node to minimize charge sharing between charge pump and loop filter. The simulated SSCP gain is about 0.5 mA/V with V_B = 0.6 V and V_{sam} ranging from 0.18 V to 1.02 V. A pulse generator is designed to provide the V_{pul+} and V_{pul-} pulse with tunable width.

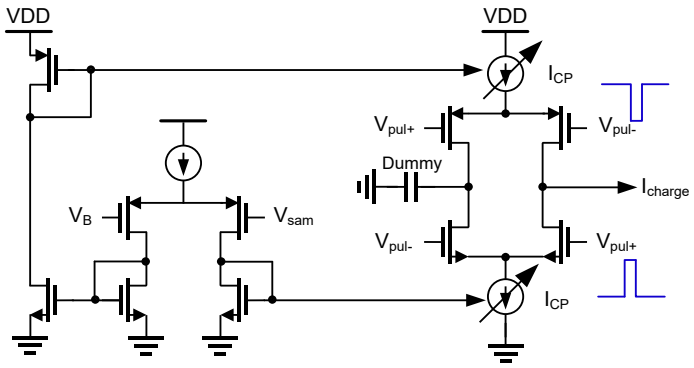


Figure 3-28 Schematic of the SSCP [60].

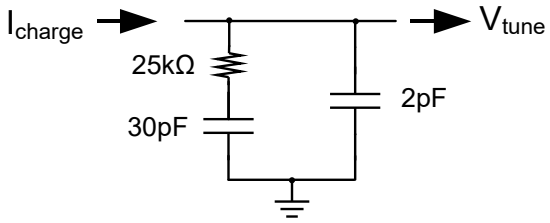


Figure 3-29 Schematic of the loop filter.

3.4.4 Loop Filter

A common 3-order filter is used as the loop filter. The structure and parameters are shown in Figure 3-29. It takes I_{charge} from SSCP as the input current, and generates a filtered control voltage (i.e., V_{tune}) to the VCO.

3.4.5 Simulation Result

With simulation results of all above blocks obtained, calculation can be performed through Matlab according to the closed-loop transfer functions in Table 3-2. The simulated output phase noise of the prototype is as in Figure 3-30, with center frequency of 2.9 GHz. Sawtooth slop and current pulse width can be tuned during simulation and measurement for an optimized bandwidth. Integrated jitter from 10 kHz to 30 MHz is 463 fs_{rms}. The target output frequency is 2.325 to 2.975 GHz. The loop bandwidth is calculated to be 0.4 MHz. Table 3-4 summarizes the parameters related to this loop bandwidth.

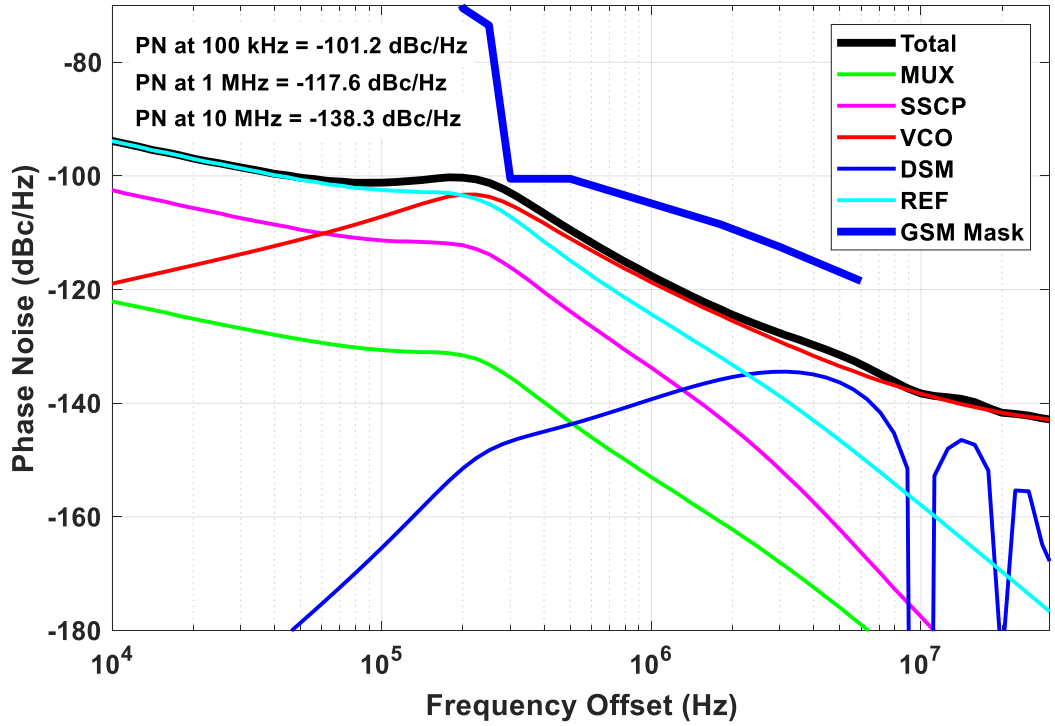


Figure 3-30 Simulation result of the SSPLL output phase noise.

Table 3-4 Summary of Parameters Related to Loop Bandwidth

Characteristics	Values
Sawtooth slope	3 GV/s
SSCP gain	500 μA/V
Current pulse width	60 ps
R_s	25 kΩ
C_p	2 pF
C_s	30 pF
K_{VCO}	50 MHz/V
Loop bandwidth	**0.4 MHz**

Figure 3-31 shows a transient simulation of the SSPLL locking (not including the AFC and FLL locking). In this simulation, $f_{REF} = 40$ MHz, $INT = 1$ and $N = 70$. Target frequency is initially 2.80994 GHz (by setting $\alpha = 0.9876$ according to (3-29)) and changed to 2.80562 GHz (by setting $\alpha = 0.1234$) at the simulation time of 50 μs. We assume the VCO control voltage is set to around 0.3 V by the FLL at the initial state. To achieve a frequency error less than 100 kHz, the simulated locking time is about 25 μs.

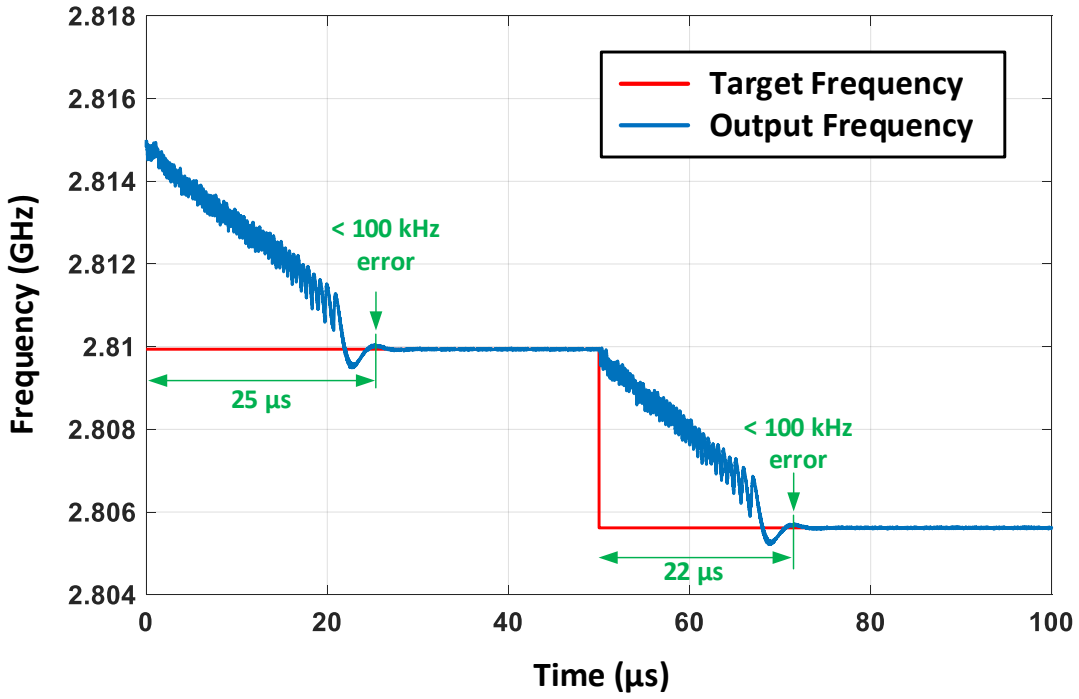


Figure 3-31 Simulation of the SSPLL locking.

3.5 Experimental Results

This PS-SSPLL prototype was fabricated in a 65 nm CMOS process. Figure 3-32 shows the die photo with active area of 700 μm × 300 μm. The VCO inductor is 300 μm × 300 μm. Two LDOs are used to provide the 1.2 V analog and digital supplies so that the measured noise performance is not degraded. Figure 3-33(a) illustrates the testbench for this work. Figure 3-33(b) shows the power consumption of each block from a 1.2 V power supply. Among the core power dissipation of 13.3 mW (excluding the output buffers), 9.8 mW is drawn by the VCO and the frequency dividers.

To characterize the prototype, it is wire-bonded to an IC package, which is soldered on a PCB for measurement. The PCB includes LDO as the power supply to the design in order to reduce supply noise. The input reference clock and the output clock from the PLL are connected to external equipment through SMA RF cables. The prototype takes a square wave reference clock input from function generator, and the PLL output is characterized by a Rohde & Schwarz FSUP signal source analyzer.

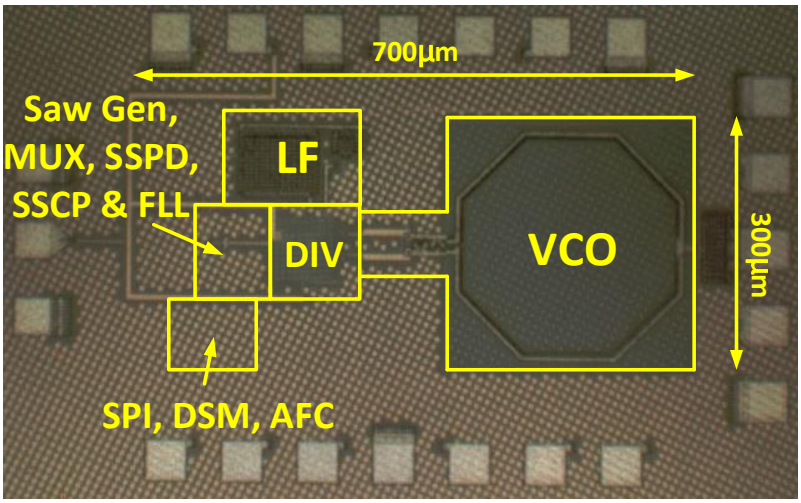


Figure 3-32 Die photograph of the fabricated PS-SSPLL prototype.

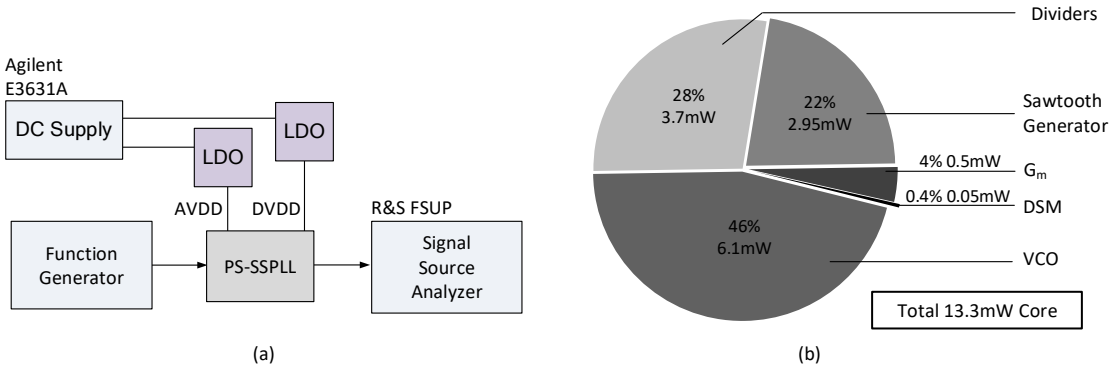


Figure 3-33 (a) Testbench of this work. (b) Power consumption of each block.

Unfortunately, the output frequency range of the fabricated prototype is about 2.6 to 3.4 GHz, which is higher than the simulated frequency range of 2.325 to 2.975 GHz. The reason for this variation is the metal dummies filled inside the inductor. Such metal dummies are filled automatically by the foundry to fulfill the design rules of the process. As a result, these dummies inside the inductor decrease the inductance and the Q factor, leading to higher VCO frequency and VCO phase noise. In the adopted fabrication process of this work, even though the dummy was added with a lower density, it still affects the design. In future designs, for better prediction, these dummies should be filled manually by designers and extracted and simulated using electro-magnetic simulation tools, even though the inductor is from the PDK.

Figure 3-34 shows the measured output spectrum of the SSPLL at a fractional output frequency of 3.051562 GHz ($\approx 76.289 \times f_{REF}$). Similar to other SSPLLs, the reference

spur is higher than the conventional divider PLLs. The measured reference spur is -31.9 dBc.

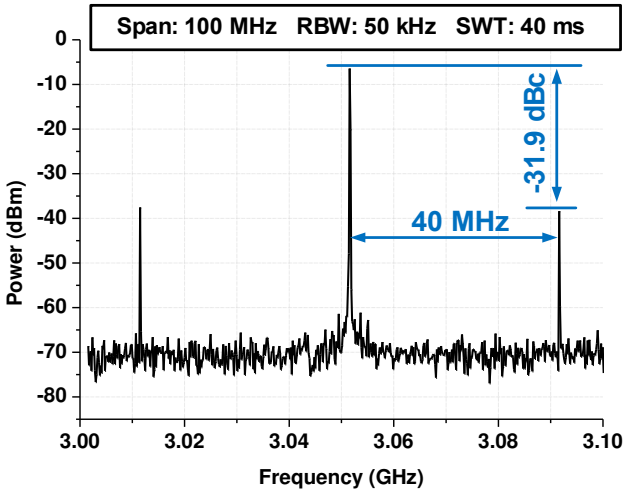


Figure 3-34 Measured reference spurs at fractional-*N* output.

To investigate the cause of the high reference spurs, we can take a look at the blocks that are triggered by the reference clock, including the sawtooth generator with embedded sampler, the phase multiplexer, and the DSM. For example, the sawtooth is enabled and disabled periodically, and draws varying at the reference frequency. Operations of these blocks may introduce disturbance to the power supply, which is coupled into the VCO and causes periodic disturbance to the VCO operation. Another possible cause is the coupling of the reference clock itself.

Disturbance to the sawtooth generator and the sampler take place in two mechanisms. Two experiments are performed in this research to investigate such mechanisms.

The first mechanism is the charge sharing at the sampler. This can be explained using Figure 3-35. Each time when the sampler changes from hold mode to track mode, the voltage at the sample capacitor (i.e., C_{sam}) and that at the sawtooth generator (i.e., C_{saw}) may be different. This causes charge sharing between the two capacitors and affects the sawtooth wave being generated, as shown in Figure 3-35(b). If the sawtooth amplitude is smaller, the voltage difference between two capacitors is probably smaller, and the impact to the sawtooth can be reduced. In the first experiment, different sawtooth slopes were

selected to compare the reference spur levels, with the results shown in Figure 3-36. A larger digital K_{saw} code indicates a larger slope. Comparison shows that the reference spur can be reduced with a smaller sawtooth slope by 2.5 dB.

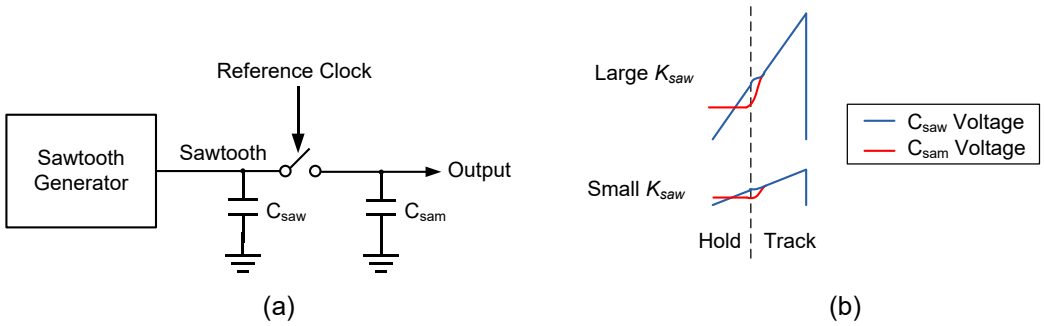


Figure 3-35 (a) Connection between the sawtooth generator and the sampling capacitor, and (b) a conceptual timing diagram of charge sharing under different sawtooth slopes.

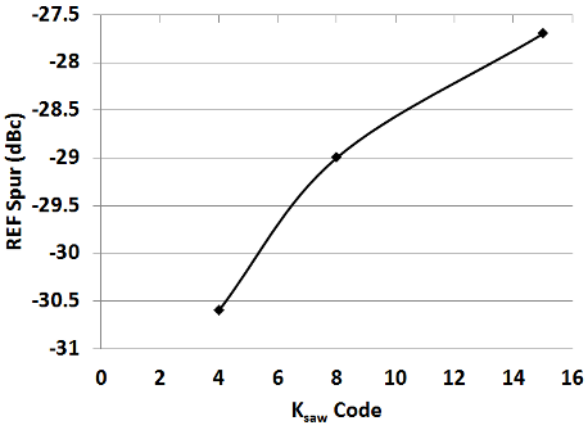


Figure 3-36 Measured reference spur levels under different sawtooth slope configurations.

The other mechanism is through load capacitance modulation of the sawtooth generator. When the sampler is in the track mode, extra load capacitance is added to the sawtooth generator, including the C_{sam} and the input capacitance of the subsequent SSCP. This also introduces a periodic disturbance. According to [61], the impact of such a disturbance is related to the duty cycle of the reference clock. In our second experiment, reference duty cycle was changed to compare the reference spurs, which is shown in Figure 3-37. Compared with the worst case at 50 % duty cycle, the reference spur at 88 % duty cycle is 2.8 dB lower. Hence, we can expect the load modulation to be a contributor for

reference spur. To achieve lower reference spurs, similar mitigation techniques as in [61] can be adopted in future PS-SSPLL.

The reference clock may also affect the VCO operation through coupling. This can be reduced if the VCO is protected by better isolation from other circuits or uses a higher VCO supply voltage to reduce its sensitivity to the disturbance.

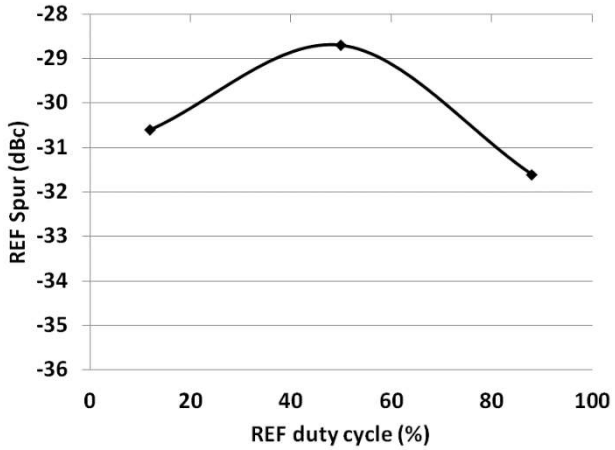


Figure 3-37 Measured reference spur levels under different reference clock duty cycles.

To verify the phase noise performance, Figure 3-38 shows a comparison between the measured output phase noise of the prototype under fractional-*N* mode (at 3.051562 GHz) and integer-*N* mode (at 3.04 GHz). During fractional-*N* operation, DSM noise slightly affects the out-of-band noise. For in-band noise, the maximum difference between integer-*N* and fractional-*N* is merely 2.1 dB. This shows that the PS-SSPLL is able to achieve low in-band phase noise as an integer SSPLL does. At the fractional-*N* output frequency, the rms jitter integrated from 10 kHz to 30 MHz is 531 fs. Since the VCO frequency is shifted from the designed value, the VCO may exhibits higher phase noise than calculated, leading to a measured noise higher than simulation result.

Figure 3-39 shows the phase noise performance comparison with prior arts before their calibration complete. If the time-consuming calibration is not permitted, this work achieved the best phase noise performance.

Figure 3-40 shows the highest fractional spur of -48.4 dBc at 313 kHz offset and the phase noise performance across the output range from 2.6 GHz to 3.4 GHz.

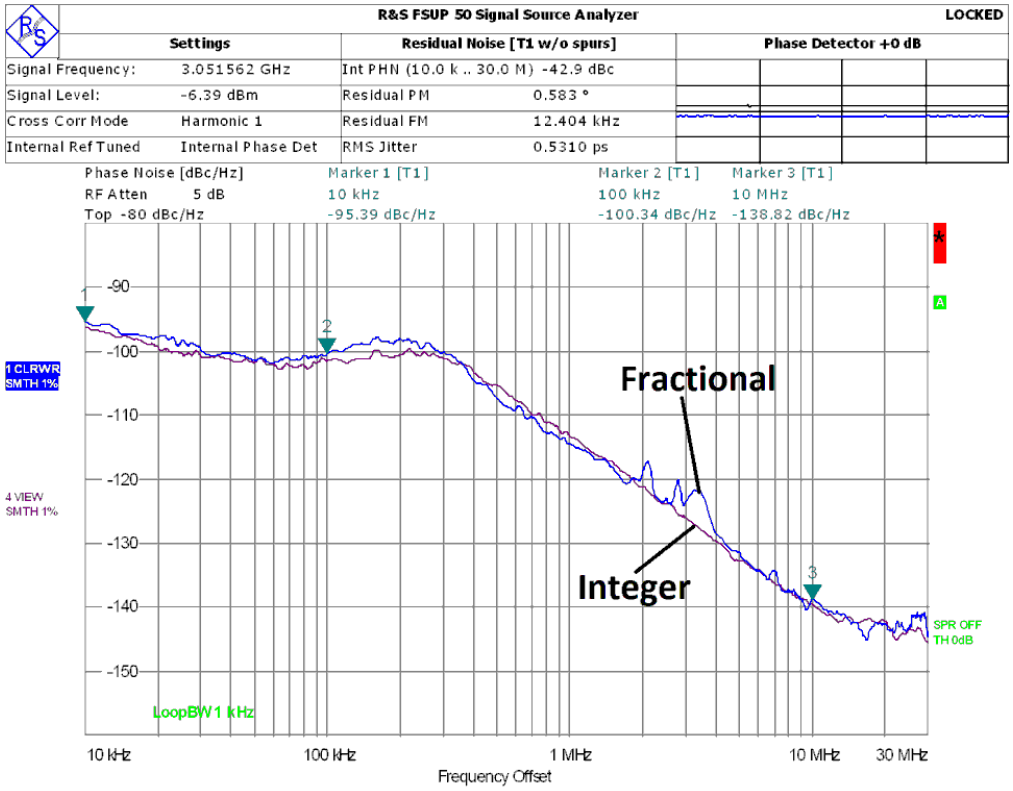


Figure 3-38 Measured phase noise of integer-*N* and fractional-*N* outputs.

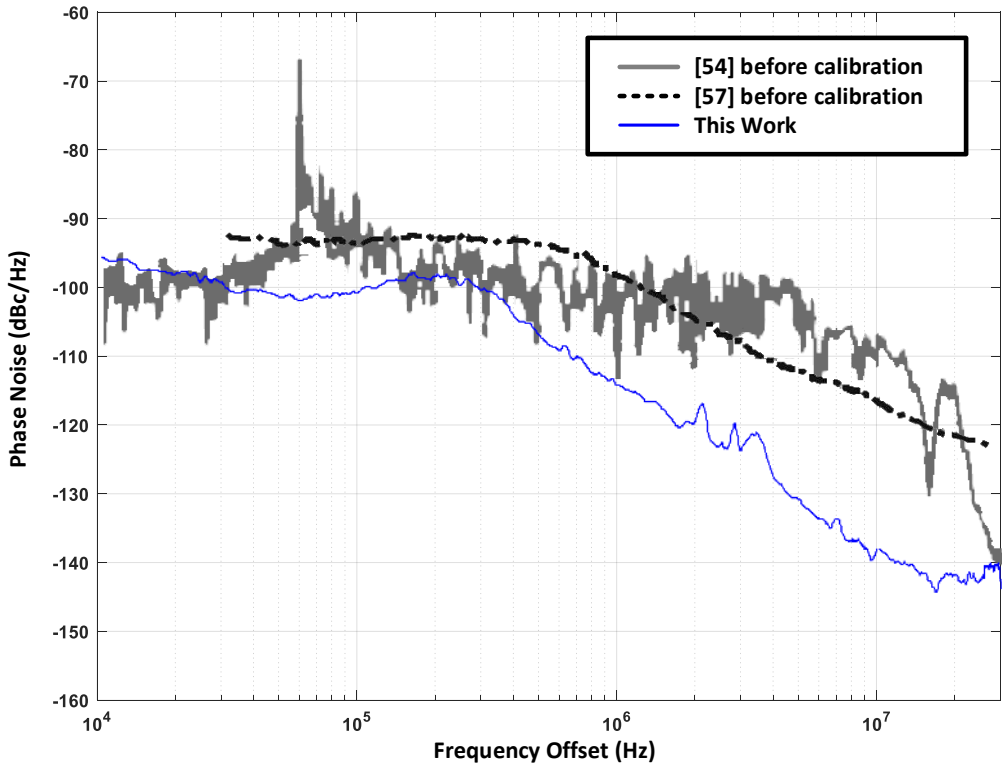


Figure 3-39 Phase noise comparison with prior arts.

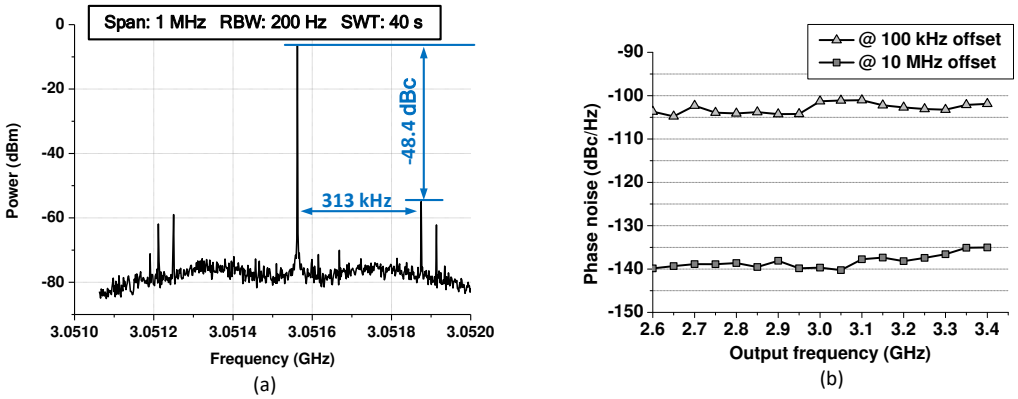


Figure 3-40 (a) Measured fractional spurs and (b) measured in-band and out-of-band noises across the PLL output range.

Table 3-5 Comparison with Other State-of-the-Art Fractional-*N* SSPLLs

Design	[54]	[57]	[58]	This work
Tech. (nm)	180	28	65	65
Architecture [1]	RS-SS	RS-SS	AC-SS	PS-SS
Freq. (GHz)	2.12-2.4	9.2-12.7	2.6-3.9	2.6-3.4
Available output scheme	Diff.	Diff.	Diff.	8-Φ (3 GHz) Quad. (6 GHz) Diff. (12 GHz)
REF (MHz)	48	40	49.15	40
Power (mW)	17.3	13	11.5	13.3
Calibration	Needed	Needed	Needed [3]	Free
Calibration time (μs)	~ 20000 (measured)	~60 (simulated)	Not mentioned	N.A.
In-band PN w/ calibration [2](dBc/Hz)	-109@50 kHz	-114@200 kHz	-110@100 kHz	N.A.
rms jitter w/ Cal (fs)	266	280	240	N.A.
FoM w/ Cal (dB) [5]	-239.1	-240	-241.8	N.A.
In-band PN w/o calibration [2](dBc/Hz)	-91 @50 kHz	-105 @200 kHz	Not mentioned	-100.3 @100 kHz
rms jitter w/o Cal (fs)	1892	~ 870 [4]	Not mentioned	531
FoM w/o Cal (dB) [5]	-222.1	~ -230.1	N.A.	-234.3
Active area (mm^2)	0.75	~ 0.66	0.23	0.21

[1] PS = phase-switching, RS = reference-shifting, AC = alias-cancelling

[2] All scaled to 3 GHz by $20\,log(f_c/3GHz)$

[3] An extra 8-b ADC operating at REF is needed

[4] Calculated from phase noise profiles

[5] $FoM = 20 \cdot \log(rms\ jitter/1s) + 10 \cdot \log(Power/1mW)$.

Table 3-5 compares this work with other state-of-the-art multi-GHz fractional-*N* SSPLLs. Note that [54], [57], and [58] do achieve better jitter performance and lower in-band phase noise after the time-consuming calibrations. For a fair comparison, noise performance with and without calibration is also listed. Under conditions without calibration, this work achieves the best jitter performance and FoM.

3.6 Summary

In this chapter, several analog PLL structures have been reviewed. Fractional-*N* SSPLL structure is chosen to be optimized owing to its capability of reducing error detector noise amplification and in-band phase noise. Two prior fractional-*N* SSPLL techniques, namely RS-SS and AC-SS techniques, have been reviewed. These prior art works suffer from the time-consuming calibration that limits their application in short-settling-time communications. This chapter has reported our studies in overcoming the time-consuming calibration.

Achievements in this chapter are listed below.

- A novel PS-SS technique has been proposed to eliminate the need for a calibration.
- A phase model has been proposed to analyze and optimize the noise performance of a PS-SSPLL.
- A PS-SSPLL prototype has been designed and implemented based on the proposed PS-SS technique.
- The prototype has been measured to verify the proposed PS-SS technique. Under a calibration-less testing condition, the prototype achieves jitter performance of 531 fs_{rms} and FoM of -234.4 dB, both are the best among the fractional-*N* SSPLL family.

Finally, the proposed PS-SSPLL has been proved to be an attractive architecture for the wireless transceivers due to the calibration-less characteristic. More generally, the idea of generating phases from VCO rather than from controllable delay cell is helpful in

terms of phase error and calibration, because the generated phase difference is directly related to the VCO period.

However, there is still some headroom in this prototype that can be further improved.

- In-band phase noise can be further improved by optimizing the reference input path. In this prototype, the input reference buffer is not optimized. The input port is a DC coupled port, so a noisy function generator has to be used for measurement. Insufficient buffering of the reference input also degrades the in-band phase noise. In future work, the input port can use an AC-coupled scheme so that the reference clock can be applied from a low-noise RF signal generator. Low-noise buffer circuit can also be used. By doing so, the in-band phase noise can be further reduced.
- VCO can be designed to operate at correct frequency band by more careful verification and simulation. The measured VCO frequency of the prototype is not at the designed value due to fabrication. This makes the output phase noise slightly higher than the simulation results. In future designs, especially in designs with inductors, electro-magnetic simulations have to be performed carefully together with the post-layout simulations in order to predict the VCO performance more precisely. In fact, post-layout simulation cannot extract inductance accurately.
- Power consumption can be further improved. In this prototype, the multi-phase VCO is realized by a high-frequency VCO and two frequency dividers. A power consumption of 9.8 mW is drawn by the VCO and two dividers. This brings significant power consumption overhead and may not be attractive for low-power applications. To reduce power dissipation, other VCO structures that provide multi-phase output can also be used, such as ring oscillators. The power consumption can be further reduced by reducing the operation time of the sawtooth generator. This time width is not optimized in this prototype.

4 IRO-TDC for Low In-Band Phase Noise Digital PLLs

In Chapter 2, we have briefly introduced the concept and benefit of digital PLL. The TDC, acting as the error detector in a digital PLL, contributes significant noise to the in-band spectrum of the digital PLL output. To reduce the digital PLL in-band phase noise, the key consideration is to reduce TDC noise. In this chapter, a review of the noise contribution of TDCs to digital PLLs and the state-of-the-art low-noise TDCs is provided, and a novel IRO technique is proposed and demonstrated to further reduce TDC in-band noise.

4.1 TDC Specifications in Digital PLL Designs

When applying a TDC for digital PLLs, designers have to be aware of the required TDC noise performance. As discussed in Chapter 2, there are mainly two types of digital PLLs. For the proposed IRO-TDC, the *Start* and *Stop* signals have the same frequency, so it is more suitable for the PLL structure with frequency dividers. In this calculation, we consider only this digital PLL structure.

Inside a digital PLL, the only two physical noises are TDC noise and DCO noise. Figure 4-1 shows the phase model of a digital PLL with frequency divider. Analysis of DSM noise is the same as in a fractional-*N* divider PLL and is not included in this model. The phase error is transformed into time error by factor $T_{REF}/2\pi$. Added with an input-referred TDC noise (i.e., $T_{n,in}$), this time error is converted into digital word with a noiseless TDC gain (i.e., g_{TDC}) and processed by the digital loop filter. The loop filter has a transfer function of $H_{LF}(e^{sT})$. Table 4-1 lists the closed-loop transfer function of the TDC and DCO noises.

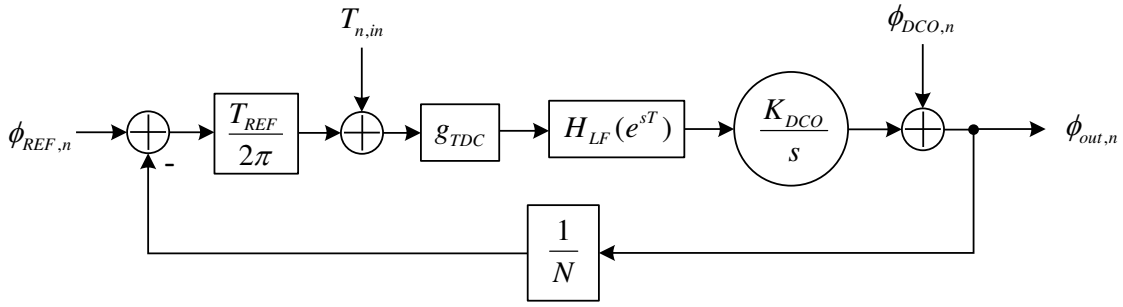


Figure 4-1 Noise model of a digital PLL with frequency divider.

Table 4-1 Closed-Loop Transfer Functions from TDC and DCO Noises to Digital PLL Output

Noise Source	Transfer Function*	Transfer Function Type
TDC	$\frac{\Phi_{out,n}}{T_{n,in}}(s) = \frac{2\pi N}{T_{REF}} \cdot \frac{G(s)}{1+G(s)}$	Low Pass
DCO Phase	$\frac{\Phi_{out,n}}{\Phi_{DCO,n}}(s) = \frac{1}{1+G(s)}$	High Pass

* Open-loop transfer function $G(s) = (T_{REF}/2\pi) \cdot g_{TDC} \cdot H_{LF}(e^{sT}) \cdot (K_{DCO}/s)(1/N)$, where T is the operation frequency of the digital loop filter, and T_{REF} is the reference clock period.

Within PLL bandwidth, the TDC noise transfer function can be approximated as

$$\frac{\Phi_{out,n,in-band}}{T_{n,in}}(s) \approx \frac{2\pi N}{T_{REF}} = 2\pi f_{DCO}. \tag{4-1}$$

Accordingly, if the double-sided PSD of the TDC noise is given as $S_{n,in}(s)$, its contribution to the PLL in-band phase noise is

$$\mathcal{L}_{TDC,in-band}(s) \approx 2(2\pi f_{DCO})^2 \cdot S_{n,in}(s), \tag{4-2}$$

which is the dominant of the PLL in-band phase noise. In other words, if a certain specification of PLL in-band phase noise is given as $\mathcal{L}_{in-band}(s)$, the required double-sided PSD of the TDC input-referred noise can be specified as

$$S_{n,in}(s) \leq \frac{\mathcal{L}_{in-band}(s)}{2}\left(\frac{1}{2\pi f_{DCO}}\right)^2. \tag{4-3}$$

In our design, the targeted in-band phase noise specification for a 3 GHz digital PLL is -105 dBc/Hz at 500 kHz offset, i.e., $\mathcal{L}_{in-band}(0.5\text{ MHz}) = 10^{-10.5}$ rad^2/Hz. Accordingly, the required TDC noise should be $S_{n,in}(0.5\text{ MHz}) \leq -73.5$ dB ps^2/Hz. In digital PLL designs, (4-3) can be used to optimize the TDC design to meet specifications.

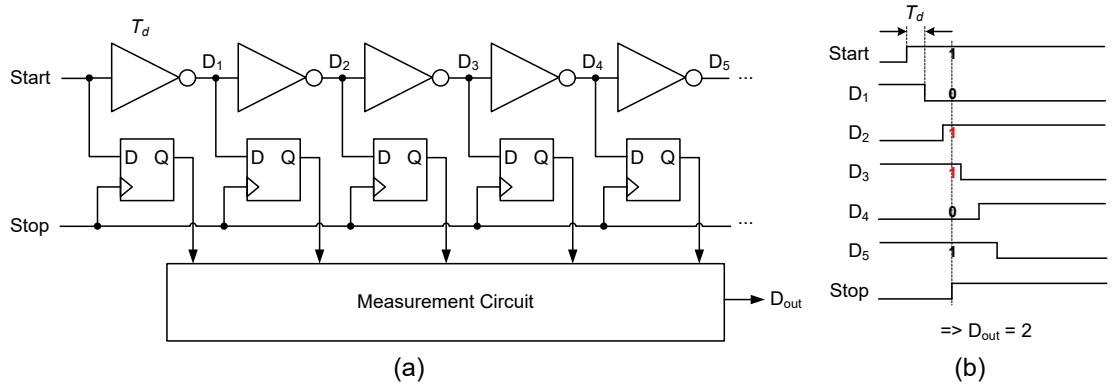


Figure 4-2 (a) Schematic and (b) timing diagram of a Flash TDC.

4.2 Literature Review of TDCs

A TDC comes in various architectures [63]-[87]. As a mimic of the simple Flash ADCs, a Flash TDC has the simplest structure [87]. In an ADC, the parameter to be converted is the input voltage. Accordingly, a set of voltage references are generated by a resistor ladder for comparison. Similarly, a circuit providing a set of time information can be used for a Flash TDC. In common implementation, a chain of inverters are used to generate such time information, as shown in Figure 4-2(a). A *Start* signal edge triggers a toggle at the output of the first stage (i.e., D_1). This toggle ripples along the inverter chain with certain stage delay, T_d. Upon the *Stop* edge, outputs of all stages are read out by the DFFs and compared by the measurement circuit. Location of the toggle is identified (where two consecutive stages have the same state, e.g., D_2 and D_3 in Figure 4-2(b)). Thus, time difference between *Start* and *Stop* events can be converted into digital code. The smaller stage delay the inverter chain can achieve, the finer time resolution can be provided. Even though a Flash TDC is easy to design and implement, its main drawback is the large stage delay. The minimum inverter delay is usually determined and limited by fabrication process (e.g., about 10 ps in a 65 nm CMOS process). In process with large feature size, this time step is usually too large for digital PLL. With feature size scaling, the Flash TDC resolution can be improved. However, it is still large and limits the in-band phase noise of a digital PLL.

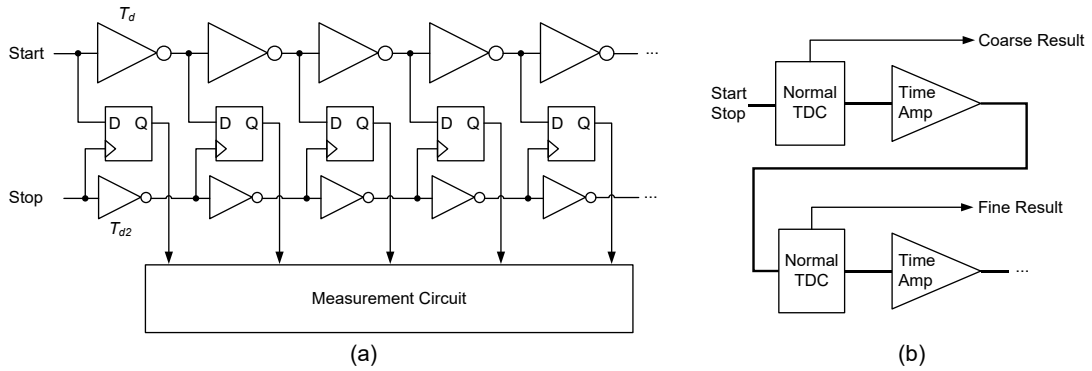


Figure 4-3 (a) Vernier TDC and (b) pipeline TDC for improved resolution.

To achieve a time resolution less than inverter delay, TDCs with sub-gate-delay resolution were proposed, such as Vernier [63] and pipeline TDCs [64]-[65]. Figure 4-3 shows the concepts of these two TDC types. A Vernier TDC propagates the *Stop* signal together with the *Start* signal, but with a shorter stage delay, T_{d2}, so that it can catch up with the *Start* ripple. The measurement circuit calculates at which stage the *Stop* ripple captures the *Start* ripple. The equivalent resolution is thus (T_d - T_{d2}). A pipeline TDC utilizes a time amplifier to amplifier the time different so that the resolution is also improved. Limitations of these TDCs include the stage mismatch and moderate resolution.

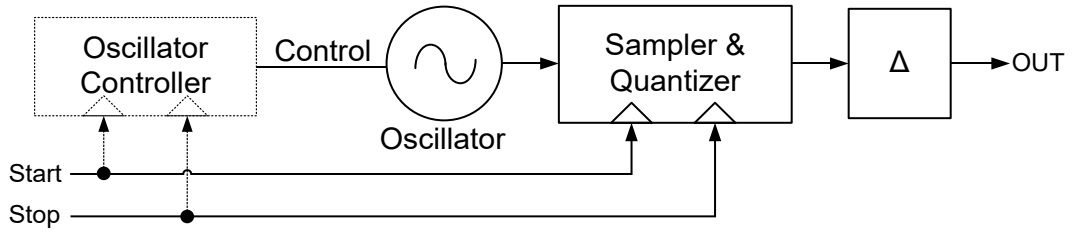


Figure 4-4 A general structure of an oscillator-based TDC.

To further improve the resolution and mismatch, oscillator-based TDCs were proposed [66]-[82]. Figure 4-4 shows a general structure of the oscillator-based TDCs. The common feature is that an oscillator providing phase information is sampled and decoded into digital output when a *Start* or *Stop* signal arrives. Since the oscillator phase is proportional to the oscillation time if the frequency is fixed, the captured phases at *Stop* and *Start* edges can be subtracted to produce the digital coding representing the time difference

between them. Whether an oscillator controller is needed or not depends on the type of the oscillator adopted.

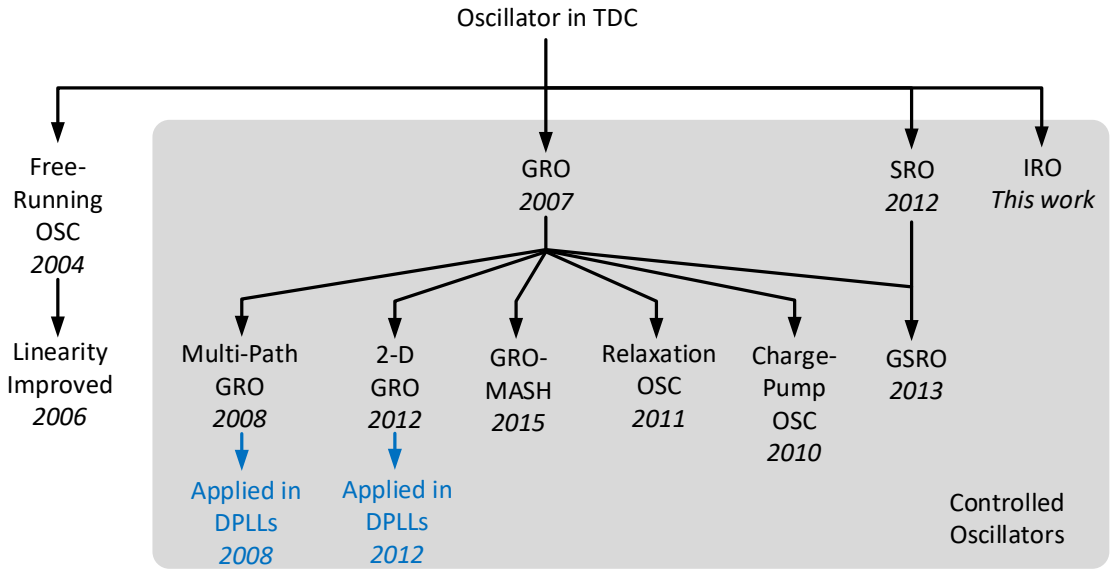


Figure 4-5 Development of the oscillator-based TDC family.

Figure 4-5 depicts the history of this TDC family. Interestingly, the development of this family is essentially the development of the adopted oscillator. In year 2004, a TDC based on a free-running oscillator (without being controlled) was proposed. It is able to scramble and reduce the impact of mismatch and quantization error [66]. There was a follow-up research about linearity calibration in 2006 [67].

Later in 2007, Helal proposed a concept of GRO with the attractive ability of performing first-order noise shaping to the mismatch and quantization error [68]. The concept of noise-shaping has been discussed in Section 3.1. Similar to the quantization error in a DSM, a noise-shaping TDC is able to attenuate the low-frequency error in order to reduce the in-band noise. When adopted in a digital PLL, the quantization error at high frequency spectrum can be reduced by the loop filter, thus introducing negligible impact to the PLL out-of-band phase noise. Since the report of the first GRO-TDC, concept of noise-shaping TDC has inspired many intelligent researchers, and various TDCs with low in-band noise have been reported. The GRO was further improved by Straayer in 2008 by using a multi-path structure [69]-[71]. This multi-path GRO-TDC was adopted in a digital

PLL prototype by Hsu [72]-[73]. Other literatures also reported application of similar GRO-TDCs in digital PLLs for improved in-band noise, such as [74]. TDCs based on GROs evolved towards higher-order noise shaping, including a 2-dimentional Vernier TDC who replaced its conventional inverters with GROs [75]-[76] (also applied in a digital PLL [77]), and a GRO-MASH TDC in 2015 [78]. Besides ring oscillator structure, the concept of gated oscillator was realized in other implementations, such as a relaxation oscillator [79]-[80] and a charge-pump oscillator [81]-[82]. In summary, during operation, oscillators in these TDCs either stop or oscillate with a fixed frequency. When the oscillator starts to oscillate or stops oscillating, a "phase skew error" is introduced due to non-idealities. The concept of skew error will be introduced later in our proposed model.

In 2012, another mode of the oscillator was proposed by Elshazly [83]-[85]. This oscillator operated at either a high frequency or a low frequency, thus was named SRO. With a constant sampling frequency, an SRO also achieves noise shaping. Since an SRO does not need to abruptly stop its oscillation, a smaller skew error is expected theoretically. Thus, the oscillator can be designed with a simpler structure to reduce power consumption. In 2014, a TDC combining both GRO and SRO as a GSRO achieved higher-order noise shaping [86]. Except the free-running oscillator, all other oscillators are called *controlled oscillators* in our discussion.

TDCs based on free-running oscillator reduce the quantization error and delay mismatch by scrambling. By contrast, both GRO and SRO further reduce such impacts through a high-pass noise-shaping transfer function. Quantization error and delay mismatch have negligible contribution to the in-band noise of GRO-TDC and SRO-TDC. However, the phase noise of the controlled oscillator, even after noise shaped, dominates the TDC in-band noise spectrum. Moreover, other noises can easily couple into the oscillator and transform into oscillator phase noise. For example, noise from power supply and substrate can couple into the oscillator, introducing oscillator phase noise and degrading the in-band noise performance. Unfortunately, there was previously no technique to reduce such oscillator phase noise. Therefore, a TDC power supply with clean

in-band noise is usually required. Besides, a GRO or SRO draws different supply current at their two operation modes. During each measurement cycle, these oscillators disturb the power supply periodically, and generate interference to other circuits through the power supply.

In this thesis, we propose an IRO as the third type of controlled oscillator to mitigate the above drawbacks.

4.3 Proposed IRO for TDCs

From development of the oscillator-based TDCs, we can find that except for the normal mode, the controlled oscillators can operate at a stop mode (i.e., GRO), or a slow mode (i.e., SRO). From the symmetry point of view, the oscillator may be changed to operate in an inverted mode, i.e., the oscillation is reversed while the frequency amplitude does not change. This inspiration brings us to the idea of an IRO. A conceptual comparison between GRO, SRO, and IRO is provided in Figure 4-6 and Table 4-2. In the following discussions in this thesis, the normal mode is called *mode 1*, while the other mode is called *mode 2*.

There are two advantages we can anticipate in an IRO before our quantitative analysis:

- Possible higher TDC gain. The frequency is essentially modulated by the input time. If the frequency can be modulated between two values with larger difference, the effect (or gain) of this modulation should be higher.
- Constant supply current. If the oscillator simply inverts the oscillation direction while its frequency amplitude is constant, the power dissipation should also be constant. Thus, the power supply and other circuits should not be affected by the TDC operation.

For the later analysis in this thesis, the GRO, SRO, and IRO-TDCs are categorized as controlled oscillator-based TDCs. Next, a quantitative analysis and comparison of this TDC family is provided.

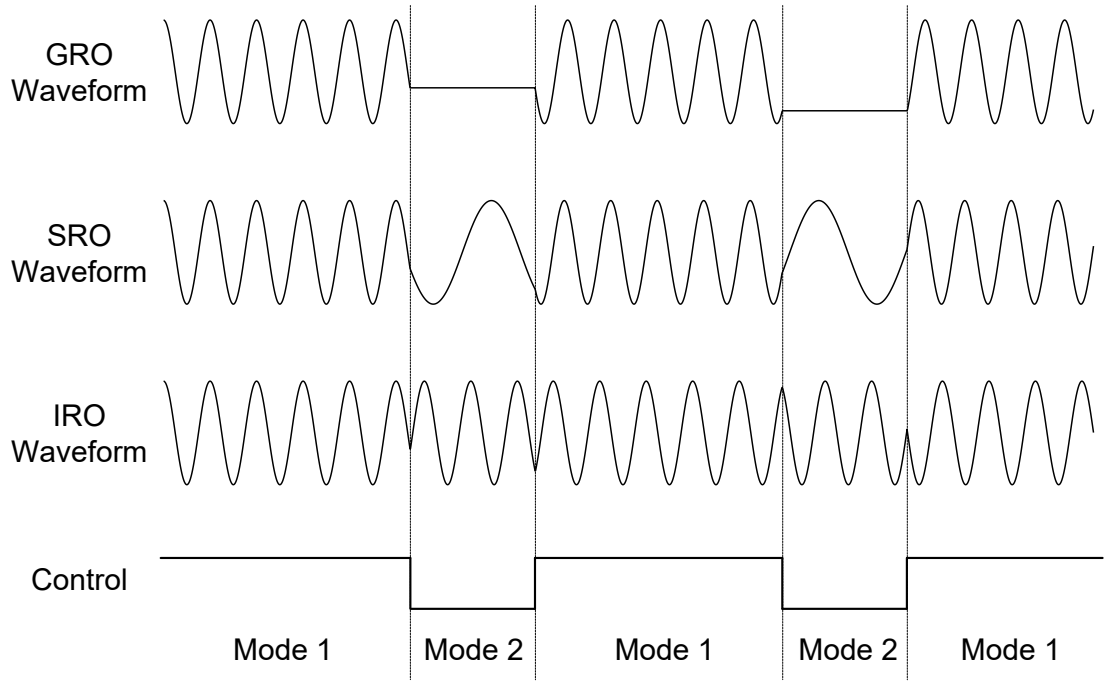


Figure 4-6 Timing diagram of GRO, SRO, and IRO voltage.

Table 4-2 A Conceptual Comparison among GRO, SRO, and IRO

Oscillator Type	Mode 1 frequency	Mode 2 frequency	Frequency Difference
GRO	$+\omega_0$	0	ω_0
SRO	$+\omega_0$	$+x\omega_0$ *	$(1-x)\omega_0$ *
IRO	$+\omega_0$	$-\omega_0$	$2\omega_0$

* $0 < x < 1,\ 0 < (1-x) < 1$.

4.4 Proposed Noise Model for Controlled Oscillator-based TDCs

To explain the noise characteristics of the proposed IRO-TDC, and compare it with GRO- and SRO-TDCs, a general noise model is proposed in this section. This general noise model applies to all the three types of TDCs. For simplicity, in our discussions, these TDCs are called XRO-TDCs, where XRO can refer to GRO, SRO, or IRO. Although their names may suggest ring oscillators, the concept of multi-mode oscillator and the model discussed below can be applied to oscillators in any implementation.

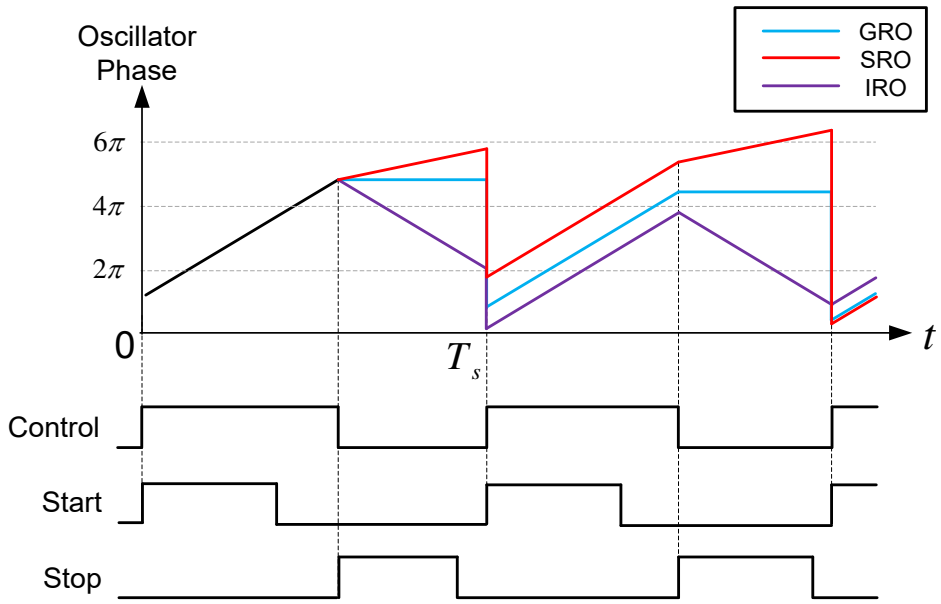


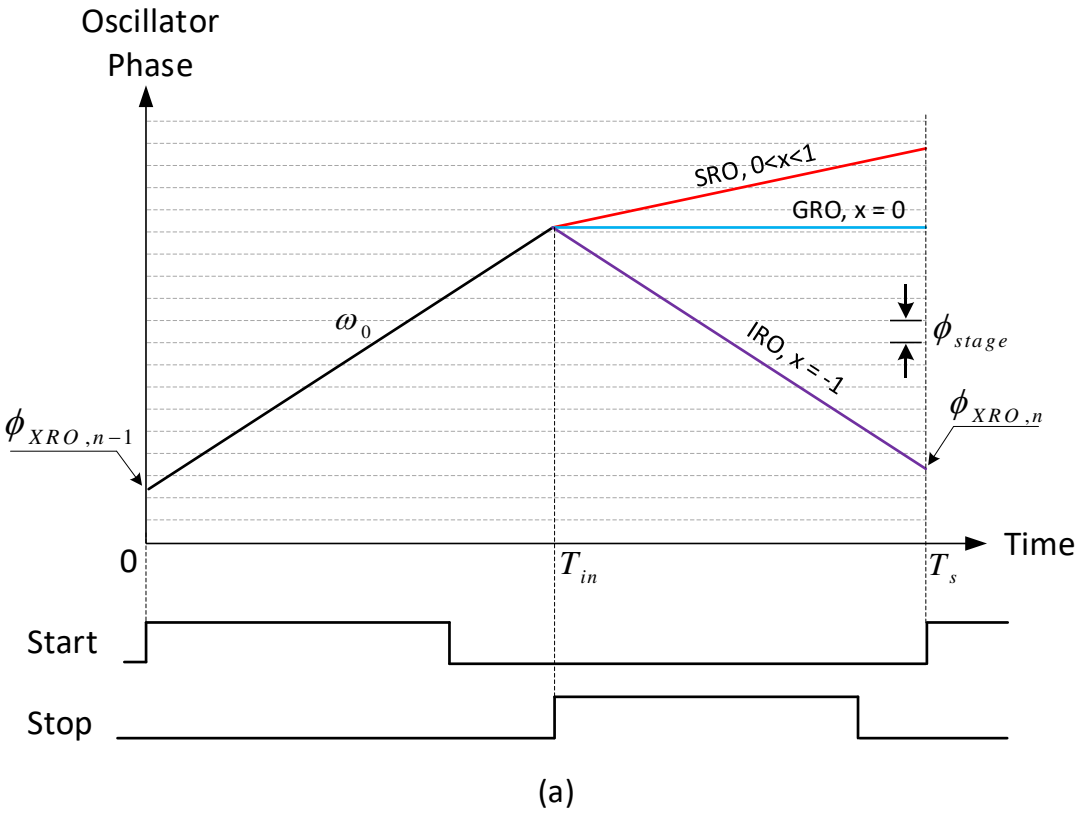
Figure 4-7 Phase-time plot of GRO, SRO and IRO.

Operation of an XRO-TDC can be described as follows. An oscillator is being controlled based on the *Start* and *Stop* signals. By doing this, the time information of *Start* and *Stop* can be converted into phase information of the oscillator. A sampler captures the oscillator phase, which is then quantized into digital signals. Since the oscillator phase is modulated by the input time, the digital signals can be differentiated to obtain the information of input time.

Figure 4-7 illustrates how the phase changes during operation. The oscillator has two modes of operation, depending on the XRO type. The controller decides which mode is being used. For easier comparison, all XROs are assumed to have the same frequency at mode 1. Upon a *Start* signal edge, the oscillator starts to oscillate in mode 1 from the previous phase. When a *Stop* signal is received, the oscillator changes to mode 2. Behaviors of mode 2 depends on the oscillator types:

- GRO: The oscillator is disabled, thus the oscillation pauses until the next *Start* edge arrives.
- SRO: The oscillator switches to a slower frequency rather than freezes its phase.
- IRO: The oscillation direction is reversed. Absolute frequency is not changed.

For all XRO types, at the next arrival of *Start*, the oscillator changes back to mode 1 and the next measurement cycle begins. The phases shown in the figure wrap back to



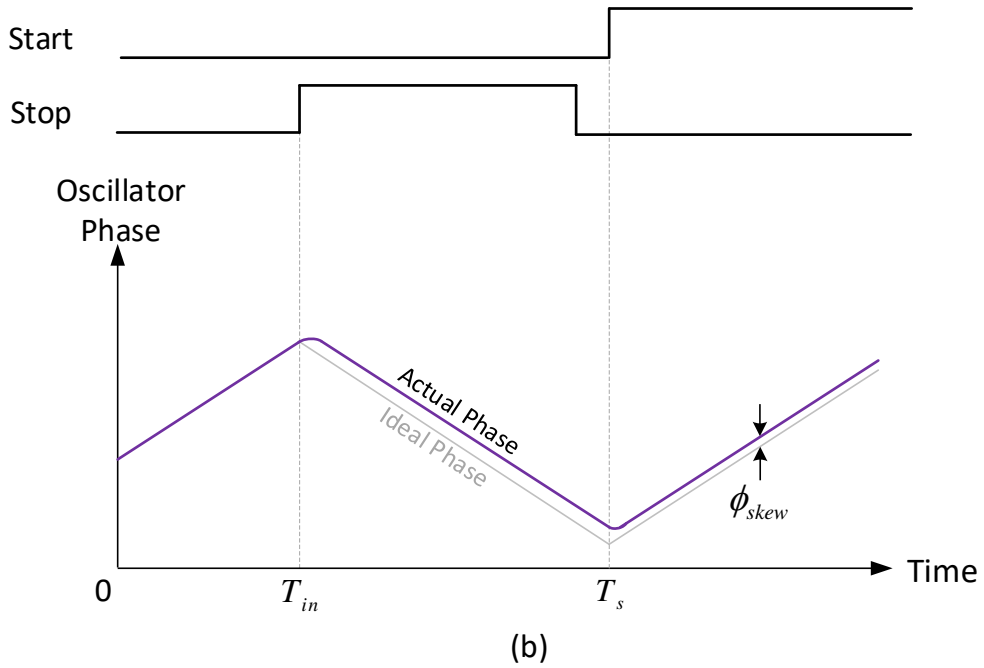


Figure 4-8 Phase-time plot showing (a) GRO, SRO and IRO phase increments during one measurement cycle and (b) IRO phase skew.

$0\sim2\pi$ due to the periodicity of the oscillator phase. Counters are adopted in the sampler for this wrap counting.

Figure 4-8(a) provides the phase increment details during a single measurement cycle. Upon a *Start* signal edge, the oscillation begins with a frequency ω_0 at the last phase of $\phi_{XRO,n-1}$. When a *Stop* signal arrives, the frequency is switched to $x\omega_0$, where the value of x depends on the XRO type:

- GRO: $x = 0$.
- SRO: $0 < x < 1$.
- IRO: $x = -1$.

At the next *Start* event, the final phase $\phi_{XRO,n}$ is captured. Since it is physically not possible to switch the XRO ideally from one mode to the other instantaneously, a random skew error ϕ_{skew} will be introduced at each switching transient, as shown in Figure 4-8(b). The value of ϕ_{skew} depends on the mechanism of the XRO and the current XRO phase. Note that although the XRO experiences two mode switches in one measurement cycle, they are combined as one ϕ_{skew} for easier explanation. Therefore, during this cycle, the total phase increment during this cycle, $\Delta\phi_{XRO}$, is

$$\begin{aligned}\Delta\phi_{XRO} &= \phi_{XRO,n} - \phi_{XRO,n-1} \\ &= \omega_0 T_{in} + \phi_{skew} + x\omega_0(T_s - T_{in}) \\ &= (1-x)\omega_0 T_{in} + x\omega_0 T_s + \phi_{skew}, \end{aligned} \tag{4-4}$$

where T_s is the sampling period, and T_{in} is the input time difference between *Start* and *Stop*.

Based on the phase increment expressed in (4-4), Figure 4-9(a) depicts the noise model of XRO-TDCs. The TDC takes T_{in} as the input, transforms it into phase increment, and performs an integration and digitization. The final digital output is obtained by the digital differentiator. During this process, the XRO-TDC converts the input signal T_{in} from time domain into phase domain, which will then be quantized and differentiated in digital domain. In the later discussions, most noise sources are analyzed in phase domain.

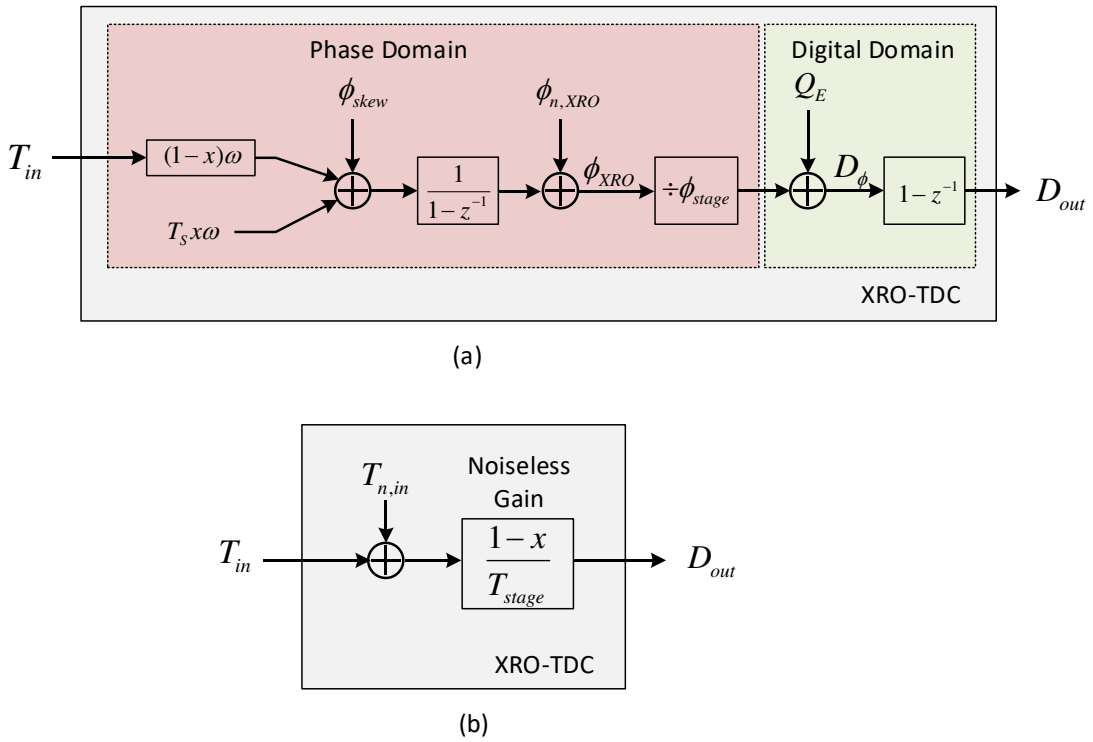


Figure 4-9 (a) Proposed noise model for XRO-TDCs, and (b) its equivalent model showing the input-referred noise.

In an XRO-TDC, two physical noise sources are skew error and oscillator phase noise, denoted as ϕ_{skew} and $\phi_{n,XRO}$, respectively. Assume there is no mismatch among the delay of each stage. The XRO phase is digitized into digital code D_ϕ with minimum distinguishable step size of ϕ_{stage} and quantization error $Q_E \cdot \phi_{stage}$. Final TDC output D_{out} is obtained by differentiating D_ϕ. According to the model in Figure 4-9(a), final TDC output is

$$D_{out} = \frac{T_{in}(1-x)\omega_0}{\phi_{stage}} + \frac{T_s x\omega_0}{\phi_{stage}} + \frac{\phi_{skew}}{\phi_{stage}} + \frac{\phi_{n,XRO}(1-z^{-1})}{\phi_{stage}} + Q_E(1-z^{-1}). \quad (4\text{-}5)$$

For the quantizer, the distinguishable phase step ϕ_{stage} is related to the stage delay T_{stage} by

$$\phi_{stage} = \omega_0 T_{stage}. \quad (4\text{-}6)$$

Substituting (4-6) into (4-5), the final TDC output can be expressed as

$$D_{out} = \left(\frac{1-x}{T_{stage}}\right) \cdot T_{in} + \left(\frac{x}{T_{stage}}\right) \cdot T_s + \left(\frac{\phi_{skew}}{\omega_0 T_{stage}}\right)$$

$$+\left(\frac{\phi_{n,XRO}(1-z^{-1})}{\omega_0 T_{stage}}\right)+Q_E(1-z^{-1}). \tag{4-7}$$

At the first term, factor $(1-x)/T_{stage}$ is the gain from T_{in} to D_{out}, thus the TDC gain.

In order to analyze various internal noises, Figure 4-9(b) shows an equivalent signal flow of the XRO-TDC. This signal flow is similar to the analysis of a voltage amplifier. The input signal T_{in} is added with an input-referred noise $T_{n,in}$ and converted with a noise-less gain of $(1-x)/T_{stage}$ into output code. All the impact of the internal noises can be represented by the input-referred noise. Thus, by analyzing $T_{n,in}$, the noise performance of an XRO-TDC can be evaluated. Using the signal flow in Figure 4-9(b), the TDC output is

$$D_{out}=\left(T_{in}+T_{n,in}\right)\cdot\frac{1-x}{T_{stage}}. \tag{4-8}$$

By equaling (4-7) and (4-8), the input-referred noise can be expressed as

$$T_{n,in}=\left(\frac{x}{1-x}\right)\cdot T_s+\frac{\phi_{skew}}{\omega_0(1-x)}+\frac{\phi_{n,XRO}(1-z^{-1})}{\omega_0(1-x)}+\frac{Q_E T_{stage}(1-z^{-1})}{1-x}. \tag{4-9}$$

Note that the first term is constant and can be regarded as a constant offset. Representations of other terms are listed as below:

- $\frac{\phi_{skew}}{\omega_0(1-x)}$ - Noise from the skew error
- $\frac{\phi_{n,XRO}(1-z^{-1})}{\omega_0(1-x)}$ - Shaped noise from oscillator
- $\frac{Q_E T_{stage}(1-z^{-1})}{1-x}$ - Shaped noise from quantizer

Factor $(1-z^{-1})$ in the last two terms implies the noise-shaping effect to oscillator phase noise and quantization error.

In order to analyze different noises, the following symbols are defined:

$S_{n,skew}$ - Noise PSD contributed from the skew error

$S_{n,XRO}$ - Noise PSD contributed from the oscillator

$S_{n,QE}$ - Noise PSD contributed from quantization error

According to (4-9), the total TDC input-referred noise PSD is

$$S_{n,in} = S_{n,skew} + S_{n,XRO} + S_{n,QE}. \tag{4-10}$$

Impact of each noise sources is discussed next.

4.4.1 Quantization Error

Based on (4-9), noise contribution from quantization error is governed by

$$S_{n,QE} = S_{Q_E} \cdot \left(\frac{T_{stage}(1 - z^{-1})}{1 - x} \right)^2, \tag{4-11}$$

where S_{Q_E} denotes the noise power density of normalized quantization error, Q_E. In this part, no mismatch is assumed among delay of each stage. The impact of such delay mismatch will be discussed in the next part.

The quantization error stems from the finite delay per stage. Figure 4-10 shows a phase quantization transfer characteristic. After captured by the sampler, the oscillator phase ϕ_{XRO} will be quantized into digital code D_ϕ. The raw quantization error $Q_{\phi,raw}$ ranges from $-\phi_{stage}$ to 0. In common calculations, a constant offset of $\phi_{stage}/2$ can be added, so the quantization error $Q_\phi = Q_{\phi,raw} + \phi_{stage}/2$ ranges from $-\phi_{stage}/2$ to $\phi_{stage}/2$.

For simplicity, a normalized quantization error is defined as $Q_E = Q_\phi/\phi_{stage}$, and it ranges from -1/2 to 1/2. Due to randomness of the input time, we can assume that the oscillator phase is stochastic. The value of Q_E is thus equally distributed within range from -1/2 to1/2, as shown in Figure 4-11(a).

As the integrated probability is 1, the probability density $P = 1$. The expected power is then

$$\sigma_{Q_E}{}^2 = \int_{-1/2}^{1/2} Q_E{}^2 \cdot P \, dQ_E = \frac{1}{12}. \tag{4-12}$$

This noise power is equally distributed in the frequency range from $-f_s/2$ to $+f_s/2$, as shown in Figure 4-11(b). Thus, the double-sided noise spectrum density is

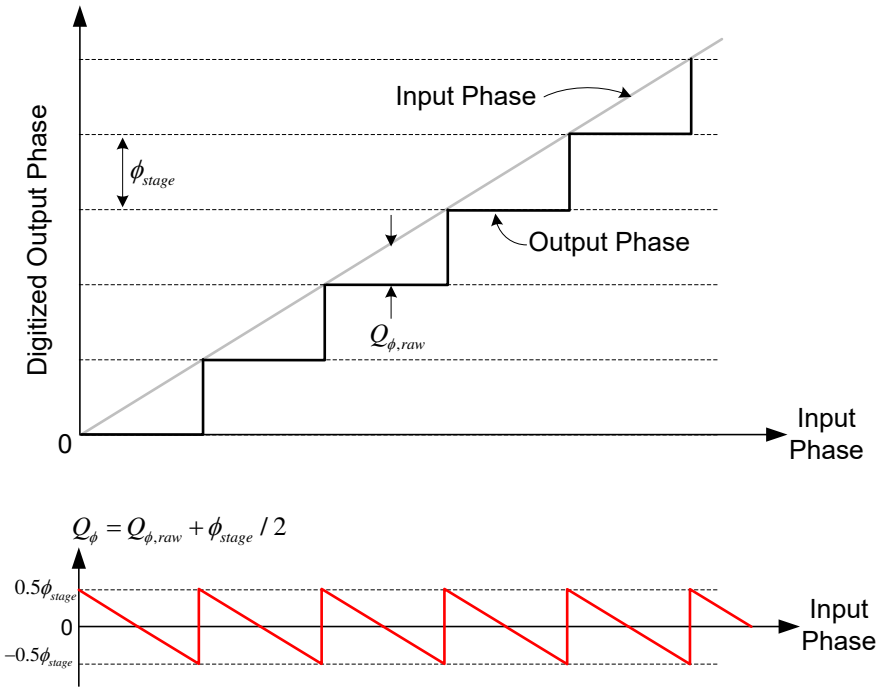


Figure 4-10 Phase quantization transfer characteristic.

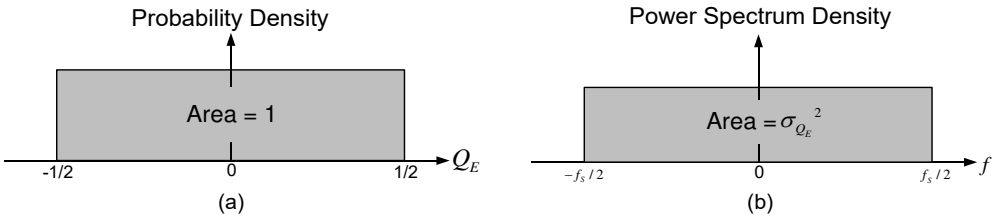


Figure 4-11 (a) Probability density and (b) PSD of quantization error.

$$S_{Q_E} = \frac{1}{12f_s}. \tag{4-13}$$

Substituting (4-13) into (4-11), and z^{-1} with $e^{-j2\pi fT_s}$ according to discrete-to-continuous time transformation, the noise from quantization error becomes

$$S_{n,QE} = \frac{1}{12f_s}\left(\frac{T_{stage}}{1-x}\right)^2 \left|1 - e^{-j2\pi fT_s}\right|^2. \tag{4-14}$$

Total in-band noise power is therefore calculated by integrating $S_{n,QE}$ from DC to signal bandwidth f_{BW}. Assuming $f_{BW} \ll f_s$, the in-band noise is

$$\sigma_{QE,rms}^2 = 2\int_0^{f_{BW}} S_{n,QE}df \approx \frac{2}{9}\left(\frac{\pi T_{stage}}{1-x}\right)^2 \left(\frac{f_{BW}}{f_s}\right)^3. \tag{4-15}$$

Note that the oscillator type (i.e., the value of x) plays an important role. With other parameters kept the same, a GRO ($x = 0$) has a lower noise than an SRO ($0 < x < 1$). An

interesting finding is that an IRO-TDC ($x = -1$) reduces the in-band quantization noise by 4 times compared with a GRO. This can be explained by the theoretically larger gain in an IRO. From another point of view, to achieve a certain noise requirement, the stage delay of an IRO can be designed to be larger than a GRO in order to reduce power consumption. From (4-15), to reduce the quantization noise, smaller stage delay and higher sampling frequency are preferred.

As an example, if $T_{stage} = 16$ ps and $f_s = 200$ MHz, noise in 3 MHz bandwidth of an IRO-TDC is merely 22 fs_{rms}. As will be seen later, this is much lower than the contribution from phase noise of the oscillator. However, (4-15) does limit the signal bandwidth as the quantization noise increases dramatically with f_{BW}.

4.4.2 Stage Delay Mismatch

The above discussion about quantization error assumes an identical delay among all delay stages. This is not true in a real implementation, where the actual delay is affected by connection routings and other mismatches of each stage. In this part, the impact of such delay mismatches is discussed.

The delay mismatch directly affects the phase quantization. Figure 4-12(a) shows an exemplary phase quantization transfer characteristic with mismatch. In contrast to the transfer characteristic without mismatch, the quantization level is no longer equally distributed, but with different size. Accordingly, the actual raw quantization error $Q_{\phi,raw}$ also loses periodicity, illustrated as blue lines. It can be regarded as the summation of mismatch-less quantization error (red lines) and a mismatch-induced error $Q_{\phi,mm}$, i.e.,

$$Q_{\phi,raw} = Q_{\phi,raw,mismatch-less} + Q_{\phi,mm}. \quad (4\text{-}16)$$

Equation (4-16) builds a quantitative relation between quantization error with and without mismatch. As can be seen in the figure, $Q_{\phi,mm}$ is a function of the oscillator phase ϕ_{XRO}. In actual implementation, function $Q_{\phi,mm}(\phi_{XRO})$ is stochastic. Accordingly, the model in Figure 4-12(b) can be expressed equivalently by Figure 4-12(c), with the impact of $Q_{\phi,mm}$ extracted. Value of $Q_{\phi,mm}$ is obtained based on ϕ_{XRO}.

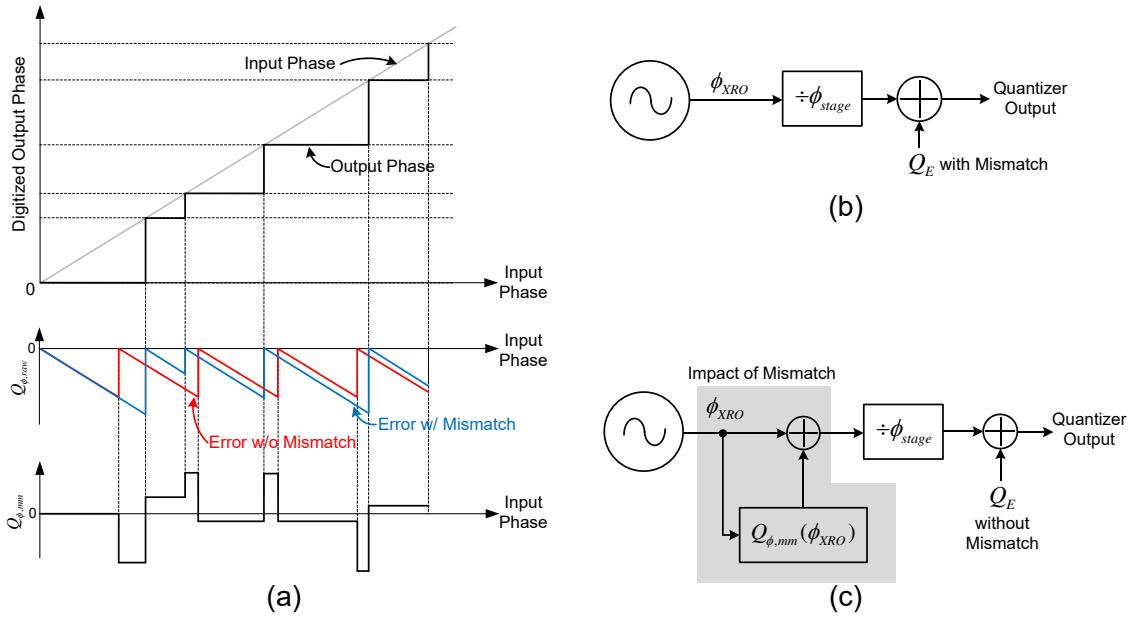


Figure 4-12 (a) Phase quantization transfer characteristic with delay mismatch. (b) Quantization model with mismatch. (c) An equivalent model that extracts the impact of mismatch.

Same as the oscillator phase and mismatch-less quantization error, $Q_{\phi,mm}$ will also be differentiated after quantization. Accordingly, it is also first-order noise shaped by $(1-z^{-1})$. In a proper design, the range of $Q_{\phi,mm}$ should be less than the ideal quantization error, Q_{ϕ}. Therefore, impact of mismatch to the in-band noise is negligible.

4.4.3 Skew Error

Based on (4-9), noise contribution from skew error is governed by

$$S_{n,skew} = S_{\phi_{skew}} \cdot \left(\frac{1}{\omega_0(1-x)}\right)^2, \tag{4-17}$$

where $S_{\phi_{skew}}$ denotes the power density of the phase skew, ϕ_{skew}.

The physical reasons of skew error vary with the mechanism of the oscillator. In a GRO, the two main reasons are charge redistribution at mode switching and voltage leakage during the disabled time [69]-[71]. In an SRO, however, the oscillation does not stop, thus the voltage leakage does not exist [83]-[85]. Causes of the phase skew in an IRO will be discussed in the next section. No matter which type of oscillator is used, phase skew cannot be eliminated as it is not physically possible to change the mode of an oscillator instantaneously because they have different dynamics in the two modes. In summary, these

interruptions cause a deviation from the ideal phase each time when the XRO changes its mode. The amount of phase skew depends on the XRO instantaneous phase ϕ_{XRO}. Function $\phi_{skew}(\phi_{XRO})$ can be simulated. Simulation details will be discussed later in Section 4.5.1. Assuming a random input, the introduced phase deviation is also scrambling, thus appears as a white noise floor in the PSD. The calculation of its PSD level depends on the distribution of $\phi_{skew}(\phi_{XRO})$, which is beyond the scope of this paper. This thesis provides a calculation similar to the quantization error based on a simplified assumption.

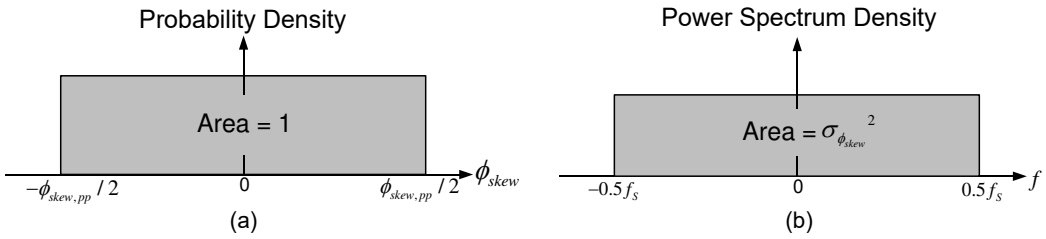


Figure 4-13 (a) Probability density and (b) PSD of phase skew.

Assume ϕ_{skew} has a range from $-\phi_{skew,pp}/2$ to $+\phi_{skew,pp}/2$, where $\phi_{skew,pp}$ is the peak-to-peak phase skew, and the probability is equally distributed, as shown in Figure 4-13(a). As the integrated probability is 1, the probability density is $P = 1/\phi_{skew,pp}$. The expected total power is then

$$\sigma_{\phi_{skew}}{}^2 = \int_{-\phi_{skew,pp}/2}^{+\phi_{skew,pp}/2} \phi_{skew}{}^2 \cdot P \, d\phi_{skew} = \frac{\phi_{skew,pp}{}^2}{12}. \quad (4\text{-}18)$$

This noise power is equally distributed in the frequency range from $-f_s/2$ to $+f_s/2$, as shown in Figure 4-13(b). Thus, the double-sided noise spectrum density is

$$S_{\phi_{skew}} = \frac{\phi_{skew,pp}{}^2}{12 f_s}. \quad (4\text{-}19)$$

Substituting (4-19) into (4-17), $S_{n,skew}$ is obtained. The in-band noise power is thus calculated by integrating $S_{n,skew}$ from DC to signal bandwidth,

$$\sigma_{skew,rms}^2 = 2 \cdot \frac{{\phi_{skew,pp}}^2}{12 f_s} \cdot \frac{f_{BW}}{(1-x)^2 {\omega_0}^2}. \quad (4\text{-}20)$$

The value of $\phi_{skew,pp}$ can be obtained from the simulation to be discussed later. Note that the assumed equal probability density function of ϕ_{skew} may not be the actual case. However, (4-20) does provides an approximation that is easy for analysis. Once again, an IRO ($x = -1$) reduces the skew noise power by a factor of 4. From (4-20), to achieve a lower skew noise in an XRO-TDC, higher sampling rate, lower phase skew, and higher oscillator frequency are preferred.

As an example, if $\phi_{skew,pp} = 15$ mrad, $f_s = 200$ MHz, and the IRO frequency is 600 MHz, the integrated noise within a 3 MHz bandwidth is 100 fs_{rms}.

4.4.4 Dead-Zone Behaviors

Except for the white noise floor in PSD, another possible effect caused by the phase skew is that dead-zones can be found in the DC transfer characteristic of the TDC, as shown in Figure 4-14. Around certain input values, the TDC output is pushed away from the ideal curve to some values and does not change with the input. It has been mentioned and measured in [71]. This thesis provides a more visible and quantitative explanation.

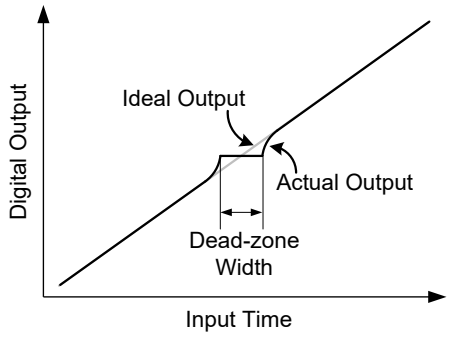


Figure 4-14 Conceptual DC transfer characteristic showing a dead-zone.

Dead-zones can be found only when the oscillator phase is not scrambled adequately. As will be detail explained later, the amount of phase skew ϕ_{skew} depends on the oscillator phase ϕ_{XRO}. Figure 4-15 illustrates how the phase skew affects an oscillator.

Each time the phase skew is generated, it is added into the oscillator and affects the future phase ϕ_{XRO}'. So $\phi_{XRO}' = \phi_{XRO} + \phi_{skew}$.

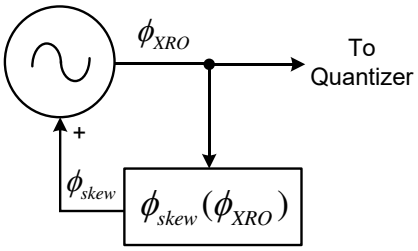


Figure 4-15 Effect of phase skew to an oscillator.

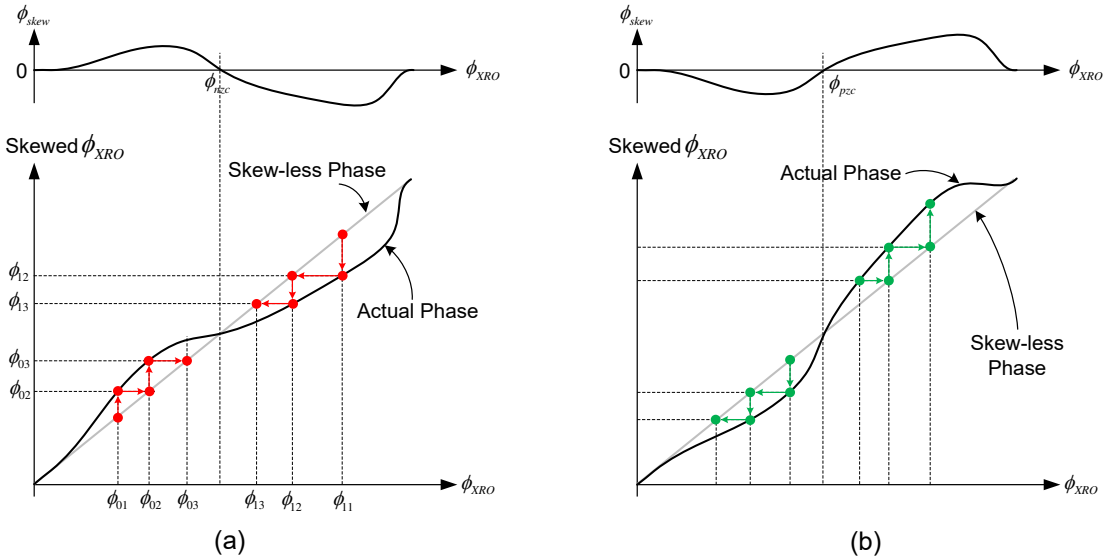


Figure 4-16 Phase changes with $2K\pi$ phase increment near (a) a negative zero-crossing point and (b) a positive zero-crossing point.

With this mechanism established, we can explain how a dead-zone is formed using Figure 4-16. Let us consider a small region near a zero-crossing ϕ_{skew} with a negative slope, as in Figure 4-16(a). To find the dead-zones, firstly, assume the skew-less oscillator phase increment during each measurement cycle is exactly $2K\pi$, i.e.,

$$\Delta\phi_{XRO} = 2K\pi, \tag{4-21}$$

where K is an integer. That is to say, ϕ_{XRO}' becomes the next ϕ_{XRO} (after wrapped). Figure 4-16(a) shows the operation under this scenario. If $\phi_{XRO} = \phi_{01}$ at some cycle, ϕ_{XRO}' becomes ϕ_{02} because of the phase skew. At the next cycle, $\phi_{XRO} = \phi_{02}$, and ϕ_{XRO}' becomes ϕ_{03}. In the subsequent cycles, ϕ_{XRO} is pushed towards a larger value as

an effect of ϕ_{skew}. In another case, if $\phi_{XRO} = \phi_{11}$ at some cycle, $\phi_{XRO}{}'$ becomes ϕ_{12} because of the phase skew. At the next cycle, $\phi_{XRO} = \phi_{12}$, and $\phi_{XRO}{}'$ becomes ϕ_{13}. Similarly, ϕ_{XRO} is pushed towards a smaller value. As a result, if the phase increment is kept $2K\pi$, the oscillator phase will be eventually pushed to the negative zero-crossing point ϕ_{nzc} regardless of the initial ϕ_{XRO}. The reader can analyze with Figure 4-16(b) using the similar flow, and will find that a positive zero-crossing point ϕ_{pzc} is not such a stable phase (but a metastable phase) because ϕ_{skew} will push ϕ_{XRO} away from ϕ_{pzc}.

From the above analysis, we can now conclude that:

- A negative zero-crossing point of ϕ_{skew} results in one dead-zone. Different value of *K* will lead the oscillator to the same dead-zone. The negative zero-crossing point of ϕ_{skew} is defined as the *stable point*.
- If more stable points exist, there will be more dead-zones.

Next, we can add some deviation to the phase increment, and assume

$$\Delta\phi_{XRO} = (1-x)\omega_0 T_{in} + x\omega_0 T_s = 2K\pi + \phi_{dev}, \tag{4-22}$$

where *K* is an integer and ϕ_{dev} is a small deviation. The phase is shown in Figure 4-17. If $\phi_{XRO} = \phi_{21}$ at some cycle, due to the phase skew, $\phi_{XRO}{}'$ becomes $\phi_{22} = \phi_{21} + \phi_{skew}(\phi_{21})$. At the next cycle, $\phi_{XRO} = \phi_{23} = \phi_{22} + \phi_{dev}$. To avoid being pushed towards the stable point, ϕ_{23} has to be further away than ϕ_{21} from the stable point, i.e.,

$$\phi_{23} = \phi_{22} + \phi_{dev} < \phi_{21}. \tag{4-23}$$

Accordingly,

$$\phi_{dev} < \phi_{21} - \phi_{22} = -\phi_{skew}(\phi_{21}). \tag{4-24}$$

Generally, to avoid being locked,

$$\phi_{dev} < -\phi_{skew}(\phi_{21}), \forall\phi_{21}. \tag{4-25}$$

In other words, in order to escape the dead-zone, deviation must be

$$\phi_{dev} < -\phi_{skew,max}. \tag{4-26}$$

Similarly, another condition that also permits the oscillator to escape the dead-zone is

$$\phi_{dev} > -\phi_{skew,min}. \tag{4-27}$$

In (4-26) and (4-27), $\phi_{skew,max}$ and $\phi_{skew,min}$ refer to the positive and negative largest ϕ_{skew} from 0.

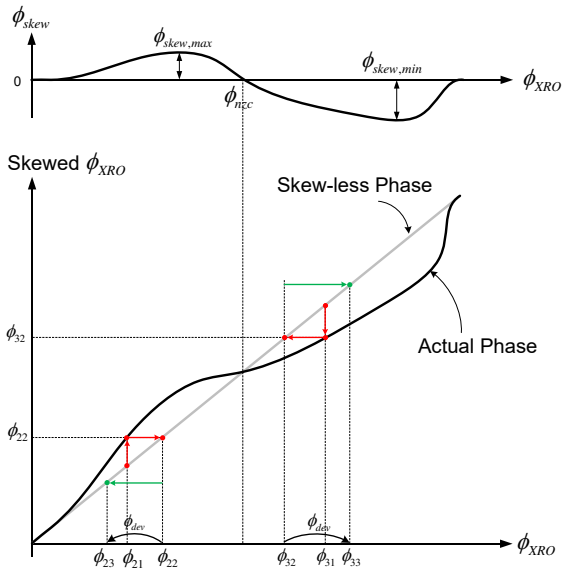


Figure 4-17 Phase changes near ϕ_{nzc} with $2K\pi + \phi_{dev}$ phase increment.

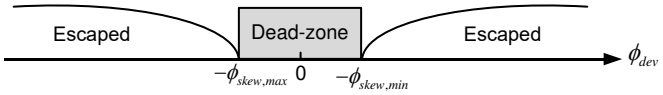


Figure 4-18 Relation between phase increment and dead-zone.

Equation (4-26) and (4-27) reveal that, a dead-zone will appear if

$$-\phi_{skew,max} < \phi_{dev} < -\phi_{skew,min}. \tag{4-28}$$

This conclusion is illustrated in Figure 4-18.

Substituting (4-22) into (4-28), the input range causing dead-zone is

$$\frac{2K\pi - \phi_{skew,max}}{(1-x)\omega_0} - \frac{xT_s}{1-x} < T_{in} < \frac{2K\pi - \phi_{skew,min}}{(1-x)\omega_0} - \frac{xT_s}{1-x}. \tag{4-29}$$

For simplicity, we define $\phi_{skew,range} = \phi_{skew,max} - \phi_{skew,min}$. The dead-zone width is thus

$$T_{dz,XRO} = \frac{\phi_{skew,range}}{(1-x)\omega_0}. \tag{4-30}$$

We can obtain the dead-zone width of a GRO ($x = 0$) as

$$T_{dz,GRO} = \frac{\phi_{skew,range}}{\omega_0}, \tag{4-31}$$

and that of an IRO ($x = -1$) as

$$T_{dz,IRO} = \frac{\phi_{skew,range}}{2\omega_0}. \tag{4-32}$$

This implies that an IRO can also reduce the dead-zone width for a same $\phi_{skew,range}$.

Certainly, the phase increment during each measurement is hardly identical. Other noises such as the thermal noise jitter of the controller and the signal input buffers can cause some deviation, ϕ_{dev}. However, (4-30) does provide an important conclusion that the dead-zone width can be reduced if ϕ_{skew} can be constrained within a smaller range. If $\phi_{skew,range}$ is even less than the phase deviation caused by the thermal jitter, dead-zone is expected to disappear completely.

To conclude, a dead-zone appears if the following two conditions are fulfilled at the same time:

- Equation (4-29) is met. In other words, the input time is close enough to certain values.
- Equation (4-29) is met for long period of time. From the locking procedure shown in Figure 4-16(a), the mechanism takes several consecutive cycles to lock the phase. If a large phase deviation occurs during this procedure, the phase escapes and is not likely to be locked.

For most TDC operations, a random input time is applied. For example, in fractional-*N* digital PLLs, the input time is quickly and sufficiently dithered by DSM. Under such condition, a dead-zone should not occur.

4.4.5 Oscillator Phase Noise

Based on (4-9), noise contribution from oscillator phase noise is governed by

$$S_{n,XRO} = S_{\phi_{n,XRO}} \cdot \left(\frac{1 - z^{-1}}{\omega_0(1 - x)}\right)^2, \tag{4-33}$$

where $S_{\phi_{n,XRO}}$ denotes the oscillator phase noise.

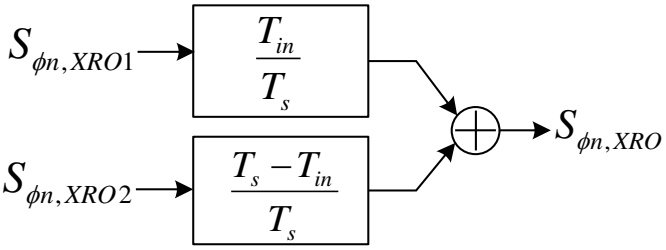


Figure 4-19 Phase noise model of dual-mode XRO.

Figure 4-19 shows the model for oscillator phase noise. Since the XRO we discuss operates in two modes, it can be modeled as two independent oscillators. The two oscillators are OSC_1 with phase noise power of $S_{\phi n,XRO1}$ and OSC_2 with $S_{\phi n,XRO2}$. Note that $S_{\phi n,XRO1}$ and $S_{\phi n,XRO2}$ are two independent noise sources. Depending on the TDC input T_{in}, the XRO is switching between OSC_1 and OSC_2 for durations T_{in} and $(T_s - T_{in})$, respectively, during which they contribute their own noise power to the XRO phase. Thus, the total XRO phase noise power is given by

$$S_{\phi n,XRO} = S_{\phi n,XRO1} \cdot \left(\frac{T_{in}}{T_s}\right) + S_{\phi n,XRO2} \cdot \left(\frac{T_s - T_{in}}{T_s}\right). \tag{4-34}$$

Discussion on $S_{\phi n,XRO1}$ and $S_{\phi n,XRO2}$ varies with XRO type. A GRO is paused after T_{in} and does not generate any noise to the phase, yielding a $S_{\phi n,XRO2} = 0$. This reveals that the GRO-TDC in-band noise depends on T_{in}, since a large T_{in} turns on the GRO for longer time and thus results in more phase noise. An SRO also shows this dependence due to different $S_{\phi n,XRO1}$ and $S_{\phi n,XRO2}$. However, for an IRO, the OSC_1 and OSC_2 can be implemented in identical structure. Therefore, OSC_1 and OSC_2 have the same phase noise PSD, i.e. $S_{\phi n,IRO1} = S_{\phi n,IRO2}$. Accordingly, the two terms in (4-34) can be combined to cancel out T_{in}, resulting in a T_{in}-independent noise in an IRO, i.e.

$$S_{\phi n,IRO} = S_{\phi n,IRO1} = S_{\phi n,IRO2}. \tag{4-35}$$

Total TDC in-band noise due to oscillator phase noise can be calculated by integrating (4-33) from DC to bandwidth. Assuming $f_{BW} \ll f_s$,

$$\sigma_{PN,rms}^2 = \int_0^{f_{BW}} S_{n,XRO} df$$

$$\approx \left(\frac{2\pi}{f_s \omega_0 (1-x)}\right)^2 \int_0^{f_{BW}} S_{\phi_{n,XRO}} f^2 df. \tag{4-36}$$

The value of $S_{\phi_{n,XRO}}$ can be obtained from simulation. Again, this noise is reduced by 4 times in an IRO ($x = -1$).

Even though it experiences a noise-shaping transfer, the noise from the oscillator still acts as the major contributor to the in-band noise for the controlled oscillator-based TDC family. As an example, if a 600 MHz oscillator is used with a moderate -90 dBc/Hz phase noise at 1 MHz offset, under a 200 MHz sampling rate, the maximum integrated noise within a 3 MHz bandwidth is about 456 fs_{rms} in a GRO. Even if an IRO is used, this noise is still as large as 228 fs_{rms}, still much larger than the noise from skew error and quantization error. Therefore, reduction of oscillator noise is the major target of a low-noise XRO-TDC.

4.4.6 IRO Phase Noise Cancellation

In previous discussion about oscillator phase noise, the oscillator noise model is suitable for GRO, SRO, and IRO. An IRO has the potential to reduce the oscillator noise. Moreover, an IRO has a unique capability of coherent phase noise cancellation. In this part, this noise-cancellation characteristic is analyzed.

The model in Figure 4-19 assumes no "coherent noise" from these two oscillators. In this thesis, a coherent noise refers to the noise that has the same physical source and transfer function to both OSC_1 and OSC_2. For example, in an IRO, noises from power supply, ground, substrate, or any component with unchanged phase noise contributions in both oscillation directions can be regarded as coherent noises. Sources of such noises depend on actual implementation of the IRO. For a GRO or SRO, there should not be coherent noise because all noise sources should have different transfer function in two operation modes.

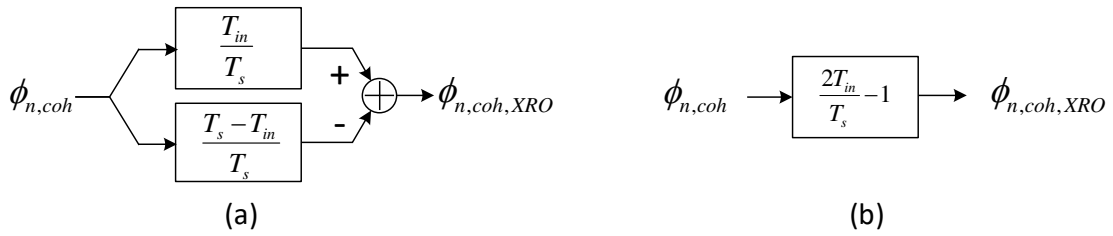


Figure 4-20 IRO coherent noise model under quasi-stationary $\phi_{n,coh}$.

To analyze such noises, the model in Figure 4-20(a) can be used. The coherent noise is normalized within one measurement cycle and denoted as $\phi_{n,coh}$. This noise affects the XRO phase through OSC_1 for a duration of T_{in}, and through OSC_2 for a duration of $(T_s - T_{in})$. Due to oscillation inversion, these two impacts are subtracted one from another, resulting in $\phi_{n,coh,XRO}$ as the total impact to phase noise. For low-frequency components of $\phi_{n,coh}$, they can be regarded as quasi-stationary signals. Figure 4-20(b) shows an equivalent model. The total contribution from coherent noise to XRO phase noise power is thus

$$S_{\phi_{n,coh,XRO}} = S_{\phi_{n,coh}} \left(\frac{2T_{in}}{T_s} - 1\right)^2, \tag{4-37}$$

where $S_{\phi_{n,coh}}$ denotes the power spectrum of coherent noise. Note that different from incoherent noises in (4-34), the noise amplitude rather than power is taken into calculation. Since $\left(\frac{2T_{in}}{T_s} - 1\right)^2$ is always between 0 to 1, (4-37) reveals a rejection or cancellation of a slow and coherent impact on the XRO phase, depending on the value of T_{in}/T_s. Specially,

$$S_{\phi_{n,coh,XRO}} = \begin{cases} S_{\phi_{n,coh}}, & T_{in}/T_s = 0 \; or \; 1 \\ 0, & T_{in}/T_s = 1/2 \end{cases} \tag{4-38}$$

refer to the XRO phase noise power without cancellation and with maximum cancellation, respectively. To evaluate the cancellation effect, a phase noise rejection ratio (PNRR) can be defined as

$$PNRR = \frac{S_{\phi n,co,XRO} \text{ with no noise canceling}}{S_{\phi n,co,XRO} \text{ with noise canceling}}. \tag{4-39}$$

According to (4-38),

$$PNRR_{dB} = -20\, log|2T_{in}/T_s - 1|. \tag{4-40}$$

Table 4-3 summarizes different characteristics of GRO-, SRO-, and IRO-TDCs based on the proposed model. Due to its higher gain with factor $(1 - x)$, an IRO-TDC achieves reduced raw resolution, phase noise contribution and in-band noise. Reduced raw resolution also implies a higher signal bandwidth. Moreover, a unique phase noise cancellation mechanism is provided by an IRO to protect the TDC from coherent noises such as power noise. Note that an IRO also implies a higher power consumption since we would like the IRO to operate at a high frequency and a small stage delay. However, as the

supply current is constant, even though the power consumption is increased, its disturbance to power supply is still much smaller than that from a GRO or an SRO.

Table 4-3 Characteristics Comparison among GRO, SRO, and IRO-TDCs

TDC type	SRO	GRO	IRO
TDC Gain	$(1-x)/T_{stage}$ *	$1/T_{stage}$	$2/T_{stage}$
Raw Resolution	$T_{stage}/(1-x)$ *	T_{stage}	$T_{stage}/2$
Scaled PN Contribution **	$1/(1-x)^2$ *	1	1/4
In-band Noise	T_{in}-dependent	T_{in}-dependent	Constant
Coherent Noise Rejection	No	No	Yes

* Note that $0 < (1-x) < 1$, and $1/(1-x) > 1$.

** Assuming same $S_{\phi n,XRO}$ and f_s. PN is short for phase noise.

4.5 IRO-TDC Implementation

The overview of the IRO-TDC prototype is depicted in Figure 4-21. The oscillator controller comprises an SR-latch which transfers the *Start* and *Stop* edges into control signal, and a buffer that generates the differential *EN*± signal with sufficient driving strength to control the IRO. The phase processor contains a phase quantizer that captures the IRO phase and a differentiator that calculates the final TDC output, D_{out}. The IRO is the critical part of this prototype as it causes most of the in-band noise. The design and implementation details for the IRO and the phase processor are discussed next.

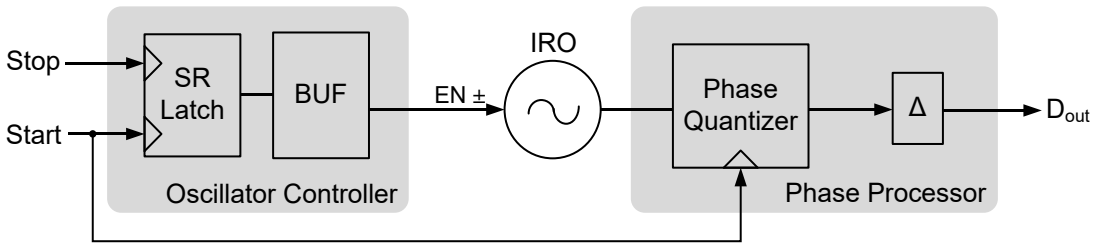


Figure 4-21 Structure of the proposed IRO-TDC.

4.5.1 Low-Skew Multi-Path IRO

In order to simulate the phase skew during circuit design, testbench in Figure 4-22 is employed. At the beginning of this test, *EN+* is initially high, and the IRO is in positive oscillation. At the time of T_{test}, a *Stop* edge arrives, *EN+/-* toggle and oscillation inverts. After a time duration of T_{width}, a *Start* edge oscillation inverts once again. The ideal phase is shown as the grey line, and the actual phase as the black line. Since it is not so straightforward to obtain the phase skew from the simulation results, a time skew, T_{skew}, is defined as the time difference between the ideal phase and the actual phase. From the figure, the relation between time skew and phase skew is

$$T_{skew} = \frac{\phi_{skew}}{\omega_0}. \tag{4-41}$$

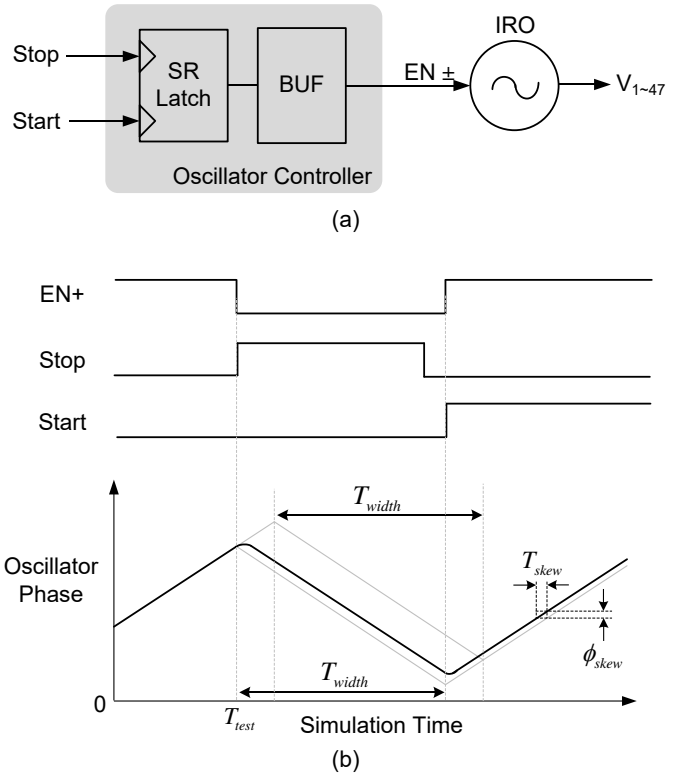


Figure 4-22 (a) Simulation testbench for the IRO phase skew and (b) an exemplarity timing diagram.

As can be seen in the timing diagram, if T_{test} is changed while keeping the same T_{width}, the ideal phase at the region after the *Start* edge is also fixed. The actual phase, however, is

changing because of different phase skew values. It can be identified by looking for the time at which a given output voltage crosses a certain level. In this simulation, the time at which V_1 = 0.6 V (half of the supply voltage) is denoted as t_{cross}. Deviation of t_{cross} is hence the deviation of T_{skew}. From this simulation, the information we need is the deviation of T_{skew} rather than its absolute values because its average value can be regarded as a constant offset. In fact, T_{skew} should have a positive average value because of the latency in the controller and other preceding circuits.

To realize an inverted oscillator, there are many options. Figure 4-23 shows a simple implementation. Each delay cell is simply two opposing inverters controlled by *EN*+/-. The delay cells form two loops for two oscillation directions, as shown in Figure 4-23(a). When *EN*+ is 1 and *EN*- is 0 (mode 1), the oscillator operates in a direction that O_1 is driving O_2 (red arrows). After *EN*+ and *EN*- toggle (mode 2), oscillation is inverted so that O_2 drives O_1 (blue arrows).

This IRO has a simple structure that can be easily designed and routed. However, it has two critical drawbacks for a low-noise TDC, including:

- Stage delay cannot be very small, resulting in a large raw resolution,
- Simulated phase skew is large due to severe charge redistribution.

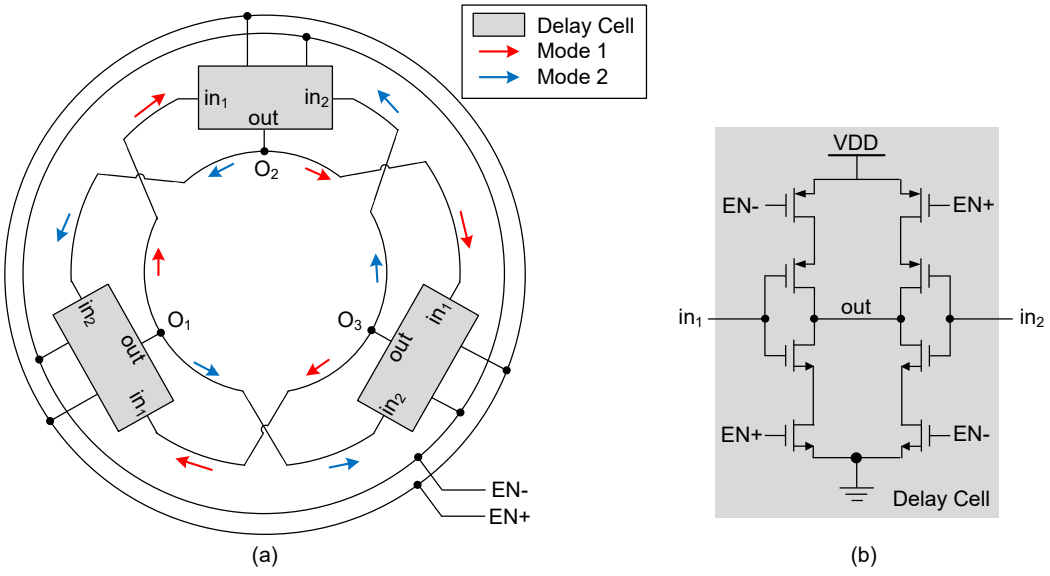


Figure 4-23 Schematic of (a) a simple IRO and (b) each of its delay cells.

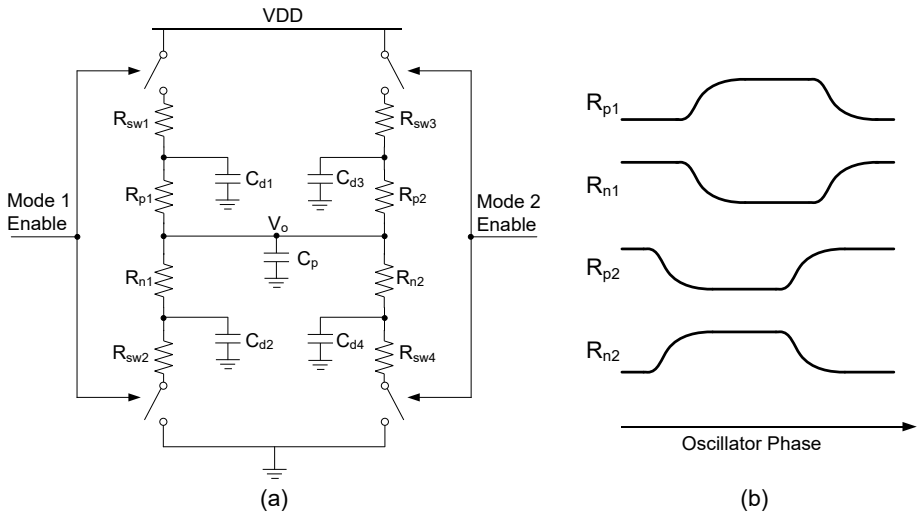


Figure 4-24 (a) An equivalent schematic of a single delay cell and (b) changes of transistor resistances.

The charge redistribution issue can be understood using Figure 4-24. Figure 4-24(a) shows an equivalent schematic of a single stage, where R_{n1}, R_{n2}, R_{p1}, R_{p2} represent the channel resistance of the driving transistors, and $R_{sw1\text{-}4}$ represent that of the enabling transistors. The values of $R_{n1,2}$ and $R_{p1,2}$ depend on the node voltages of the last stage and the next stage (i.e., in_1 and in_2 in Figure 4-23). If the oscillator is inverted during a V_o transition, $C_{d1\sim4}$ and C_p have different voltages. Charges on these components will be redistributed through $R_{n1,2}$ and $R_{p1,2}$ so that they fulfill a new set of dynamics, and the voltage of V_o is thus affected. The amount of this disturbance on V_o depends on the values of $R_{n1,2}$ and $R_{p1,2}$, which change with oscillator phase, as shown in Figure 4-24(b). Accordingly, the skew introduced at the inversion depends on the oscillator phase.

To extend this conclusion to the whole IRO, a cartoon of the phase skew as in Figure 4-25(a) can be used. The skew should be periodic since all stages have similar behavior. However, skew at a rising transition and that at a falling transition may be different. The waveform shown in the figure is a conceptual example. The total phase skew is then a simple summation of each section. If there is only one transition stage at any time, the skew should be large because the whole oscillator exhibits the maximum and minimum skew of each stage periodically.

Table 4-4 lists the post-layout simulation results and calculated characteristics based on the proposed model with a sampling rate of 200 MHz. Raw resolution is 25.5 ps and integrated in-band noise is 414 fs_{rms}.

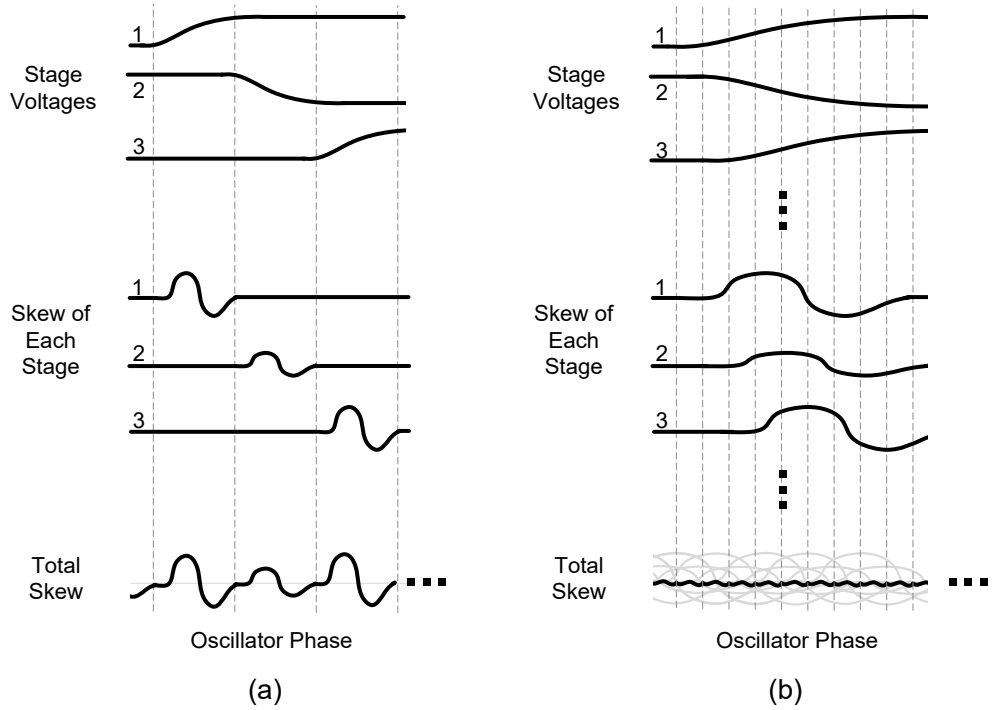


Figure 4-25 (a) Total IRO phase skew contributed from each transition stage. (b) Phase skew mitigated through averaging by extended transitions.

Table 4-4 Post-Layout Simulation and Calculation Results of the Simple IRO Implementation with 200 MHz Sampling Rate

Characteristics		Values
Frequency		3.27 GHz
Power		1.4 mW
T_{stage}		51 ps
Raw resolution		25.5 ps
$T_{skew,pp}$		13.4 ps
Widest dead-zone		6.7 ps
Skew noise	1 MHz BW	193 fs_{rms}
	3 MHz BW	335 fs_{rms}
Phase noise	1 MHz BW	224 fs_{rms}
	3 MHz BW	244 fs_{rms}
Skew & phase noise	1 MHz BW	296 fs_{rms}
	3 MHz BW	414 fs_{rms}

To mitigate the skew, [70] provides a potential approach by utilizing a multi-path oscillator. The idea is to extend the transition duration so that there are several transition stages at any given time. By doing this, the impact of the transition stages can be averaged to some extent, as shown in Figure 4-25(b).

To realize the multi-path oscillator, an intuitive approach is to use the outputs from several preceding stages to drive a certain delay unit through a multi-input-single-output inverter. Figure 4-26 shows the multi-path IRO structure in this prototype. Figure 4-26(a) depicts a conceptual schematic of the IRO, and Figure 4-26(b) shows the detail schematic including the first delay cell. Each delay cell comprises two opposing yet identical drivers (i.e., driver *A* and *B*) driving the same output port. For example, when *EN+* is high and *EN-* is low, the IRO is at mode 1, and all drivers *A* are connected to power supply while drivers *B* are disabled. At this mode, V_1 is driven by V_{47}, V_{43}, V_{39}, V_{37}, and V_{35}. After EN+/- toggle (i.e., IRO mode 2), drivers *B* are enabled while *A* are disabled, and V_1 is driven by V_2, V_6, V_{10}, V_{12}, and V_{14}. With more input ports and inputs from stages further away, the output can start to charge or discharge earlier, thus a shorter stage delay can be achieved. In the prototype, each of all drivers A and drivers B contains five inputs and one output. Totally 47 cells are used and connected following the sequence shown in the figure.

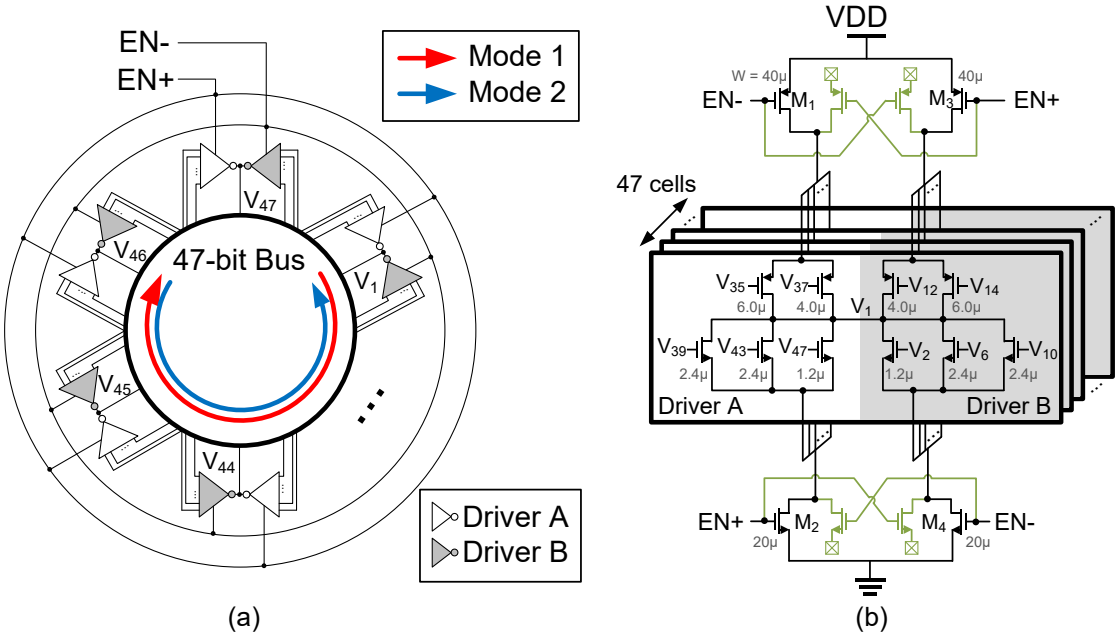


Figure 4-26 (a) Topology and (b) schematic of the multi-path IRO.

Table 4-5 Post-Layout Simulation and Calculation Results of the Multi-Path IRO Implementation with 200 MHz Sampling Rate

Characteristics		Values
Frequency		665 MHz
Power		5 mW
T_{stage}		16 ps
Raw resolution		8 ps
$T_{skew,pp}$		4 ps
Widest dead-zone		2 ps
Skew noise	1 MHz BW	58 fs_{rms}
	3 MHz BW	100 fs_{rms}
Phase noise	1 MHz BW	106 fs_{rms}
	3 MHz BW	116 fs_{rms}
Skew & phase noise	1 MHz BW	121 fs_{rms}
	3 MHz BW	153 fs_{rms}

To further reduce the skew due to charge redistribution, the enabling transistors of all delay cells are combined into four global transistors (i.e., $M_{1\sim4}$), instead of using individual enabling transistors for each delay cell. This brings two advantages in terms of the skew. Firstly, the four drain capacitances of the enabling transistors are shared by all 47 cells, resulting in an averaging of the charge redistributions in all stages. Secondly, the number of transistors that accept *EN*+/- signals is reduced. Mismatch of the signal arriving time is greatly reduced compared with using $47 \times 2 = 94$ transistors. During toggling, some charge is injected into the supply signals through the gates of the enabling transistors. This injected charge also affects the redistribution mechanism. In order to reduce this charge injection, transistors with identical gate width are added to compensate for the injection. These transistors are colored in Figure 4-26(b) since they have no function to the operation but just to cancel out the injected charge. In this IRO implementation, there is no transistor acting as a coherent noise source.

During the layout procedure of this IRO, only the delay cell is customized. With the reusable delay cell layout completed, the IRO layout is accomplished by customized placement and automatic routing using Cadence Virtuoso Chip Assembly Router. Such an automatic routing is helpful to implementations of this IRO and future IRO designs

because it can shorten design cycle. During automatic routing, matching rule is applied to the total wire length of each oscillator nodes to reduce mismatch. However, this routing still introduces some mismatch that breaks the symmetry so that the transition duration of each stage is not equal, and the phase skew mitigation through averaging mechanism is affected.

Table 4-5 summarizes the IRO post-layout simulation and calculation results under a 200 MHz sampling rate. Compared with the results in Table 4-4, raw resolution is reduced to 8 ps and integrated in-band noise is reduced to 153 fs_{rms}. Therefore, a multi-path structure can achieve better quantization noise and in-band noise performance.

Figure 4-27 shows the simulated current consumption of the IRO and the oscillator controller with a 1.2 V supply. When *EN+/-* toggle, the oscillator introduces small spikes into the power supply, and the average current consumption is not changed. These spikes can be easily attenuated by decoupling capacitors and should have negligible effect to the other circuits. For comparison, the current consumption of a GRO is also plotted. When a GRO is gated, the total supply current is reduced by about 4.2 mA. This is a much larger disturbance. In a digital PLL, such a disturbance can affect other circuits and lead to higher reference spurs at the DCO output.

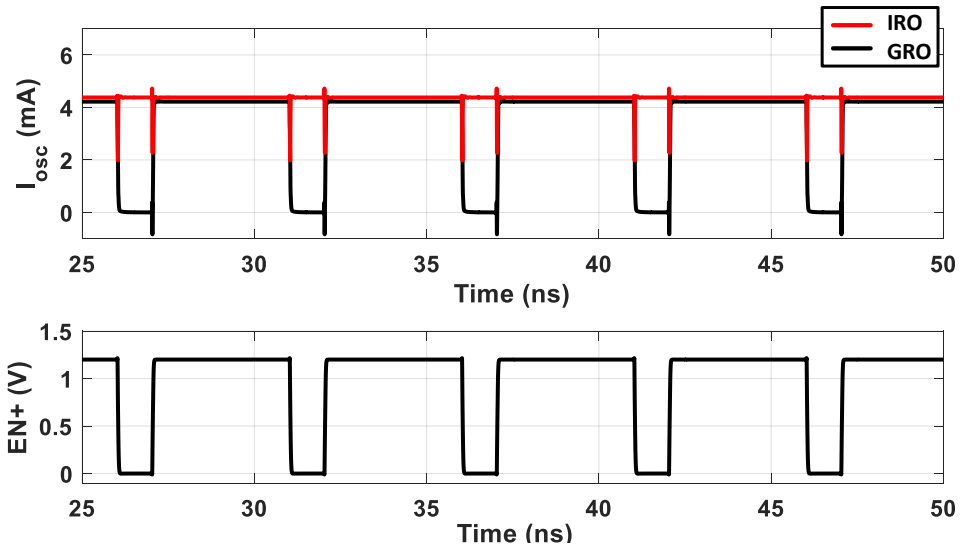


Figure 4-27 Simulated supply currents of GRO and IRO (including oscillator controllers) with same transistor sizes.

4.5.2 Phase Processor

The function of the phase processor is to capture the oscillator phase and calculate the final TDC output. Quantization of the phase is divided into fractional quantization (within an oscillator cycle) and the integer quantization (due to wrapping). Both parts are realized by Verilog code, and the whole phase processor is synthesized and routed using automatic digital flow. In this section, we provide the design details of both parts.

Fractional Quantization

To convert the phase into digital information, the node voltages of the oscillator can be digitized and mapped to a digital code representing oscillator phase. The phase of the oscillator can be determined by the location of the transition stage, where the voltage is neither a stable high nor a stable low. Figure 4-28 illustrates the fractional quantizer adopted in our prototype. Figure 4-28(a) shows the schematic, and Figure 4-28(b) is a timing diagram and truth table showing the identifying of a stable '0', a stable '1', or a transition state ('TX') of an output node. If the node voltage is below or above both threshold voltages, the stage is in a stable '0' or '1' state, respectively. If the node voltage is between two thresholds, a transition state 'TX' is identified. The two threshold voltages levels can be configured digitally during measurement in order to observe more details about the oscillator node characteristics. Upon the sampling edge, DFFs capture the comparator outputs, V_L and V_H. A transition locator identifies the digital state of each node. By doing this, the location of the transition stage can be found. With all node states and the transition location determined, the oscillator phase can be mapped to a digital code, D_ϕ, ranging from 0 to 93. Totally $47 \times 2 = 94$ output levels are used to represent the fractional phase. D_ϕ is differentiated to obtain D_{frac}, a digital representation of the fractional phase increment.

This fractional quantizer is adopted in our prototype. However, it has some drawbacks to the overall performance. Some of these adverse effects can be observed in the next section about measurement results. From a systematic point of view, we explain these effects before moving forward to the experimental results.

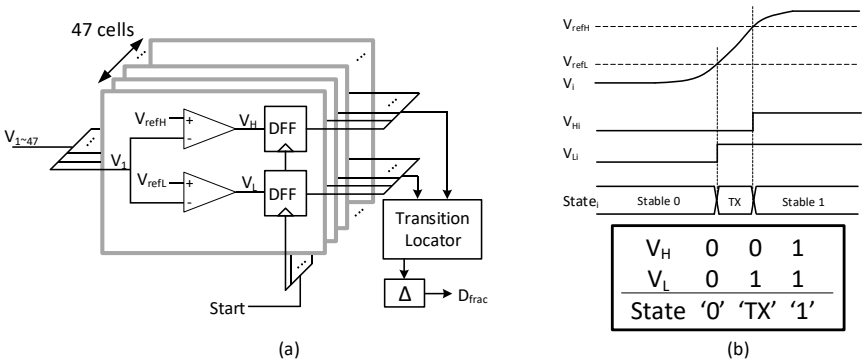


Figure 4-28 (a) Schematic of fractional quantization and (b) state identification truth table.

The first effect is the increased quantization error. Due to the extended transition states, there may be several stages in transition state at the same time. The quantizer may map this result to a wrong digital output code, equivalently increasing the quantization error. Fortunately, since quantization error will be noise shaped, and this has negligible impact to the TDC in-band noise.

Secondly, the inaccurate transition location (i.e., a deviated digital output code) may also lead to a dead-zone wider than calculated. For example, if the oscillator phase is near the dead-zone, but not really locked, the inaccurate transition location may still generate a constant output code, as shown in Figure 4-29. Therefore, an observed dead-zone may seem wider than the calculation result.

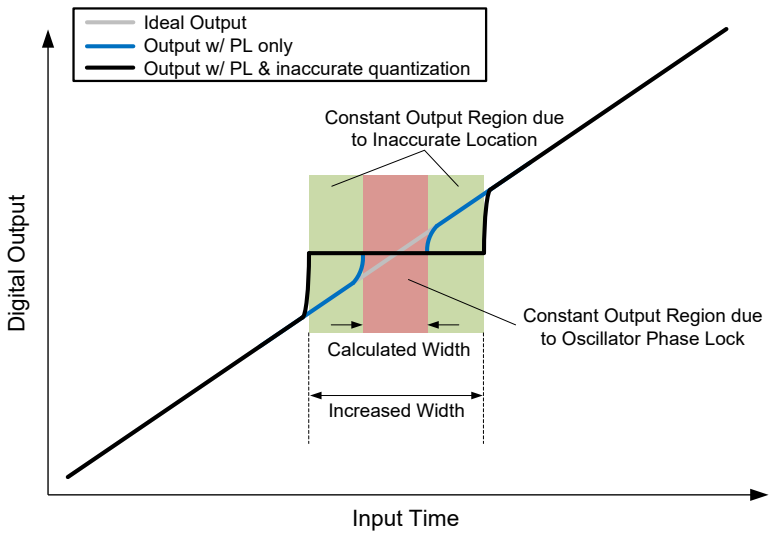


Figure 4-29 Dead-zone due to phase lock (PL) and inaccurate quantization.

Lastly, the comparators and DFFs bring some power consumption overhead.

One mitigation approach is to use a phase quantizer that divides all the nodes into several *cells* such that each cell contains at most one delay element in transition. Figure 4-30 shows how it has been implemented [70]. The oscillator nodes are grouped into several cells with a certain pattern, so that there is only one transition stage at each cell. Transition stage location is performed in each cell, and the results will be summed to generate a more accurate digital code. Identification of '1', '0', and 'TX' is based on the digital node state rather than voltage comparator results. For example, if two consecutive stages have the same '1' or '0' state, one of these two stages is identified as 'TX'. This quantizer structure is not employed in this prototype. However, it can be modified and adopted in the future design of the IRO-TDC.

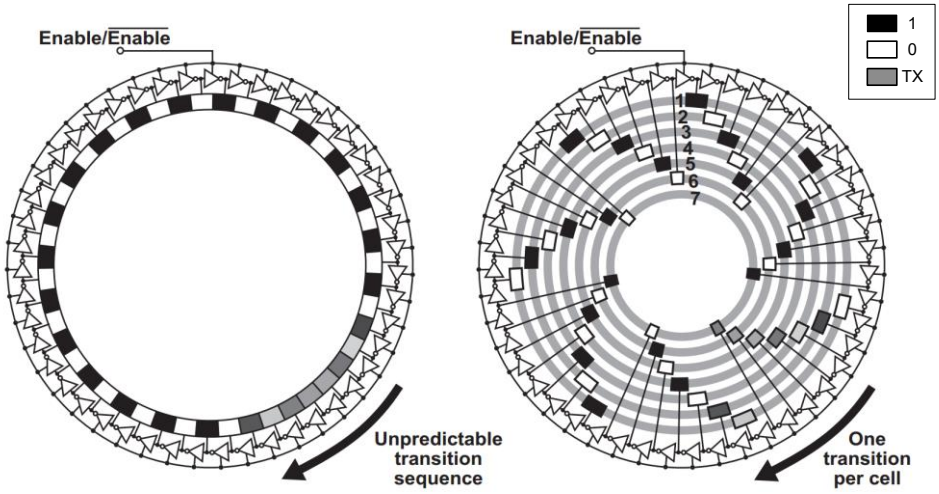


Figure 4-30 (a) A transition locator with location error, and (b) a regrouped locator that can reduce this error [70].

Integer Quantization

As the oscillator operates periodically, a fractional quantization is not enough because it cannot process the wrapping. Therefore, a wrap counter is required. In contrast to a GRO or SRO, an IRO is inverted and the wrap counter needs to perform both +1 and -1 counting. This challenge is depicted in Figure 4-31. When the IRO oscillates following a defined positive direction (mode 1), the counter counts up following the red arrow. When

the IRO is inverted (mode 2), the counter counts down following the blue arrow. Conceptually, all the voltage waveforms in mode 2 would be the backstepping of those in mode 1. As can be seen in the figure, these two counting modes cannot simply use the rising edge or falling edge as their triggering edge because both edges appear in both modes.

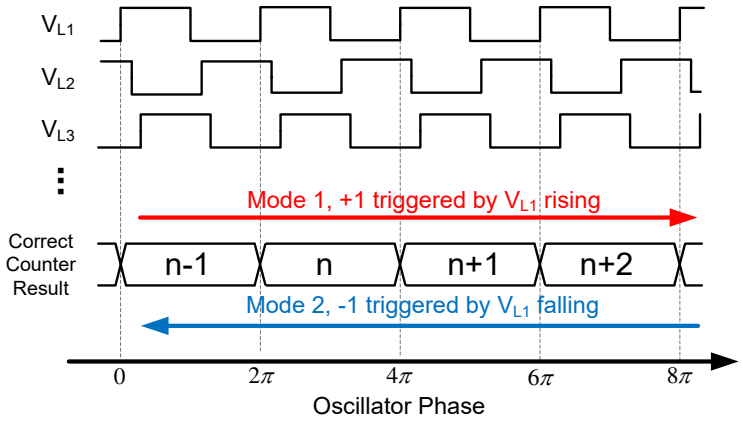


Figure 4-31 Timing diagram of a correct wrap counting.

Although the counting edge is not as straightforward as in a unidirectional counter, we can still identify the +1 and -1 trigger using additional conditions. Let us consider the waveform of V_{L24} and V_{L1}. When V_{L24} = '1', a V_{L1} rising edge during can be taken as the +1 triggering edge. Accordingly, when V_{L24} = '1', the V_{L1} falling edge should be used as the -1 triggering edge. Figure 4-32 provides a counter design that can realize this function. To avoid conflict with the fractional quantization, the counter takes V_{L24} as an arbiter signal and V_{L1} as the trigger signal.

Another challenge is the count-and-read racing problem, illustrated in Figure 4-33. During operation, the counting is triggered by the oscillator, and the counting result is to be read by the sampling clock. These are two asynchronous events. After each counting edge, the counting result has to be stable well before the sampling edge to fulfill the readout setup time. After the readout, the counting result has to be stable within the readout hold time. If the sampling edge is too close to the counting edge, the counter settling time has to be very short, leading to an extremely high-power design. In fact, it is not practical to guarantee the setup time and hold time.

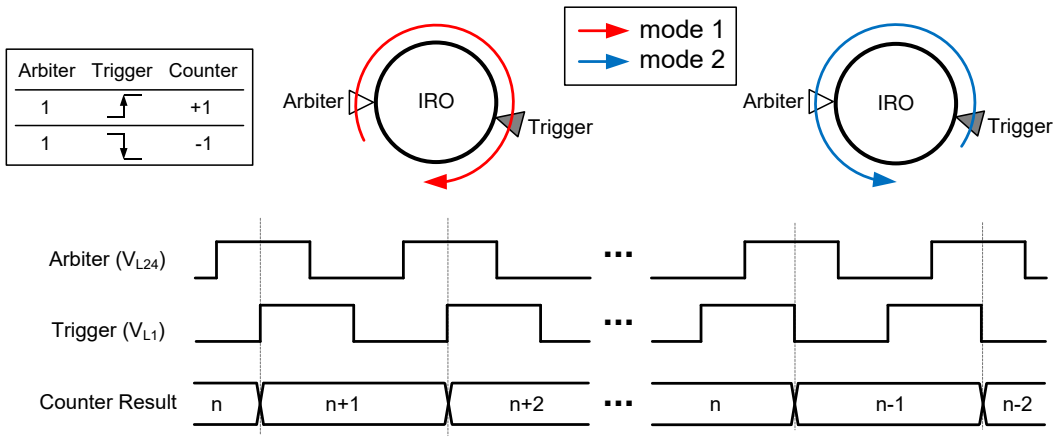


Figure 4-32 Wrap counter truth table and timing diagram of ± 1 counting.

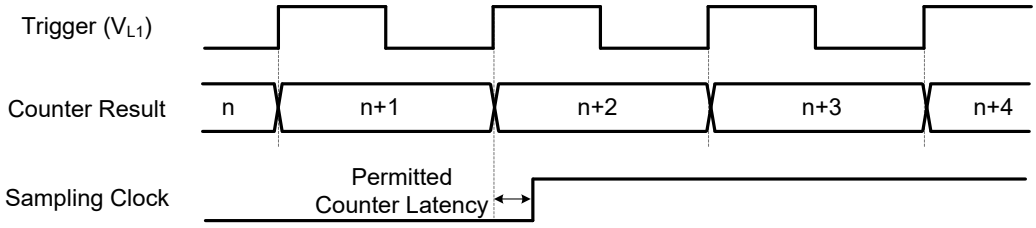


Figure 4-33 Timing challenge in asynchronous count-and-read operation.

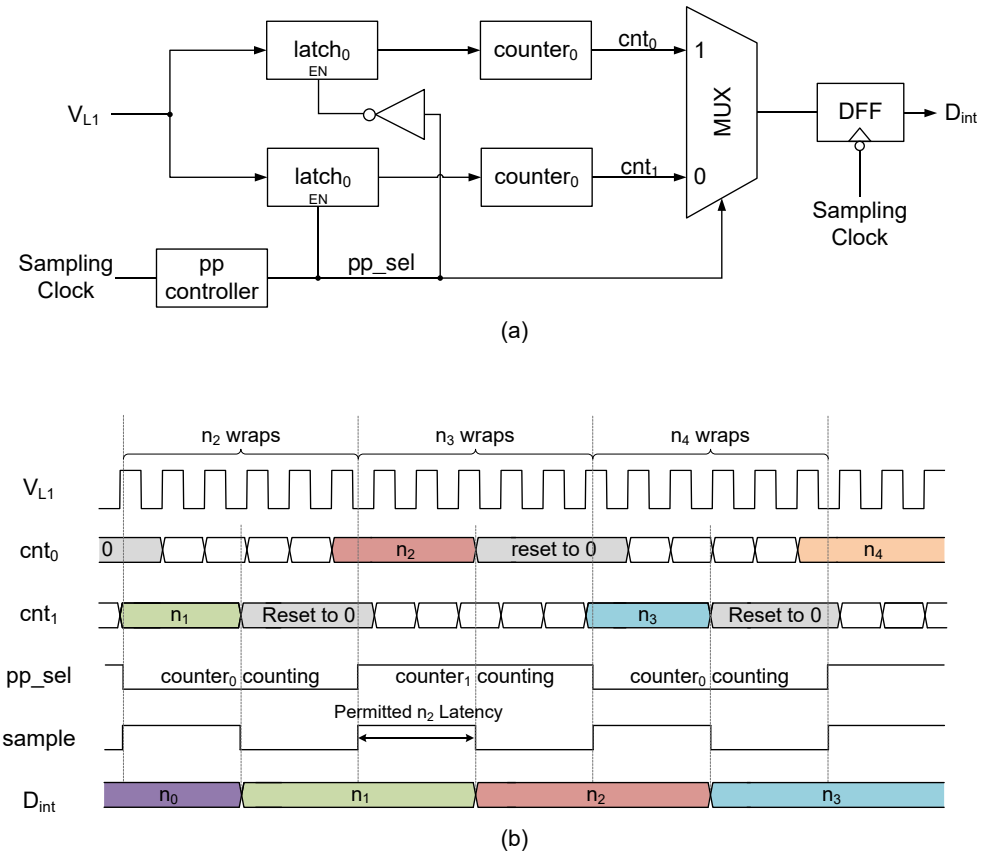


Figure 4-34 (a) Structure and (b) timing diagram of the ping-pong counter.

In this prototype, a ping-pong counter shown in Figure 4-34 is adopted. The concept of ping-pong operation stems from high-throughput digital circuit design. The idea is to feed the input alternatively into two or more parallel paths with identical function, in order to achieve a high-throughput design using the low-throughput paths. Similar concept is used in time-interleaved ADCs for high sampling rate. The idea is adopted in this design to permit enough stabling time for the counters. Figure 4-34(a) shows the conceptual structure of the ping-pong counter. Two latches are used to split the trigger signal which is fed alternatively into two counters. A multiplexer determines which counter output is used for each sampling event. A ping-pong controller decides the operation sequence through toggling *pp_sel*. Figure 4-34(b) shows an exemplary timing diagram to explain its operation. When *pp_sel* = 0, latch_0 is transparent and latch_1 is holding a constant output, so counter_0 is counting and counter_1 is holding its result. Until the next sampling edge arrives and *pp_sel* toggles, counter_0 outputs the counting result (e.g., n_2) of a complete cycle, and counter_1 takes over the counting of the next cycle. This result is held and selected by the multiplexer. At the next falling edge of the sampling clock, it is transferred to the output port, D_{int}, representing the integer phase increment. Each counter is reset to 0 after being read, and ready for the next measurement cycle. For each counter, the permitted settling time before readout is permitted is about $0.5T_s$ (2.5 ns for a 200 MHz sampling rate). Therefore, setup time and hold time can be easily guaranteed.

The final TDC output, D_{out}, is simply the combinition of fractional and integer phase increment results,

$$D_{out} = D_{int} \times 94 + D_{frac}. \tag{4-42}$$

4.6 Experimental Results

The proposed IRO-TDC is fabricated in a 65 nm CMOS process with an active area of 280 μm × 330 μm. Figure 4-35(a) depicts a microphotograph of the prototype chip. Figure 4-35(b) provides the details of the total 13.2 mW core power consumption from a 1.4 V supply. A 1.8 V digital output level shifter is designed for robust transmission of D_{out} to

the external logic analyzer. A significant portion of 47 % (6.24 mW) of total power consumption is drawn by the comparators in the phase processor.

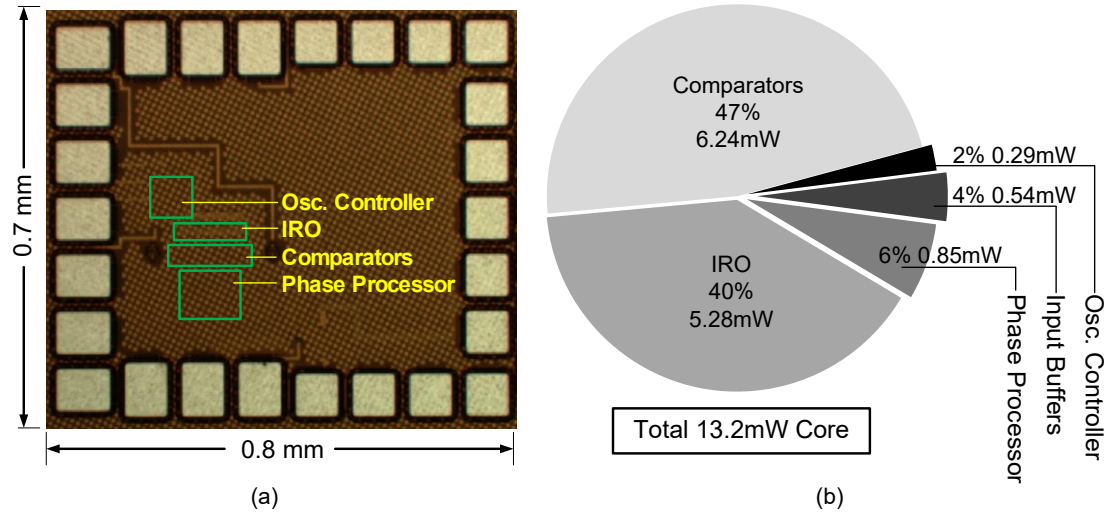


Figure 4-35 (a) Microphotograph and (b) power consumption of the IRO-TDC prototype.

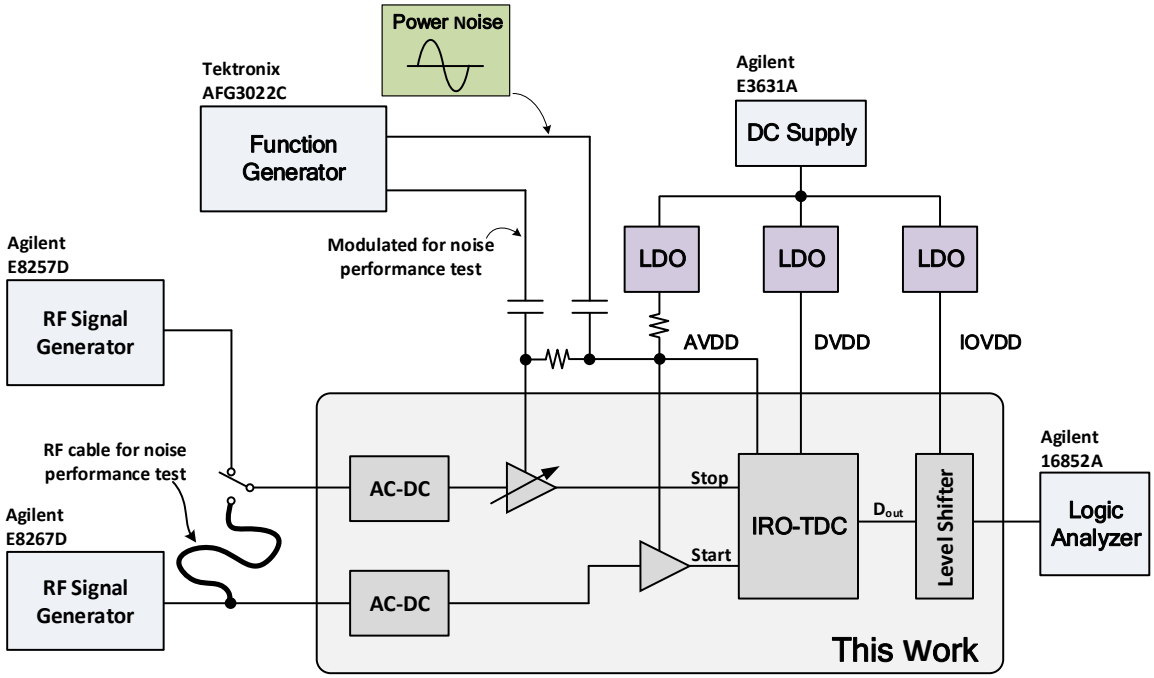


Figure 4-36 Testbench for IRO-TDC.

Figure 4-36 illustrates the testbench used to characterize the prototype TDC. To mimic a standard SoC scenario, three independent supplies, *AVDD*, *DVDD* and *IOVDD*, are provided by LDO regulators. Measurements for this work include a dead-zone test

(comprising a static test and a large-signal dynamic test), a small-signal dynamic test for noise performance, and a phase noise cancellation test. Depending on the test, the *Stop* signal is applied either by another RF signal generator or by a split signal from the same source of the *Start* signal. During all these tests, the sampling rate (i.e., the frequency of *Start* signal) is 200 MHz.

4.6.1 Dead-Zone Test

According to our previous analysis, the phase skew may cause dead-zones in the DC transfer characteristic if the sweeping is slow enough. To characterize the dead-zone performance, the *Stop* signal is applied by another RF signal generator. The frequency of *Stop* signal is 150 Hz lower than the *Start* signal in order to generate a slow ramp input. The captured TDC output sequence is then filtered by the 3 MHz digital low-pass filter (LPF). Figure 4-37(a) provides the DC transfer characteristic. Figure 4-37(b) is a zoom-in view of Figure 4-37(a), showing the dead-zone at $D_{out} = 0$ with a width of about 20 ps. Calculated least significant bit (LSB) from the DC transfer characteristic is 8.43 ps.

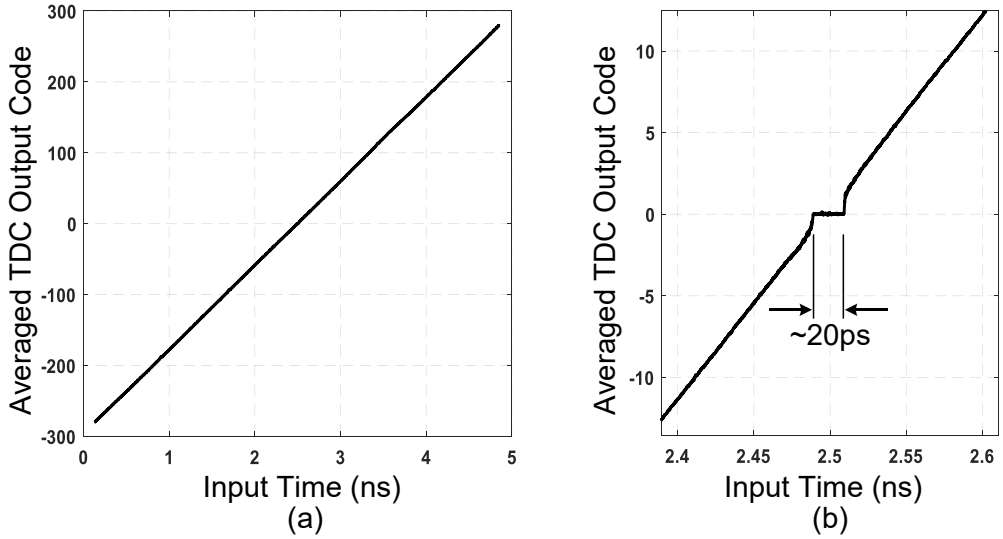


Figure 4-37 Static test results showing (a) DC transfer characteristic and (b) the widest dead-zone near TDC output code = 0.

According to our discussions in Section 4.4.4, the dead-zone of an IRO-TDC should be smaller than a GRO-TDC. However, the measured dead-zone is wider than the

simulated result. This is mostly because of the fractional quantization error, as discussed in Section 4.5.2.

Dead-zones are predicted to disappear if the phase increment is scrambled adequately. A large signal with higher frequency can be applied in order to verify this prediction as well as the TDC operation under a large-scale input. Figure 4-38(a) plots the TDC output when a 100 kHz input is applied with 2.5 ns_{pp} sinusoid (limited by equipment) in addition to a 2.67 ns offset. The phase of the *Stop* signal in this test is modulated. This input signal is about 50 % full scale of the TDC input range. Figure 4-38(b) shows a zoom-in view of the TDC output near $D_{out} = 0$, where a dead-zone was found in the DC transfer characteristic. Under such an adequate scrambling, the dead-zone disappears because the phase locking process fails to converge. In fact, no dead-zone was observed during this test.

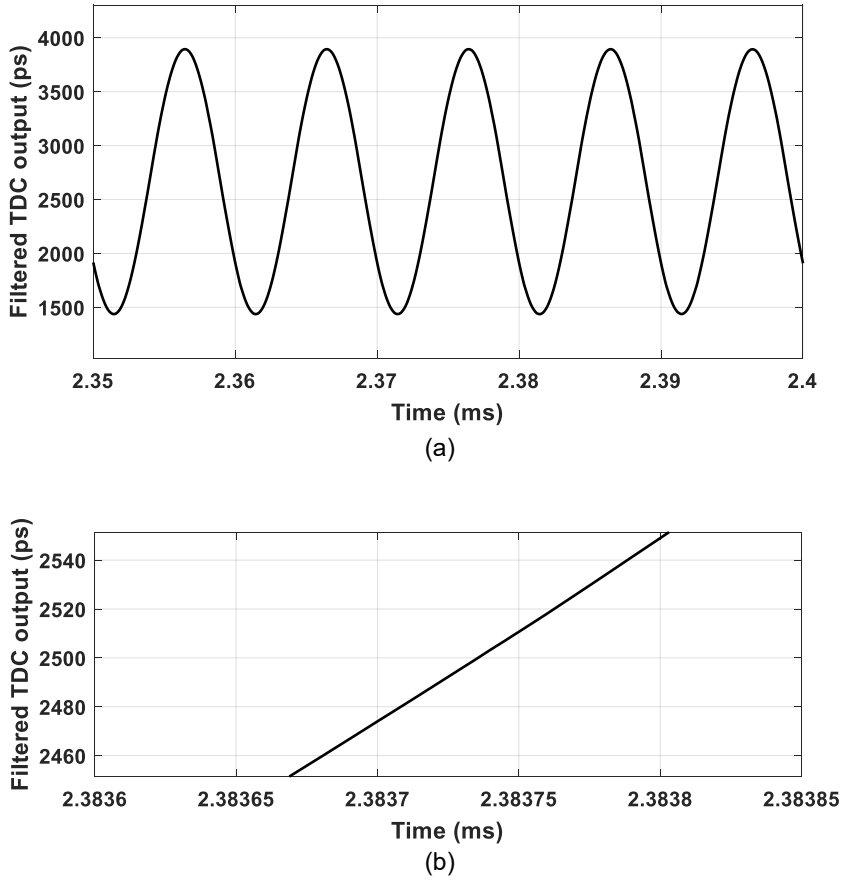


Figure 4-38 A 3 MHz-filtered time domain IRO-TDC output for a 100 kHz, 2.5 ns_{pp} input signal with ~ 2.67 ns offset, showing (a) the output waveform and (b) a zoom-in view near the widest dead-zone.

4.6.2 Noise Performance Test

For ADC measurement, a full-scale sinusoidal input signal is applied, and the output is analysis to evaluate the noise performance. However, it is difficult to generate a time domain large-amplitude sinusoidal input signal that spans the entire TDC range. Moreover, the linearity of a time domain large signal that can be generated from an equipment is usually poor at a 200 MHz frequency. For example, if a clock with phase modulation with 5 ns peak-to-peak amplitude is used as the Stop signal, such a large amplitude phase modulation has large distortion (i.e. large harmonic tones and large jitter) due to the limited equipment resolution. Therefore, a small signal is commonly used to characterize the noise performance of a noises-shaping TDC [69]-[71], [78], [83]-[85], [86].

The testbench in Figure 4-36 is used for the small-signal test. The *Start* signal is split into two, one of which is delayed through an RF cable to generate input offset. This delayed signal is further modulated by a delay buffer and used as the *Stop* signal. This removes the impact of input jitter from the equipment since both clocks are generated from the same clock source. After collecting the output data, we can examine the output sequence in both the time and frequency domain.

Figure 4-39 shows both the measured frequency and time domain output with a 100 kHz input of 1.8 ps_{pp} sinusoid in addition to an offset of 2.76 ns. In Figure 4-39(a), the 65,536-point fast Fourier transform (FFT) is performed with a Hanning window on 16 sequential collects, and averaged to obtain the double-sided PSD plot. The measured PSD is in good agreement with the theoretical profile of IRO phase noise contribution at lower frequencies. The integrated noise up to 3 MHz is 196 fs_{rms}, implying an equivalent resolution of 679 fs. If the bandwidth is reduced to 1 MHz, the measured integrated noise is reduced to 145 fs_{rms}, implying an equivalent resolution of 502 fs. The actual quantization noise is higher than calculated because of the adopted phase quantizer, as explained in Section 4.5.2. As can be seen in the noise PSD, even though a poor phase quantization does not affect the in-band noise, a wider bandwidth can be expected if more accurate quantization is adopted. By looking at the filtered time domain output after a 3 MHz digital

LPF in Figure 4-39(b), the TDC is clearly able to resolve a 1.8 ps_{pp} signal, whereas a classical Vernier TDC with a quantization step of 679 fs would struggle owing to the lack of quantization noise scrambling.

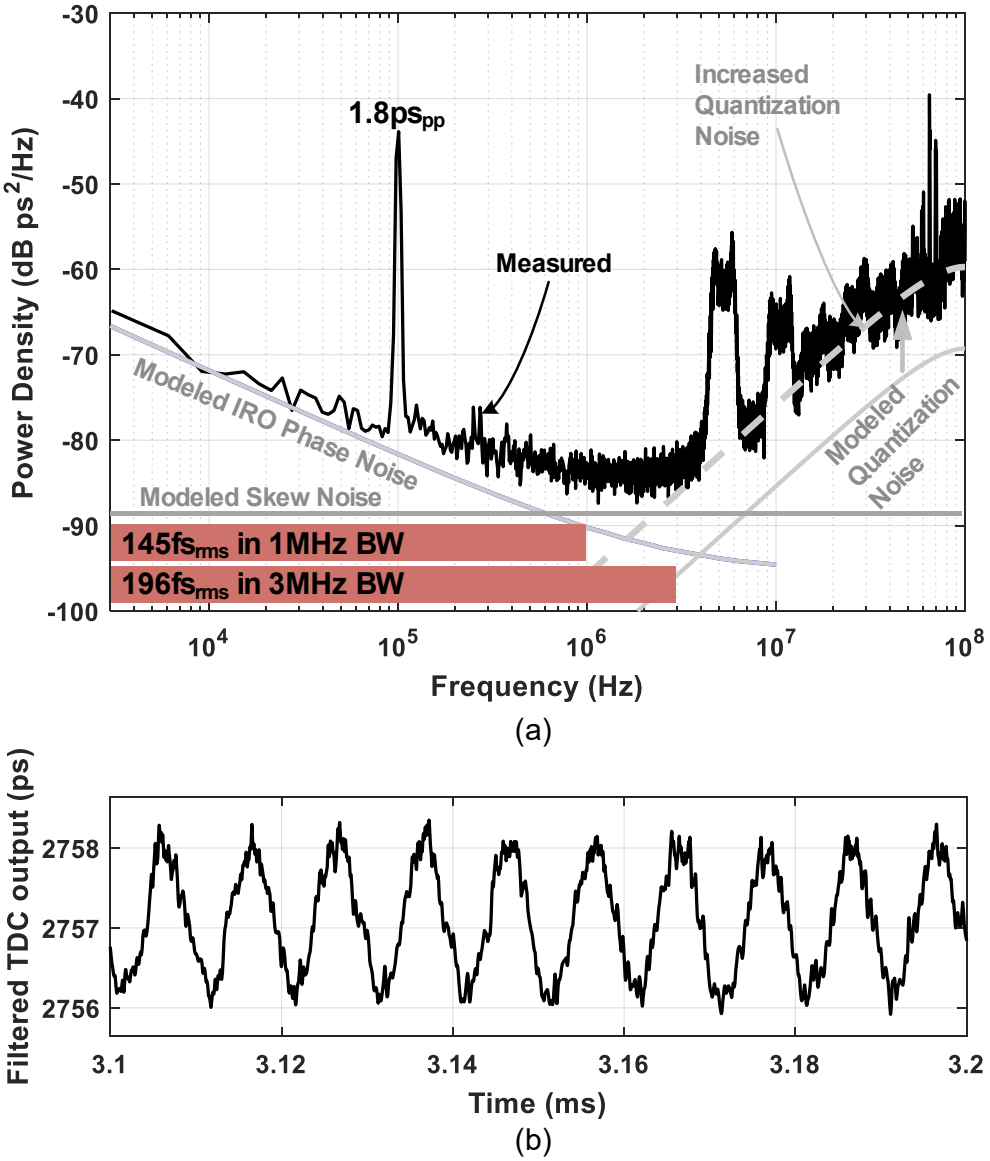


Figure 4-39 Measured IRO-TDC output for a 100 kHz 1.8 ps_{pp} input signal with ~ 2.76 ns offset, showing (a) a double-sided PSD and (b) time domain output after a 3 MHz digital LPF.

Table 4-6 lists the simulated and calculated TDC noise for comparison. The calculated total in-band noise is approximately 122 fs_{rms} within 1 MHz bandwidth and 166 fs_{rms} within

3 MHz. The difference between measured and calculated noise is caused by jitters of the signal splitter, external RF cable, input buffer, and pulse generator.

When this IRO-TDC is applied in a digital PLL, (4-2) can be used to estimate its contribution to PLL in-band phase noise based on the measured TDC noise. By using a DC input, the TDC noise profile can be obtained. This profile is very close to the one in Figure 4-39(a). Figure 4-40 shows its calculated contribution to PLL in-band phase noise with an output frequency of 3 GHz. Due to the wide TDC signal bandwidth, the PLL bandwidth can be configured within a large range of 3 MHz.

Table 4-6 Simulated and Calculated Results of IRO-TDC In-Band Noise

Characteristics	**Noise in 3 MHz BW (fs_{rms})**	**Noise in 1 MHz BW (fs_{rms})**
Skew noise, $\sigma_{skew,rms}$	100	58
Oscillator noise, $\sigma_{PN,rms}$	116	106
Increased quantization noise, $\sigma_{QE,rms}$	~ 65	~ 13
Calculated total noise	~ 166	~ 122
Measured total noise	196	145

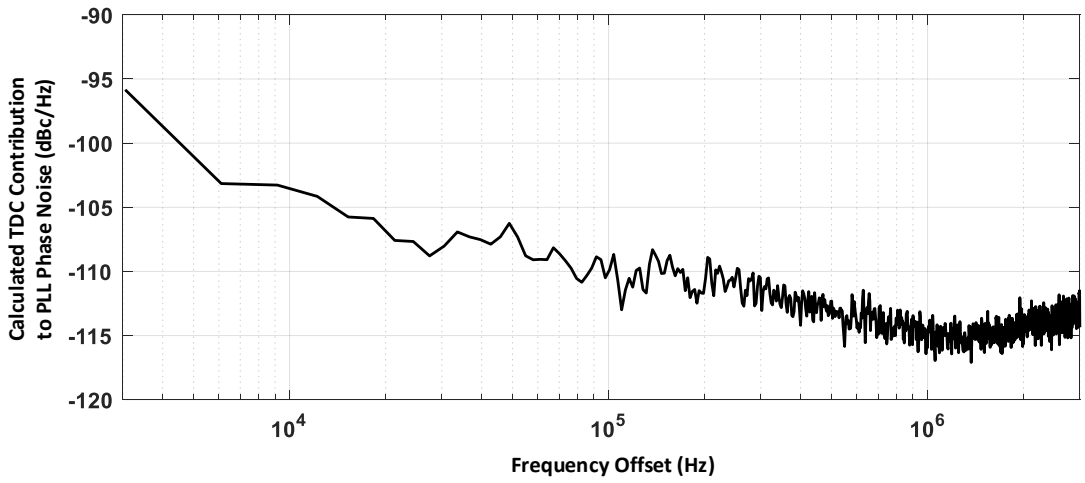


Figure 4-40 Calculated TDC contribution to a 3 GHz PLL output phase noise (without considering PLL bandwidth).

4.6.3 Phase Noise Cancellation Test

A unique feature of the IRO-TDC is the capability of coherent phase noise cancelling. To verify this function, coherent phase noise can be added to the TDC intentionally. Noise from power supply is one of the sources of coherent phase noise, and it can be easily generated and applied to the prototype.

During this test, a sinusoidal signal is injected into AVDD to mimic power supply noise. In order to identify the impact of the injected noise and to ensure sufficient current supply, the LDO is kept as in the small signal test. The *Stop* signal is AC-modulated with 10.8 ps_{pp} to monitor whether the measured signal power will be affected by the noise cancellation. According to (4-40), the *Stop* signal offset can be controlled to obtain different PNRR. The IRO is predicted to exhibit some PNRR when $0 < T_{in}/T_s < 1$, and nearly no cancellation when $T_{in}/T_s \to 0$ or 1. As an example, Figure 4-41 shows this difference between strong cancellation (T_{in}/T_s is about 0.48) and very weak cancellation (T_{in}/T_s is about 0.96) with a 50 kHz power noise, in which a 25 dB noise cancellation is clearly seen and the wanted signal is not affected.

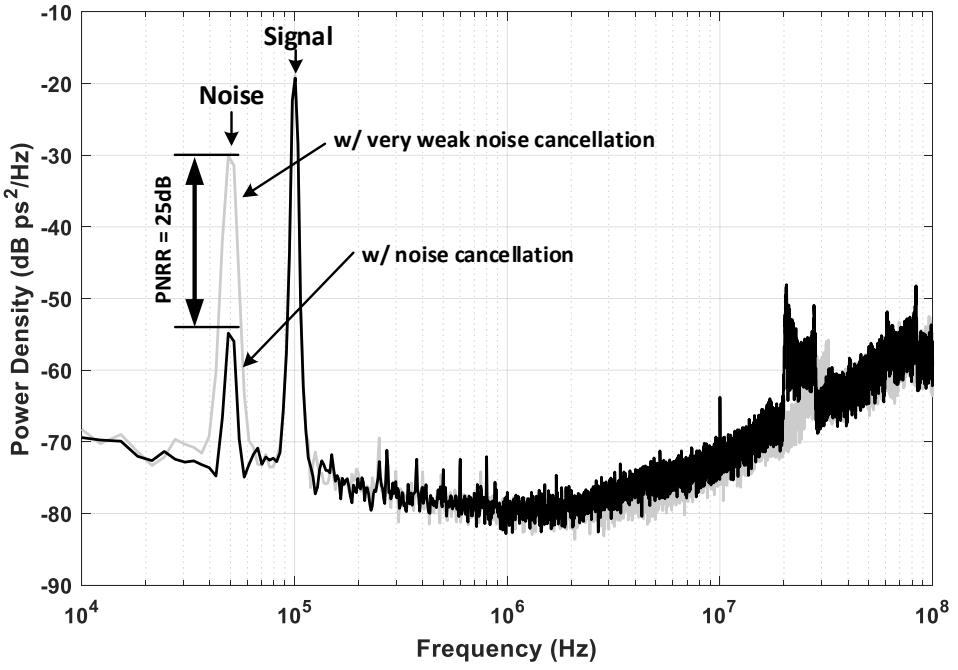


Figure 4-41 PNRR obtained from PSD comparison between outputs with strong and very weak noise cancellation.

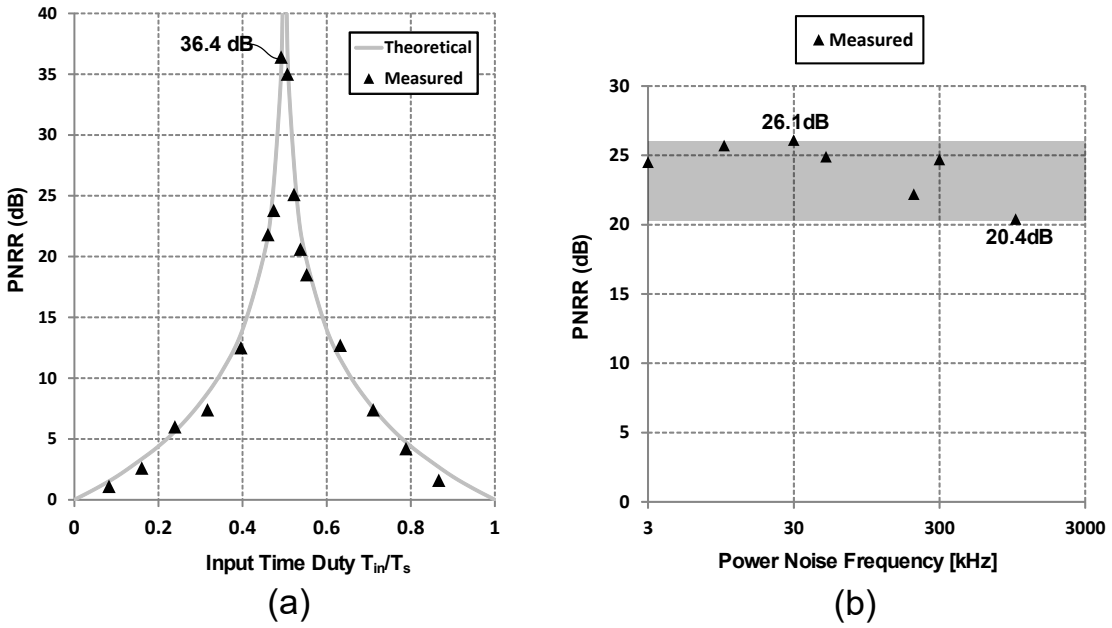


Figure 4-42 Measured PNRR under (a) different T_{in}/T_s and (b) different noise frequencies.

If *Stop* signal is completely not applied to the TDC, it would be $T_{in}/T_s = 1$, implying no cancellation at all. By definition, the PNRR should be obtained through comparing the output with this setting and the output with certain T_{in}/T_s values. In this way, however, we cannot see whether the wanted signal is affected because there is no input signal at all if *Stop* is not applied. In fact, the PNRR obtained through this way is quite close to the comparison results obtained by using a weak cancellation (i.e., $T_{in}/T_s \approx 0.96$) since the PNRR at $T_{in}/T_s \approx 0.96$ is merely 0.7 dB.

Figure 4-42 illustrates the PNRR performance under different conditions. Figure 4-42(a) plots the PNRR with different T_{in}/T_s. The measured PNRR agrees well with the calculated results from (4-40). A maximum PNRR of 36.4 dB is observed at $T_{in}/T_s = 0.4918$. For digital PLLs, a digital offset can be used to bias the input time to IRO-TDC for maximum PNRR. Figure 4-42(b) shows the PNRR performance within the signal bandwidth, in which the power noise frequency is swept from 3 kHz to 800 kHz. Power noise injection at higher frequencies was not performed due to the strong attenuation by the capacitors and power supply. Measured PNRR ranges from 20.4 dB to 26.1 dB across the testing frequencies. At higher frequencies (e.g., 800 kHz), the noise injection is affected by

on-chip decoupling capacitors, resulting in a larger deviation from the calculated PNRR. In fact, during this test, the noise amplitude at high-frequency injection is $7\times$ larger than that in lower frequencies. This reveals that high-frequency power supply noise is easily attenuated and should have little impact to the TDC noise. Since the coherent phase noise is added through the power supply, PNRR obtained from this test can also be regarded as power supply rejection ratio (PSRR).

Performance of the prototype is summarized and compared with state-of-the-art noise-shaping TDCs in Table 4-7. Except for the GRO measured with a small T_{in} offset of 1.6 ns, the proposed IRO-TDC achieves the lowest integrated noise in a large signal bandwidth of 3 MHz using a moderate sampling frequency. Moreover, a unique in-band noise cancellation of up to 36.4 dB PNRR is achieved in the IRO-TDC. Due to this PNRR, the TDC can be protected from coherent noises such as power supply noise, ground noise, substrate noise, etc. For example, in this test, the PNRR can be regarded as PSRR which can protect the TDC from power supply noise. Note that the voltage comparators in the phase processor account for 6.24 mW (47%) of the total power consumption. This power can be reduced in future design using a phase processor with a more digital sense, such as the phase quantizer in [70]. Although the power consumption is not optimized in this work, the IRO-TDC draws constant supply current and generates little interference to the power supply. Accordingly, a friendly power supply interface is provided in this IRO-TDC.

Table 4-7 Comparison with Other Start-of-the-Art Noise-Shaping TDCs

Design	[70]	[75]	[78]	[79]	[83]	[86]	This work	
Process (nm)	130	90	65	130	90	65	65	
Oscillator Type	GRO	2D-GRO	GRO MASH	Relax. Osc.	SRO	GSRO	IRO	
Area (mm^2)	0.04	0.027	0.03	0.11	0.02	0.05	0.09	
Sampling Rate (MS/s)	50	25	150	50	500	200	200	
Input range (ns)	12.3 [1]	40	5.4	20	12.5	4	5	
BW (MHz)	1	0.8	15	0.1	1	4	3	1
$\sigma_{TDC,rms}$ (fs)	80 [3]	924 [3]	760	1616 [2]	315	455	196	145
Resolution (ps)	0.28 [3,4]	3.2	2.64	5.6	1.09 [4]	1.58	0.68	0.5
Power (mW)(4)	21 [3]	3.6	3.52	1.7	2	4.26	13.2	
Supply current	Varying	- [5]	- [5]	- [5]	Const. [6]	Varying	Const.	
ENOB	15 [3]	14	11	12	13	11	13	
TDC FoM (dB) [7]	171 [3]	167	164	151	170	160	163	161
Coherent noise cancellation (dB)	No	No	No	No	No	No	Up to 36.4	

[1] with 6 ps raw resolution and 11 bit range.

[2] Estimated $\sigma_{TDC,rms} = \sqrt{Resolution^2/12}$.

[3] Depends on input value, T_{in}.

[4] Estimated resolution $= \sqrt{{\sigma_{TDC,rms}}^2 \times 12}$.

[5] Not mentioned.

[6] Pseudo-differential structure.

[7] TDC FoM = $20\log_{10}$(Input range rms/$\sigma_{TDC,rms}$) + $10\log_{10}$(BW/Power) [dB].

4.7 Summary

In this chapter, in-band noise performance limitation of the digital PLL has been reviewed and the importance of the TDC has been emphasized. TDCs based on controlled oscillators have the potential of achieving low in-band noise and have been selected to be investigated

and optimized in our research. This chapter has reported our effort in reducing the in-band noise by introducing an IRO technique to this TDC family.

4.7.1 Achievements

Achievements in this chapter are listed below.

- A novel IRO technique has been proposed to further reduce in-band noise of the controlled oscillator-based TDCs.
- A noise model for noise analysis of GRO-, SRO-, and IRO-TDCs has been established for a systematic summary of the controlled oscillator-based TDC family and for future researches.
- An IRO-TDC prototype has been designed and implemented. Multi-path structure has been adopted for the IRO to reduce skew error.
- The in-band noise reduction and coherent noise cancellation have been verified with measurement results of the IRO-TDC prototype. An integrated noise of 196 fs_{rms} within a 3 MHz bandwidth has been achieved, with a coherent PNRR of up to 36.4 dB. Integrated noise reduces to 145 fs_{rms} if bandwidth reduces to 1 MHz.

At last, the IRO-TDC has been proved to be capable of reducing in-band noise and rejecting coherent noise. Such features will be helpful to digital PLLs. To our knowledge, this is the first demonstration that utilizes oscillation inversion to reduce impact of oscillator phase noise.

Except for the customized delay cells and the differential controller buffer, the whole IRO-TDC prototype can be implemented with the help of automatic tools and digital flow. Design and verification of the proposed IRO-TDC can take advantages of the development of these tools in future advanced CMOS technologies.

In CMOS processes with even smaller feature size, the stage delay will be even smaller. This will result in an even lower quantization noise. Delay mismatch will be increased with smaller feature size, resulting in an increased mismatch noise. However, as explained in Section 4.4.2, this mismatch noise is high-pass shaped and has negligible impact to the TDC in-band noise performance.

4.7.2 Possible Drawbacks and Mitigations

Fractional Quantizer

As mentioned in Section 4.5.2, a fractional quantizer with many comparators is used in the prototype for measurement purpose. This quantizer structure imposes increased quantization error, wider dead-zones, and power consumption overhead. Fortunately, dead-zones can be avoided in normal digital PLL operation. Even though the power consumption is not low, the supply current is constant and the disturbance to power supply is negligible. Most importantly, the increased quantization error does not degrade in-band noise. However, the raised quantization noise profile does reduce the signal bandwidth of the TDC. When applied to digital PLL, this will affect the total bandwidth of the TDC and the digital PLL. Besides, large amount of supply current is drawn by the comparators.

In order to increase bandwidth and reduce power dissipation, future researches are recommended to investigate purely digital fractional quantizers.

IRO Power Consumption

In order to compare with the GRO in [70], a 47-stage multi-path IRO is used in the prototype. In future IRO designs, the power consumption can be reduced by using simpler implementation with fewer stages, at the cost of increased quantization noise and perhaps higher skew noise. Therefore, signal bandwidth may be reduced accordingly. Future designers can modify the IRO structure for different power consumption and signal bandwidth specifications.

Phase Skew Error

A multi-path structure is employed in our IRO prototype to reduce phase skew error. However, this can be further reduced for even lower in-band noise. Automatic routing and coupling between difference nodes are the main reasons for this error. For future designs, other IRO implementations with smaller phase skew can be investigated.

5 Conclusions and Recommendations

5.1 Conclusions

In this thesis, we have reviewed some PLL fundamentals and CMOS technology development and presented our anticipation that analog PLLs are preferable in future SiP technologies and digital PLLs are more suitable for future SoC technologies. Accordingly, we have introduced, analyzed, and demonstrated two in-band phase noise reduction techniques, including a PS-SS technique for analog PLL and an IRO-TDC technique for digital PLL. Two research works have been reported in this thesis.

In the first work, we aimed to propose techniques to achieve low in-band phase noise in analog PLLs and to eliminate the need for the time-consuming calibration in prior fractional-*N* SSPLLs. A calibration-free PS-SS technique was proposed for fractional-*N* operation. For quantitative analysis, a phase model was established to predict and to optimize the PLL phase noise. To verify the calibration-free low-noise operation, a PS-SSPLL prototype was designed, implemented, fabricated, and measured. The key requirement of this technique is the multi-phase feedback from the VCO. To guarantee short settling time, a VCO+divider structure was adopted in our prototype. As a side benefit, an eight-phase output was provided from the PLL. Measurement results showed that the PS-SSPLL required no calibration to operate. Under the calibration-less test condition, the PS-SSPLL achieved the best jitter performance, phase noise performance and FoM compared with other state-of-the-art fractional-*N* SSPLL works.

In the second work, we aimed to provide TDC techniques to reduce in-band phase noise of digital PLLs. Since TDC noise is the major contributor to the digital PLL in-band noise, we proposed a low-noise IRO-TDC technique. For a systematic comparison and summary, a noise model was established for GRO-, SRO-, and IRO-TDC analysis. In-band noise of this TDC family is limited by the oscillator phase noise. To our knowledge, the proposed IRO is the first demonstration of utilizing oscillation inversion to reduce the

impact from oscillator phase noise. An IRO-TDC prototype was designed, fabricated, and measured to verify the low-noise characteristics. Measurement results showed that the IRO-TDC has the capabilities of in-band noise reduction and in-band coherent noise cancellation. Besides, the IRO-TDC has a reduced disturbance to power supply. With all these features, the IRO technique was proved to be compelling in reducing in-band phase noise of a digital PLL. For TDCs based on more sophisticated controlled oscillators in future, the proposed noise model can be further revised accordingly for noise performance optimization.

5.2 Recommendations for Future Research

In-band phase noise performance of PLLs is becoming increasingly important for wireless communications. The advanced CMOS technologies empower both analog and digital PLLs to be important players in diverse applications and products. Reduction of PLL in-band phase noise is an exciting and profitable area for future research. Based on the proposed techniques in this thesis, the area that merits future works is discussed below.

On the Propose PS-SS Technique

Similar to a prior RS-SS technique, the proposed PS-SS technique tries to align the feedback clock and the reference clock. To perform such an alignment, either the phase of feedback clock or the phase of reference clock needs to be adjusted. The core idea of the proposed PS-SS is to obtain the phase shifting steps directly from the VCO rather than from other signal sources such as a calibrated DTC in RS-SS. Since the phase shifting steps are inherently related to VCO phase, a PS-SS radically eliminating the calibration. There are many approaches to generate such phase shifting steps. Although a VCO+divider structure is successfully used in our prototype, future designs can also choose other approaches. For example, quadrature VCO or ring VCO can be adopted in future designs to provide the multi-phase feedback signal.

However, when choosing the means to generate multi-phase feedback, designers are recommended to consider power consumption and area overhead. For example, in much higher output frequencies such as 10 GHz, it is not worthwhile to use VCO+divider structure because a 40 GHz VCO and two frequency dividers at 40 GHz and 20 GHz require very high power consumption. Other lower-power methods should be adopted for such scenario.

In short, the proposed PS-SS technique suggests future designs to generate the phase shifting steps directly from VCO phase, so that calibration is no longer needed and the PLL with low in-band noise can be adopted in more applications.

On the Propose IRO Technique

The concept and model we proposed in IRO-TDC can be extended in future designs in many aspects.

Firstly, the core idea of IRO is to maximize the TDC gain, so that the input-referred noise can be reduced. This concept can be extended to other fields as long as modulation is involved, as illustrated in Figure 5-1. In general, in this structure, a modulator converts an input parameter (e.g., α) into an internal parameter (e.g., β), and a subsequent processor operates based on parameter β and generates an output. Impact of the processor internal noise can be reduced by maximizing the gain from α to β. With the same amount of noise or error in the subsequent processor, a larger gain can reduce the input-referred noise. In order to obtain a large difference of β, we can simply change its polarity rather than its absolute value (i.e., its amplitude).

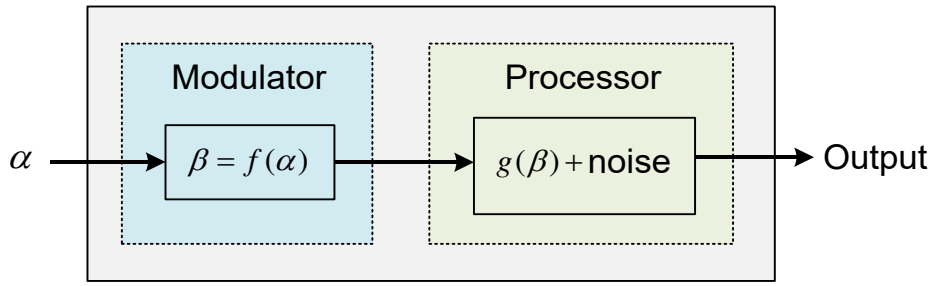


Figure 5-1 Concept of data processing with modulation.

In terms of an XRO, α is the input time and β is the oscillator frequency. An IRO provides two oscillation frequencies of $+\omega_0$ and $-\omega_0$, achieving a large difference of $2\omega_0$ for this varying parameter. Thus, impact of phase domain noise, such as oscillator phase noise, can be reduced. In some hardware, changing only the polarity of a parameter has little impact to other properties. In our IRO case, the power consumption is kept constant.

Secondly, the noise model proposed for XRO-TDC can be used in future designs in controlled oscillator-based TDC family. For example, for TDCs based on more complicated oscillators such as GSRO or other combination of GRO, SRO, and IRO, the model can be modified accordingly for noise prediction and design optimization.

Thirdly, similar to the GRO development, the IRO implementation should not be limited to ring oscillators. Other oscillator structures such as charge-pump oscillators, relaxation oscillators, and even LC oscillators are possible substitutes in IRO-TDCs.

Lastly, from a mathematical point of view, the proposed IRO realizes another important transformation from time domain to phase domain. In XRO-TDCs, the physical parameter being modulated is the instantaneous oscillator frequency, $\omega(t)$. It can be expressed as

$$\omega(t) = x(t)\omega_0. \tag{5-1}$$

Hence, the XRO is actually modulating factor $x(t)$. Let us denote the first mode of all XROs as $x(t) = 1$. A GRO provides $x(t) = 0$ in the other mode, implying a direct time-to-phase conversion that can add with previous phase. An SRO has an $x(t)$ of 0~1 in the other mode, implying a time-to-phase conversion with a controllable scaling factor. An IRO can set $x(t) = -1$, implying a subtraction in the time-to-phase conversion. Table 5-1 summarizes these mathematical operations. If a more complicated oscillator combines the functions of GRO, SRO, and IRO, in principle, it can transform time information into phase domain with all these inherent operations. By doing this, a much more sophisticated process in time domain is possible. Functions provided by these

oscillators are helpful to future time domain data processing, especially in future finer technologies where time resolution and noise performance can be continuously improved.

Table 5-1 Mathematical Operations in Time-to-Phase Conversions in GRO, SRO, and IRO

XRO Type	**Mode 1**	**Mode 2**	**Operation in Time-to-Phase Conversion**
GRO	$x(t) = 1$	$x(t) = 0$	Direct Conv./ Addition
SRO		$x(t) = 0{\sim}1$	Scaling
IRO		$x(t) = -1$	Subtraction

Author's Publications

Journal Papers:

1. **Zhipeng Liang**, Xiang Yi, Kaituo Yang, Chirn Chye Boon, "A 2.6-3.4 GHz fractional-*N* sub-sampling phase-locked loop using a calibration-free phase-switching-sub-sampling technique," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 2, Feb. 2018.
2. Xiang Yi, Chirn Chye Boon, Guangyin Feng and **Zhipeng Liang**, "An eight-phase in-phase injection-coupled VCO in 65-nm CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 3, pp. 299-301, March 2017.
3. X. Quan, X. Yi, C. C. Boon, K. Yang, C. Li, B. Liu, **Z. Liang**, Y. Zhuang, "A 52–57 GHz 6-bit phase shifter with hybrid of passive and active structures," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 3, pp. 236-238, March 2018.
4. F. Meng, D. Disney, B. Liu, Y. B. Volkan, A. Zhou, **Z. Liang**, L. Selvaraj, L. Peng and C. C. Boon, "Heterogeneous integration of GaN and BCD technologies and its applications to high conversion-ratio DC-DC boost converter IC," *IEEE Transactions on Power Electronics*, accepted.

Patent:

1. **Z. Liang**, C. C. Boon, X. Yi and J. S. Kee, "Time-to-digital converter," U.S. Patent, filed May 25, 2018. NTU ref: 2018-009-04-US.
2. **Z. Liang**, C. C. Boon, X. Yi and J. S. Kee, "時間至數位轉換器," China Patent, applied May 25, 2018. NTU ref: 2018-009-02-CN.
3. **Z. Liang**, C. C. Boon, X. Yi and J. S. Kee, "Time-to-digital converter," Singapore Patent, filed March 27, 2018. NTU ref: 2018-009-01-SG.

Conference Papers:

1. Xiang Yi, **Zhipeng Liang**, Guangyin Feng, Chirn Chye Boon and Fanyi Meng, "A 93.4-to-104.8 GHz 57 mW fractional-N cascaded sub-sampling PLL with true in-phase injection-coupled QVCO in 65 nm CMOS," *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, 2016, pp. 122-125.
2. Xiang Yi, **Zhipeng Liang**, Chirn Chye Boon, "A 20.2-57.1 GHz inductor-less divide-by-4 divider chain," presented at the *Progress in Electromagnetic Research Symposium (PIERS)*, Singapore, 2017, pp. 1312-1318.
3. Xiang Yi, Kaituo Yang, **Zhipeng Liang**, *et al*., "A 65nm CMOS carrier-aggregation transceiver for IEEE 802.11 WLAN applications," *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, 2016, pp. 67-70.

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