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Including SMT ferrite beads in DC power bus and high-speed I/O line modeling

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Abstract: Surface mount technology (SMT) ferrite beads are often used in high-speed digital circuit designs to mitigate noise. The common modeling approach is to include SMT ferrite beads as equivalent lumped LCR circuits. The work presented in this paper included SMT ferrite beads as a frequency-dependent impedance in a PEEC-like modeling tool denoted CEMPIE, a circuit extraction approach based on a mixed-potential integral equation formulation. Agreement with measurements demonstrates the approach. The applications shown are segmentation of power areas for noise isolation, and I/O line filtering.

INTRODUCTION

Ferrite materials have a low eddy-current loss at frequencies up to hundreds of mega-Hertz. This unique property makes it very useful for frequency selective attenuation [1]. SMT ferrite beads are often used in high-speed digital PCB design, due to their compact size and easy assembly. For EMC purposes, they can suppress high-frequency noise, while not affecting the low frequency components of the fundamental signal [2].

Mitigating simultaneous switching noise in a DC power bus is critical for a high-speed digital circuit design. Decoupling capacitors are commonly used to bypass the high-frequency noise, preventing it from propagating in the power bus. SMT ferrite beads can be combined with these capacitors to "tune" power bus resonant frequencies [3]. Another practice is using power islands to isolate the high-frequency noise. The typical impedance of a ferrite bead is very low at the low frequencies near DC, but relatively high in the RF range; therefore, it can be used to connect segmented power portions with the same logic level, to provide a DC connection and maintain RF isolation [4]. They are also used for low-pass filtering [5]. For example, placing two ferrite beads in series in an I/O line, and a capacitor between the two and to ground results in a two-pole, low-pass T-filter for the two-conductor transmission line.

SMT ferrite beads are commonly modeled as equivalent lumped circuits. The simplest model is a series LR circuit [1]. However, as shown in Figures 1 and 2, the impedance of a typical SMT ferrite bead cannot be well characterized by a lumped circuit with frequency independent elements over a wide frequency range. Therefore, in this work, a frequency-dependent impedance that results from measurements is included into the full-wave modeling, which handles the DC power bus and I/O line structures, and accounts for the SMT ferrite used in the circuit.

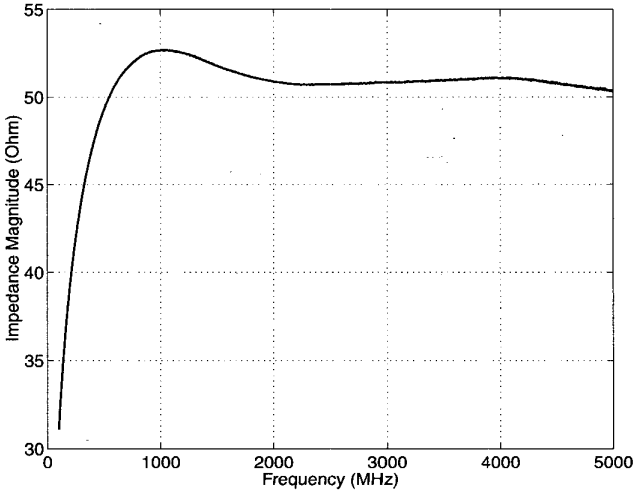

Figure 1: Impedance magnitude of a typical ferrite bead.

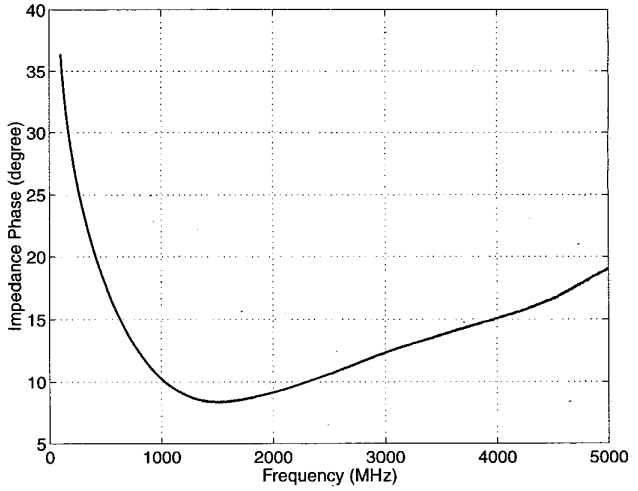

Figure 2: Impedance phase of a typical ferrite bead.

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APPROACH

The full-wave modeling approach used in this work is a mixed-potential integral equation formulation with circuit extraction, denoted CEMPIE. It is an application of the partial element equivalent circuit (PEEC) method in multi-layer dielectric media [6], and very suitable for DC power bus and other multi-layer planar circuit modeling [7], [8].

The CEMPIE formulation is similar to the formulation of classical scattering problems. An incident electric field is assumed, and Green's functions are generated for the multi-layer dielectric media. Conducting surfaces are then replaced by induced surface currents and charges. By enforcing boundary conditions on these conducting surfaces for the vector sum of the incident and induced electric fields, an integral equation results. This equation is discretized and tested using a standard Method of Moments procedure. By further assuming the electric potential over each mesh cell is constant, a final system matrix equation is established as [7]

$$[\mathbf{Y}][\varphi] = -[\mathbf{I}^e], \tag{1}$$

where $[\mathbf{I}^e]$ is the impressed node current vector; $[\varphi]$ is the node scalar-potential vector; and, $[\mathbf{Y}]$ is the system admittance matrix. A SPICE compatible equivalent circuit can then be extracted from (1), and various simulations performed in SPICE.

The approach is not very computationally efficient on both the simulation speed and the storage memory for some simple frequency investigations, such as S-parameter and input impedance. Therefore, a modified approach with an iterative equation solver was introduced in [9]. The system matrix equation (1) is directly transferred to the equation solver without changes. Then, external lumped circuit elements, as well as excitations (sources), are added into the system admittance matrix. Each lumped circuit element or source can be characterized using a simple element admittance matrix and/or a source vector. Most entries of the element admittance matrix and the source vector are zero, except at several special locations, which are related to the circuit nodes where the element or source is connected into the circuit model. If one of the nodes is the common ground node, its corresponding row and column is eliminated. All element admittance matrices corresponding to all externally incorporated lumped circuit elements and sources should be added to (1). Similarly, all source vectors sum up, forming the impressed node current vector. Then, the new system matrix equation becomes

$$[\mathbf{Y}'][\varphi'] = -[\mathbf{I}^{e\prime}]. \tag{2}$$

Note that the number of total circuit nodes may increase after incorporating lumped circuit elements and sources. Then, (2) is solved using an iterative method.

In this study, SMT ferrite beads were measured, and treated as a frequency-dependent impedance. The element admittance matrix could be obtained from the impedance measurement, and was frequency-dependent as well. Then the SMT ferrite beads were included in the modeling by modifying the system admittance matrix at every frequency point. In this fashion, the frequency-dependent behavior of SMT ferrite beads can be well characterized.

MODELING EXAMPLES

Power Plane Segmentation

Two typical structures using SMT ferrite beads were studied. Figure 2 shows the top view of a DC power bus structure with isolated power planes. The top and bottom planes of the PCB represented the power and ground layers, respectively. The ground layer was solid. A zigzag gap separated the power plane completely, and the gapped portions were connected by an SMT ferrite bead. An SMA PCB mount jack was placed in each portion of the power plane. The impedance of the ferrite bead was measured from 100 MHz to 1.8 GHz, using an HP4291A impedance analyzer with an SMT test fixture. The measured results, which are frequency-dependent, were incorporated into the CEMPIE extracted circuit by modifying the system admittance matrix at every frequency point. All other structures, including the power bus and the SMA connector, were modeled using the CEMPIE approach. Figure 3 shows the comparison of the measured and modeled $|S_{21}|$ results between the two test ports. The results agree favorably in the entire frequency range.

I/O Line Filtering

Another test geometry was an I/O line with a T filter. As shown in Figure 4, two SMT ferrite beads and a 47 pF SMT capacitor formed the T filter between two portions of a microstrip trace. The trace width was 2 mm. The impedances of the ferrite beads and the capacitor were measured using an HP8753D network analyzer from 100 MHz to 5 GHz. An SMA fixture was used to measure the SMT devices, and measurement planes were rotated right to the bonding pads of the DUTs (device under test). The CEMPIE approach was applied to the microstrip line, as well as the two test ports, and an equivalent circuit results. The SMT devices were then incorporated into the equivalent circuit by modifying the system admittance matrix. Both the measured and modeled $|S_{21}|$ results between the two test ports are shown in Figure 5. Agreement is demonstrated up to 5 GHz.

CONCLUSION

An approach to include SMT ferrite beads in DC power bus and high-speed I/O line modeling was presented in this paper. The frequency-dependent impedance of an SMT ferrite was measured, and then incorporated into the CEMPIE extracted circuit by modifying the admittance matrix. Examples demonstrated its effectiveness. The approach can be used to model various structures with SMT ferrite beads, and develop guidelines for power-island and noise filtering designs.

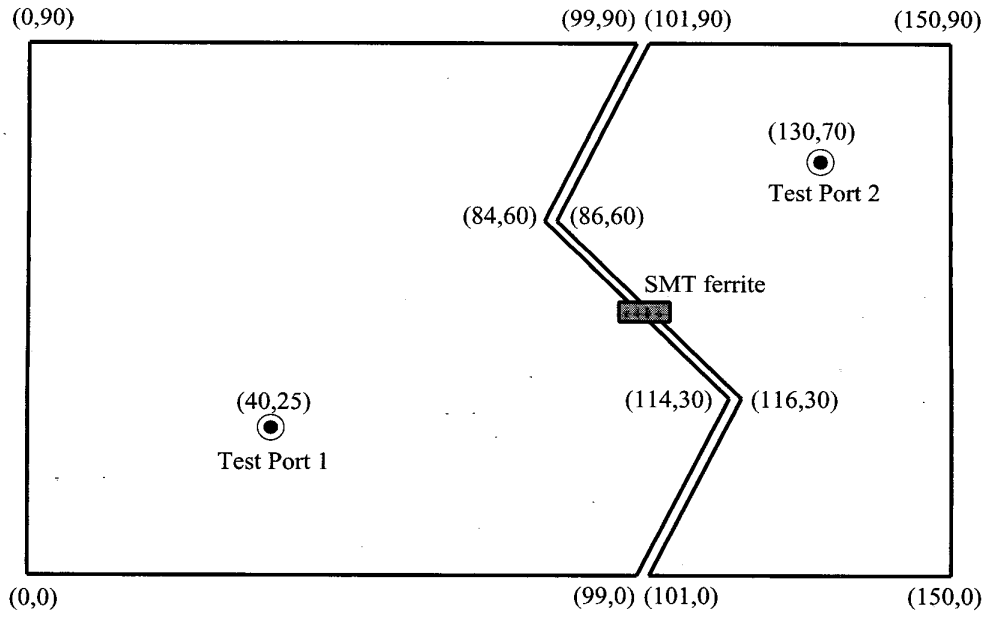

Figure 3: A DC power bus with gapped power plane and an SMT ferrite connection.

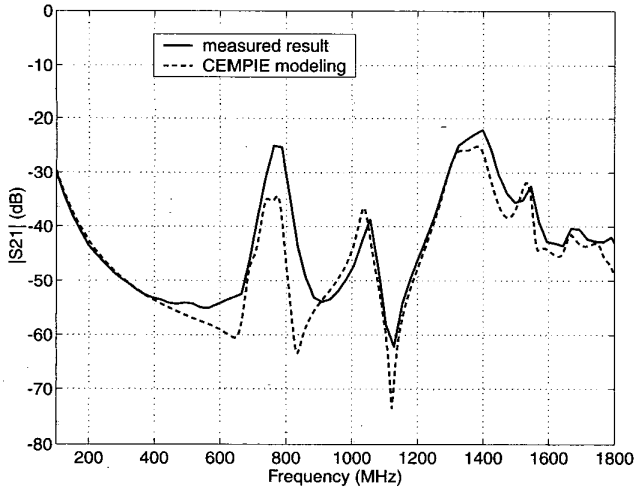

Figure 4: Comparison between the measured and modeled $|S_{21}|$ results for the DC power bus shown in Figure 3.

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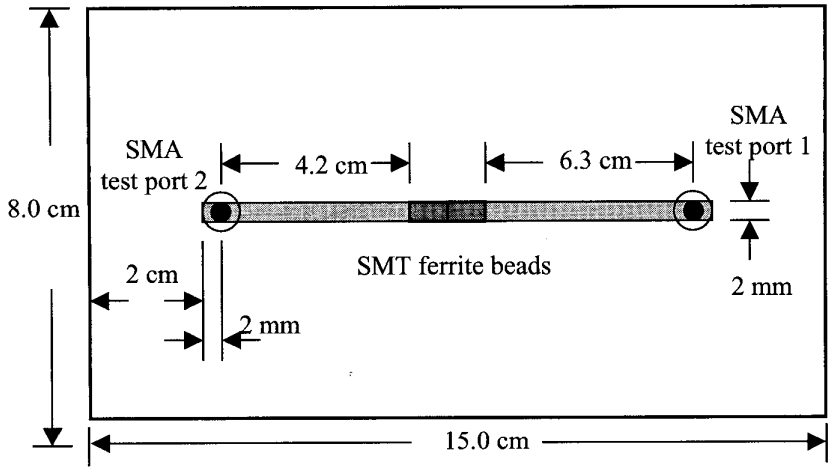
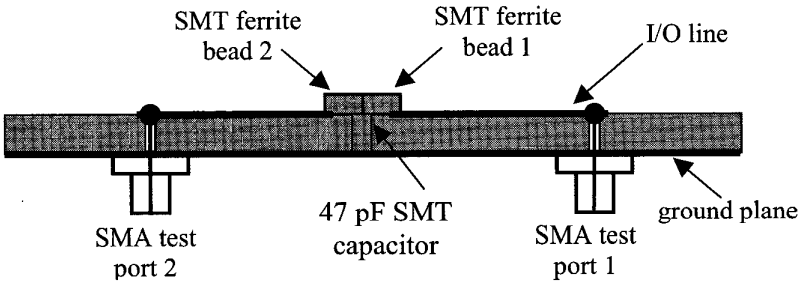


(a)



(b)

Figure 5: An I/O line with a T filter: (a) top view, (b) side view.

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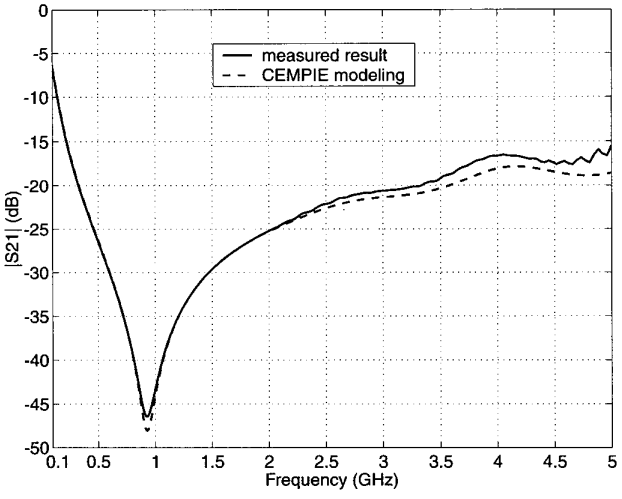

Figure 6: Comparison between the measured and modeled $|S_{21}|$ for the I/O line shown in Figure 5.