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Increasing the noise margin in organic circuits using dual gate field-effect transistors

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Complex digital circuits reliably work when the noise margin of the logic gates is sufficiently high. For p-type only inverters, the noise margin is typically about 1 V. To increase the noise margin, we fabricated inverters with dual gate transistors. The top gate is advantageously used to independently tune the threshold voltage. The shift can be quantitatively described by $\Delta V_{\text{th}} = (C_t/C_b) V_{\text{top gate}}$, where C_t and C_b are the top and bottom gate capacitances. We show that by adjusting the top gate biases, the noise margin of dual gate inverters can be significantly improved up to about 5 V. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2904624]

Organic integrated circuits are being developed for application in contactless radio-frequency identification transponders.[1] The most complex reported digital integrated circuit is a functional 64 bit code generator comprising of about 2000 field-effect transistors.[2] Complex circuits face a reliability issue. An integrated circuit usually fails if only one of the logic gates does not properly function. The larger the population of logic gates, the larger the parameter spread, and the larger the probability for failure.

The noise margin is defined as "the maximum allowable spurious signal that can be accepted by a gate while still giving correct operation."[3] Because the output of one logic gate is the input of the next logic gate, the noise margin is calculated as the side of the largest square that can be inscribed between the input-output characteristics and its mirrored image. Due to statistical variation of the threshold voltage and of the other transistor parameters, the noise margin in one or more actual logic gates can become too small. This may result in a failure of the logic gates with insufficient noise margin and may cause a failure of the entire circuit. If we neglect hard faults, to ensure robust circuit functionality and, hence, effective yield, the noise margin of each gate must be above a certain minimum value.[4,5]

The threshold voltage has a very strong influence on the noise margin of an organic inverter.[4] For a given gate oxide-semiconductor system, the threshold voltage is normally fixed. To independently tune the threshold voltage, we apply a second gate.[6–8] The resulting dual gate transistor then combines a single semiconductor layer, top and bottom gate dielectrics, and shared source and drain electrodes. These transistors have previously been used to increase the on/off current ratio and subthreshold slope. Furthermore, dual gate transistors are reported to operate as single AND gates.[9] Here, we apply dual gate transistors to optimize the noise margin of logic gates.

As a semiconductor, we used poly(triarylamine) (PTAA). The chemical structure is depicted in Fig. 1. Dual gate transistors were fabricated using heavily doped p-type Si wafers as bottom gate electrode with a 1000 nm thermally oxidized SiO_2 layer as the bottom gate dielectric. Gold source and drain electrodes were defined by photolithography. A 10 nm titanium layer was used for adhesion. The SiO_2 layer was passivated with hexamethyldisilazane prior to semiconductor deposition. PTAA films were spin coated from toluene with a layer thickness of approximately 80 nm. On the PTAA, the top gate insulator polyisobutylmethacrylate was spin coated from a butanol solution. This resulted in a layer of about 400 nm, on which the top gate gold electrode was evaporated through a shadow mask. All devices were annealed for 2 h in dynamic vacuum of ~5 $\times 10^{-4}$ mbar. The electrical measurements were performed in vacuum at 40 °C using a HP4155B semiconductor parameter analyzer.

The transfer characteristics for a PTAA transistor are presented in Fig. 1. There is hardly any hysteresis. The linear and saturated mobility derived from the corresponding trans-
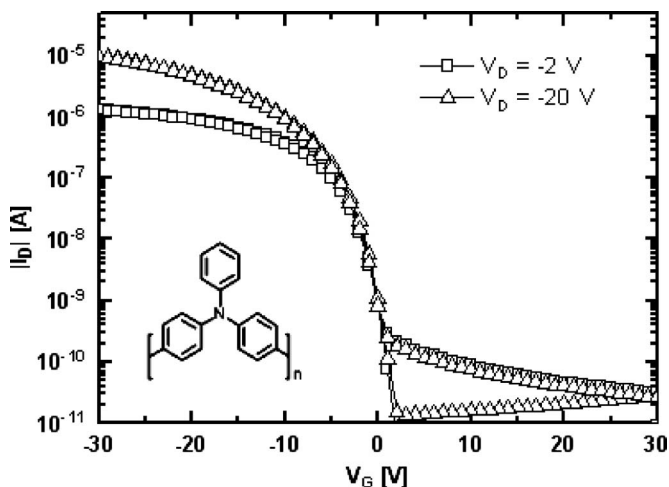

FIG. 1. Linear and saturated transfer characteristics of a poly(triarylamine) (PTAA) field-effect transistor measured using drain biases of −2 and −20 V. The channel length and width are 10 and 10 000 μm, respectively. The inset shows the chemical structure of PTAA.

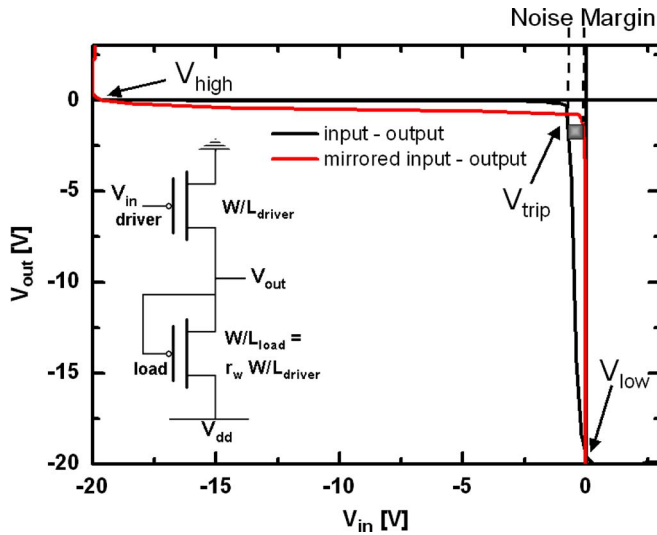a)Electronic mail: m.spijkman@rug.nl.

FIG. 2. (Color online) Input-output characteristics of a typical $V_{gs}=0$ inverter. The inset shows the inverter schematic. The enclosed square represents the noise margin as obtained by maximizing the square between the input-output characteristics and its mirror image.
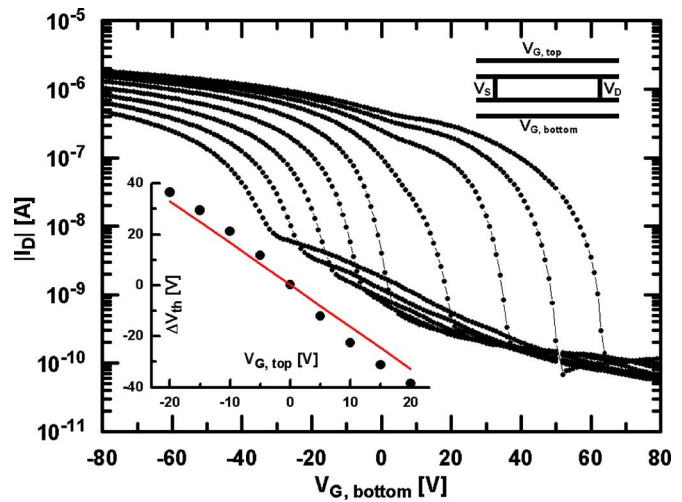

FIG. 3. (Color online) The absolute value of the drain current of a dual gate transistor is presented on a semilogarithmic scale as a function of the bottom gate bias. The top gate bias is varied from left to right in steps of 5 V starting at +20 to −20 V. The inset graph shows the measured (circles) and calculated (line) threshold shift. The other inset is a schematic of a dual gate transistor.

fer curves amounts to 1.7×10^{-3} and 1.9×10^{-3} cm^2/V s. The threshold voltage as obtained from a linear extrapolation of the transfer curve is −2.6 V and the pinch-off voltage, i.e., the onset of accumulation, is +2 V. Figure 1 shows that the channel is already accumulated at 0 V gate bias, i.e., the transistors are "normally ON."

Discrete transistors were combined into inverters. Because the pinch-off voltage is positive, we use "$V_{gs}=0$" logic.[10] The circuit schematic is presented in Fig. 2. The gate of the load is shorted with the source, hence $V_{gs}=0$. The inverter operates as a voltage divider controlled by the input voltage. To convert a logic "1" into a logic "0," the output voltage, V_{out}, should be close to the negative supply voltage, V_{dd}, when there is 0 V applied to the driver gate, V_{in}. The resistance of the load should be much smaller than that of the driver. This is realized by increasing the W/L of the load by a factor $r_w = (W/L_{load})/(W/L_{driver})$. When the input voltage is low, $V_{in} = V_{dd}$, the driver transistor is turned on. The output voltage is pulled up from a logic 0 to a logic 1. The operation is demonstrated by the experimental input-output characteristics, as presented in Fig. 2.

As already noted, logic gates that have too small noise margin because of spread in the transistor parameters may cause the failure of the whole circuit. Neglecting hard faults, thus, the yield of a digital circuit can be assumed to be the joint probability that all logic gates have a noise margin larger than an acceptable minimum. To ensure yield while increasing the number of gates, the ratio between average noise margin and its standard deviation has to increase.[11] A ratio of four will ensure good yield in a 10^4 gates circuit, while a ratio of five is enough to get good yield in a 10^6 gates circuit.[11] Figure 2 shows that the noise margin of the inverter, indicated as the black square, is about 0.6 V. This is a typical value for p-type only logic[10] when using these supply voltages. The voltage at which the input voltage is identical to the output voltage is the trip voltage. In an ideal inverter, the trip point should be at the center of the supply range. Figure 2 shows that the trip point is close to 0 V input bias. The asymmetric position severely limits the noise margin.[1,10]

To increase the noise margin, we used dual gate transistors. The linear transfer characteristics measured at a source-drain bias of −2 V are presented in Fig. 3 for top gate biases ranging from −20 to 20 V in steps of 5 V. The transfer curve at 0 V top gate bias is similar to the one from a single gate transistor. Figure 3 shows that the transfer curves systematically change with the applied top bias. In first order approximation, we can describe the shift of the transfer curve, ΔV_{th}, by

$$\Delta V_{th} = \frac{C_t}{C_b} V_{Gtop}, \tag{1}$$

where C_t and C_b are the top and bottom dielectric capacitances per unit area, and V_{Gtop} is the applied top gate potential. The inset of Fig. 3 shows that Eq. (1) perfectly describes the change in threshold voltage. A positive top gate bias partially depletes the bottom accumulation channel. To compensate the depletion, the bottom gate bias has to be adjusted by an equivalent shift, as given by Eq. (1). The transfer curve shifts to the left. A negative top gate bias creates a second accumulation channel at the top interface. This creates an additional current that effectively shifts the transfer characteristic to the right. The transfer curves at negative top gate biases of −5 V through −20 V show a "hump" at the bottom gate bias of about 10 V. This hump resembles a crossover from a field-dominated current to a bulk dominated current as explained for single gate field-effect transistors.[12] At these bias conditions, the top channel is accumulated while the bottom channel is depleted. With increasing bottom gate bias, the depletion depth increases toward the top channel. The charge density in the accumulated top channel is much larger than in the bulk semiconductor. An extra voltage is thus needed to deplete the top channel. Therefore, a hump is obtained in the dual gate transfer curve for negative top gate biases. Finally, the off currents in Fig. 3 are comparable to the top gate currents. Hence, the off current is a parasitic top gate leakage current.

Subsequently, we fabricated inverters using the dual gate transistors, according to the same schematic presented in
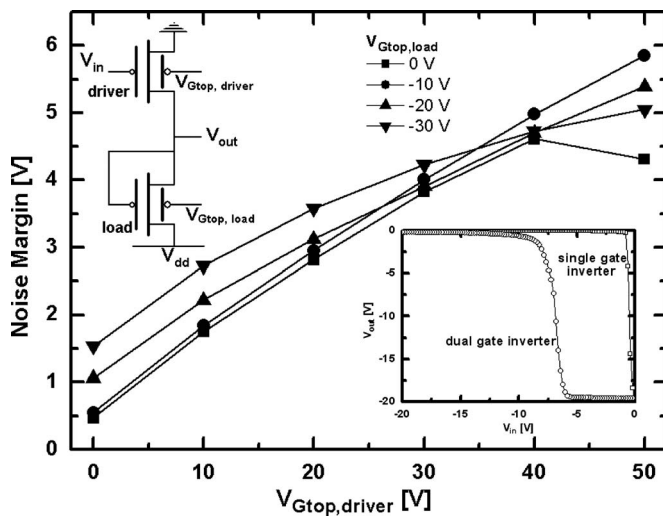
FIG. 4. The noise margin of dual gate inverters as a function of the top gate bias on the driver transistor for several top gate biases on the load transistor. The supply voltage V_{dd}, was set at -20 V. The insets show the schematic of the dual gate inverter and the improvement gained in input-output characteristics by using a dual gate inverter.

Fig. 2. The supply voltage was set at -20 V. For each value of the top gate biases of the driver and the load, the noise margin was determined from the static input-output voltage characteristics. The noise margin is presented, in Fig. 4, as a function of the top gate bias of the driver transistor, for several values of the top gate bias on the load transistor. Figure 4 shows that the noise margin can be greatly improved by using dual gate transistors. The noise margin increases from about 0.5 V for the single gate inverters to about 5.9 V for the dual gate inverters.

As shown in Fig. 2, the noise margin is severely limited by the asymmetric position of the trip point. Ideally, this should be at the center of the supply range $V_{in} = V_{dd}/2$ and $V_{out} = V_{dd}/2$. The asymmetry is due to the fact that the load and the driver transistors have the same pinch-off voltage. Altering the geometry factor $r_w = (W/L_{load})/(W/L_{driver})$, only shifts the position of the logic 0. The pinch-off voltage of the driver determines the input voltage at which the inverter switches from V_{dd} to ground. To optimize the trip voltage, the pinch-off voltage of the driver, therefore, has to be shifted to the left, to more negative values. As can be seen in Fig. 3, the shift can be realized in dual gate transistors by applying a positive top gate bias. Consequently, the noise margin increases with positive top gate bias on the driver, as shown in Fig. 4. The bias on the load transistor hardly influences the noise margin. We note however that the load dominates the switching speed during dynamic operation, as its small current pulls down the output node very slowly compared to the large on current supplied by the driver when the output is pulled up. By applying a negative bias to the top gate of the load we can increase the pull-down current, and hence the speed, without compromising the noise margin.

In conclusion, we have fabricated dual gate transistors. The top gate can advantageously be used to change the threshold voltage. The shift is quantitatively described by Eq. (1). We show that by adjusting the top gate biases in dual gate inverters, the noise margin can be brought from a typical value of less than 1 to about 5 V. This drastic improvement will pave the way to the fabrication of large, complex and robust organic circuits.[13,14]

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