Increasing Voltage Utilization in Split-Link, Four-Wire Inverters

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***Abstract*—Three-phase four-wire inverters, with either three-leg or four-leg topology, are useful for interfacing distributed generation to networks of unbalanced loads, but neither of the available circuit topologies is ideal. The split-link three-leg topology (with six switches) suffers from poor dc voltage utilization compared with the four-leg topology (with eight switches). The four-leg topology has an electromagnetic compatibility (EMC) difficulty because it imposes large-amplitude high-frequency voltages between the dc-link busbars and ground. To obtain both good dc voltage utilization and good EMC performance, it is proposed to use a split-link inverter with an active balancing circuit (also eight switches). The balancing circuit is used to modulate the dc busbar offset voltage to make better use of the available dc-link voltage. The optimum voltage term is established to be a third harmonic term, and the dc voltage utilization is improved. A deadbeat controller supplemented with a repetitive controller is designed to give good tracking and good disturbance rejection for the busbar offset voltage. System performance is studied through an experimental test rig.**

***Index Terms*—Busbar offset modulation, dc link, four-wire inverter, repetitive control, voltage utilization.**

I. Introduction

WHEN a distribution network supplied by inverters has unbalanced loads, a four-wire inverter (with a neutral connection in addition to three-phase connections) can be used to provide full control over the phase voltages and thereby ensure good voltage quality. There are two common ways to provide the neutral connection: retaining a three-leg inverter structure but splitting the dc link with a pair of capacitors to provide the fourth wire [1]–[3] and retaining a single dc-link capacitor [4]–[6] by providing a fourth leg (pair of switches). The split-link topology is simpler and uses fewer semiconductors (six compared with eight) but introduces the problem of ensuring close voltage sharing between the split capacitors and the need to attenuate voltage ripple off them. A large neutral current (produced by either unbalanced or nonlinear loads) causes a large perturbation to the split voltages. Such a perturbation needs to be compensated for in the phase-voltage control scheme and risks malfunction of the inverter. Voltage balancing controllers, such as dynamic hysteresis current control [3], have been proposed to overcome the problem, but the zero-sequence current can still cause large dc voltage imbalance. The voltage deviation can be attenuated by using larger dc-link capacitors but with an obvious penalty in cost and size. The split-link topology requires that the phase-voltage peak is less than or equal to the split dc-link voltage (normally half the total dc-link voltage), whereas the four-leg inverter can allow a line-voltage peak equal to half the total dc-link voltage. This gives an approximately 15% advantage in dc voltage utilization in favor of the four-leg inverter. Another factor to consider in inverter selection is the high-frequency common-mode voltages with respect to ground produced by switching. Since there are significant parasitic capacitances between the dc busbars, packages, heat sinks, and ground, there can be significant common-mode current flows through long paths involving ground. These are known to be a source of electromagnetic compatibility (EMC) problems [7]. In this paper, a proposal is made to improve the voltage utilization of the split-link inverter when fitted with an active balancer. The aim is to retain the EMC advantage of this structure and to extend the use of the active balancing circuit beyond just maintaining equal split voltages to modulating these voltages to achieve the same dc voltage utilization as the four-leg structure. The resulting inverter has the attractive EMC properties of the split-link three-leg inverter combined with the better voltage utilization of the four-leg inverter. It will use the same number of switches as the four-leg inverter.

The paper will establish the required form of split voltage modulation to obtain maximum dc voltage utilization. It will then discuss how the capacitors and balancing circuit inductor are chosen and how the split voltage controller can be designed using a plug-in repetitive control scheme [8], [9]. The chosen design is verified experimentally. A circuit simulation is used to verify that the common-mode voltage imposed across the parasitic capacitance of the dc link, and the resulting current, are less onerous than in a four-leg inverter.

II. Comparison of Four-Wire Inverter Topologies

In simple terms, the role of a four-wire inverter is to produce a balanced set of phase voltages with respect to neutral

$$V_{\mathrm{an}}(t) = V_1 \sin(2\pi f_1 t)$$
$$V_{\mathrm{bn}}(t) = V_1 \sin\left(2\pi f_1 t - \frac{2}{3}\pi\right)$$
$$V_{\mathrm{cn}}(t) = V_1 \sin\left(2\pi f_1 t + \frac{2}{3}\pi\right). \quad (1)$$

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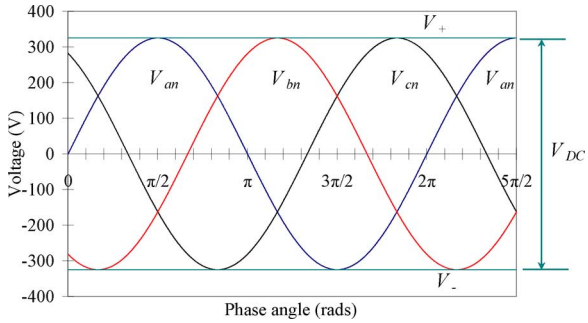

Fig. 1. Illustration of the dc-link voltage required for phase voltages with an amplitude of 330 V (peak).

To achieve this with a split-link three-leg inverter requires the total dc-link voltage to be

$$V_{\mathrm{DC}} \geq 2V_1. \tag{2}$$

This assumes that the total dc voltage V_{DC} is split equally to form the two busbar voltages, V_+ and V_-, as illustrated in Fig. 1, where $V_+ = -V_-$ and $V_{\mathrm{DC}} = V_+ - V_-$.

An advantage of the four-leg inverter is that when space-voltage vector modulation (SVM), is applied, the dc voltage utilization (defined as the maximum phase voltage magnitude relative to the dc-link voltage) can be increased by approximately 15% compared to the three-leg, split-link case [4]. SVM applied to three-wire inverters also has this advantage compared to carrier-based, pulsewidth modulation (PWM), with a sinusoidal reference [10]. However, in three-wire carrier-based PWM, the same 15% advantage can be achieved by adding a zero-sequence third harmonic term [11], [12] to the reference for the PWM. This term will be present in the inverter phase voltages but not in the line voltages. These two methods are equivalent under certain circumstances, and extensive research comparing and contrasting the methods is available [12]–[14]. It is not possible to use injection of a third harmonic reference term with a four-wire inverter because the injected signal will also be present in the phase voltage of the loads. Thus, in the four-wire case, SVM of a four-leg inverter has a voltage utilization advantage (of 15%) over a carrier-based PWM of a split-link three-leg inverter.

In the split-link three-leg inverter, the inverter dc busbars are at well-defined voltages (the capacitor voltages) with respect to neutral and are not subject to significant common-mode voltage with respect to ground if the neutral is well grounded. In contrast, in the four-leg design, the busbars are subject to high-frequency voltage transitions with respect to neutral and ground as the fourth leg connects the two busbars to neutral in an alternating pattern at the switching frequency. Proposals have been made to reduce the common-mode voltage problem of the four-leg inverter. For instance, use of zero vectors can be avoided [15], [16], but this also reduces the dc-link utilization.

On the basis of EMC performance, it would be attractive to choose the split-link three-leg inverter. To overcome the voltage balancing problem, it is possible to fit an active balancing circuit to the split link using two additional semiconductor switches (the equivalent of a fourth leg) so that current can be injected into the split capacitors. This approach was discussed in [17], and a control solution was provided. The active control of the split link can also yield a reduced capacitor size over the passively balanced split link. The actively balanced split-link circuit is shown in Fig. 2. The pair of capacitors is the key element, the split voltage sources are for analysis purposes only, and, in practice, a single power source would be present. It has been assumed that the neutral line is solidly connected to ground, but this connection could be replaced with a grounding impedance. The parasitic capacitors between each busbar and ground have been reduced to a single capacitance C_{og} between the midpoint of the source and ground. It is clear that connecting the split point to neutral and indirectly to ground prevents the parasitic capacitors from being exposed to large voltage transitions.

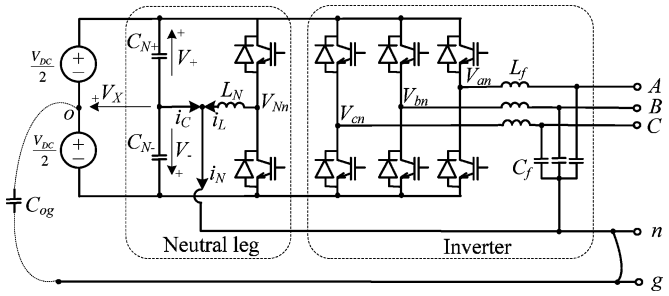

Fig. 2. Actively balanced split-link inverter.

A shortcoming of the actively balanced split-link inverter is that the number of semiconductor switches is equal to that of the four-leg inverter, but the dc voltage utilization is only that of the split-link three-leg inverter (in other words, the 15% advantage of the fourth leg is not achieved). However, this is on the assumption that the dc-link voltage is equally split and the offsets of two busbar voltages are fixed. The proposal in this paper is to modulate a busbar offset voltage so as to allow higher maximum phase voltages.

III. Optimal Modulation of the Busbar Offset Voltage

The busbar offset voltage V_X, shown in Fig. 2, is defined as the displacement of the notional midpoint o from the split point of the dc link ($V_X = V_{\mathrm{ON}}$ in this topology). It can be expressed as offset

$$V_X = V_+ - \frac{1}{2}V_{\mathrm{DC}} = V_- + \frac{1}{2}V_{\mathrm{DC}}$$

or, equivalently

$$V_X = \frac{V_+ + V_-}{2}.$$

If the dc-link voltage is equally split, V_X is zero. V_X will be modulated to ensure that the two busbar voltages are sufficient to establish the required positive and negative peaks of the phase voltages

$$\begin{aligned} V_+ &\geq V_{\max}(t) = \max\left(V_{\mathrm{an}}(t), V_{\mathrm{bn}}(t), V_{\mathrm{cn}}(t)\right) \\ V_- &\leq V_{\min}(t) = \min\left(V_{\mathrm{an}}(t), V_{\mathrm{bn}}(t), V_{\mathrm{cn}}(t)\right). \end{aligned} \tag{3}$$

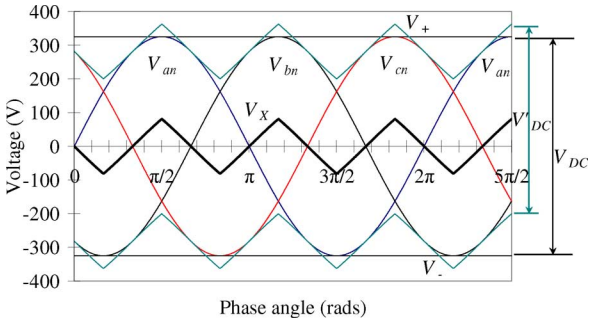

Fig. 3. Illustration of reduced $V_{\rm DC}$ when V_X tracks the midpoint of the phase voltage extremes.

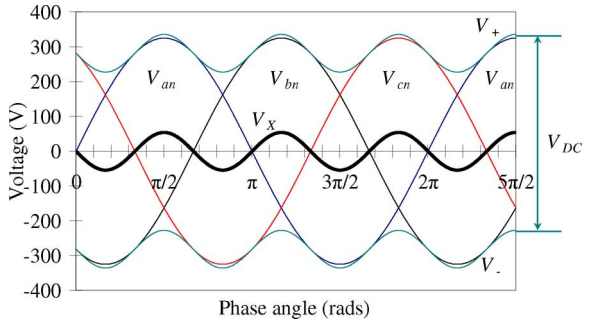

Fig. 4. Illustration of reduced $V_{\rm DC}$ when V_X is third harmonic.

The total dc-link voltage required under this condition, $V'_{\rm DC}$, is the difference between the busbar voltages

$$V'_{\rm DC} \geq V_{\max}(t) - V_{\min}(t). \tag{4}$$

An obvious method to obtain a minimum dc voltage that fulfills (4) is for V_X to follow the arithmetic midpoint of $V_{\max}(t)$ and $V_{\min}(t)$

$$V_X(t) = \frac{1}{2}\left(V_{\max}(t) + V_{\min}(t)\right). \tag{5}$$

Fig. 3 illustrates the variation of V_X, V_+, and V_-. It can be seen that the new required dc voltage, $V'_{\rm DC}$ is less than that required in Fig. 1 where no modulation of V_X occurred. The improvement in dc voltage utilization can be quantified by considering the segment from $\pi/6$ to $\pi/2$ as an example. In this segment $V_{\max}(t) = V_{\rm an}(t)$ and $V_{\min}(t) = V_{\rm bn}(t)$. Equation (4) then becomes

$$\begin{aligned} V'_{\rm DC} &\geq V_{\rm an}(t) - V_{\rm bn}(t) \\ &= V_1 \sin(2\pi f_1 t) - V_1 \sin\left(2\pi f_1 t - \frac{2}{3}\pi\right). \end{aligned} \tag{6}$$

In other words, $V'_{\rm DC}$ must exceed the line voltage peak and this occurs at $\pi/3$ and has a value of $\sqrt{3}V_1$. The required dc voltage is

$$V'_{\rm DC} \geq \sqrt{3}V_1 = \frac{\sqrt{3}}{2}V_{\rm DC} \approx \frac{1}{1.15}V_{\rm DC}. \tag{7}$$

Thus, the 15% advantage in dc voltage utilization of the four-leg inverter has also been achieved here. It can be verified that (5) and (7) fulfill the conditions in (3).

The waveform of V_X produced by (5) and illustrated in Fig. 3 consists of segments of sine waves with a period of one-third of the fundamental but also containing higher triplen harmonics. It would be challenging to reproduce this as a voltage on the dc-link capacitors. An alternative would be to use a sine wave of the same period, i.e., a third harmonic, as illustrated in Fig. 4 and (8)

$$V_X(t) = V_3 \sin(-3 \times 2\pi f_1 t). \tag{8}$$

As shown in the Appendix, the amplitude of the third harmonic that yields the best dc voltage utilization is one-sixth of the amplitude of the fundamental, and it yields an advantage of 15% over the standard split-link arrangement. The principle is the same as injecting a third harmonic term in three-wire three-leg inverters [8], but here the third harmonic is applied to the busbar potentials.

The modulating signal used for each phase voltage must now be modified to account for the variation of the busbar offset. The phase a voltage as a function of the switch duty cycle d_a or depth of modulation m_a is defined in (9) (note: $0 \leq d_a \leq 1$, $d_a = \frac{1}{2}(1 + m_a)$, and $-1 \leq m_a \leq 1$)

$$\begin{aligned} V_{\rm an} &= d_a V_+ + (1 - d_a)V_- \\ &= \frac{1}{2}(1 + m_a)V_+ + \frac{1}{2}(1 - m_a)V_- \\ &= \frac{1}{2}m_a V_{\rm DC} + V_X. \end{aligned} \tag{9}$$

To achieve a desired phase voltage requires

$$m_a = \frac{2}{V_{\rm DC}}(V_{\rm an}^{\rm ref} - V_X).$$

IV. Neutral Leg Modeling and Control

A. Modeling of the Neutral Leg

The busbar offset voltage can be controlled by injecting a current through the inductor L_N under the influence of the *fourth* leg voltage V_{Nn} as shown in Fig. 2. The capacitor current is composed of the inductor current used for control, and the neutral current is required by the load, which here is considered a disturbance. The following equations apply:

$$\begin{aligned} i_C &= C_{N+}\frac{dV_+}{dt} + C_{N-}\frac{dV_-}{dt} \\ &= 2C_N\frac{dV_X}{dt} \text{ if } C_{N+} = C_{N-} = C_N \end{aligned} \tag{10}$$

$$\begin{aligned} L_N\frac{di_L}{dt} &= V_{Nn} = d_N V_+ + (1 - d_N)V_- \\ &= m_N\frac{V_{\rm DC}}{2} + V_X \end{aligned} \tag{11}$$

where d_N is the duty cycle of the neutral leg transistors and $m_N = 2d_N - 1$ is the depth of modulation. The state equations of the system are

$$\begin{cases} 2C_N\dot{V}_X = i_N - i_L \\ L_N\dot{i}_L = V_X + \dfrac{V_{\rm DC}}{2}m_N. \end{cases} \tag{12}$$

B. Selection of Split-Link Components

It is now necessary to choose suitable component values. Clearly, it is advantageous to choose small-valued components for reasons of cost and volume but the following factors need to be considered.

1) The cutoff frequency of the neutral leg circuit must be above $3f_1$ so as to be able to control V_X to follow the third harmonic reference. Ignoring the external disturbance i_N the transfer function from the depth of modulation m_N to the busbar offset voltage V_X can be obtained from (12)

$$\frac{V_X}{m_N}(s) = \frac{V_{\rm DC}}{2} \times \frac{1}{1 + 2C_N L_N s^2}. \tag{13}$$

This cutoff frequency condition therefore determines the product of the inductance and capacitance and shows that small values are required.

2) It is desirable that the magnitude of the third harmonic current required to create V_X should not be large. This condition indicates that, within the confines of condition (a), the capacitor size should be reduced. The amplitude of the third harmonic current required for a voltage of $|V_X| = \frac{1}{6}V_1$ is

$$|I_{f_3}| = \frac{1}{6}V_1 2\pi \times 3f_1 C_N = \pi f_1 C_N V_1. \tag{14}$$

A disadvantage of choosing C_N small for this reason is that i_N will have a large effect on the busbar voltages, and so. good disturbance rejection from the controller is needed.

3) There are switching frequency ripples present in the capacitor voltages, and it is desirable to keep them small. Therefore a large capacitance is desirable. An estimate of the amplitude of the ripple can be gained by considering the fundamental term of a square-wave voltage of amplitude $V_{\rm DC}$ and frequency f_s and the effect an LC circuit has in attenuating this. Clearly, both L_N and C_N should be large to keep the ripples small.

$$|V_{\rm Ripple}| \approx \frac{V_{\rm DC}}{4\pi^3 C_N L_N f_s^2}. \tag{15}$$

C. Controller Design

Equation (12) forms the basis of a state-space model of the neutral leg system. We choose the state vector to be $\mathbf{x} = [V_X \ \dot{V}_X]$ and treat i_N as a disturbance term in vector δ. This choice of state vector will remove the need to measure i_L for state feedback and leave only V_X to be measured

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}u + \boldsymbol{\delta}$$

where

$$\mathbf{A} = \begin{bmatrix} 0 & 1 \\ \dfrac{1}{-2C_N L_N} & 0 \end{bmatrix}, \mathbf{B} = \begin{bmatrix} 0 \\ \dfrac{V_{\rm DC}}{-4C_N L_N} \end{bmatrix},$$

$$u = m_N, \text{ and } \boldsymbol{\delta} = \begin{bmatrix} 0 \\ \dfrac{\dot{i}_N}{2C_N} \end{bmatrix}.$$

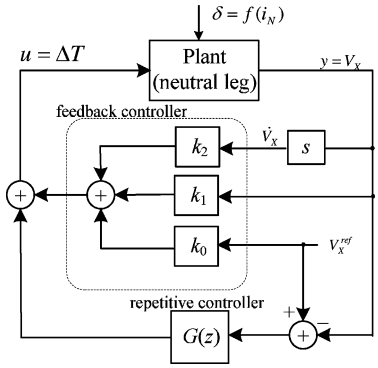

Fig. 5. Control system. A deadbeat feedback controller and a repetitive controller are connected in parallel.

A controller was designed to force the busbar offset voltage to track the third harmonic reference voltage. A deadbeat controller supplemented by a repetitive controller was chosen to give good tracking and the ability to reject periodic neutral current disturbance [8]. The general arrangement is shown in Fig. 5.

A discrete-time controller was designed using the procedure outlined here. A discrete time from the state-space representation (ignoring the disturbance) is

$$\begin{bmatrix} V_X(k+1) \\ \dot{V}_X(k+1) \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} \begin{bmatrix} V_X(k) \\ \dot{V}_X(k) \end{bmatrix} + \begin{bmatrix} g_1 \\ g_2 \end{bmatrix} \Delta T(k) \tag{16}$$

where

$$\phi_{11} = 1 - \frac{T^2}{4C_N L_N} \quad \phi_{12} = T$$

$$\phi_{21} = -\frac{T}{2C_N L_N} \quad \phi_{22} = 1 - \frac{T^2}{4C_N L_N}$$

$$g_1 = -\frac{V_{\rm DC}}{4C_N L_N} T \quad g_2 = -\frac{V_{\rm DC}}{4C_N L_N}$$

where T is the sampling interval, which is chosen to be the switching period $1/f_s$, and $\Delta T = m_N T$ is the width of the applied switching voltage pulse.

The output equation is $y(k) = V_X(k)$. A suitable control law is

$$\Delta T(k) = k_0 V_X^{\rm ref}(k) + k_1 V_X(k) + k_2 \dot{V}_X(k) \tag{17}$$

where

$$\begin{cases} k_0 = 1/g_1 \\ k_1 = -\phi_{11}/g_1 \\ k_2 = -\phi_{12}/g_1 \end{cases}$$

and $V_X^{\rm ref}(k)$ is the reference value.

Under ideal conditions, this deadbeat control will yield an output at the end of the sampling period equal to the reference value

$$Y(k+1) = V_X(k+1) = V_X^{\rm ref}(k). \tag{18}$$

In practice, there are disturbances and uncertainties in the circuit parameters and perfect deadbeat control cannot be achieved. A

TABLE I
INVERTER PARAMETERS

Output power	30 kW	Neutral capacitor C_{N+}, C_{N-}	25 μF
Phase voltage	330 V (peak)	Neutral inductor L_N	2.5 mH
AC frequency	50 Hz	Filter capacitor C_f	50 μF
Switching frequency	10 kHz	Filter inductor L_f	1.35 mH

plug-in repetitive controller can be connected in parallel with an existing controller without affecting its stability [8]. The repetitive controller will attenuate (ideally to zero) disturbances of the chosen period including the harmonic terms. The transfer function of the controller in the discrete-time form is

$$G(z) = k_g \frac{Q(z) \times z^{-(N-N_2)}}{1 - Q(z) \times z^{-N}} \tag{19}$$

where k_g is the gain, $N = f_s/f_1$, N_2 is the delay number, and $Q(z) = 0.25 \cdot (z + 2 + z^{-1})$ is a first-order filter.

V. EVALUATION AND ANALYSIS

The proposed variable busbar offset strategy was tested experimentally using an inverter with the circuit arrangement of Fig. 2 and with parameters as set out in Table I. The control was implemented on a digtal signal processor. To illustrate some features, the same system was simulated using the simulation package PSCAD/EMTDC.

The dc-link voltage was chosen on the basis of producing a peak phase voltage of 330 V. With the busbar offset voltage modulated with a peak of 55 V, this gives a required dc-link voltage of 572 V. To accommodate semiconductor and filter voltage drops, a link voltage of $V_{\rm DC} = 585$ V was chosen.

For a 50-Hz system, the split point is modulated at $3f_1 = 150$ Hz and the filter cutoff is constrained according to (13)

$$C_N L_N < \frac{1}{2(2\pi \times 3f_1)^2} = 5.623 \times 10^{-7}\ \mathrm{s}^2.$$

The maximum ripple at switching frequency (10 kHz) of the busbar offset voltage was chosen to be 1 V, and (15) further constrains the filter design

$$C_N L_N > \frac{V_{\rm DC}}{4\pi^3 V_{\rm Ripple} f_s^2} = 4.717 \times 10^{-8}\ \mathrm{s}^2.$$

Choosing a value of 1.5 A for the third harmonic current amplitude in the link capacitors gives, via (14), a limit for the capacitance

$$C_N < \frac{I_{f_3}}{\pi f_1 V_1} = 28.94\ \mu\mathrm{F}.$$

A value of $C_N = 25\mu$F was chosen. The compromise chosen for the filter cutoff was $f_c = 450$ Hz, which led to a choice of $L_N = 2.5$ mH. The resultant voltage ripple is $V_{\rm Ripple} = 0.704$ V and capacitor current is $I_{f_3} = 1.296$ A. Deadbeat control design according to (17) gave controller parameters of $k_0 = -4.2735 \times 10^{-6}$, $k_1 = 4.1026 \times 10^{-6}$, and $k_2 = 4.2735 \times 10^{-10}$.

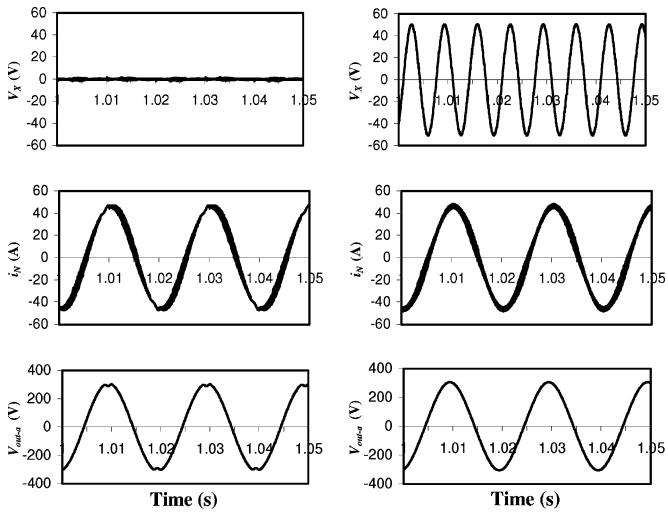

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Fig. 6. Simulation results. From top to bottom: busbar offset voltage, V_X; neutral current, i_N; and phase a output voltage after the LC filter, $V_{\rm an}$. (a) With unmodulated busbar offset and (b) with third harmonic busbar offset.

A severe test of the ability of the controller to maintain the correct busbar offset voltage is to test the four-wire system with a single-phase load (which is an extremely unbalanced three-phase load) with return of current via the neutral. A resistive–inductive load of 5.76 Ω in series with 8 mH was chosen for the test giving a neutral current of approximately 50 A. With $V_{\rm DC}$ set at 585 V and V_1 at 330 V, the modulation of the phase legs will saturate if the busbar offset voltage is not varied ($V_X = 0$) and, in turn, the output voltage of the filter, $V_{\rm an}$ will be distorted. Its total harmonics distortion (THD) is 2.83%. This is illustrated in simulation in Fig. 6(a) and experimentally verified in Fig. 7(a). It is worth noting in passing that the active balancer has successfully held the busbar offset voltage at zero despite the large amplitude neutral current. Fig. 6(a) and (b) shows that with the busbar offset voltage modulated with a 55 V at 150 Hz, the output voltage is not distorted because the link voltage is better utilized. The THD of the output voltage is 1.35%.

An important reason to adopt the split-link four-wire topology is to improve EMC through reduction of high-frequency voltage variation of the inverter busbars with respect to ground. This was tested in simulation and is shown in Fig. 8. The common-mode voltage $V_{\rm og}$ applied across the link-to-ground parasitic capacitance $C_{\rm og}$ of the inverter was studied for both the split-link inverter and a four-leg inverter using a standard symmetrical SVM switching technique [4]. The capacitance was set to 2.7 nF. Because the current through this capacitor flows in

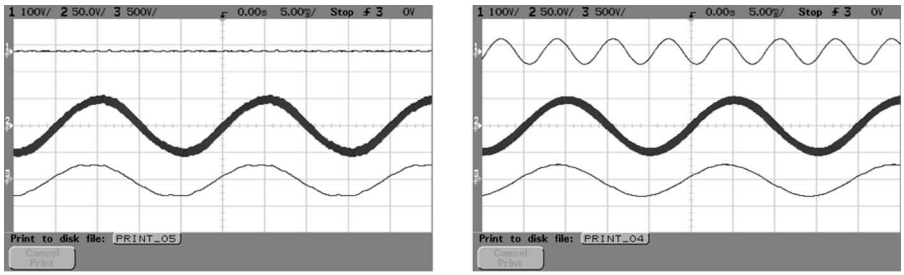

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Fig. 7. Experimental results. From top to bottom: Busbar offset voltage, V_X, 100 V/division (measured with potential divider of two 47 kΩ resistors between V_+ and V_- busbars); neutral current, i_N, 50 A/division and phase a output voltage after the *LC* filter, $V_{\rm an}$, 500 V/division. Time axis is 5 ms/division. (a) With unmodulated busbar offset and (b) with third harmonic busbar offset.

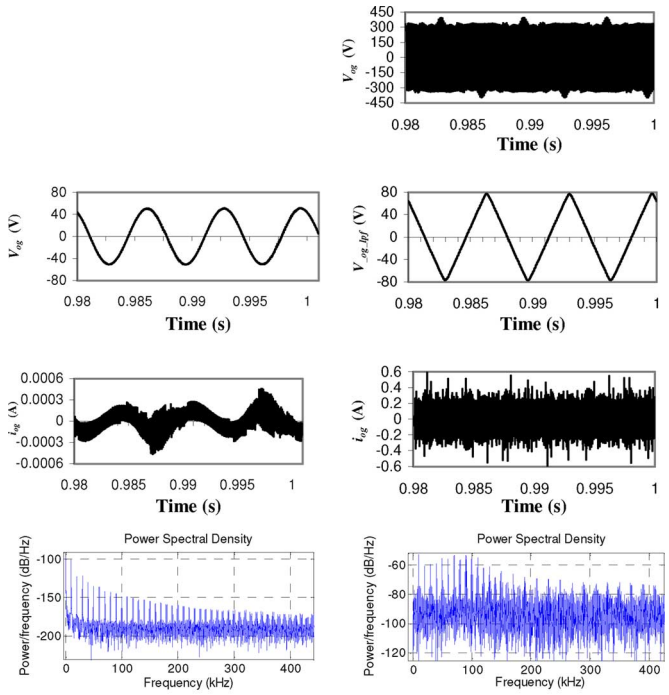

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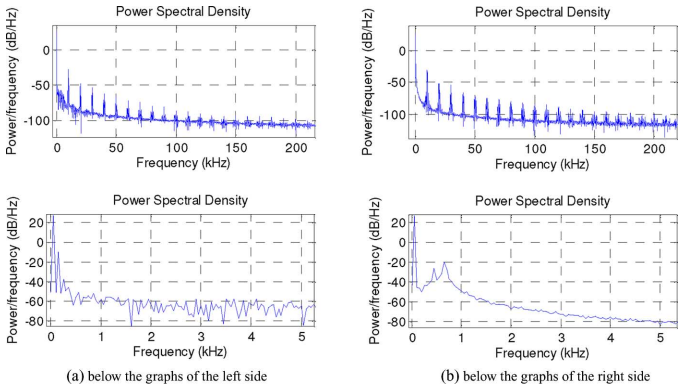
Fig. 8. Simulation of common-mode voltage $V_{\rm og}$ [including a filtered version in (b)] and common-mode currents, $i_{\rm og}$ in time and frequency domains. (a) Split-link inverter with modulated busbar offset and (b) four-leg inverter with SVM.

large-area common-mode paths, it can be a serious source of EMC problems. Its spectrum is, therefore, a relative measure of EMC performance.

The common-mode voltage $V_{\rm og}$ in the split-link inverter is the third-harmonic term (55 V at 150 Hz) plus the ripple voltage remaining after filtering by C_N and L_N as described by (15). This is shown in Fig. 8(a), which reveals that the common-mode current is approximately 0.5 mA. For the four-leg inverter with SVM, $V_{\rm og}$ is a rectangular wave of 330 V at 10 kHz, as seen in the top plot of Fig. 8(b), which is rich in switching frequency terms but also has an underlying low-frequency component. A notch filter of

$$\frac{1}{s} \times (1 - e^{-s/10000}) \frac{10000}{s + 10000}$$

was used to remove the 10-kHz switching frequency to reveal the low-frequency component $V_{\rm og\_lpf}$ as also shown in Fig. 8(b).



(a) below the graphs of the left side (b) below the graphs of the right side

Fig. 9. Power spectrum density analysis for phase output voltage $v_{\rm an}$. (a) Split-link inverter with modulated busbar offset and (b) four-leg inverter with SVM.

The total common-mode current is much higher at 0.4 A. The frequency spectra of $i_{\rm og}$ show that the split-link inverter has a switching frequency component more than 40 dB below that of the four-leg inverter and that the switching frequency harmonics are some 80–90 dB lower to beyond 50 kHz.

The waveforms of output voltages for the two inverters were also compared. The THDs are 1.35% for the split-link inverter and 1.2% for the four-leg inverter. Both are small. There is not much difference in spectra of the output voltages especially in the high-frequency ranges, but a relatively high third harmonic term (150 Hz) was found for the split-link inverter and resulted in a slightly higher THD, as shown in Fig. 9. This can be explained using (9) in that the third harmonic busbar offset voltage would be present in the output voltage, although most of this component will have been removed by modifying the depth of modulation m_a. It should be noted that only open-loop control was used for producing the output voltages for the two inverter topologies in this paper. If closed-loop control is used, THDs can be reduced further for both the split-link inverter with the modulated busbar offset and the four-leg inverter with SVM.

VI. Conclusion

It has been shown that it is feasible to modulate the busbar offset voltage of a split-link, three-leg, four-wire inverter using an active balancing circuit, and by doing so, the dc voltage utilization can be improved to match that of an SVM

four-leg inverter. No advantage in number of switches is achieved because the active balancer is the equivalent of a fourth leg, but a significant advantage is found in the spectrum of the voltage across any parasitic capacitance between the dc link and ground. The split-link inverter has much lower amplitude common-mode voltage at switching frequency since it comprises only the ripple across the split-link capacitors rather than the full square-wave voltage of the fourth leg. It has been shown in simulation and experiment that a deadbeat controller with an additional repetitive controller (for disturbance rejection) can successfully create the correct reference voltage for the busbar offset. That reference voltage has been established as a third harmonic voltage of one-sixth the amplitude of the phase voltage fundamental.

APPENDIX

To find the optimal magnitude of the third harmonic voltage for the busbar offset modulation, it is sufficient to examine the interval from $\pi/6$ to $\pi/2$. We seek the magnitude that allows the smallest dc voltage to be used for a given phase voltage

$$\begin{aligned} V_+ &= \frac{1}{2}V_{\rm DC} + V_X(t) \\ &\geq V_{\rm an}(t) \end{aligned} \tag{A1}$$

$$\begin{aligned} V_{\rm DC} &\geq 2V_{\rm an}(t) - 2V_X(t) \\ &= 2V_1\sin(2\pi f_1 t) + 2V_3\sin(3\times 2\pi f_1 t) \\ &= 2V_1\left(\sin(\theta) + A_3\sin(3\theta)\right). \end{aligned} \tag{A2}$$

It is convenient to define the third harmonic magnitude relative to the fundamental of the phase voltage, $A_3 = V_3/V_1$ and to use the angle $\theta = 2\pi f_1 t$. The maximum voltage required occurs at the angle where $\frac{dV_{\rm DC}}{d\theta}$ is zero

$$\frac{dV_{\rm DC}}{d\theta} = 2V_1\left(\cos\,\theta + 3A_3\cos 3\theta\right) = 0. \tag{A3}$$

The solutions to (A3) within $\pi/6$ to $\pi/2$ are $\theta = \cos^{-1}0 = \frac{1}{2}\pi$ and $\theta = \cos^{-1}\sqrt{(9A_3-1)/12A_3}$. The sign of the second differential will indicate whether a maxima or minima exists

$$\frac{d^2V_{\rm DC}}{d\theta^2} = -2V_1\left(\sin\theta - 9A_3\sin 3\theta\right). \tag{A4}$$

Considering first the case of $\theta = \frac{1}{2}\pi$, the second differential is

$$\frac{d^2V_{\rm DC}}{d\theta^2} = 2V_1(9A_3 - 1). \tag{A5}$$

Equation (A5) indicates that if $A_3 > 1/9$, then $\theta = \pi/2$ is a minimum point, whereas, if $A_3 < 1/9$, then $\theta = \pi/2$ is a maximum point. When $A_3 = 1/9$, the maximum voltage required is

$$V_{\rm DC} \geq 1.778V_1. \tag{A6}$$

For the second case of $\theta = \cos^{-1}\sqrt{(9A_3-1)/12A_3}$, the amplitude must be $A_3 > 1/9$. The second differential and dc voltage required are

$$\frac{d^2V_{\rm DC}}{d\theta^2} = \sqrt{\frac{3A_3+1}{12A_3}}(1-9A_3) \tag{A7}$$

$$V_{\rm DC} \geq 2V_1A_3\left(\frac{3A_3+1}{3A_3}\right)^{3/2}. \tag{A8}$$

For $A_3 > 1/9$, $d^2V_{\rm DC}/d\theta^2 < 0$ and (A8) will yield the maximum voltage required. Differentiating (A8) with respect to A_3 and setting the result to be zero will give the values of A_3 that cause the lowest or highest required voltage.

$$\frac{dV_{\rm DC}}{dA_3} = 2V_1\left(\frac{3A_3+1}{3A_3}\right)^{1/2}\left(\frac{6A_3-1}{6A_3}\right) = 0. \tag{A9}$$

The solutions to (A9) are $A_3 = -1/3$ (which can be discarded) and $A_3 = 1/6$, which when substituted into (A8) gives

$$V_{\rm DC} \geq \sqrt{3}V_1. \tag{A10}$$

In summary, the first case of a maximum at $\theta = \pi/2$ using $A_3 < 1/9$ requires $V_{\rm DC} \geq 1.778V_1$, whereas the second case with a maximum at $\theta = \cos^{-1}\sqrt{(9A_3-1)/12A_3}$ using $A_3 = 1/6$ requires $V_{\rm DC} \geq 1.731\,V_1$, so, the second case is preferred. This result is the same as that obtained for the three-leg, three-phase inverter.

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