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Independent closed loop control of di/dt and dv/dt for high power IGBTs

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Abstract: As the insulated gate bipolar transistor (IGBT) modules have their own specific characteristic switching forms, their turn-on and turn-off times are changed according to practical applications. For the conventional gate drives, gate resistors are used to adjust the turn-on and turn-off times which change switching losses that have a significant amount in total losses. Collector current rate of change, di_C/dt and collector-emitter rate of change, dv_{CE}/dt are dependent on each other and they affect operating parameters in high power converters. Relations between current and voltages during the switching transitions are given and effects of the changes in electrical parameters for the operation of IGBT are described. Thereafter, closed-loop gate drive with analog control that performs independent control of di_C/dt and dv_{CE}/dt of a new generation IGBT module platform for high power applications is proposed. Unlike conventional gate drives, proposed closed-loop drive makes constant di_C/dt possible while dv_{CE}/dt is decreased to increase the efficiency of the power conversion system. This leads to decrease of the switching losses without changing the electromagnetic interference (EMI), IGBT voltage, and current stresses which are related with the rate of change of collector current. Simulations are performed in a double pulse test circuit in which new package next high power density dual (nHPD^2) family MBM450FS33F Hitachi dual IGBT with 3300V 450A ratings is modelled.

Key words: Closed-loop gate drive, insulated-gate bipolar transistors (IGBTs), switching losses, turn-on and turn-off energy

1. Introduction

Insulated gate bipolar transistors (IGBTs) are widely used in a variety of areas. Especially in high power converters, high voltage and high currents make switching behaviour of IGBTs important to be worked in the safe operating area (SOA). Gate drivers are employed to drive the IGBT with the desired gate current and also for safety switching. Conventional gate drives (CGDs) control switching transients di_C/dt and dv_{CE}/dt of IGBTs by manual selection of several gate resistors. Gate resistance also results in the variation of switching delay time that affects the control performance of power converters. CGDs control overshoot of the collector voltage and IGBT short circuit by active clamping and desaturation monitoring methods to protect IGBTs and the other components in a power electronics system [1–4]. di_C/dt changes related with dv_{CE}/dt according to gate current which affects the switching losses, electromagnetic interference (EMI) issue and peak electrical

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characteristics as shown in Figure 1. EMI problems are directly related with the value of di_C/dt which requires control of the current rate of change [5].

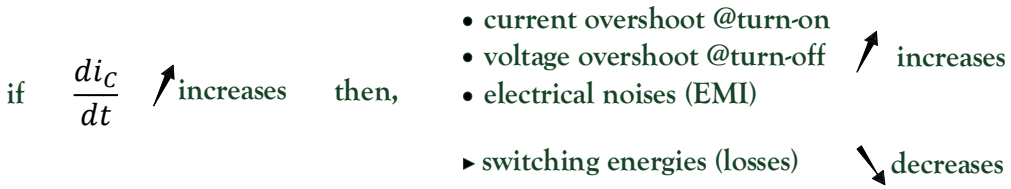


Figure 1. di_C/dt effects over electrical characteristics.

Ideal IGBT drive's capability is to turn the IGBT at specified levels of di_C/dt and dv_{CE}/dt regardless of load current, dc-link voltage, or junction temperature and to keep it within the SOA by means of controllable current and voltage peaks. In addition, the gate driver should be designed to withstand IGBT terminal voltage against high common-mode (CM) dv_{CE}/dt transients.

The rate of change of collector current (di_C/dt) is described in (1) for turn-on and turn-off, respectively [6];

$$\begin{aligned} \frac{di_C}{dt} &= \frac{V_{GG} - (V_T - \frac{I_L}{2g_m})}{\frac{R_g C_{ies}}{g_m} + L_s}, \quad \text{at turn-on} \\ \frac{di_C}{dt} &= \frac{V_T - V_{GG} + \frac{I_L}{2g_m}}{\frac{R_g C_{ies}}{g_m} + L_s}, \quad \text{at turn-off} \end{aligned} \tag{1}$$

where V_{GG} is gate voltage, I_L is load current, g_m is IGBT transconductance, R_g is external gate resistance, C_{ies} is IGBT input parasitic capacitance, V_T is IGBT threshold voltage, L_s is the stray inductance between the IGBT chip emitter and the Kelvin emitter terminal of the IGBT. As seen in (1), gate resistance R_g is not dominant to change di_C/dt against transconductance of IGBT for CGDs. High delay time also occurs with CGD when gate resistor value is increased [6].

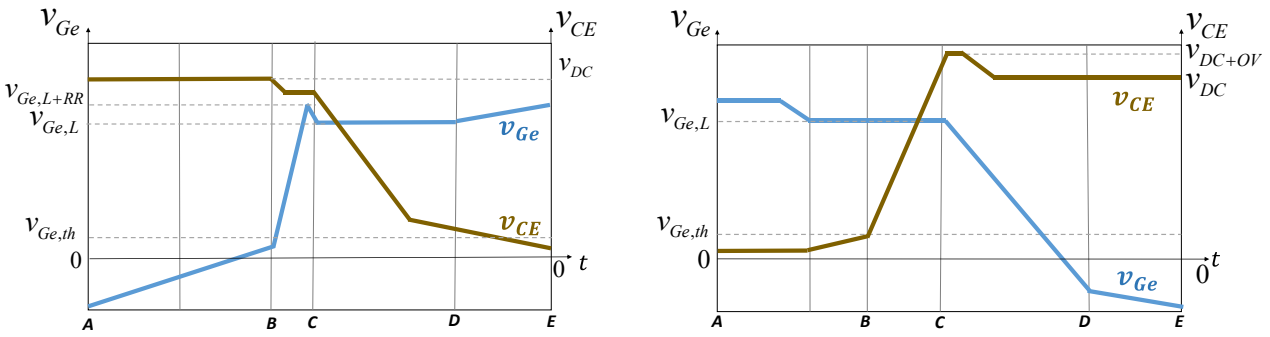
The rate of change of collector-emitter voltage depends actually on Miller capacitance and IGBT gate current which is defined as

$$\frac{dv_{CE}}{dt} = -\frac{V_{GC}}{dt} = -\frac{i_G}{C_{GC}} \tag{2}$$

Figure 2 shows the relations of gate voltage and collector-emitter voltage at turn-on and at turn-off switching intervals. Each interval are divided into characteristic sections which are detailed in Table 1. dv_{CE}/dt always changes when the gate voltage is constant. This switching interval is called Miller Plateau. During the Miller Plateau, the gate voltage (v_{GE}) and so the gate current (i_g) is constant [7, 8]. This is shown with phase B-C at turn-on in Figure 2(a) and phase C-D at turn-off in Figure 2(b). According to (2), dv_{CE}/dt depends on Miller capacitance (C_{GC}) and gate current (i_g) where Miller capacitance is related to IGBT module in which the characteristic value cannot be changed. Therefore, the only control parameter that can change the dv_{CE}/dt can be gate current for CGDs.

Besides (1), the rate of collector current change is calculated as a function of gate current and the input capacitance as given in (3),

$$\frac{di_C}{dt} = g_m \frac{dv_{GE}}{dt} = g_m \frac{i_G}{C_{ies}} \simeq g_m \frac{i_G}{C_{GE}} \tag{3}$$



(a) at turn-on (b) at turn-off

Figure 2. Collector-emitter and gate voltage waveforms for one switching cycle.

Table 1. IGBT turn-on and turn-off processes.

Intervals	Turn-on	Turn-off
(A-B)	Input capacitance C_{GE} is charged.	Input capacitance C_{GE} is discharged.
(B-C)	Gate voltage passes through the $v_{(GE,th)}$. IGBT starts to conduct. v_{CE} starts to decrease.	Constant gate voltage area (Miller Plateau). v_{CE} increases and reaches DC link voltage.
(C-D)	Constant gate voltage area (Miller Plateau). v_{CE} decreases its final minimum value immediately.	v_{CE} overshoots and sits on v+. v_{GE} passes through the $v_{GE,th}$. IGBT stops conducting.
(D-E)	Gate voltage reaches its final positive value.	Gate voltage reaches its final minimum value.

According to (3), the rate of collector current change depends on transconductance of the IGBT, gate current, and the gate-emitter capacitance where g_m and C_{GE} cannot be changed at the driver side. Gate current is again the only control parameter that changes the di_C/dt.

As a result, in CGDs, di_C/dt and dv_{CE}/dt can only be changed by gate resistor. Both di_C/dt and dv_{CE}/dt cannot be changed separately and setting one of them will result in the other one being fixed at a certain value. In order to control the rate of changes independently, they have to be adjusted individually, which cannot be performed in CGDs. An IGBT module with an antiparallel power diode is actually designed to achieve bidirectional current flow. The dynamic behaviours of the power diode are significantly impacting the transient switching of IGBT. Analysing the dynamic characteristics of power diodes shows that the peak reverse recovery current, I_{RR} given in (4), is proportional to the reverse recovery current rate of change, di_R/dt, which is the same as the collector current rate of change also at the commutation of antiparallel diode and the IGBT at turn-on [9].

$$I_{RR} \simeq 2.810^{-6} BV_{BD} \sqrt{I_F di_R/dt} \tag{4}$$

where I_F is diode forward current, BV_{BD} is diode breakdown voltage. The voltage overshoot, v_{OV}, is also proportional to the rate of change of the IGBT collector current during the turn-off and expressed as in (5)

$$v_{OV} = L_s \frac{di_C}{dt} \tag{5}$$

where L_s is the stray inductance of complete circuit.

The overshoot of the collector-emitter voltage occurs at turn-off and current overshoot occurs at turn-on, but all of these stresses that affect the SOA of the IGBT, and EMI issues of the system are related to collector current rate of change, di_C/dt. Decreasing gate resistor to reduce energy losses results in increase of di_C/dt and dv_{CE}/dt together and this leads to increase of overshoots of the IGBT, which is an undesirable situation for the power converters. Overshoots are decreased with increase of gate resistor, but this causes higher energy dissipation which affects the thermal state and the life of the IGBT module. The tradeoffs between EMI issue and switching losses are investigated in many studies such as in [10].

Many studies have been carried out on IGBT gate drive. There are active and closed-loop gate drive methods that change the switching transients by changing gate resistors [11, 12], change gate current parallel with pulse waveform according to feedbacks of collector current and collector-emitter voltage [13–26] and change gate voltage according to different switching periods [27, 28]. Closed-loop gate drive methods that directly change the pulse width modulation (PWM) voltage and thus control the gate current are given in [5, 6, 29–45]. Digital control methods are given in [29–37]. Analog-to-digital controller (ADC) and digital-to-analog controller (DAC) converters are used for feedbacks and the digital control algorithm are achieved in a field programmable gate array (FPGA). These methods have drawbacks of delay in ADC and DAC that affect the switching delay times. Much more effective methods use analog control for the feedback algorithm. With the high bandwith operational amplifiers (OPAMPs), the control loop achieved high accuracy and minimum delays for the switching. These methods are proposed with di_C/dt control only [5, 6, 38], dv_{CE}/dt control only [39–43], and both di_C/dt and dv_{CE}/dt control [44, 45].

In order to overcome the disadvantages of the CGDs, the proposed gate drive method is developed. Since voltage and current transitions take place in different time intervals, di_C/dt and dv_{CE}/dt rates of high power IGBT module can be controlled independently in a closed-loop system. A new type half-bridge 3300V, 450A Hitachi IGBT module (MBM450FS33F) is used to apply the switching algorithm proposed in this paper, which provides some challenge and improved performance against other closed-loop gate drive studies. MBM450FS33F module is a new chip design IGBT which is physically new platform for high power IGBT module category. They have advantages of 75% reduction of inductance, 20% increase in power density and scalable design to increase the current capability of high power converters. The proposed IGBT gate drive control method achieves drive parameters over other closed-loop methods as outlined below:

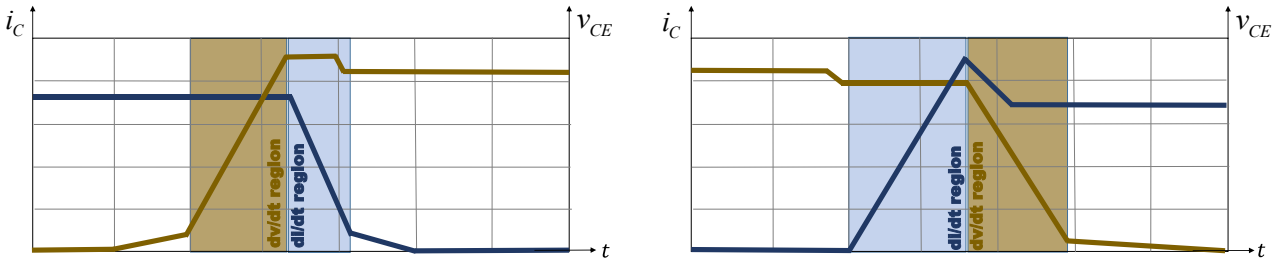
1. High DC bus voltage: Closed-loop analog gate control designs given in the literature switch IGBTs under maximum 1000VDC bus voltage. The proposed control method is studied when DC bus voltage is 1830VDC which is much more critical especially at turn-off. The new method implements effective control with faster turn-off dv_{CE}/dt value.

2. Module scalable design: MBM450S33F IGBT module is designed according to parallel operation to increase the power capacity. The proposed gate drive method controls di_C/dt and this helps to achieve transient equal current sharing (TECS) in paralleling operation.

3. Low inductance sensing: MBM450FS33F IGBT module offers low inductance internal design to reduce oscillations in converter systems. Sensing the voltage slope with high oscillations at the transition time interval over low inductance is a challenge for the active gate drivers. The proposed gate drive senses di_C/dt accurately using parasitic inductance, L_{Ee}, between the main emitter and Kelvin emitter of the IGBT module.

2. Proposed closed-loop gate drive

Ideally, it is clear in Figure 3 that collector-emitter voltage change is zero in the region of collector current change, and collector current change is zero in the region of collector-emitter voltage change, which means that the changes of v_{CE} and i_C do not occur at the same switching transition times.



(a) at turn-off (b) at turn-on

Figure 3. Collector-emitter voltage and collector current behaviours at one switching cycle.

Due to the diode reverse recovery current at turn-on, the collector current, which has a peak in the turn-on state, drops to the normal level while the negative current change coincides with the collector voltage change. Although this situation initially causes change in dv_{CE}/dt, its effect during the turn-on will be very small.

Because switching speeds are independent of each other during the turn-on and turn-off intervals, single controller can easily be used for simultaneous control of dv_{CE}/dt and di_C/dt. This allows separate current and voltage control loops with one controller, which makes the control system simple.

The proposed closed-loop gate drive circuit model that includes di_C/dt and dv_{CE}/dt feedbacks are given in Figure 4, where collector-emitter voltage and Kelvin emitter voltage are used as inputs for the analog controller. The feedback proportional to dv_{CE}/dt is obtained directly from capacitor C_V and resistor R_{F1} which is a phase-lead compensation structure that is used to measure the collector-emitter voltage slope (dv_{CE}/dt). Derivative voltage, calculated as in (6), then feeds the input of Opamp 1.

$$v_{CE,dv_{CE}/dt} = R_{F1} \cdot C_V \cdot dv_{CE}/dt \tag{6}$$

Feedback proportional to di_C/dt feeds input of the Opamp 3 which is obtained from the stray inductance L_{Ee}. Output feedback voltage ($v_{Ee,di_C/dt}$) is filtered and scaled with R-C-R integrator circuit and calculated as in (7) when $R_{FB_6} << R_{FB_5}$. C_{FB} is selected to filter the MHz level voltage oscillations over the L_{Ee}.

$$\begin{aligned} v_{Ee} &= -L_{Ee} di_C/dt, \\ (v_{Ee} - v_{Ee,di_C/dt})/R_{FB_6} &= C_{FB} \cdot dv_{Ee,di_C/dt}/dt \end{aligned} \tag{7}$$

k_v and k_i, given in (8), are two feedback gains that are used to adjust di_C/dt and dv_{CE}/dt. These gains remain constant throughout the entire switching cycle according to desired di_C/dt and dv_{CE}/dt values. Two different control loops are active in successive times over a single PI controller. Although both control loops have separate gains, they operate on the common control reference PWM voltage. Feedback voltages are added to v_{PWM} reference PWM voltage and v_C control voltage occurs after the PI block. PWM control signal (v_{PWM}) remains at the desired constant value at the positive cycle during the transition period of positive di_C/dt and

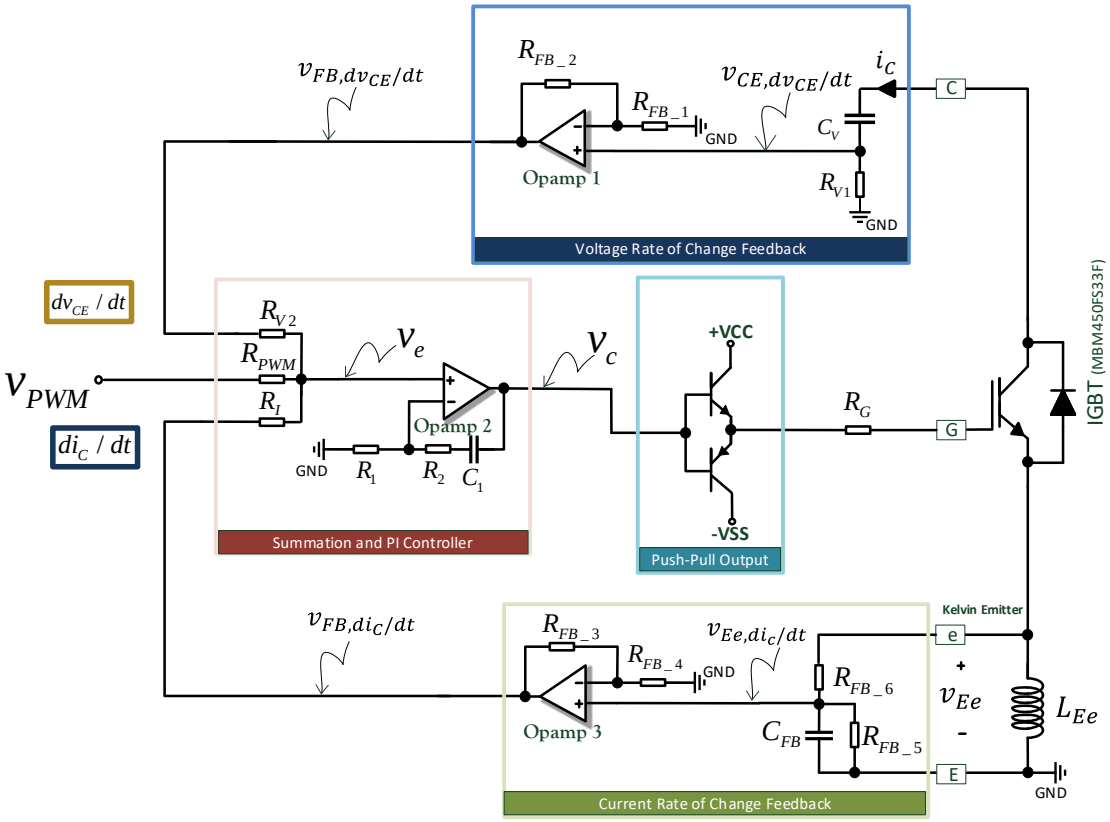


Figure 4. Proposed closed-loop control circuit diagram.

negative dv_{CE}/dt; and during the transition period of negative di_C/dt and positive dv_{CE}/dt, v_{PWM} stays at the required constant value at the negative cycle. $v_{FB,di_C/dt}$ is feedback voltage of di_C/dt, $v_{FB,dv_{CE}/dt}$ is feedback voltage of dv_{CE}/dt as given in (9).

$$k_v = 1 + \frac{R_{FB_2}}{R_{FB_1}} \quad \text{and} \quad k_i = 1 + \frac{R_{FB_3}}{R_{FB_4}} \tag{8}$$

$$\begin{aligned} v_{FB,dv_{CE}/dt} &= k_v \cdot v_{CE,dv_{CE}/dt}, \\ v_{FB,di_C/dt} &= k_i \cdot v_{Ee,di_C/dt} \end{aligned} \tag{9}$$

A control error voltage (v_e) is generated by current and voltage feedbacks that are added to the reference PWM voltage (v_{PWM}) in the closed loop as seen in Figure 5. Because the change intervals of the v_{CE} and i_C are different from each other, their feedback sample voltages occur in succession. They do not affect their control loop and this feature leads to seperate change of di_C/dt and dv_{CE}/dt on their own active intervals.

Error voltage is applied to the PI controller to generate the control voltage (v_c). PI controller can be built by fast operational amplifier where (ideal) gains can be written as in (10). After the PI unit, push-pull drive is used to provide the needed current to drive IGBT module.

$$K_p = 1 + R_2/R_1, \quad K_I = 1 + R_1/C_1 \tag{10}$$

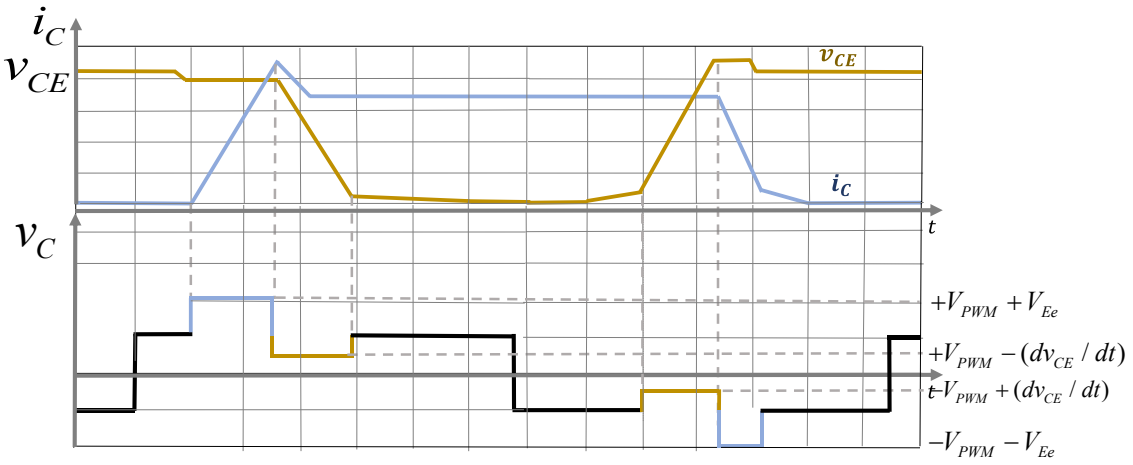


Figure 5. Complete cycle of switching with feedback voltages of di_C/dt and dv_{CE}/dt.

3. Simulations

Double pulse test power circuit and gate drive control circuit is modelled in ANSYS Simplorer. New package 3300V 450A dual IGBT modules have been recently designed by manufacturers. These modules are easy to be used in parallel in power converters with the advantages of high power density and easy scalable features. The dynamic behaviour model of MBM450FS33F IGBT module is generated to use in analysis. v_{GE}-i_C, v_{CE}-i_C, v_F-i_F, Z_{thjc}-t waveforms are used directly from the module datasheet. Parameters which are used to model the IGBT module are listed as in Table 2.

Table 2. Input parameters for IGBT model.

Symbol	Definition	Value
C_{in}	Input capacitance	24nF
C_r	Feedback (miller) capacitance	1nF
R_G	Internal gate resistance	6.2 Ω
L_{G_Ext}	External gate stray inductance	2nH
L_{tot}	Total lead stray inductance	9nH
R_{tot}	Total lead resistance	18 mΩ

The circuit as in Figure 6 is simulated and different situations are investigated in this part. Pulse width is chosen as 10 μs. DC-link voltage v_{DC} is 1800 VDC. System line inductance L_s is 60 nH. The load inductance L_{LOAD} is 1200 μH and its resistance R_{LOAD} is 2 mΩ. Collector current level goes up to 450 A at turn-on interval. As the MBM450FS33f dual IGBT module is selected, its inductance L_{Ee} between kelvin emitter and power emitter is calculated as 3 nH which is used for feedback inductance for di_C/dt. This emitter inductance value is extracted from the IGBT short circuit test waveforms of the manufacturer.

3.1. Load variations in proposed gate control

Collector current changes with different load values. Normally, for the conventional gate drivers, increasing the system load leads collector current to rise that results with the increase of di_C/dt. T_{on} turn-on time

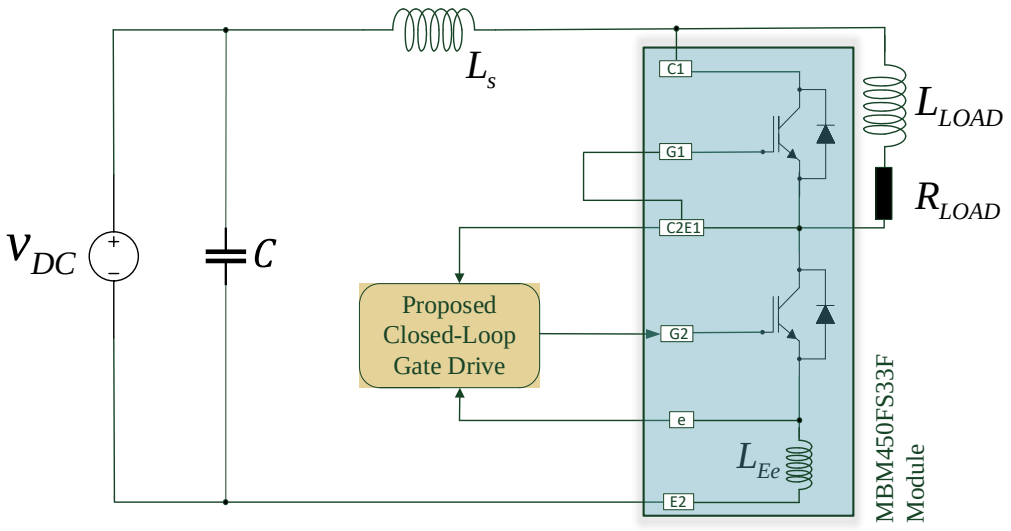
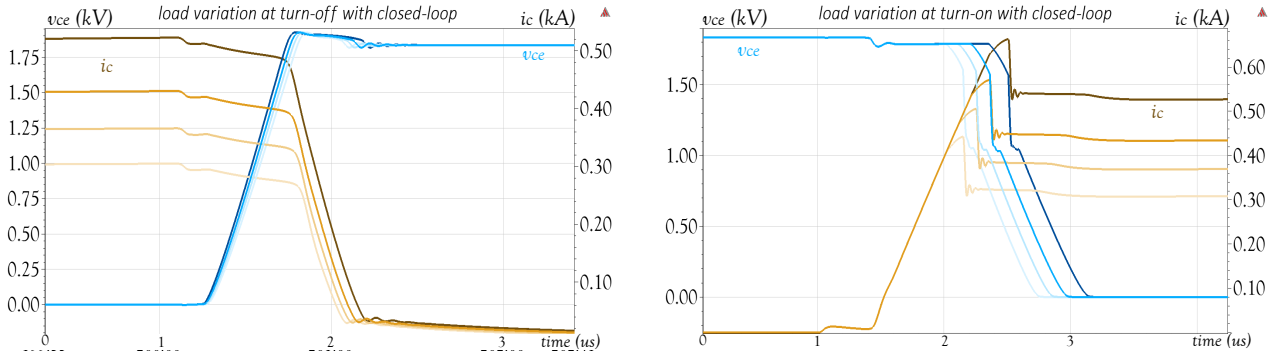


Figure 6. Double pulse test circuit with feedbacks.

increases with the collector current while T_{off} turn-off time decreases with the collector current as depicted in the datasheet of the MBM450FS33F IGBT module.

For the proposed di_C/dt and dv_{CE}/dt closed-loop control, it can be seen from Figures 7a and 7b that load variations do not affect the rates of change of current and voltage. Their rates of change become stable at turn-off and turn-on switching cycles, which means that the load current does not change the electrical stresses during the switching instant.



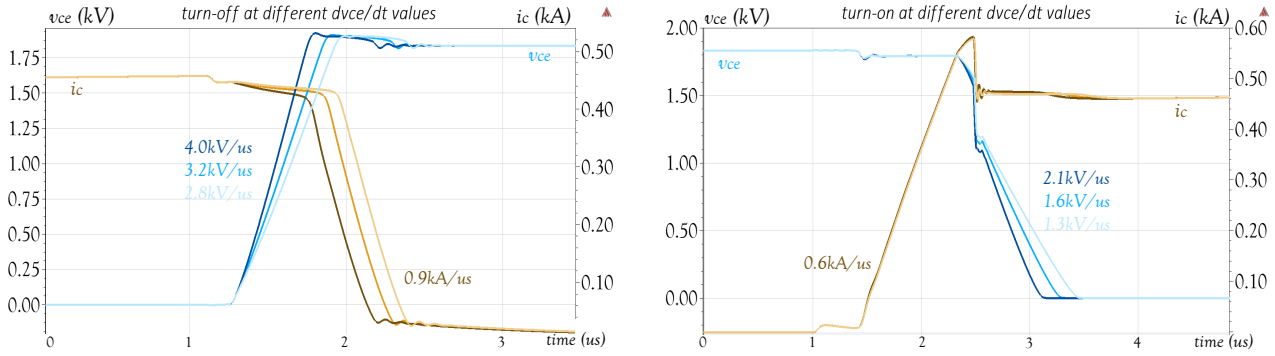
(a) at turn-off. (b) at turn-on.

Figure 7. Simulation results of v_{CE} and i_C waveforms for load variation at turn-off and turn-on.

3.2. di_C/dt and dv_{CE}/dt independent control

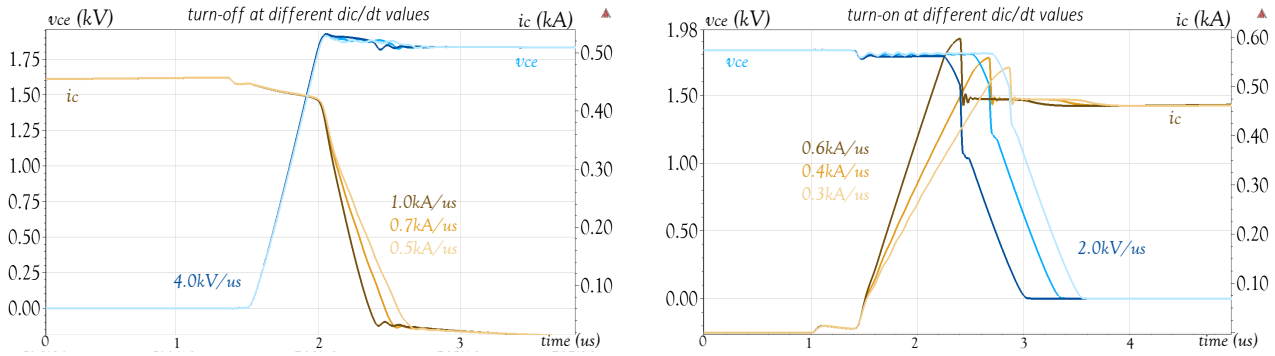
To explain the basic function of the proposed independent control, feedback gains are changed in simulations and all i_C and v_{CE} waveforms are curved together. Figures 8a and 8b shows the turn-off and turn-on switching transitions for a variation of dv_{CE}/dt when the di_C/dt is kept constant. By changing the feedback resistor of R_{FB_2} in the dv_{CE}/dt feedback loop, it is seen that only dv_{CE}/dt changes with $4kV/\mu s$, $3.2kV/\mu s$, and $2.8kV/\mu s$ at turn-off and $2.1kV/\mu s$, $1.6kV/\mu s$, and $1.3kV/\mu s$ at turn-on. di_C/dt stays constant with $0.9kA/\mu s$ at turn-off and $0.6kA/\mu s$ at turn-on simultaneously.

Figures 9a and 9b show the turn-on and turn-off switching transitions for a variation of di_C/dt when the dv_{CE}/dt is kept constant. By changing the feedback resistor of R_{FB_3} in the di_C/dt feedback loop, it is seen that only di_C/dt is changing with $1kA/\mu s$, $0.7kA/\mu s$, and $0.5kA/\mu s$ at turn-off and $0.6kA/\mu s$, $0.4kA/\mu s$, and $0.3kA/\mu s$ at turn-on. dv_{CE}/dt stays constant with $4kV/\mu s$ at turn-off and $2kV/\mu s$ at turn-on in all switching cycles. In conventional gate drives, peak of the collector-emitter voltage v_{CE} normally increases when the di_C/dt increases at turn-off, whereas the overshoot of v_{CE} is same in all di_C/dt values with the proposed closed-loop gate drive as seen in Figure 9a.



(a) at turn-off (b) at turn-on

Figure 8. Simulation results of v_{CE} and i_C waveforms for (a) turn-off and (b) turn-on at different dv_{CE}/dt values when di_C/dt is constant.



(a) at turn-off. (b) at turn-on.

Figure 9. Simulation results of v_{CE} and i_C waveforms for (a) turn-off and (b) turn-on at different di_C/dt values when dv_{CE}/dt is constant.

3.3. Comperative study with CGDs

The following study is derived in order to show the benefits of the proposed control against open loop, i.e. resistive CGD. Comparison is done with the same 3.3kV, 450A IGBT half-bridge model (Hitachi MBM450FS33F) based on switching losses. Turn-off and turn-on waveforms of switching transients for i_C and v_{CE} are shown in Figures 10a and 10b, respectively. Left column shows the closed-loop control, rigth column shows the CGDs waveforms at turn-off and turn-on. Waveforms are derived to show the controllability of the current and voltage change speed in the current study. dv_{CE}/dt is set to 1.8kV/μs and gate resistors of the CGD are adjusted for the same dv_{CE}/dt value with the closed-loop drive for turn-on analysis. In CGD, di_C/dt is measured as

0.4kA/μs. dv_{CE}/dt is set to 3.3kV/μs and gate resistors of the CGD are adjusted for the same voltage slope as the closed-loop drive for turn-off analysis. In CGD, di_C/dt is measured as 0.4kA/μs. However, contrary to CGDs, due to the independent control of current, di_C/dt is set to be 0.8kA/μs at turn-on and 1.1kA/μs at turn-off for the proposed closed-loop control. In addition to illustrate the slope differences of di_C/dt, Figure 10 shows also the energies at turn-on and turn-off. The proposed gate drive enables decrease of switching energies significantly by its ability to set di_C/dt faster than CGDs. As a result, the comperative study shows that di_C/dt can be changed while dv_{CE}/dt is constant by using the closed-loop gate drive technique which is not possible with CGDs. Restrictions of SOA operation and EMI can be solved to decrease power losses of the IGBT module with independent control of voltage and current slope which is described in detail in the following section.

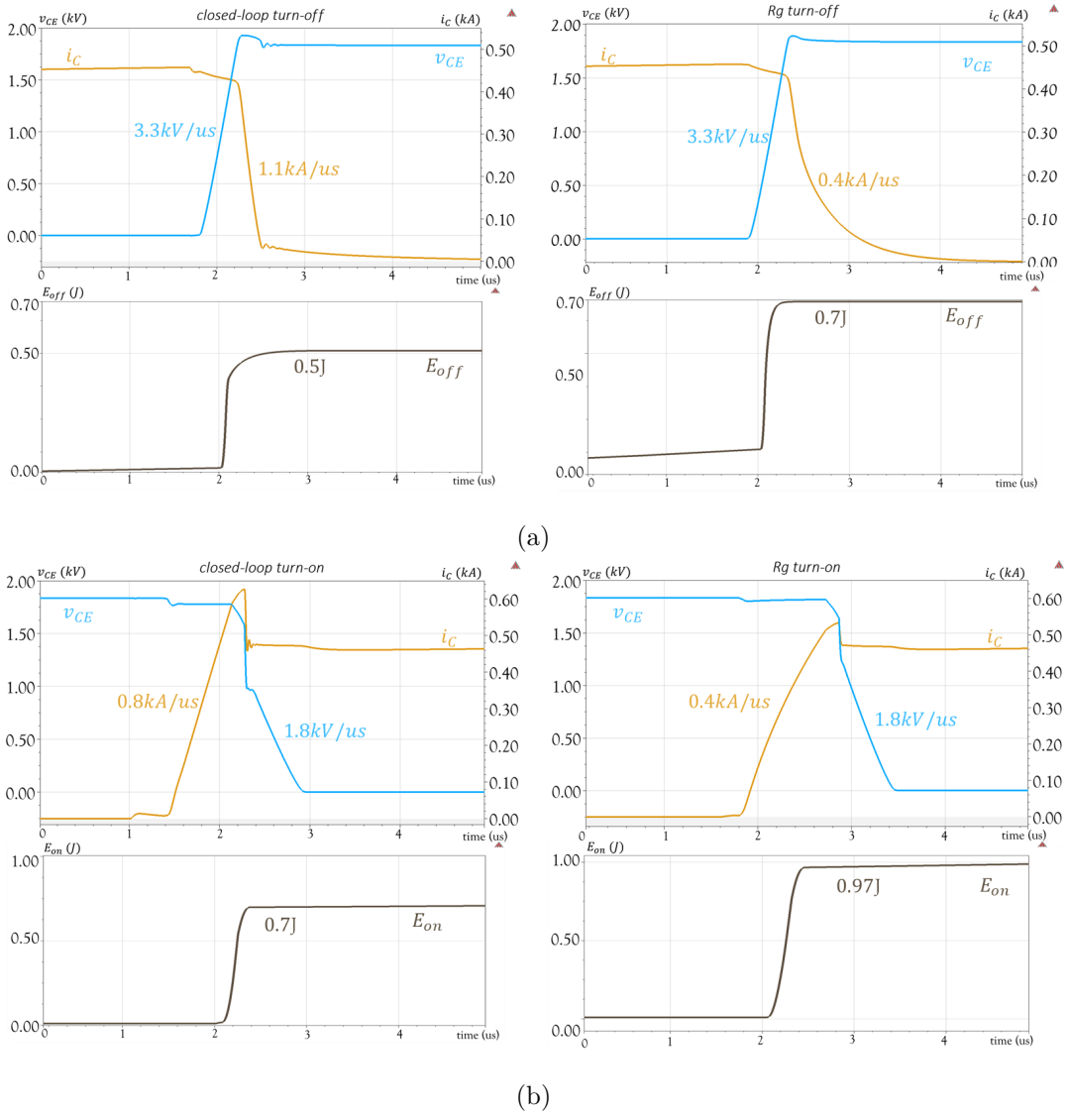


Figure 10. Simulation comparison of CGD and closed-loop voltage and current waveforms for (a) turn-off and (b) turn-on at different di_C/dt values when dv_{CE}/dt is constant.

3.4. dv_{CE}/dt control with constant di_C/dt

The critical issue for the proposed gate drive is the ability to change dv_{CE}/dt without changing di_C/dt by using feedback gain k_v. Therefore, energy losses of the IGBT module in the operation of high power energy conversion can be decreased without the increase of overshoots of the v_{CE} and i_C at turn-off and turn-on, respectively. Also, EMI issue is not affected. The relationship of the switching system parameters of the proposed gate control is seen in Figure 11.

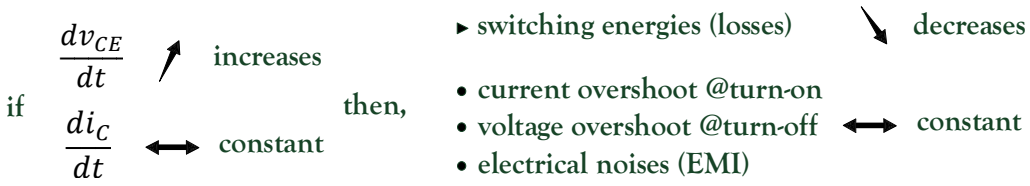


Figure 11. Proposed algorithm's effect over the electrical characteristics.

In order to describe the effect of the proposed switching algorithm over the energy losses, mathematical expressions are given [46]. The voltage and current waveforms are considered to be linear to simplify the switching energy expressions. Discrete change areas of the voltage and current waveforms make energy expressions dv_{CE}/dt and di_C/dt related basically as given in (11).

Turn-on switching energies are expressed in three parts which are voltage slope related, $E_{on,dv_{CE}/dt}$, current slope related, $E_{on,di_C/dt}$, and reverse recovery related, $E_{on,irr}$. Turn-off switching energies are expressed in three parts which are voltage slope related, $E_{off,dv_{CE}/dt}$, current slope related, $E_{off,di_C/dt}$, and tail current related, $E_{off,tail}$ for turn-off switching interval. It can be seen in (12) that by the proposed method, increase of the dv_{CE}/dt leads to decrease of the E_{on} and E_{off} in which di_C/dt is constant.

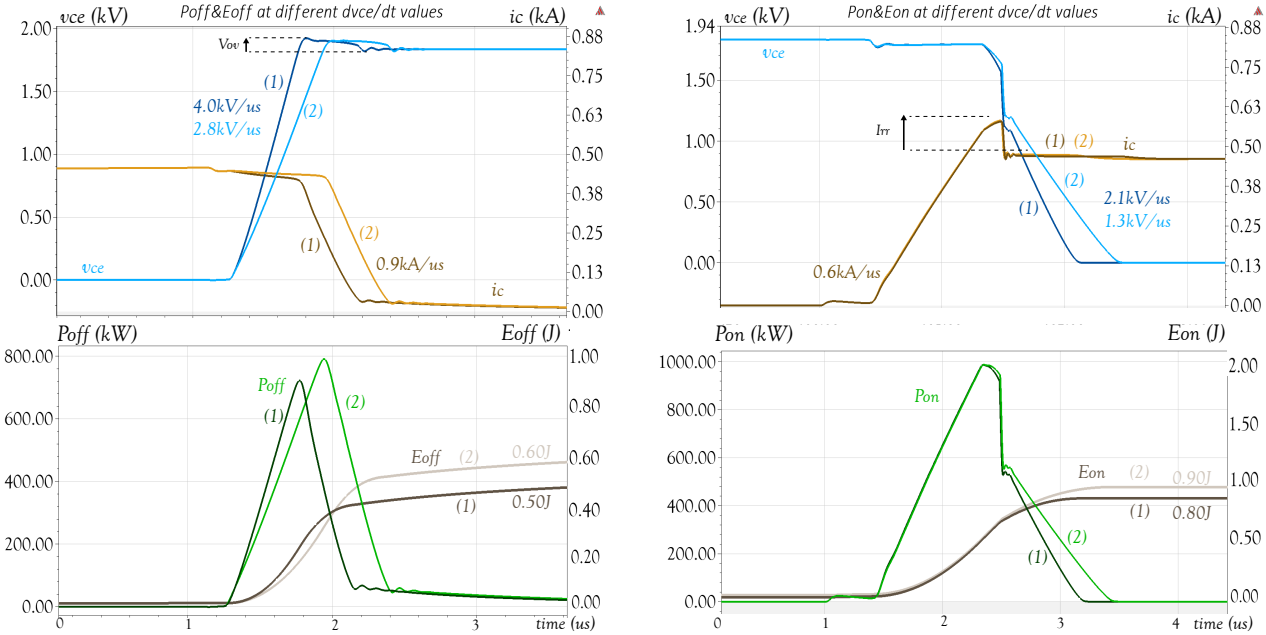
$$\begin{aligned} E_{on} &= E_{on,dv_{CE}/dt} + E_{on,di_C/dt} + E_{on,irr} \\ E_{off} &= E_{off,dv_{CE}/dt} + E_{off,di_C/dt} + E_{off,tail} \end{aligned} \tag{11}$$

$$\begin{aligned} E_{on} = \underbrace{\frac{i_L.v_{DC}}{2} \cdot \frac{v_{DC}}{\mid dv_{CE}/dt \mid} \cdot (1-\sigma_s)^2}_{E_{on,dv_{CE}/dt}} + \underbrace{\frac{i_L.v_{DC}}{2} \cdot \frac{i_L}{\mid di_C/dt \mid} - \frac{1}{2} \cdot L_s \cdot i_L^2}_{E_{on,di_C/dt}} \\ + \underbrace{(i_L \cdot \sqrt{\frac{Q_{rr}}{\mid di_C/dt \mid}} + Q_{rr}) \cdot v_{DC} \cdot (1-\sigma_s)^2}_{E_{on,irr}} \end{aligned} \tag{12}$$

$$E_{off} = \underbrace{\frac{i_L.v_{DC}}{2} \cdot \frac{v_{DC}}{\mid dv_{CE}/dt \mid} \cdot (1+\sigma_s)^2}_{E_{off,dv_{CE}/dt}} + \underbrace{\frac{i_L.v_{DC}}{2} \cdot \frac{i_L}{\mid di_C/dt \mid} + \frac{1}{2} \cdot L_s \cdot i_L^2}_{E_{off,di_C/dt}} + \underbrace{v_{DC} \cdot Q_t}_{E_{off,tail}}$$

where v_{DC} is the DC-link voltage, Q_{rr} is the stored reverse recovery charge of the diode, σ_s is the ratio between voltage drop across L_s and voltage v_{DC} during the current slope, and Q_t is the stored charge extracted by the tail current.

Figures 12a and 12b show the main principle idea of the proposed hard switching method clearly. E_{on} and E_{off} change according to change in dv_{CE}/dt with the di_C/dt kept constant. It is clearly seen that, by the proposed control technique, without changing di_C/dt, switching energy losses can be adjusted. As di_C/dt is constant, collector-emitter voltage peak (v_{ov}) and collector current peak (i_{rr}) stay constant at turn-off and turn-on, respectively.



(a) at turn-off (b) at turn-on

Figure 12. Simulation results of E_{off} and E_{on} at different dv_{CE}/dt values when di_C/dt is constant.

4. Conclusion

A new type of closed-loop gate drive technique based on di_C/dt and dv_{CE}/dt feedback control is proposed in this paper. Different change time intervals of current and voltage allows dv_{CE}/dt and di_C/dt to be controlled with the same PWM reference gate voltage. Control of current and voltage slopes independently leads to reduction of the switching energy losses for a constant di_C/dt while changing dv_{CE}/dt. Constant di_C/dt limits the collector-emitter voltage (v_{CE}) and collector current (i_C) overshoots and conducted and radiated-mode noise levels in the power conversion system. Otherwise, in CGDs, there has to be a trade-off between losses and safety operation parameters like EMI, voltage and current overshoots.

The control method is implemented using the double pulse test circuit and model of a new type nHPD^2 series MBM450FS33F Hitachi high power IGBT is used for the simulations. Feedbacks and control side of the closed-loop gate drive are implemented using analogue circuits. The new closed-loop control method achieves very high speed switching at high voltage ($>$1800VDC) especially at turn-off transient in which voltage overshoot occurs. With the high-accuracy current slope control over very low internal inductance sensing, the proposed closed-loop control enables paralleling of MBM450FS33F IGBT modules that have scalable design to increase power in a converter system. CGDs employed in different IGBT modules with same gate resistors results in various levels of safe operating area issues. Unlike the conventional methods, the closed-loop gate drive allows hardware to be used with different models of IGBT modules without changing gate resistors.

Despite its advantages, the proposed gate drive control may have some limitations at the implementation. The system can be sensitive to electronic component tolerances because the proposed method is composed of analogue circuits. Proper selection of operational amplifiers should be done to avoid control limitations, such as voltage drift due to the temperature, slew rate and common mode rejection ratio. Since turn-on and turn-off transitions are in nanosecond levels, high analogue control bandwidth has to be used to achieve accurate dv_{CE}/dt and di_C/dt feedback signals. PCB layout design is critical to avoid electrical noises because of high current switching at high voltage.

As a future research, the proposed control method will be tested with different IGBT models and performance of the method will be analysed. In addition, transfer functions of the whole closed-loop system will be conducted to confirm the new control method. Some traction converter-based system disturbances such as IGBT thermal effect and instantaneous DC bus voltage fluctuations will be modelled to test the stability of the proposed control method.

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