Indirect Feedback Compensation of CMOS Op-Amps

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Abstract—**This paper presents the design of CMOS op-amps using indirect feedback compensation technique. The indirect feedback compensation results in much faster and low power op-amps, significant reduction in the layout size and better power supply noise rejection.**

Keywords- CMOS, indirect feedback compensation, miller compensation, operational amplifier.

I. INTRODUCTION

CMOS Op-amps are one of the important building blocks of modern integrated systems. The op-amps have been commonly stabilized using direct (or Miller) compensation in the past. This method achieves dominant pole compensation by pole-splitting due to Miller effect [1]. However, the connection of the compensation capacitance (C_c) between the outputs of the gain stages, leads to a right hand plane (RHP) zero. The RHP zero decreases the phase margin, and thus requires a larger C_c to compensate the op-amp. This in turn results in a decrease in the unity gain frequency ($f_{un}= g_{m1}/2\pi C_c$). Also the op-amp stability degrades when the load capacitance C_L becomes comparable to C_c as C_L must be much less than $g_{m2}C_c/g_{m1}$ for stability [2].

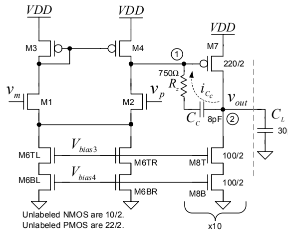


Figure 1. Two stage op-amp with miller (direct) compensation and zero-nulling resistor.

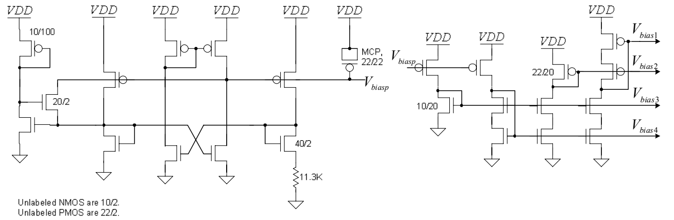


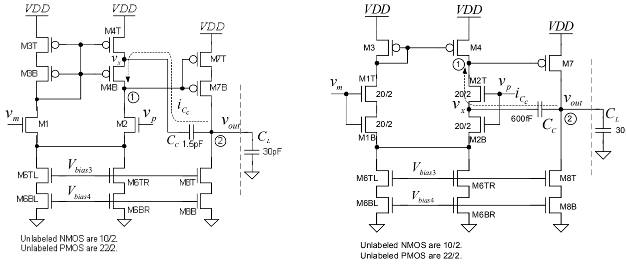
Figure 2. The self-biased reference ciruit used for baising the op-amps.

This paper introduces indirect feedback compensation technique which leads to much faster op-amps with significant reduction in the layout size. Fig. 1 shows a direct (Miller) compensated op-amp with an RHP zero-nulling resistor R_z. The op-amps presented in this paper are designed with AMI's CN5 (0.5µm) process, biased with a regulated drain BMR (Beta Multiplier Reference) bias circuit shown in fig.2 [3], and drive up to 30pF off-chip load.

II. INDIRECT FEEDBACK COMPENSATION

In a direct compensated two-stage op-amp, the current feedback through the compensation capacitor C_c can be approximated as $i_{C_c} \approx v_{out}/(1/j\omega C_c)$. By indirectly feeding this current to the output of the diff-amp, pole splitting and hence op-amp compensation can be achieved. Also by avoiding connecting the compensation capacitor directly to the output of the diff-amp, the right hand plane (RHP) zero is eliminated.

The compensation current can be fed indirectly to the output of the diff-amp using, 1) a common gate amplifier [2], 2) a cascode structure, and 3) MOSFETs laid out in series with one device operating in triode region [3].



(a) (b)

Figure 3. Two stage op-amp topologies with indirect compensation.

Fig. 3 shows op-amp topologies in which the feedback current is indirectly fed back to an internal low-impedance node. The low impedance node is created by laying out the MOSFETs in series, in which one of the devices is in triode. The topology in fig.3b results in a better PSRR (Power Supply Rejection Ratio) due to isolation of compensation capacitance from *VDD* and ground noise. As a guideline, the feedback current must always be fed back to a low-impedance internal node for high speed op-amps.

III. ANALYTICAL MODEL

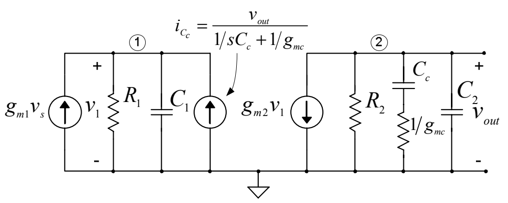


Figure 4. Model used to estimate bandwidth with indirect compensation.

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To determine the frequency response of the op-amp with indirect feedback compensation, the generalized model seen in fig. 4 is employed.

Summing currents at node 1 gives,

$$-g_{m1}v_s + \frac{v_1}{R_1 \| \frac{1}{sC_1}} + \overbrace{\frac{v_{out}}{1/sC_1 + 1/g_{mc}}}^{i_{C_c}} = 0 \qquad (1)$$

where 1/g_{mc} is the resistance looking into the node v_x, where feedback current is injected.

For the output node (node 2), $v_{out} = -g_{m2}v_1X_2$, where $X_2 = R_2 \| X_{C_L} \| (R_c + X_{C_c})$ is the total impedance on node 2, $R_c = 1/g_{mc}$ and $R_a = 1/g_{m1}$. (2)

On solving equations 1&2, the op-amp frequency response is estimated as,

$$\frac{v_{out}}{v_s} = \frac{-A_v\left(1+\frac{jf}{f_z}\right)}{\left(1+\frac{jf}{f_1}\right)\left(1+\frac{jf}{f_2}\right)\left(1+\frac{jf}{f_3}\right)}, \text{ where} \qquad (3)$$

$$f_z = \frac{g_{mc}}{2\pi.C_c}, \text{ which is a left hand plane (LHP) zero,} \qquad (4)$$

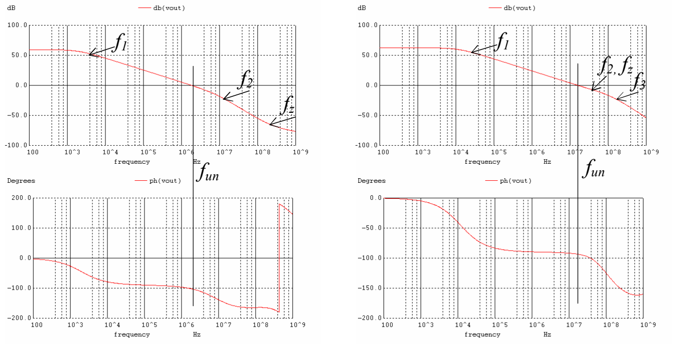
$$f_1 = \frac{1}{2\pi.g_{m2}R_1R_2C_c}, \qquad (5)$$

$$f_2 = \frac{g_{m2}R_1C_c}{2\pi.C_L(R_cC_c + R_1C_1)} \approx \frac{g_{m2}C_c}{2\pi.C_LC_1}, \text{ and} \qquad (6)$$

$$f_3 = \frac{R_cC_c + R_1C_1}{2\pi.R_1C_1R_cC_c} \approx \frac{1}{2\pi.R_cC_C}. \qquad (7)$$

The unity gain frequency (gain-bandwidth) of the op-amp is

$$f_{un} \approx f_1A_v = \frac{g_{m1}R_1g_{m2}R_2}{2\pi.g_{m2}R_1R_2C_c} = \frac{g_{m1}}{2\pi.C_c} \; (\approx f_z \text{ if } g_{m1} \approx g_{mc}). \qquad (8)$$

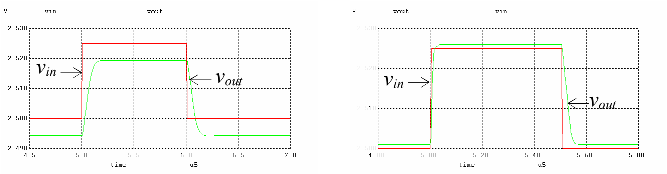


Direct (Miller) compensation

Indirect feedback compensation

Figure 5. Magnitude and phase responses of the opamps with direct (fig. 1) and indirect feedback (fig. 3b) compensation.

Fig. 5 shows the simulated frequency response for a direct (fig. 1) and an indirect feedback compensated op-amp (fig. 3b). The LHP zero (f_z) adds to the phase response and enhances the speed of the op-amp. Intuitively, at high speeds the phase shift through C_c causes the output signal to feed back and add to the signal at node 1. This positive feedback enhances the speed of the op-amp. The location of second pole (f_2) is at a considerably higher frequency. The net result is that, a higher value of unity gain frequency (f_{un}) can be set without affecting the stability of the op-amp. Moreover the load capacitance can be considerably large for a given phase or gain margin [3]. Thus the indirect feedback compensation results in much faster op-amp circuits and consumes significantly less layout area at the same power. The compensation capacitance value is reduced by 4 to 10 times, when indirect feedback compensation is used [4]. Also, the indirect feedback compensated op-amps are low power as the second stage need not be boosted much to push f_2 away from f_{un}.



Direct compensation, t_s=300ns

Indirect compensation, t_s=50ns

Figure 6. Step responses of an opamp with direct and indirect compensation.

Fig. 6 compares the step responses and settling times (t_s) for direct and indirect compensated op-amps and confirms that the latter is much faster than the former.

IV. PROGRESS AND FUTURE WORK

Two and three stage Op-amps with direct and indirect compensation are designed and being fabricated on a chip using AMI's CN5 process. The fabricated op-amps will be tested and the results will be compared with the analytical model.

V. CONCLUSION

The indirect feedback compensation is a practical and superior technique for compensation of op-amps and results in faster and low power op-amps with much smaller layout size. The indirect feedback compensation can also be extended to three (or more) stage op-amps [3].

REFERENCES

[1] P. R. Gray and R. G. Meyer, "MOS Operational Amplifier Design: A Tutorial Overview," *IEEE Journal of Solid-State Circuits*, vol. 17, pp. 969-982, Dec. 1982.

[2] B. K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 18, pp. 629-633, Dec. 1983.

[3] R. J. Baker, *CMOS: Circuit Design, Layout and Simulation, 2nd ed.* Boise, ID: Wiley-IEEE, 2005, pp. 531-538.

[4] R. J. Baker, "Design of High-Speed CMOS Op-Amps for Signal Processing," *IEEE/EDS WMED,* April, 2005.