Indirect Finite Control Set Model Predictive Control of Modular Multilevel Converters

Mohsen Vatani, *Student Member, IEEE,* Behrooz Bahrani, *Member, IEEE,*
Maryam Saeedifard, *Senior Member, IEEE,* and Morten Hovd, *Senior Member, IEEE*

Abstract—The modular multilevel converter (MMC) is a potential candidate for medium/high-power applications, specifically for high-voltage direct current transmission systems. One of the main challenges in the control of an MMC is to eliminate/minimize the circulating currents while the capacitor voltages are maintained balanced. This paper proposes a control strategy for the MMC using finite control set model predictive control (FCS-MPC). A bilinear mathematical model of the MMC is derived and discretized to predict the states of the MMC one step ahead. Within each switching cycle, the best switching state of the MMC is selected based on evaluation and minimization of a defined cost function. The defined cost function is aimed at the elimination of the MMC circulating currents, regulating the arm voltages, and controlling the ac-side currents. To reduce the calculation burden of the MPC, the submodule (SM) capacitor voltage balancing controller based on the conventional sorting method is combined with the proposed FCS-MPC strategy. The proposed FCS-MPC strategy determines the number of inserted/bypassed SMs within each arm of the MMC while the sorting algorithm is used to keep the SM capacitor voltages balanced. Using this strategy, only the summation of SM capacitor voltages of each arm is required for control purposes, which simplifies the communication among the SMs and the central controller. This paper also introduces a modified switching strategy, which not only reduces the calculation burden of the FCS-MPC strategy even more, but also simplifies the SM capacitor voltage balancing algorithm. In addition, this strategy reduces the SM switching frequency and power losses by avoiding the unnecessary switching transitions. The performance of the proposed strategies for a 20-level MMC is evaluated based on the time-domain simulation studies.

Index Terms—Bilinear model, calculation load reduction, circulating current control, model predictive control (MPC), modular multilevel converter (MMC).

I. INTRODUCTION

THE MODULAR multilevel converter (MMC) has become the most promising converter topology for medium/high voltage applications, specifically for the high-voltage direct current (HVDC) converter stations. Compared to other multilevel converters, the MMC is modular and scalable, which can conceptually meet any voltage level requirements. Furthermore, it can provide a superior harmonic performance as the output voltage is built based upon stacking up of a large number of identical submodules (SMs), resulting in a sinusoidal voltage waveform with less filtering efforts.

One of the main technical challenges associated with the control of an MMC is the choice of its pulse width modulation (PWM) strategy along with the control of its internal dynamics, i.e., circulating currents and SM capacitor voltages. Over the past few years, various PWM and control strategies have been proposed/investigated for the MMC [1]–[9]. Among them, model predictive control (MPC)-based strategies, compared to the other strategies, include the nonlinearity of the MMC dynamics in the control while providing a fast dynamic response.

The finite control set MPC (FCS-MPC) strategy has been applied to a wide range of power converters [10]. The main idea behind the FCS-MPC strategy is to use the finite number of switching states of a converter to calculate a predefined cost function associated with the MMC control objectives. The switching state that results in the minimum value for the cost function is selected as the best switching state of the converter within the next switching cycle. The FCS-MPC strategy has an acceptable computational load for majority of power converters [11]–[14]. However, its real-time application to the MMC with a large number of SMs, which is the case for medium/high-voltage applications, is impeded.

One of the first attempts to use the FCS-MPC strategy to control the MMC is reported in [15] and [16], in which one step ahead prediction of the ac-side current, circulating currents, and SM capacitor voltages is calculated for all possible combination of the switching states, and the switching state that results in the minimum value for a defined cost function is selected. In [17] and [18], a current predictive method with a long prediction horizon is used to control the load currents within a predetermined boundary around their references while minimizing the SM capacitor voltage variations and circulating currents. Furthermore, by accounting for the number of the switching transitions in the defined cost function, the average switching frequency is minimized as well. In [19], the FCS-MPC strategy is examined for the control of the MMC under unbalanced conditions with reduced sensitivity to disturbances and measurement noises. In [20], a direct MPC strategy is used for the control of MMC-STATCOMs while in [21], the experimental results of the MPC strategy is compared with the

cascaded proportional-integral controller for a medium-voltage MMC with two SMs in each arm.

The main drawback of the aforementioned MPC-based strategies is that in the selection process of the best switching state, the cost function is calculated for all possible combinations of the switching states. As the number of SMs increases, the number of switching options increases exponentially, which makes the real-time implementation of the MPC strategy challenging.To address this issue, three independent predictive controllers are proposed in [22] for the ac-side currents, circulating currents, and SM capacitor voltages along with three different cost functions to select the best switching states. Although this method reduces the calculation load, the impact of each predictive controller on the other control variables is not investigated. As the control variables depend upon each other, this method does not provide the flexibility of maintaining a trade-off among ac-side current tracking error, minimizing circulating current and capacitor voltage ripple.

In this paper, a new FCS-MPC strategy is proposed to control the MMC. The proposed strategy determines the number of inserted/bypassed SMs within each arm of the MMC while the conventional sorting algorithm is used to keep the SM capacitor voltages balanced. A bilinear model of the MMC is developed to predict the behavior of the MMC states one step ahead. Using this model, only the summation of SM capacitor voltages of each arm is required for control purposes, which simplifies the communication between hundreds of the SMs and the central controller. A cost function is defined to select the best number of inserted SMs within each arm to minimize the ac-side current tracking error and circulating currents and to maintain the SM capacitor voltages at their references. This paper also introduces a modified switching strategy, which not only decreases the calculation burden of the FCS-MPC strategy even more, but also simplifies the sorting algorithm for the voltage balancing of the SMs and avoids unnecessary switching transition of each SM. Performance of the proposed FCS-MPC strategy for a 20-level MMC is evaluated based on time-domain simulation studies.

The rest of this paper is organized as follows. In Section II, the bilinear mathematical model of the MMC is derived and formulated. In Section III, the proposed indirect FCS-MPC strategy is presented in details. Section IV reports the simulation results and Section V concludes this paper.

II. BILINEAR MODEL OF THE MMC

The circuit diagram of a three-phase MMC is shown in Fig. 1 in which each phase-leg consists of two arms, i.e., an upper arm (represented by subscript, "u") and a lower arm (represented by subscript, "l"). Each arm is comprised of N series-connected, nominally identical, half-bridge SMs, one inductor, and one resistor. Each SM can provide two voltage levels at its terminals, i.e., zero or $v_{Cmi,j}$, $m = u, l$; $i = 1, 2, \ldots, N$, $j = a, b, c$, depending on the state of its two complementary switches S_1 and S_2. The resistor R models the power losses within each arm of the MMC. The series inductor L limits the short-circuit current of the MMC and removes the high-frequency harmonics of the arm currents. Considering a
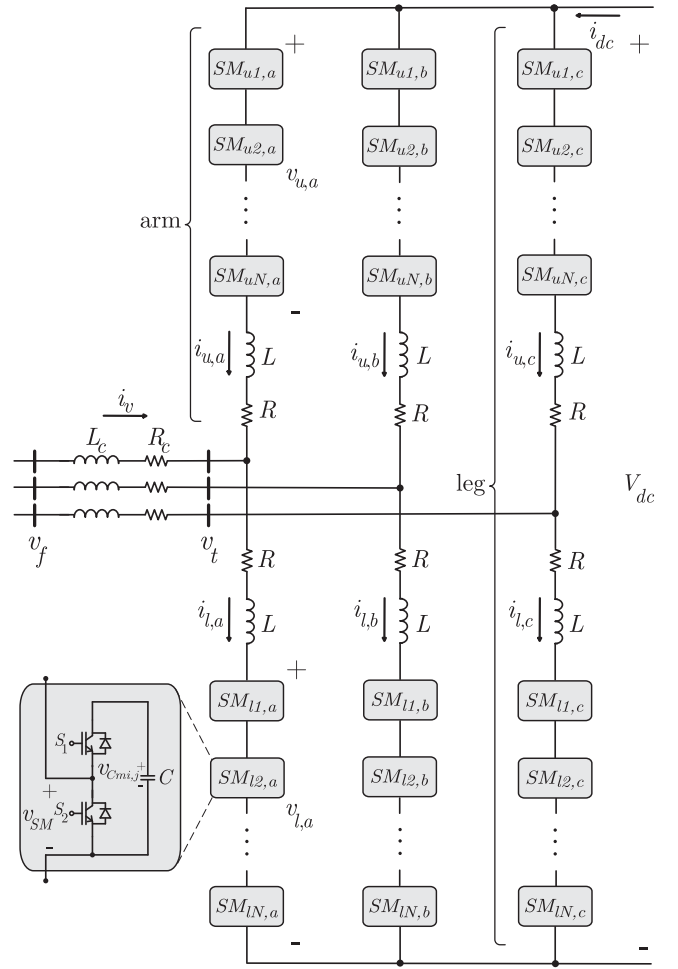

Fig. 1. Circuit diagram of the MMC.

fictitious midpoint in the dc side of Fig. 1, the mathematical equations, governing the dynamic behavior of MMC in phase j, are as follows:

$$\frac{V_{dc}}{2} - v_{u,j} - Ri_{u,j} - L\frac{di_{u,j}}{dt} + R_c i_{v,j} + L_c\frac{di_{v,j}}{dt} - v_f = 0 \quad (1)$$

$$-\frac{V_{dc}}{2} + v_{l,j} + Ri_{l,j} + L\frac{di_{l,j}}{dt} + R_c i_{v,j} + L_c\frac{di_{v,j}}{dt} - v_f = 0. \quad (2)$$

Based on Fig. 1, the arm currents $i_{u,j}$ and $i_{l,j}$ can be expressed as follows:

$$i_{u,j} = \frac{-i_{v,j}}{2} + i_{cir,j}$$

$$i_{l,j} = \frac{i_{v,j}}{2} + i_{cir,j} \quad (3)$$

where $i_{cir,j}$ is the circulating current flowing through the three phases of the MMC and is calculated by

$$i_{cir,j} = \frac{i_{u,j} + i_{l,j}}{2}. \quad (4)$$

Adding (1) and (2) and substituting $i_{v,j}$ for $i_{l,j} - i_{u,j}$ from (3) yield

$$\frac{di_{v,j}}{dt} = \frac{-(R + 2R_c)}{L + 2L_c}i_{v,j} + \frac{v_{u,j} - v_{l,j}}{L + 2L_c} + \frac{2v_{f,j}}{L + 2L_c}. \quad (5)$$

Subtracting (2) from (1) and substituting $2i_{\text{cir},j}$ for $i_{u,j} + i_{l,j}$ from (4), the dynamic equation of circulating current in each phase is expressed as

$$\frac{di_{\text{cir},j}}{dt} = -\frac{R}{L}i_{\text{cir},j} - \frac{1}{2L}\left(v_{u,j} + v_{l,j}\right) + \frac{1}{2L}V_{\text{dc}}. \quad (6)$$

Each arm voltage is generated based on inserting and bypassing a specific number of SMs. A controller should determine the number of inserted SMs within each arm by calculating the insertion indices $n_{u,j}$ and $n_{l,j}$ for the upper and lower arms, respectively, to maintain the voltages $v_{u,j}$ and $v_{l,j}$ at their reference values. When an SM is inserted into the circuit, depending on the direction of the corresponding arm current, its capacitor voltage is changed. Therefore, a capacitor voltage balancing algorithm is required to keep the SM capacitor voltages balanced. This algorithm should select $n_{u,j}$ ($n_{l,j}$) of the N SMs within the upper (lower) arm to be inserted, depending on the direction of arm current and capacitor voltages.

Assuming that the SM capacitor voltages are well balanced at their reference values, i.e., $v_{m,j}^{\Sigma}/N$ where $v_{m,j}^{\Sigma}$ represents the summation of all capacitor voltages in arm m of phase j, the arm voltage is expressed by

$$v_{m,j} = \frac{n_{m,j}v_{m,j}^{\Sigma}}{N}. \quad (7)$$

The dynamics of the total capacitor voltages of each arm is expressed by

$$\frac{dv_{m,j}^{\Sigma}}{dt} = \frac{i_{m,j}}{C_{m,j}^{e}} = \frac{n_{m,j}.i_{m,j}}{C} \quad (8)$$

where C_m^e is the effective equivalent capacitance of inserted SMs in arm m. Substituting for $i_{u,j}$ and $i_{l,j}$ from (3) to (8), the following equations are deduced:

$$\frac{dv_{u,j}^{\Sigma}}{dt} = -\frac{n_{u,j}}{2C}i_{v,j} + \frac{n_{u,j}}{C}i_{\text{cir},j} \quad (9a)$$

$$\frac{dv_{l,j}^{\Sigma}}{dt} = \frac{n_{l,j}}{2C}i_{v,j} + \frac{n_{l,j}}{C}i_{\text{cir},j}. \quad (9b)$$

Substituting for $v_{u,j}$ and $v_{l,j}$ from (7) in (5) and (6), the external and internal dynamics of the MMC are represented by

$$\frac{di_{v,j}}{dt} = \frac{-(R+2R_c)}{L+2L_c}i_{v,j} + \frac{n_{u,j}v_{u,j}^{\Sigma} - n_{l,j}v_{l,j}^{\Sigma}}{N(L+2L_c)} + \frac{2v_{f,j}}{L+2L_c} \quad (10a)$$

$$\frac{di_{\text{cir},j}}{dt} = -\frac{R}{L}i_{\text{cir},j} - \frac{1}{2L}\left(n_{u,j}v_{u,j}^{\Sigma} + n_{l,j}v_{l,j}^{\Sigma}\right) + \frac{1}{2L}V_{\text{dc}}. \quad (10b)$$

Based on (9b) and (10b), the state space equation of the MMC can be expressed by (11) where $x = \begin{bmatrix} i_{v,j} & i_{\text{cir},j} & v_{u,j}^{\Sigma} & v_{l,j}^{\Sigma} \end{bmatrix}^T$

TABLE I
NUMBER OF POSSIBLE CONTROL ACTIONS FOR
THE FCS-MPC STRATEGIES

N	3	5	7	10	15	20	50	100
direct FCS-MPC	20	252	3432	10^5	10^8	10^{11}	10^{29}	10^{59}
indirect FCS-MPC	16	36	64	121	256	441	2601	10201

is the state vector and $u = \begin{bmatrix} u_1 & u_2 \end{bmatrix}^T = \begin{bmatrix} n_{u,j} & n_{l,j} \end{bmatrix}^T$ is the input vector. Equation (11) as shown at the bottom of the page is in the standard form of a continuous bilinear system represented by [23]

$$\dot{x}(t) = Ax(t) + \sum_{i=1}^{2} B_i x(t)u_i(t) + d(t). \quad (12)$$

Based on (12) and assuming a sampling time of T_s, the discrete-time bilinear model of the MMC, based on a forward Euler approximation, is obtained as

$$\begin{aligned} x_{k+1} = &(T_s A + I)x_k + T_s B_1 x_k u_{1,k} \\ &+ T_s B_2 x_k u_{2,k} + T_s d_k. \end{aligned} \quad (13)$$

Equations (12) and (13) show that the MMC is a nonlinear multi input multi output system where the nonlinearity consists of the products between the states and inputs. Furthermore, as the number of inputs is lower than the number of controlled states, the controller design is not a trivial task. On the other hand, the first state has a sinusoidal reference and transforming the bilinear model to the rotating dq frame results in time varying B_1 and B_2 matrices, which are difficult to handle [24]. As a result, the classical controllers are not sufficiently well-suited for MMC control. In this paper, an indirect FCS-MPC based strategy is developed to control the bilinear dynamics of the MMC.

III. FCS-MPC FORMULATION

In the FCS-MPC strategy, a predefined cost function is calculated one step ahead for all possibilities in the control action, and the best control action, which minimizes the cost function, is selected. However, an MMC, especially with a large number of SMs, has a significant number of switching states, making the implementation of the FCS-MPC strategy challenging as the computational burden becomes a major issue. Although a direct FCS-MPC strategy for an MMC-based back-to-back HVDC system is introduced in [15], the number of switching combinations, shown in Table I, grows exponentially as the number of SMs increases. In the direct FCS-MPC strategy, within each sampling period, N combinations of

$$\dot{x}(t) = \underbrace{\begin{bmatrix} -\frac{R+2R_c}{L+2L_c} & 0 & 0 & 0 \\ 0 & -\frac{R}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{A} x(t) + \underbrace{\begin{bmatrix} 0 & 0 & \frac{1}{(L+2L_c)N} & 0 \\ 0 & 0 & -\frac{1}{2NL} & 0 \\ -\frac{1}{2C} & \frac{1}{C} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}}_{B_1} x(t)u_1 + \underbrace{\begin{bmatrix} 0 & 0 & 0 & -\frac{1}{(L+2L_c)N} \\ 0 & 0 & 0 & -\frac{1}{2NL} \\ 0 & 0 & 0 & 0 \\ \frac{1}{2C} & \frac{1}{C} & 0 & 0 \end{bmatrix}}_{B_2} x(t)u_2 + \underbrace{\begin{bmatrix} \frac{2v_f(t)}{L+2L_c} \\ \frac{V_{\text{dc}}(t)}{2L} \\ 0 \\ 0 \end{bmatrix}}_{d} \quad (11)$$

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

4

IEEE TRANSACTIONS ON SMART GRID

$2N$ options, i.e., C_N^{2N}, in each phase are considered to select the best one.

To resolve this issue, an indirect FCS-MPC strategy can be used to determine the insertion indices $n_{u,j}$ and $n_{l,j}$ while a sorting algorithm carries out the SM capacitor voltage balancing task. By considering the developed bilinear model of the MMC in (11), not only the power flow is controlled, but also the circulating currents and capacitor voltages are regulated at their reference values. In the proposed strategy, the number of control actions is equal to $(N+1)^2$, since there exist $N+1$ voltage levels to be selected in each arm. As listed in Table I, compared with the direct MPC strategy in [15], the number of switching states of the proposed indirect FCS-MPC is significantly reduced. Furthermore, in the direct FCS-MPC strategy, the FCS-MPC controller should collect all of the SM capacitor voltages to select the next inserted SMs. This requires the transmission of all SM capacitor voltage information to the main controller processor. However, in the proposed indirect FCS-MPC strategy, a field programmable gate array (FPGA) can be used as a local controller to execute the sorting algorithm without involving the central controller. Consequently, instead of collecting a large number of measured SM capacitor voltages, only their summation is sent to the central controller. The central controller, which is typically a digital signal processing (DSP), executes the indirect FCS-MPC strategy by receiving the required measurements from the FPGA. Subsequent to the execution of the indirect FCS-MPC strategy in the DSP, only the insertion indices are sent to the FPGA. This arrangement results in a lower communication delay and easier installation and maintenance of the system.

A. Indirect FCS-MPC Strategy Using the Bilinear Model

This subsection presents the indirect FCS-MPC strategy for the selection of the best insertion index of each arm. The bilinear model of the MMC presented in Section II is used to predict the behavior of the MMC one step ahead. This prediction is performed for all possible insertion indices in each arm. Subsequently, the index that minimizes the cost function is selected. The cost function for each phase is defined as follows:

$$J_j = c_1 \left| i_{v,j,\mathrm{ref}} - i_{v,j} \right| + c_2 \left| i_{\mathrm{cir,ref}} - i_{\mathrm{cir},j} \right| \\ + c_3 \left| v_{\mathrm{dc,ref}} - v_{u,j}^\Sigma \right| + c_4 \left| v_{\mathrm{dc,ref}} - v_{l,j}^\Sigma \right| \quad (14)$$

where each state and its reference are evaluated at time step $k+1$, and the coefficients c_1 to c_4 are weighting factors, which determine the relative importance/priority of each control objective. All the states are predicted within time step $k+1$ using (13) and the measurements of the states within time step k.

The first term in the cost function (14) represents the tracking error of the ac-side current. The ac-side reference current is generated based on power equations in the rotating dq frame [25]. The second term in (14) is to minimize the ac components of the circulating current. The reference for the circulating current is calculated based on the real power

transferred to the dc side by

$$I_{\mathrm{dc,ref}} = -\frac{P}{V_{\mathrm{dc,ref}}}, \quad I_{\mathrm{cir,ref}} = \frac{I_{\mathrm{dc,ref}}}{3}. \quad (15)$$

The third and fourth terms in (14) are to maintain the summation of the SM capacitor voltages of each arm at its reference value. The sorting algorithm balances the individual SM capacitor voltages. This means that the SM capacitors have the same voltages within each time instance. As a result, by regulating the summation of all SM capacitor voltages at its reference value, not only the magnitude of SM capacitor voltage ripple decreases, but also its average voltage is regulated at V_{dc}/N.

The following steps summarize the proposed indirect FCS-MPC strategy:

1) one step ahead prediction of the states using (13) for all possible values of $n_{u,j}$ and $n_{l,j}$, i.e., $(N+1)^2$ options in total;
2) selection of the insertion indices $n_{u,j}$ and $n_{l,j}$ that minimize the cost function (14);
3) carrying out the capacitor voltage balancing task based on the sorting algorithm and the insertion indices.

B. Calculation Burden Reduction

Although the proposed indirect FCS-MPC strategy, compared to the direct FCS-MPC strategy, significantly reduces the calculation burden, it still should deal with a large number of switching options for an MMC with hundreds of SMs in each phase-leg. In this subsection, a method to reduce the number of switching options in the FCS-MPC strategy is proposed.

The reduction of the number of switching control actions within each time step is achieved by considering only the neighboring index values with respect to their previously applied values. This consideration is sensible as multistep jumps in the number of inserted SMs are not desirable. Consequently, there is no need to consider all the options for the insertion index and a limited neighborhood for the current index suffices. In this paper, at most one change in the insertion index of each arm is considered within each time step, which reduces the number of possible actions options to 9 for each leg. This, in turn, simplifies the sorting algorithm as well. Having only one possible change in the insertion index, instead of sorting all of the SM voltages, it is sufficient to find the minimum/maximum of the SM voltages, which is quite straightforward. If the calculated new index is the same as the previous one, no change in the state of the inserted SMs occurs. If the new index is one level higher than the previous one, it is sufficient to insert one of the bypassed SMs while keeping all the inserted SMs. In this situation, based on the direction of the corresponding arm current, two decisions can be made. If the current is positive (charging capacitors), the SM with the minimum voltage among the bypassed ones is turned on. If the current is negative (discharging capacitors), the SM with the maximum capacitor voltage among the bypassed ones is turned on. If the new index is lower than its previous value, it is sufficient to turn off one of the inserted SMs without changing the status of

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.
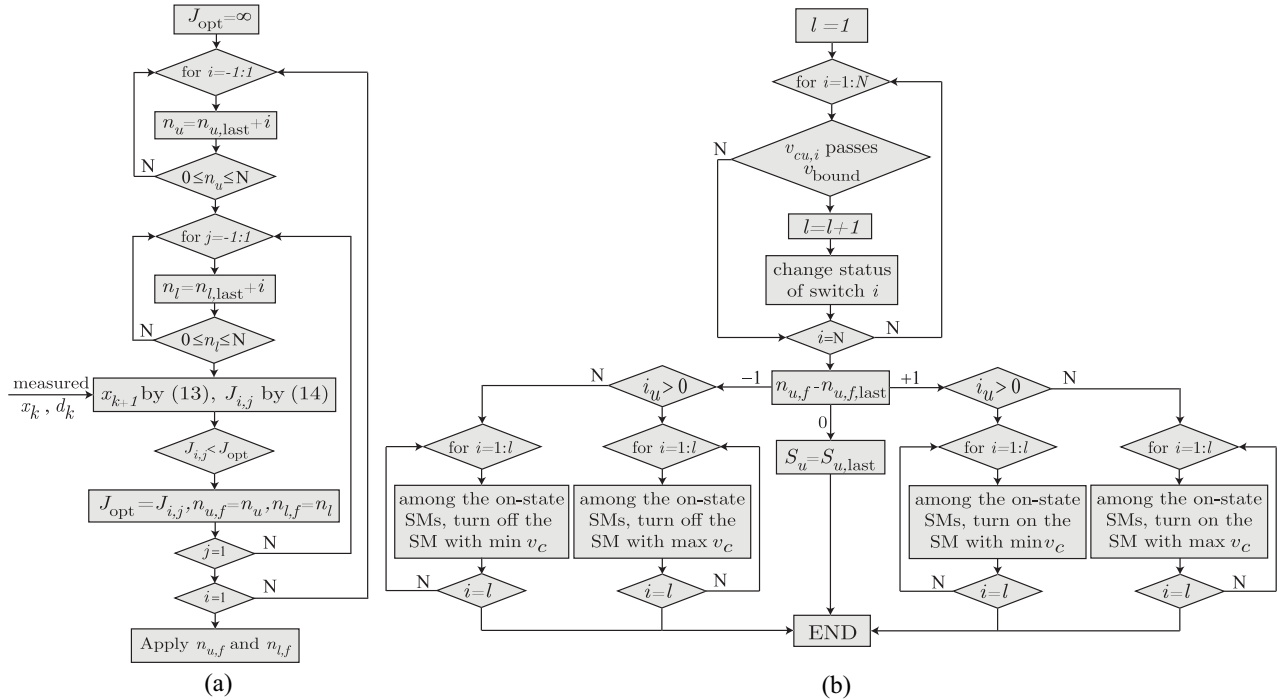
VATANI *et al.*: INDIRECT FCS-MPC OF MMC

5

Fig. 2. Implementation block diagram of the reduced indirect FCS-MPC strategy with voltage tolerance band. (a) Insertion index calculation. (b) Modified sorting algorithm.

bypassed ones. In this case, for a positive current, the SM with the maximum voltage among the inserted ones is turned off while for a negative current, the SM with the minimum voltage among the inserted ones is turned off.

Applying this strategy, within each execution period of the FCS-MPC strategy, the switching status of at most one SM is changed. As a result, the maximum switching frequency of each SM is limited to f_s/N where $f_s = 1/T_s$. However, by considering the fact that the insertion index does not change within some of the execution periods of the FCS-MPC strategy, the average switching frequency of the SMs drops below $f_s/2N$ in the steady state.

With adopting this method to insert/bypass SMs, it is possible that the SM that stays inserted or bypassed for a long time, experiences a larger voltage variation than the desired tolerance band. In this paper, the acceptable peak-to-peak value of the SM capacitor voltage tolerance band is set to 2%, that is

$$\left| \frac{v_{\text{bound},m,j} - v_{\text{mean},m,j}}{v_{\text{mean},m,j}} \right| < 0.01$$

where

$$v_{\text{mean},m,j} = \frac{v_{m,j}^{\Sigma}}{N}. \qquad (16)$$

To control the voltage tolerance band of capacitor voltages, the SM capacitor voltages are measured/monitored. If an SM capacitor voltage exceeds its voltage band, its switching state is changed, and in the selection process of the sorting algorithm, its voltage is also considered in selecting the maximum or minimum SM voltages. The procedure to implement the proposed control strategy is summarized in the diagram of

TABLE II
SIMULATION PARAMETERS

Parameter	Value
MMC nominal power (base power)	50 MVA
AC system nominal voltage (base voltage)	138 kV
Short circuit ratio at the PCC	5
AC source inductance (L_S)	150 mH
Nominal frequency	60 Hz
Transformer voltage rating (T)	138 kV/30 kV
Transformer power rating	55 MVA
Transformer inductance	0.05 pu
Transformer resistance	0.01 pu
Grid side converter inductance (L_C)	5 mH
Grid side converter resistance (R_C)	0.03 Ω
Arm inductance (L)	3 mH
Arm resistance (R)	1 Ω
Submodule capacitance (C)	14000 μF
DC side reference voltage	60 kV
Number of SMs per arm (N)	20
Sampling time (T_s)	100 μs

Fig. 2. By considering the capacitor voltage tolerance band, the switching frequency of each SM is increased. However, the magnitude of the SM capacitor voltage fluctuation is maintained within an acceptable range.

IV. SIMULATION RESULTS

To evaluate the performance of the proposed control strategies, a three-phase MMC with 20 SMs per arm, as shown in Fig. 3 is simulated. The parameters of the simulated system are listed in Table II.

The set-points for the transferred real and reactive power at $t = 0$ are set to 25 MW and 0 MVar, respectively. A real power flow reversal command is applied at $t = 0.12$ s by changing the reference of real power to $P_{\text{ref}} = -25$ MW. This scenario

6

IEEE TRANSACTIONS ON SMART GRID

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.
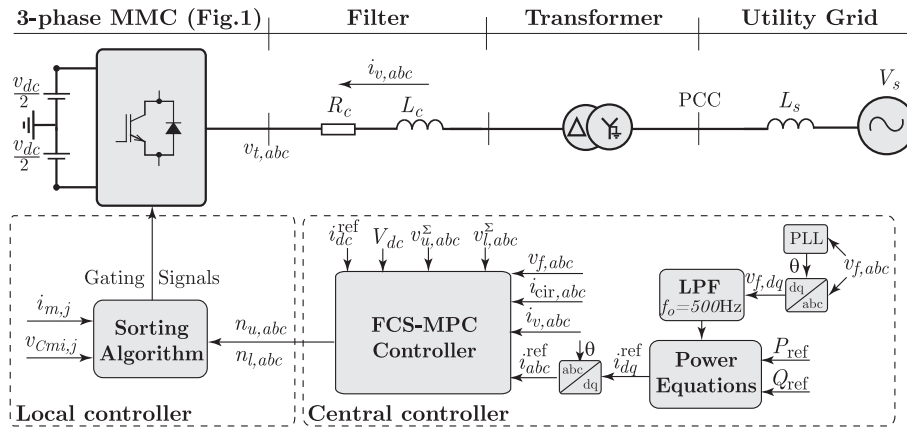
Fig. 3. Control block diagram of the MMC.

is applied in all case studies in the following subsections. The coefficients of the cost function in (14) are set to $c_1 = 1$, $c_2 = 0.5$, and $c_3 = c_4 = 0.005$.

A. Indirect FCS-MPC Strategy

The simulation results of the indirect FCS-MPC strategy, presented in Section III-A, are shown in Fig. 4. The conventional sorting algorithm [6] is used to maintain the SM capacitor voltages balanced while the FCS-MPC strategy calculates the insertion indices for the upper and lower arms of each phase.

Fig. 4 shows the dynamic response of the MMC to the power flow reversal command. Fig. 4(a) shows the corresponding changes in the transferred real and reactive power. The summation of the SM capacitor voltages in the upper arm of phase a ($v_{u,a}^{\Sigma}$) is shown in Fig. 4(b). The ripple magnitude of the summation of all capacitor voltages around the reference value is less than 1.5%, even during the real power reversal transient. Fig. 4(c) shows the circulating current of phase a ($i_{\text{cir},a}$), which follows its reference during steady state and transient. Fig. 4(d) shows phase-a current, which tracks its sinusoidal reference fairly quickly. The SM capacitor voltages of the upper arm in phase a ($v_{Cu,a}$) are shown in Fig. 4(e). As shown, the sorting algorithm maintains all the capacitor voltages balanced. The 2% tolerance band of the SM capacitor voltages defined in (16), is shown with the dashed lines. The results shown in Fig. 4 verifies that the indirect FCS-MPC strategy is able to minimize the ac-side current tracking error and circulating current, and to maintain the SM capacitor voltages at their references.

B. Reduced Indirect FCS-MPC Strategy

The simulation results of the reduced indirect FSC-MPC strategy, presented in Section III-B, are shown in Fig. 5. In this strategy, within each sampling period, at most one change in each insertion index is allowed. The SM capacitor voltages are kept balanced based on using the sorting algorithm till $t = 0.055$ s, when the voltage balancing is carried out by changing the status of the SM with minimum
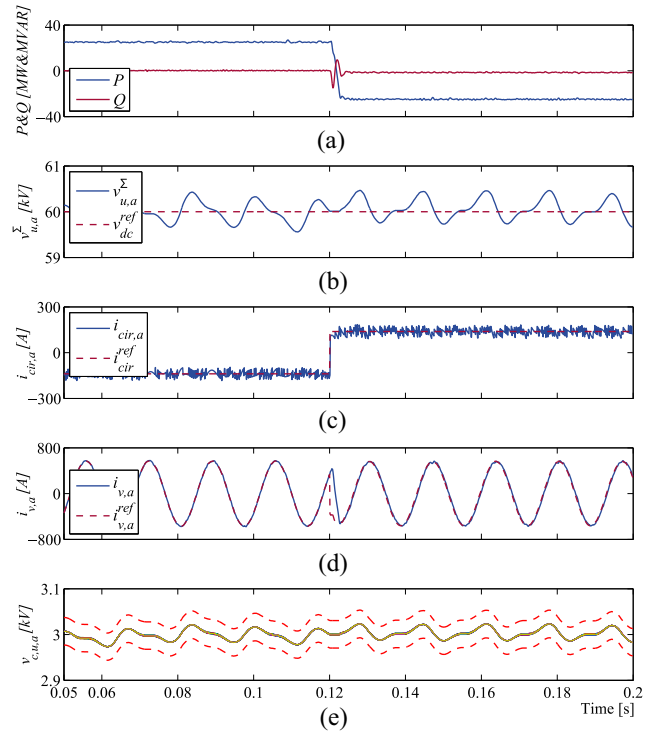

Fig. 4. Simulation results of the indirect FCS-MPC strategy. (a) Real and reactive power. (b) Summation of the SM capacitor voltages in the upper arm of phase a. (c) Phase-a circulating current. (d) Phase-a current. (e) SM capacitor voltages in the upper arm of phase a.

or maximum voltage as explained in Section III-B, afterwards. Although the switching frequency of the SMs and the calculation burden of the FCS-MPC strategy decrease significantly, all the waveforms still closely follow their references within an acceptable range. The waveforms shown in Fig. 5 are identical to those in Fig. 4. In Fig. 5(a), the transient time for power reversal increases to 7 ms, compared to 5 ms for the indirect FCS-MPC strategy. The tolerance band of the SM capacitor voltage summation, as shown in Fig. 5(b), increases to 1.8% peak to peak, while the circulating current, shown in Fig. 5(c), is not changed. In addition, subsequent to the transient, it takes around 5 ms for the ac-side current in Fig. 5(d) to follow its reference, compared to 3 ms for the

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.
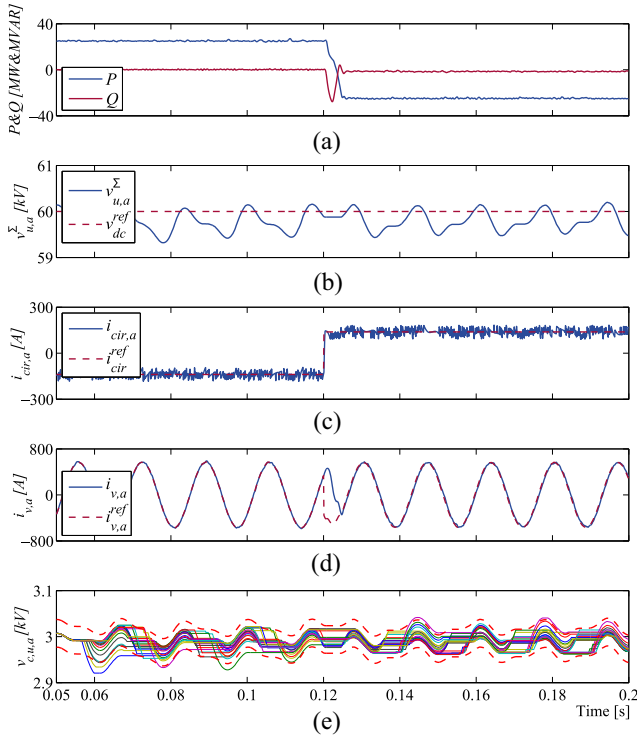
VATANI *et al.*: INDIRECT FCS-MPC OF MMC

7

Fig. 5. Simulation results of the reduced indirect FCS-MPC strategy. (a) Real and reactive power. (b) Summation of the SM capacitor voltages in the upper arm of phase *a*. (c) Phase-*a* circulating current. (d) Phase-*a* current. (e) SM capacitor voltages in the upper arm of phase *a*.
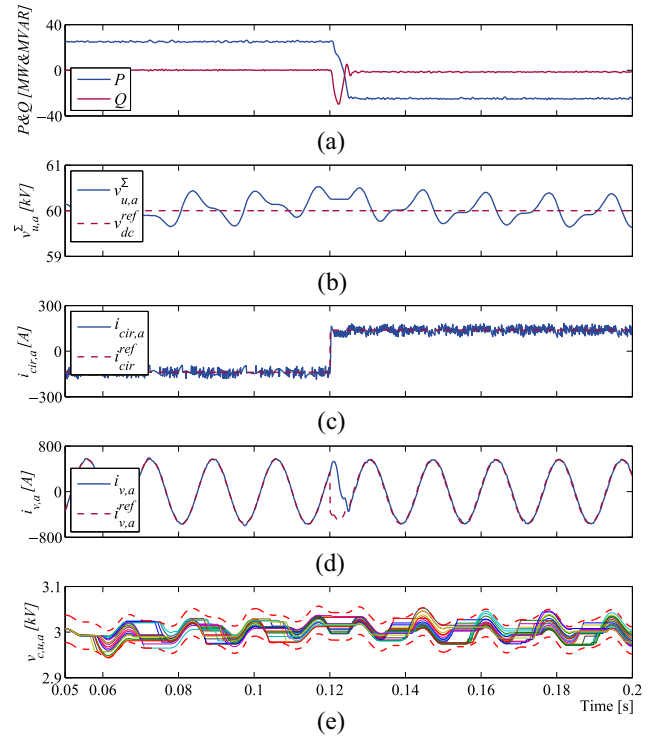

Fig. 6. Simulation results of the reduced indirect FCS-MPC strategy with 2% tolerance band on the capacitor voltage ripples. (a) Real and reactive power. (b) Summation of the SM capacitor voltages in the upper arm of phase *a*. (c) Phase-*a* circulating current. (d) Phase-*a* current. (e) SM capacitor voltages in the upper arm of phase *a*.

indirect FCS-MPC strategy. The capacitor voltages of all SMs in upper arm of phase *a* are shown in Fig. 5(e). Although the SM voltages are closely maintained at their reference value, i.e., $V_{u,a}^{\Sigma}/N$, the magnitude of the capacitor voltages of some of the SMs exceed the 2% tolerance band depicted by dashed lines. The results of Fig. 5 verify satisfactory performance of the reduced indirect FCS-MPC strategy in response to power reversal command, with sacrificing the magnitude of the SM capacitor voltage variations.

C. Reduced Indirect FCS-MPC Strategy With Tolerance Band on the SM Capacitor Voltages

The simulation results of the reduced FCS-MPC strategy by considering a 2% tolerance band on the magnitude of the SM capacitor voltages are shown in Fig. 6. The waveforms shown in Fig. 6 are identical to those in Fig. 5. By controlling the voltage tolerance band of the capacitor voltages, which results in a slight increase in the switching frequency of the SMs, the transition time of the power reversal decreases to 6 ms, the ripple component of $v_{u,a}^{\Sigma}$ decreases to 1.7% peak to peak, and the transition time of the ac-side current decreases to 4 ms. In addition, Fig. 6(e) shows that all SM capacitor voltages are kept within the 2% tolerance band. The results of Fig. 5 verify the capability of reduced indirect FCS-MPC strategy with the tolerance band control in maintaining the SM capacitor voltages within the acceptable range while providing satisfactory performance in the control of other state variables.

D. Power Losses, Switching Frequency, and Voltage Tracking Error Comparison

The performance of the proposed strategy, in terms of power losses, switching frequency, SM capacitor voltage tracking error, and total harmonic distortion (THD), are compared with the FCS-MPC strategies presented in [22] and circulating current suppressing controller (CCSC) presented in [2]. The comparison results are listed in Table III. The estimated switching and conduction losses are calculated as the percentage of the transferred real power based on the IGBT 5SNA1300K450300 datasheet information. The applied loss calculation method is based on the characteristic curves of the semiconductor devices and simulated currents and voltages as described in [26]. The junction temperature is set to $T_j = 125\,°C$. The average switching frequency of the MMC for all strategies is calculated as the average switching frequency of all SMs from the activation time of the reduced FCS-MPC strategy, i.e., $t_1 = 0.055\,s$, till the end of simulation time, i.e., $t_2 = 0.25\,s$ as follows:

$$f_{\text{ave}} = \sum_{j=a,b,c} \sum_{m=l,u} \sum_{i=1}^{20} f_{mi,j} \qquad (17)$$

where $f_{mi,j}$ is the average switching frequency of *i*th SM in the arm *m* of phase *j*.

The average deviation of the SM capacitor voltages from their mean value $v_{\text{mean},m,j}$ provided in (16), at sampling instant

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

8   IEEE TRANSACTIONS ON SMART GRID

TABLE III
COMPARISON OF POWER LOSSES, SWITCHING FREQUENCY,
VOLTAGE TRACKING ERROR, AND THD FOR
VARIOUS MMC CONTROL STRATEGIES

Method	Cond. loss%	Sw. loss%	f_{ave}	v_{mean} error	v_{ref} error	THD %
Indirect FCS-MPC	0.1867	2.61	3531	0.3084	17.12	2.04
C_1 [22] $\lambda = 0$	0.1808	2.45	3403	0.3866	26.95	2.00
C_1 [22] $\lambda = 10$	0.1803	1.75	2349	0.9817	28.22	2.24
CCSC [2]	0.1838	2.68	3521	0.3138	23.38	2.55
Reduced FCS-MPC	0.1861	0.136	174	10.07	22.13	2.18
Reduced $\Delta V < 2\%$	0.1861	0.153	187	9.03	21.34	1.96
C_2 [22]	0.1801	0.274	264	10.91	31.62	2.22

k, is calculated by

$$v_{mean,error,k} = \frac{1}{120} \sum_{j=a,b,c} \sum_{m=l,u} \sum_{i=1}^{20} \left| v_{C,mi,j,k} - v_{mean,m,j,k} \right| \tag{18}$$

and the average deviation of the SM capacitor voltages from their reference value v_{dc}/N, at sampling instant k, is calculated by

$$v_{ref,error,k} = \frac{1}{120} \sum_{j=a,b,c} \sum_{m=l,u} \sum_{i=1}^{20} \left| v_{C,mi,j,k} - \frac{v_{dc}}{N} \right|. \tag{19}$$

The voltage errors shown in Table III are the average values of (18) and (19) within the time period t_1 to t_2.

As shown in Table III, the switching frequency, power losses, and THD of the indirect FCS-MPC strategy using the sorting algorithm is in the order of controllers proposed in [2] and [22]. However, in the proposed indirect FCS-MPC strategy, by considering the summation of SM capacitor voltage tracking error as a term in the cost function (14), smaller tracking error of reference voltage is resulted for each SM. As expected, the reduced indirect FCS-MPC strategy has the same conduction losses as the indirect strategy while the switching frequency and switching losses are reduced approximately 20 times. Although in the reduced indirect FCS-MPC method, the tracking voltage error from the mean voltage is increased, the tracking reference voltage error remains the same. On the other hand, comparing the switching losses and frequency of the reduced indirect FCS-MPC strategy with and without the tolerance band control of the SM capacitor voltages shows that despite the limited magnitude of the SM capacitor voltage ripple, the switching losses and frequency are slightly increased. Comparing the proposed reduced indirect FCS-MPC strategy with the method C_2 in [22] confirms the superiority of the proposed method in terms of SM capacitor voltage control with less switching frequency and power losses.
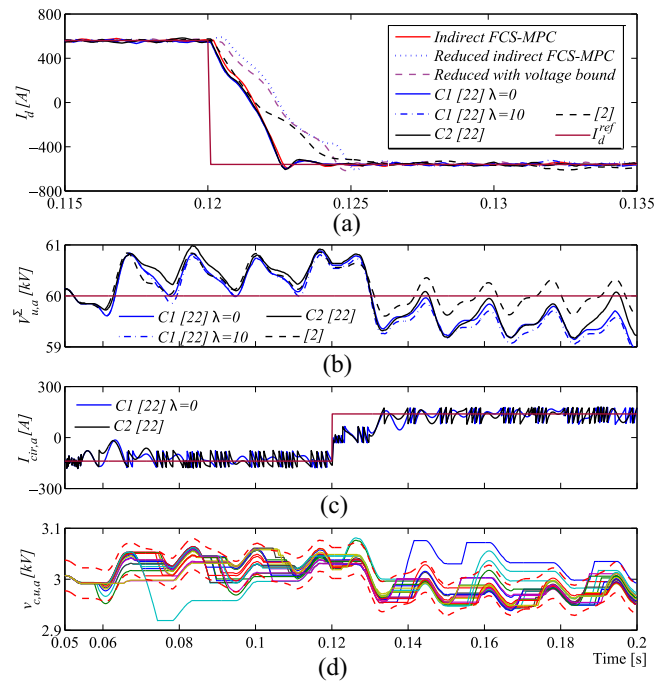

Fig. 7. Simulation results of various control strategies. (a) d-axis current component of the ac-side current. (b) Summation of the SM capacitor voltages in the upper arm of phase a. (c) Phase-a circulating current. (d) SM capacitor voltages in the upper arm of phase a.

E. Dynamic Response Comparison

The simulation results show that in the reduced indirect FCS-MPC strategy, transferred real power, ac-side currents, and capacitor voltages follow their references as desired. Although the steady-state responses are the same for both the indirect and reduced indirect FCS-MPC strategies, the reduced FCS-MPC strategy shows a slower dynamic response. In Fig. 7(a), the d-axis current component of the ac-side current for all control strategies during power reversal command is shown. As expected, the reduced FCS-MPC strategy has a slower response since the rate of changes of its switching transitions is limited. However, the indirect FCS-MPC strategy provides a faster dynamic response compared to the CCSC strategy with the same average switching frequency. On the other hand, although the reduced indirect FCS-MPC has the same speed as the CCSC method, it is slower than the FCS-MPC methods proposed in [22].

Fig. 7(b) shows the summation of the SM capacitor voltages in the upper arm of phase a ($v_{u,a}^{\Sigma}$), for the control methods in [2] and [22]. The results of Fig. 7(b) confirm the superiority of the proposed strategy in terms of the SM capacitor voltage control. The circulating current of phase a ($i_{cir,a}$) for the FCS-MPC methods in [22] is shown in Fig. 7(c). As shown in Fig. 7(c), the proposed strategy in [22], compared to the proposed indirect and reduced indirect FCS-MPC strategies, shows a slower dynamic response for circulating currents. The SM capacitor voltages in the upper arm in phase a ($v_{Cu,a}$) are shown in Fig. 7(d) for the FCS-MPC method C_2 in [22]. Although the switching frequency is higher than that of the reduced indirect FCS-MPC strategy with the tolerance band presented in Fig. 6(e), the magnitude of the SM capacitor

voltage ripple exceeds the 2% tolerance band depicted by dashed lines.

V. Conclusion

In this paper, an indirect FCS-MPC strategy is proposed for the control of the MMC. A discrete bilinear mathematical model of the MMC is developed to predict the one-step ahead behavior of the MMC. A cost function is defined to select the best insertion index of each arm to minimize the ac-side currents tracking error and the circulating currents, and to maintain the summation of the SM capacitor voltages of each arm at their reference values. The proposed FCS-MPC strategy is combined with the conventional sorting algorithm to obtain a reasonable computational burden. This paper also introduces a modified switching strategy, which leads to even less calculation burden and simpler sorting algorithm for an MMC with a large number of SMs in each arm. In addition, the communication load between the MMC and its central controller is reduced, and the unnecessary switching transitions of the SMs are avoided. Simulation results are provided to confirm and validate the effectiveness of the proposed strategies.

References

[1] L. Angquist *et al.*, "Open-loop control of modular multilevel converters using estimation of stored energy," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2516–2524, Nov./Dec. 2011.

[2] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[3] G. Bergna *et al.*, "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," *IEEE Trans. Ind. Appl.*, vol. 60, no. 6, pp. 2360–2371, Jun. 2013.

[4] G. Bergna *et al.*, "A generalized power control approach in ABC frame for modular multilevel converters based on Lagrange multipliers," in *Proc. 15th IEEE Eur. Conf. Power Electron. Appl. (EPE)*, Lille, France, Sep. 2013, pp. 1–8.

[5] Z. Li *et al.*, "An inner current suppressing method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4873–4879, Nov. 2013.

[6] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[7] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Mar. 2014.

[8] H. Nademi, A. Das, and L. Norum, "Modular multilevel converter with adaptive observer of capacitor voltages," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 235–248, Jan. 2014.

[9] A. Antonopoulos, L. Angquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, Barcelona, Spain, 2009, pp. 1–10.

[10] J. Rodriguez *et al.*, "State of the art of finite control set model predictive control in power electronics," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 1003–1016, May 2013.

[11] D. E. Quevedo, R. P. Aguilera, M. A. Perez, P. Cortes, and R. Lizana, "Model predictive control of an AFE rectifier with dynamic references," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3128–3136, Jul. 2012.

[12] M. Preindl and S. Bolognani, "Model predictive direct speed control with finite control set of PMSM drive systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 1007–1015, Feb. 2013.

[13] M. Vatani and M. Hovd, "Predictive control of converter switches in a multi-terminal HVDC system," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Vienna, Austria, 2013, pp. 3699–3704.

[14] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded H-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2691–2699, Aug. 2010.

[15] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel converter for a back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1538–1547, Jul. 2012.

[16] J. Qin and M. Saeedifard, "Predictive control of a three-phase DC-AC modular multilevel converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Raleigh, NC, USA, Sep. 2012, pp. 3500–3505.

[17] B. Riar, T. Geyer, and U. Madawala, "Model predictive direct current control of modular multi-level converters," in *Proc. IEEE Int. Conf. Ind. Technol. (ICIT)*, Cape Town, South Africa, Feb. 2013, pp. 582–587.

[18] B. Riar, T. Geyer, and U. Madawala, "Model predictive direct current control of modular multilevel converters: Modelling, analysis and experimental evaluation," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 431–439, Jan. 2014.

[19] R. N. Fard, H. Nademi, and L. Norum, "Analysis of a modular multilevel inverter under the predicted current control based on finite-control-set strategy," in *Proc. 3rd Int. Conf. Elect. Power Energy Convers. Syst.*, Istanbul, Turkey, Oct. 2013, pp. 1–6.

[20] F. Hassan and W. Crookes, "Direct model predictive control for medium voltage modular multi-level STATCOM with and without energy storage," in *Proc. IEEE Int. Conf. Ind. Technol. (ICIT)*, Athens, Greece, 2012, pp. 932–937.

[21] J. Bocker, B. Freudenberg, A. The, and S. Dieckerhoff, "Experimental comparison of model predictive control and cascaded control of the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 422–430, Mar. 2014.

[22] J.-W. Moon, J.-S. Gwon, J.-W. Park, D.-W. Kang, and J.-M. Kim, "Model predictive control with a reduced number of considered states in a modular multilevel converter for HVDC system," *IEEE Trans. Power Del.*, to be published.

[23] P.-O. Gutman, "Stabilizing controllers for bilinear systems," *IEEE Trans. Autom. Control*, vol. 26, no. 4, pp. 917–922, Aug. 1981.

[24] P. Münch, D. Görges, M. Izák, and S. Liu, "Integrated current control, energy control and energy balancing of modular multilevel converters," in *Proc. 36th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Glendale, AZ, USA, 2010, pp. 150–155.

[25] A. Yazdani and R. Iravani, *Voltage-Sourced Converters in Power Systems: Modeling, Control, and Applications*. Hoboken, NJ, USA: Wiley, 2010.

[26] U. Drofenik and J. W. Kolar, "A general scheme for calculating switching- and conduction-losses of power semiconductors in numerical circuit simulations of power electronic systems," in *Proc. Int. Power Electron. Conf. (IPEC)*, Niigata, Japan, 2005, pp. 4–8.

Mohsen Vatani (S'11) received the B.Sc. degree from the Isfahan University of Technology, Isfahan, Iran, and the M.Sc. degree from the Amirkabir University of Technology, Tehran, Iran, in 2008 and 2011, respectively, both in control engineering. He is currently pursuing the Ph.D. degree from the Department of Engineering Cybernetics, Norwegian University of Science and Technology, Trondheim, Norway.

His current research interests include model predictive control, control of modular multilevel converters, and multiterminal high voltage dc systems.

Behrooz Bahrani (S'07–M'12) received the B.Sc. degree from the Sharif University of Technology, Tehran, Iran; the M.Sc. degree from the University of Toronto, Toronto, ON, Canada; and the Ph.D. degree from Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland, in 2006, 2008, and 2012, respectively, all in electrical engineering.

He is currently a Post-Doctoral Fellow with the Georgia Institute of Technology, Atlanta, GA, USA. His current research interests include control of power electronic systems, applications of power electronics in power and traction systems, and grid integration of renewable energy resources.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

10
IEEE TRANSACTIONS ON SMART GRID

Maryam Saeedifard (SM'11) received the Ph.D. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2008.

She was an Assistant Professor with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA. She is currently an Assistant Professor with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA. Her current research interests include power electronics and applications of power electronics in power systems.

Morten Hovd (SM'14) received the Ph.D. degree in process control from the Department of Chemical Engineering, University of Trondheim, Trondheim, Norway, in 1992.

He was a Professor of Process Control in the Department of Engineering Cybernetics, Norwegian University of Science and Technology, Trondheim. He has held visiting positions at the University of California–San Diego, La Jolla, CA, USA, and the University of Cambridge, Cambridge, U.K. His current research interests include decentralized control, model predictive control, and control performance monitoring.