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Indium Phosphide Membrane Nanophotonic Integrated Circuits on Silicon

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Photonic integration in a micrometer-thick indium phosphide (InP) membrane on silicon (IMOS) offers intrinsic and high-performance optoelectronic functions together with high-index-contrast nanophotonic circuitries. Recently demonstrated devices have shown competitive performances, including high side-mode-suppression ratio (SMSR) lasers, ultrafast photodiodes, and significant improvement in critical dimensions. Applications of the IMOS devices and circuits in optical wireless, quantum photonics, and optical cross-connects have proven their performances and high potential.

1. Introduction

Photonic integrated circuits (PICs) is regarded not only as the key enabling technology for the modern telecommunications but also revolutionary for emerging applications ranging from data communications, precision metrology, sensing, and imaging.[1] Indium phosphide (InP)-based PICs are being both academically attractive[2,3] and commercially successful,[4,5] due to its intrinsic laser and amplifier integration and high optoelectronic efficiencies, which include optical gain, electron velocity, and electro-optic coefficients (e.g., the Pockels and Kerr coefficients) at 1.55 μm telecom wavelength band.

More functionalities demand more complex circuits. The complexity directly impacts the performance specification of the PICs. For instance, to achieve more wavelength channels and higher data capacity in the wavelength division multiplexing (WDM) transceiver PICs, high parallelization of laser and modulator arrays is essential.[6] Currently, the highest integration complexity reported among InP PICs is about 1700 components per chip,[5] reported in 2014. Adding more components to the PIC is still possible, but at the cost of larger chip areas and higher risks at yield. In contrast, the integration density per unit chip area has not been improved over more than 10 years.[7] The major limiting factor is the low optical confinement in the ridge waveguide structures on InP substrate, as shown in **Figure 1**a. This leads to waveguide dimensions of several micrometers and bending radii of tens to hundreds of micrometers.[1]

The optical confinement in the waveguides can be enhanced by inserting a low-index optical buffer layer between the waveguide and the substrate carrier, as shown in Figure 1b. The waveguide layer becomes a thin membrane with high vertical index contrast, whereas the rib waveguide fully etched into the membrane layer provides strong horizontal optical confinement. A waveguide of 400 nm in width and 300 nm in height results in single-mode (SM) operation for transverse electric (TE) and transverse magnetic (TM) modes, as shown in **Figure 2**. The similar philosophy has already been applied and matured in the silicon-on-insulator (SOI) platforms,[8,9] for their passive

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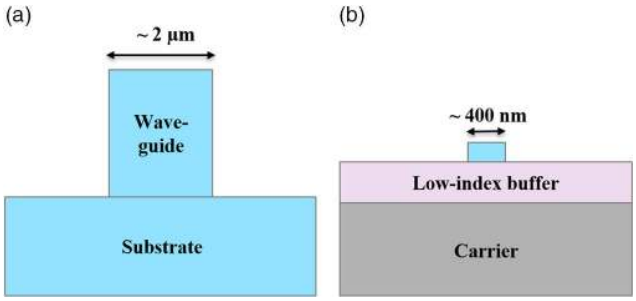

Figure 1. Schematic illustrations of a) a conventional InP ridge waveguide on a substrate, and b) a high-confinement InP membrane waveguide.

circuitries. Moreover, recent realizations of membrane distributed feedback (DFB) lasers on silicon[10,11] have revealed that high optical confinement can be achieved also in laser structures through layerstack innovation in a -membrane, which leads to the benefits of enhanced confinement factors in quantum wells (QWs) and reduced threshold.

The InP membrane on silicon (IMOS) platform[12,13] developed at Eindhoven University of Technology has the potential to achieve enhanced optical confinement in both active and passive devices. It features intrinsic amplifiers and lasers, monolithically integrated with nanophotonic waveguides and circuitries in a single sub-micrometer-thick InP membrane. In this article, we review the recent technology, device, and circuit development of the IMOS platform and discuss its potentials in emerging applications.

2. Membrane Integration Technology

The current approach of active–passive integration in IMOS is based on the twin-guide structure,[14,15] where the p-i-n amplifier structure is epitaxially grown and processed on top of a 300 nm thin passive waveguiding layer, as shown in **Figure 3**a. The entire active–passive membrane is bonded onto a silicon carrier wafer with ≈2 μm of benzocyclobutene (BCB) and SiO_2 stacks. The BCB polymer provides good thermal stability (glass transition temperature >350 °C), chemical resilience, and planarization capability,[16,17] which are crucial to creating wafer-scale defect-free membranes. The coupling between the amplifier and the waveguide is through an adiabatic taper structure as shown in Figure 3b. Due to the fact that the active and passive guides have very similar refractive indices (3.3 and 3.2, respectively) and are separated by only a 100 nm-thick n-contact layer, the coupling is very efficient (transmission >98% and back-reflection <−30 dB) in a length of just 20 μm.[14,15]

The major process steps for the twin-guide active–passive integration are shown in **Figure 4**. The process starts with defining deeply etched markers, the active–passive transition tapers and half of the semiconductor optical amplifier (SOA) structure, followed by surface passivation and p- and n-metallization (see Figure 4a). These are the prebonding steps of the double-sided technology. The bonding is performed at wafer-to-wafer scale, followed by a wet-chemical removal of the substrate and the etch-stop layers (see Figure 4b). The process continues to define structures on the freshly revealed and flat membrane surface after the bonding step. These include the realization of the second half of the SOA, deep and shallow waveguides, gratings, etc. (see Figure 4c). These postprocessing steps align to the deeply etched markers in the membrane created before bonding. Finally, the buried metal contacts are opened for electrical probing (see Figure 4d).

This active–passive integration scheme can be further extended to integrate more functionalities, for instance, unitraveling carrier (UTC) photodiodes,[18] broadband electro-absorption modulators (EAMs),[19] metallic grating couplers,[20,21] etc., in a single layer

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Jos J.G.M. van der Tol received his Ph.D. in physics from the University of Leiden, The Netherlands. Subsequently, he joined KPN, and involved in research on integrated optics for telecommunications. This included modeling of waveguides, design of electro-optical lithium niobate devices, and their fabrication. Furthermore, he worked on guided wave InP components. He was also active in optical networks, focusing on survivability, introduction scenarios, and management issues. Currently, he works at the University of Technology Eindhoven in The Netherlands, on opto-electronic integration, polarization issues, and photonic membranes.

Kevin Williams received the B.Eng. from the University of Sheffield, UK, and the Ph.D. from the University of Bath, UK, in 1995. He moved to the University of Cambridge, UK, in 2001 and was elected Fellow at Churchill College. In 2011, he has focused on photonic integration technology. He is the chair of the Photonic Integration research group at Eindhoven University of Technology.

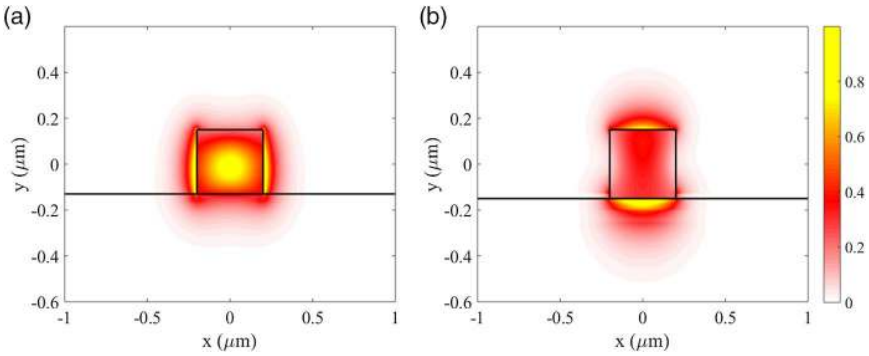

Figure 2. Intensity profiles of the a) TE and b) TM fundamental modes in the IMOS nanophotonic waveguides with width of 400 nm and height of 300 nm.

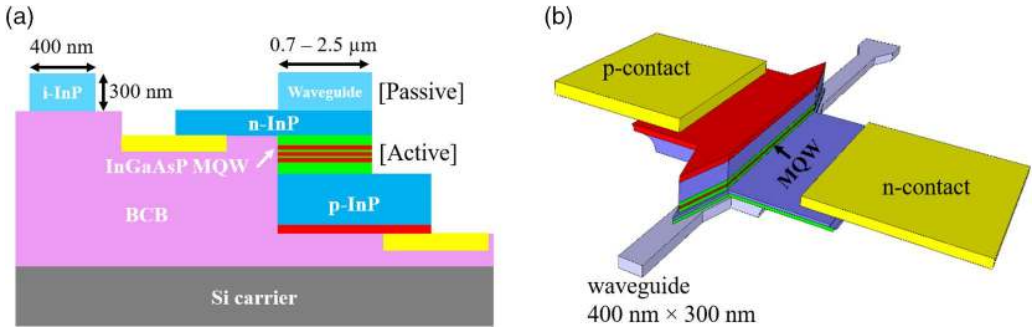

Figure 3. a) Cross-sectional view of the IMOS twin-guide active–passive integration scheme. b) 3D artist's impression of an IMOS amplifier with adiabatic taper coupled to passive waveguide.

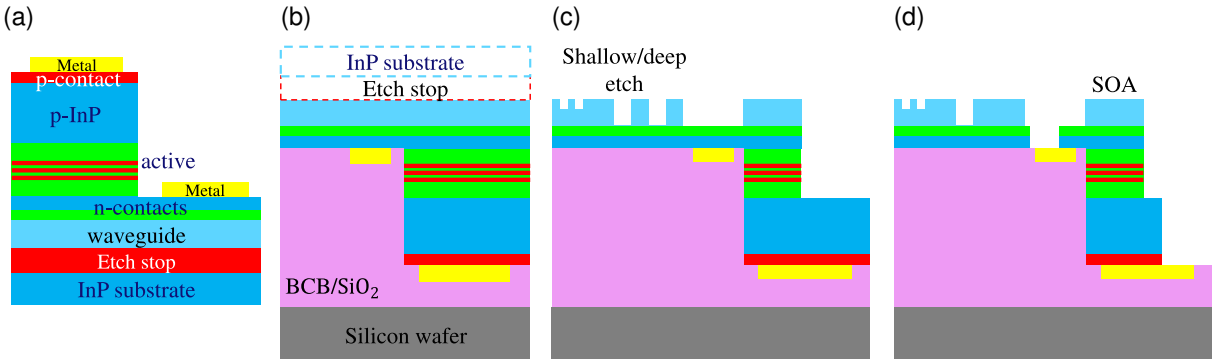

Figure 4. Schematic illustrations of the twin-guide active–passive fabrication process. a) Prebonding structure definition; b) wafer bonding and membrane formation; c) postbonding structure definition; and d) metal electrodes opening.

of membrane. One proposed approach to the function extension takes advantage of the double-sided processing scheme, where two different active layerstacks can be integrated on either side of the 300 nm passive waveguide layer. This allows a membrane laser integrating with a UTC diode or an EAM without the need of regrowth processes. A detailed discussion of this integration concept can be found in the study by van der Tol et al.[12] For integrating more than two active functions in the membrane, butt-joint regrowth can be considered. For instance as proposed in the study by Pogoretskiy et al.,[15] extra n-doped layers can be grown and processed using a double-sided scheme to form a slot-waveguide polymer modulator, at the opposite side of the amplifier/laser, whereas an extra p-doped layer can be regrown at the amplifier/laser side to form the UTC photodiode. The active and passive devices that have been demonstrated so far in IMOS platform will be discussed in Section 3.

Since the recent report in the studies by van der Tol et al.,[12,13] various technology developments have been achieved. The double-sided processing technique,[12,13,22] which allows for etched and deposited structures on both sides of the membrane,

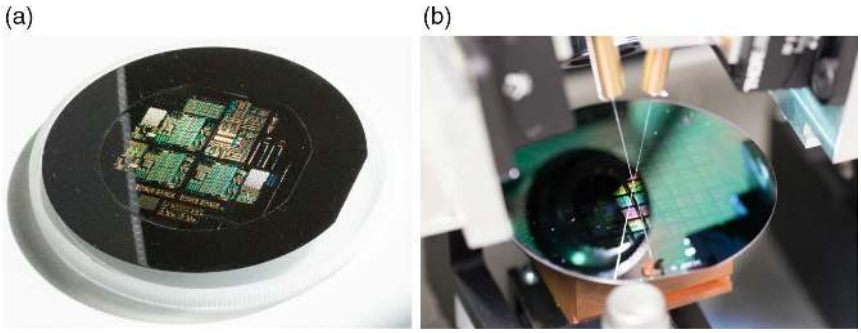

Figure 5. a) An IMOS wafer with 2 in. InP membrane bonded on a 3 in. silicon carrier wafer. The InP membrane is based on the active–passive layerstack shown in Figure 3a and contains membrane amplifiers and lasers (see Section 3.2). b) An IMOS wafer (3 in. InP membrane bonded on 3 in. silicon) under full-wafer measurement using vertical fiber coupling. The 3 in. InP membrane is 300 nm thick and contains passive circuitries patterned by the ASML 193 nm deep ultraviolet (UV) scanner. (Photos courtesy of F.A. Lemaitre.)

has been applied to a wide range of devices, including the >67 GHz UTC photodiodes,[18] the membrane amplifiers, and lasers[14,15] and the metallic grating couplers.[20,21] The full processing is being performed on 2 and 3 in. full wafer scale, as shown in **Figure 5**.

Metal vias can act as the electrical interconnection between photonic devices (such as lasers and photodiodes) and electronics drivers in the silicon layer,[23] or as heat sink to extract the heat generated in the lasers to the cooled silicon carrier.[24,25] The via technology has been developed in the IMOS platform and integrated as a part of the laser process flow.[15,26] It is achieved by etching a slope through the polyimide (PI) overcladding layer to support evaporated metals connecting p-electrode of the laser and the surface of the silicon, as shown in **Figure 6**. The same metallization step also creates metal routings and high-speed radio frequency (RF) transmission lines on top of the PI layer (see Section 3.3). The sloped PI supporting structure help to avoid sharp corners and to achieve a continuous metal layer. This is especially crucial for future gold plating process to thicken the metal for improved electrical and thermal conduction.

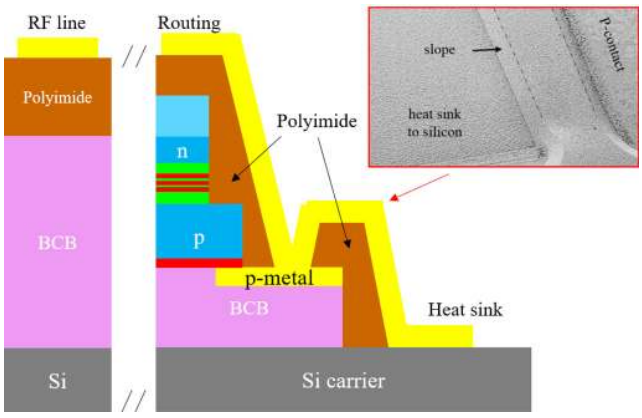

Figure 6. Schematic illustrations of the IMOS metallization scheme (n-electrode of the amplifier and passives are not shown). A PI overcladding layer is used for planarization and support of metal routings. In areas where semiconductor materials are fully removed, the metal layer on top of PI acts as a high-speed RF transmission line. The metallization also connects the p-electrode of the laser to the silicon for heat sinking purpose. The inset picture shows a scanning electron microscopy (SEM) image of the fabricated heat sink structure.[26]

The scanner lithography has been used for manufacturing of the conventional InP PICs[4] and the SOI passive circuits[27] and has demonstrated high precisions (90 nm critical dimensions), improved critical dimension control, and reduced waveguide losses. The scanner lithography process has been implemented in the IMOS process flow, using an ASML PAS5500/1100B 193 nm deep ultraviolet scanner tool.[28] In addition, offering a reduced waveguide loss, a unique advantage of using the scanner lithography in the IMOS double-sided process flow is that the ultraflat epitaxy-quality surface, which is crucial for optimal scanner lithography quality, can be obtained for two times (instead of only one for conventional InP and SOI cases) during the process flow: one being the epitaxial wafer surface for the first lithography, and another being the epigrade surface after bonding and removing the InP substrate and etch-stop layers. This gives additional freedom in device design and process optimizations and adds value to the overall uniformity and reproducibility of the process. The overlay of pre- and postbonding structures is similar to the electron-beam lithography (EBL) process. The deeply etched markers realized before bonding (see Figure 4a) will be filled with dielectrics. After the bonding, the InP membrane materials at the marker area can be removed to reveal the dielectric pattern, which can be recognized in the scanner tool and used directly as the alignment markers for postbonding processes.

Similar to the silicon and oxide etch selectivity in the SOI platform,[29] the InP and InGaAs(P) etch selectivity in the IMOS makes it an attractive platform for realizing compact and energy-efficient nano-opto-electro-mechanical systems (NOEMS).[30–32] A major advantage of NOEMS structures in IMOS platform is the access to the SOA layerstack. The heterostructure of the IMOS layerstack provides natural etch-stop interfaces between different material compositions, which are crucial for realizing suspended structures with good dimension control and minimal damage. In addition, such NOEMS on IMOS will be intrinsically compatible with the amplifiers, light sources, and detectors. Recent demonstration of a NOEMS phase modulator based on this technology is discussed in Section 4.3.

3. Device Building Blocks

IMOS platform provides a promising approach to laser-integrated nanophotonic devices and circuits. Various devices have been reported in past publications and summarized in the study by van der Tol et al.[12] In this section, we mainly focus on the new device development and provide a comparative study of performance enhancements induced by improved technologies.

3.1. Waveguide and Passive Devices

New development of passive devices is shown in **Table 1**, with previous results in italic font for comparison. Performance improvements of the devices are largely attributed to the use of the scanner lithography instead of the EBL. It is clear that the enhanced critical dimension control and the reduced roughness in the scanner lithography have led to a series of improved devices: lower propagation loss in straight waveguides and microrings; lowered insertion loss and reduced phase error (thus crosstalk) in arrayed waveguide gratings (AWGs).

New device types, such as photonic crystal (PhC) reflectors, reflective arrayed waveguide grating (R-AWG) and subwavelength grating couplers, have been demonstrated. It is worth mentioning that the PhC reflector has proven to be a promising building block, not only as a highly efficient and broadband on-chip mirror but also as an enabler of other complex devices, such as the R-AWG and the Fabry–Pérot lasers (see Section 3.2).

3.2. Amplifiers and Lasers

Based on the successful demonstration of an IMOS SOA at room temperature and continuous wave operation,[14] the SOA building block has been combined with other passive building blocks to form various laser cavities and tuning mechanisms.[15]

A summary of the recently demonstrated lasers on IMOS is shown in **Table 2**. Distributed Bragg reflector (DBR) lasers using the aforementioned high-reflectivity PhC reflectors have all shown good threshold current density of 2 kA cm^{-2}, which corresponds to about 20 mA threshold current for a 500 μm long cavity. Tunable lasers can be constructed by inserting two microring filters into the PhC DBR laser cavity. The two microrings have slightly different free spectral ranges (FSRs) such that the number of the filter passbands within the gain spectrum can be controlled by the Vernier effect. The demonstrated tunable laser has shown a SM behavior with good side-mode-suppression ratio (SMSR) of more than 30 dB over 25 nm tuning range, with only thermo-optic tuning of the microrings. The highest SMSR achieved in this tunable laser is 45 dB. The threshold current density is slightly higher than that of the conventional DBR lasers, due to the additional cavity loss induced by the two microrings, which can be reduced in the future by optimizing the ring coupling condition. The wall-plug efficiencies of the two lasers are below 1%. Possible sources of the relatively low efficiencies can be due to the high intracavity loss induced by relatively rough waveguide and underperforming mirrors due to fabrication errors in the particular run.

Index-coupled DFB lasers have been realized by controlled grating etch into the passive waveguide layer on the backside of the SOA structure.[42] This approach, as shown in **Figure 7**, offers a flexible control over the DFB coupling strength by simply controlling the etch depth. The grating coupling coefficient κ can be tuned from 0 to 200 cm^{-1} for an etch depth from 0 to 300 nm (complete waveguide etch). The grating etching step is independent of the SOA process flow, therefore does not compromise the SOA design and performance. The demonstrated DFB laser on IMOS contains a relatively weak grating due to a shallow etch (120 nm into the 300 nm thick waveguiding layer), with which the fiber grating couplers are also designed and realized. The resulting coupling coefficient κ is 40 cm^{-1}, which is much weaker than other InP membrane and silicon hybrid DFB lasers with κ values in the order of hundreds to thousands per centimeters.[43–45] The weak coupling leads to a long laser cavity.

Table 1. Recent development of the IMOS passive devices.

Device	Key performance	Reference	Remarks
Waveguide	*2.5–3.5 dB cm^{-1}*	[33,34]	*EBL patterned*
	1.8 dB cm^{-1}	[28]	Scanner patterned
PhC reflector	>90% reflectivity	[35]	Scanner feasible
AWG	*10 dB loss; 10 dB crosstalk*	[36]	*EBL patterned*
	3.5 dB loss; >20 dB crosstalk	[37]	Scanner patterned
R-AWG	6.7 dB loss; 10 dB crosstalk	[38]	EBL patterned
Microring	*$Q = 15\,500$*	[39]	*EBL patterned*
	$Q = 62\,000$	[28]	Scanner patterned
Sub-λ grating coupler	1.2 dB to SM fiber	[20]	EBL patterned

Table 2. Recent demonstrations of the IMOS amplifiers and lasers.

Device	Key performance	Reference	Remarks
SOA	110 cm^{-1} net modal gain @ 4 kA cm^{-2}	[14]	No heat sink
DBR laser	2 kA cm^{-2} threshold current density	[40]	PhC DBR reflectors[35] used
	1 mW in waveguide		
	30 dB SMSR		
	0.6% Wall-plug efficiency		
Tunable laser	2.4 kA cm^{-2} threshold current density	[41]	PhC DBR cavity with intracavity Vernier filters
	0.44 mW in waveguide		
	25 nm tuning range		
	>30 dB SMSR over tuning range (45 dB highest)		
	0.3% Wall-plug efficiency		
DFB laser	2.5 kA cm^{-2} threshold current density	[42]	$\kappa L = 4$
	13 mW in waveguide		
	60 dB SMSR		
	10% Wall-plug efficiency		

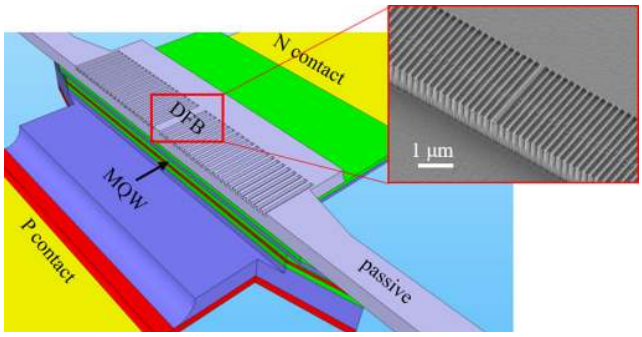

Figure 7. Schematic illustrations of the IMOS DFB laser with gratings shallowly etched into the passive waveguiding layer on the backside of the SOA. The inset picture shows a SEM image of the fabricated DFB structure.[42] Note that, this 3D image is flipped as compared with the one in Figure 3b.

Together with a uniform grating patterning, this contributes to an improved spectral purity.[46] The demonstrated DFB laser on IMOS with 1 mm long weakly coupled cavity has shown SMSR of more than 60 dB for the current injection range between 70 and 90 mA.[42] The SMSR value is the highest reported so far in DFB lasers on silicon to our best knowledge. An optical power of 1 mW in the fiber and a grating coupler loss of 11 dB (due to fabrication error) were measured, indicating a laser output power of 13 mW per facet. Considering the *I*–*V* characteristics of this laser diode,[42] a wall-plug efficiency of 10% can be obtained.

It should be mentioned that although the fabricated lasers shown in Table 2 have heat sink vias (see Figure 6) connecting their p-electrodes to the silicon carrier, the performance improvement is not obvious as compared with the lasers without thermal vias. It is mainly due to the fact that the metal is too thin (only 300 nm). Future improvement includes an additional gold plating process to thicken the metal up to several micrometers.

3.3. Broadband RF Lines

RF transmission lines are crucial elements for on-chip interconnection and routing of the electrodes in high-speed photonic devices to the access points of the electronics. The RF lines should be broadband and not limiting the intrinsic bandwidths of the photonic and electronic devices.[47]

In IMOS platform, the thick BCB/dielectric bonding layer and the PI planarization layer together form an effective decoupling of the RF transmission lines to the silicon carrier. Beneath the RF metal stack, all of the InP active–passive layerstack is also removed completely, making sure of the decoupling to photonic functions. The realization scheme of the RF transmission lines is shown in Figure 6.

Coplanar transmission lines have been fabricated on the IMOS platform, during the same metallization step for the via creation (see Section 2). About 300 nm gold metal was used. The layout of the transmission line is shown in **Figure 8**. The coplanar waveguides are terminated with 100 μm pitch ground–signal–ground (GSG) probe pads to facilitate the *S*-parameter measurement using the vector network analyzer. Three different lengths of 0, 250, and 500 μm were measured, and then the data were extrapolated to longer lengths of 1 and 2 mm. The S21 and S11 data are shown in Figure 8b for two different coplanar waveguide geometries with 1 mm length. As shown, the S21 only experienced ≈1 dB attenuation after 1 mm of transmission at 50 GHz frequency, indicating the broadband and low loss properties of the RF lines. The influence of different signal line and gap widths (up to 50% change) to the high-speed performance is negligible. The impedance of the transmission lines are extracted and shown in Figure 8c. Nearly frequency-independent impedance around 60 Ω has been obtained. The impedance can be tuned by the geometrical parameters to achieve impedance matching to the connected photonic and electronic devices. The experiments have shown that broadband RF interconnections up to several millimeters in length are feasible on IMOS platform, enabling full exploitation of the intrinsic bandwidths of the membrane optoelectronics.

4. Emerging Applications

In this section, we discuss several applications that have been recently investigated using IMOS devices and circuits. We focus on the unique opportunities that IMOS brings to these applications.

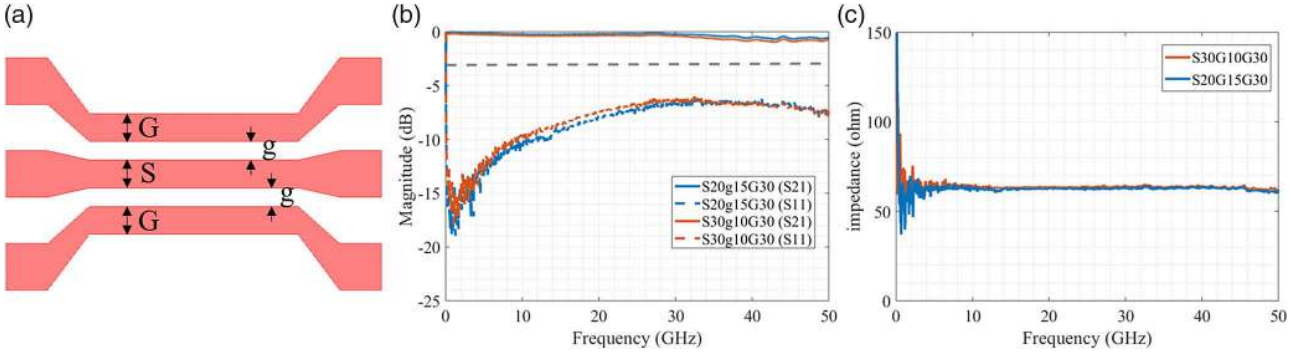

Figure 8. a) Schematic of the coplanar transmission line for *S*-parameter measurement, b) The S21 and S11 of two transmission lines (1 mm long) up to 50 GHz, c) the impedance of various transmission lines (2 mm long) as a function of frequency. The short codes in the figure legends represent the geometry of the transmission lines. For instance, S20g15G30 represents a transmission line with signal line width (*S*) of 20 μm, line gaps (*g*) of 15 μm, and ground line width (*G*) of 30 μm.

4.1. Optical Wireless Communication and Sensing

The grating couplers are promising candidates as integrated optical antennas for optical wireless communication (e.g., light fidelity [LiFi]) and sensing (e.g., light detection and ranging [LiDAR]) applications. High integration density and scalability in the SOI grating coupler arrays have been demonstrated and have shown optical beam forming and steering from a single chip.[48–51] The unique opportunities for IMOS lie in the intrinsic integration of high-performance active devices and the performance enhancement of the grating antennas using double-sided processing.[52,53]

Based on the ultrafast (>67 GHz) UTC photodiode demonstrated in IMOS platform,[18] its combination with optical antennas has been exploited for the use as an integrated optical wireless receiver.[52,54,55] The concept uses an on-chip optical antenna (e.g., a grating coupler) for efficient free-space to chip coupling, cascaded by a UTC photodiode for high-speed signal detection. The bandwidth-efficiency bottleneck in conventional free-space receivers (top illuminated photodiodes) can be eliminated,[55] as shown in **Figure 9**. It is clear that for the waveguide-coupled case (Figure 9b), the electrical bandwidth of the photodiode can be kept at the same high value regardless of the beam size, to which the grating coupler can be relatively easily adapted. Numerical simulation has shown that the grating coupler has still a high efficiency of 50% for large beam diameters beyond 60 μm.[55] For the top illuminated case (Figure 9a), the photodiode area has to increase for increased beam sizes. This leads to a reduced bandwidth. A quantitative study, using practical values of the responsivities, resistances, and capacitances and carrier dynamics for the two types of photodiodes, has shown that for beam diameters larger than 10 μm, the cascaded receiver has higher theoretical data capacity as compared with the top-illuminated counterpart.[55] For beam diameters larger than 50 μm, the difference in data capacity can be more than three times. In this theoretical analysis, nonlinear phenomenon such as diode saturation was not included as the application is typically working at relatively low optical power level (milliwatts and below).

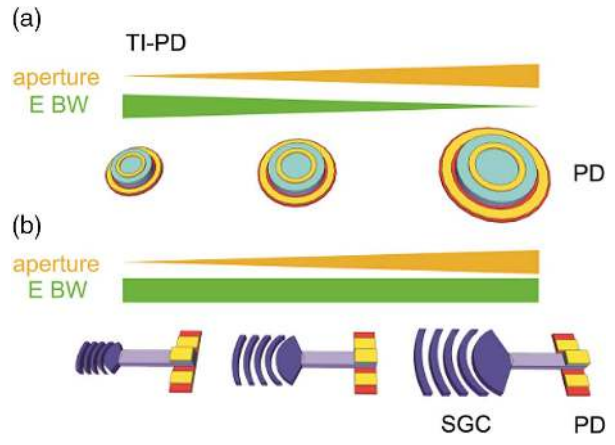

Figure 9. The operation principle of a) the conventional optical wireless receiver (top illuminated photodiode) and b) novel cascaded receiver on IMOS platform. Reproduced with permission.[55] Copyright 2017, IEEE.

It should be noticed that the grating coupler can have its potential limitations in terms of the field of view (FoV). The interference nature of the grating puts a boundary to the range of angles within which light with a certain wavelength can be efficiently captured. The FoV also depends on the spot size of the grating. Therefore, the grating couplers may not be suited for situations with wide angle variations and very large beam diameters.

The overall concept of the cascaded receiver, however, is still very promising. The first-stage light capturing is not limited to grating-type antennas. The grating couplers used in this first demonstration can be replaced by other integrated optical antenna concepts with wider FoV. Potential candidates include metasurfaces[56] and on-chip microlenses.[57]

In the system experiment of the first-generation cascaded receiver, 40 Gbit s^{-1} on–off keying (OOK) signal transmission has been achieved under a simulated wireless scenario: 2.4 km of SM fiber and 2 m of free-space path. Furthermore, the sensitivity to the wavelength and the angle of the incident beam were investigated, revealing a −3 dB FoV of 7.5° and an optical bandwidth of 30 nm.[55]

The successful demonstration of the single receiver can be scaled up to an optical wireless wavefront receiver (OWWR) with an grating antenna array to sample the incident wavefront of the free-space optical beam. The sampled optical signals in each channels will contain both intensity and phase information of the sampled wavefront. The signals can be further processed to reconstruct both the intensity (the signal) and phase profile (the incident angle) of the incident beam. The additional phase information is extremely valuable for an active beam tracing.[52] A proposed OWWR circuit layout, consisting of 4 × 4 compact grating antenna array, thermo-optic phase shifters, optical power combiners, and a UTC photodiode, is shown in **Figure 10**. The proposed antenna array is designed to sample fixed points of a large free-space incoming beam. The sampled optical signals from the grating array are combined by the power combiners and eventually fed to the UTC photodiode. The phase front of the incoming beam can be reconstructed by reading out the applied voltages (i.e., the tuned phases) on each of the phase shifters, at the moment when the latter are tuned to achieve maximum photocurrent. This extra angle information can be valuable to create awareness of relative positions between the transmitter and the receiver. A fabricated grating element used in the 4 × 4 array is also shown in the figure, featuring a compact footprint of only $3 \times 4\,\mu m^2$.

Reconfigurable optical wireless transceivers have also been proposed,[58] taking advantage of the reconfigurable gating behavior in a p-i-n SOA structure. The operation speed of such a p-i-n diode with QWs as the absorption medium will be limited to about 20–30 GHz in theory. It cannot replace the UTC photodiodes for high-performance optical wireless receivers, but can offer a cost-effective (no additional regrowth and processing of the UTC layerstack) approach to realizing both transmitter and receiver functions on a single chip.

The double-sided processing technology can enhance the efficiency of an individual grating antenna by incorporating a backside metal layer.[20,21] Such flexibility is not easily accessible in SOI platforms. The efficiency of the grating can be boosted with the assistance of the metal layer, which reflects all the downward

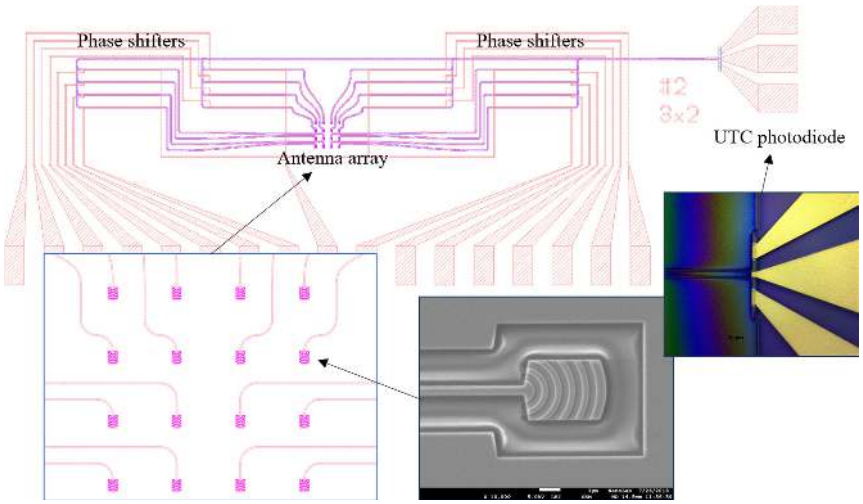

Figure 10. The proposed circuit layout of an OWWR, which is composed of 4 × 4 compact grating antenna array for wavefront sampling, thermo-optic phase shifters for phase reconstruction, optical power combiners and a UTC photodiode for signal detection.

light to upward direction. A grating-to-fiber coupling efficiency of 75% has been achieved,[20] which is a significant boost comparing with the 30 % efficiency in conventional grating designs without metal reflector.[12]

The intrinsic on-chip amplification and light sources that IMOS technology offers can provide high scalability (e.g., WDM transceivers) and reconfigurability (e.g., reconfigurable transceivers) solutions on a single chip. Moreover, the combination of nanophotonic circuits with ultrafast optoelectronic devices can enable a seamless cointegration of optical wireless and microwave systems.[59] Several key devices, such as the UTC photodiode and tunable laser, are essential for both optical wireless and microwave photonics.[60,61] The sharing of the key devices across different frequency bands can lead to powerful wireless systems-on-chip.

4.2. Integrated Quantum Photonics

The nanophotonic waveguides in the IMOS platform has opened up new opportunities for studying and utilizing strong light-matter interactions in InP. The index contrast and dimensions of the SM InP membrane waveguide are very similar to those of the SOI waveguides, as shown in **Table 3**. Such submicrometer-dimensioned waveguides provide tight optical confinement, resulting in a highly concentrated optical field profile within the InP core as well as on the InP/air (or dielectrics) interfaces (see Figure 2).

Such nanophotonic waveguides have attracted much attention in the application of quantum optics, taking advantage of the high third-order ($\chi^{(3)}$) nonlinearity. Recent open access to the silicon photonics foundry services has led to a range of SOI devices and circuits for entangled photon pair generation[72] and quantum distribution.[73]

IMOS can potentially offer several advantages over SOI, for instance, the intrinsic on-chip quantum light sources, as well as the access to the InP material system which has higher third-order nonlinearities. The optical Kerr coefficient in InP is about 5–10 times higher than that of the silicon, as shown in Table 3. The higher Kerr coefficient can enable stronger processes at lowered optical power level. First experiments on nonlinearities in IMOS devices have been conducted in the study by Thourhout et al.[74] In that work, an IMOS microring resonator ($Q > 40\,000$) was used as an entangled photon pair source using the spontaneous four-wave mixing (SFWM) process. The photon pair generation rate (PGR) obtained from this InP microring resonator is 145 MHz mW^{-2}, which is comparable with the state-of-the-art SOI microring resonator (PGR 149 MHz mW^{-2}[75]) with a doubled Q factor and halved radius. This revealed promising aspects of IMOS nanophotonic circuitry for the quantum photonics applications.

Table 3. Basic and nonlinear properties of InP waveguide in IMOS platform and Si waveguide in SOI platform around wavelength of 1.55 μm.

Property	InP membrane	SOI
Index contrast (Δn)	2.2	2.6
Dimensions [nm^2]	400 × 300	500 × 220
Kerr coefficient [10^{-18} m^2 W^{-1}]	27[62]	3–6[63,64]
TPA coefficient [cm GW^{-1}]	14.6–33[65–67]	0.6–1.0[63,64]
FCA cross section [10^{-17} cm^2]	4–7.2[66,67]	1.24–1.45[63,68]
Free carrier lifetime [ns]	0.5[a),b)][69]	3–4[68,70]
Electron mobility[c)] [10^3 cm^2 (V · s)$^{-1}$]	2[71]	0.25[71]
Absorption[c)] [cm^{-1}]	3[71]	9[71]

[a)]radiative lifetime; [b)]bulk InP; actual lifetime in InP membrane will be shorter; [c)]at n-dopant concentration of 10^{18} cm^{-3}.

Similar to the silicon, other nonlinear processes such as the two photon absorption (TPA) and free carrier absorption (FCA) coexist with the $\chi^{(3)}$ process in InP waveguides, first reported in the study by Johnson and Painter.[76] The TPA and FCA coefficients in InP are higher than those in silicon (see Table 3). Therefore, the benefit of higher $\chi^{(3)}$ in InP will be restricted to relatively low optical power level. At higher power level, TPA

starts to dominate and the free carriers generated by TPA will cause FCA. The consequences include reduced Q factor and blue shift of the resonant peaks,[74,77] which reduce the single photon generation rate.

Free carrier lifetime plays a critical role in the FCA process. The free carrier lifetime in InP waveguides can be shorter than that in SOI waveguides, due to the direct bandgap, as shown in Table 3. However, both are in the (sub)nanosecond range (0.5 ns for InP and 3–4 ns for SOI). Note that the 0.5 ns value comes from bulk InP crystal.[69] It is known that the actual free carrier lifetime in highly confined waveguides will be even shorter due to enhanced surface recombination.[68,78] Therefore, the actual free carrier lifetime in the InP membrane waveguides will be shorter than the bulk value of 0.5 ns. Reducing the carrier lifetime is a viable route to further suppressing the impact of TPA and FCA. In SOI waveguides, several approaches have been proposed and experimented, such as intentional recombination centers,[68] biased p-i-n diode[70] and enhanced surface recombinations.[78] Reduced carrier lifetime down to as short as 12.2 ps has become feasible.

Similar approaches can be applied to IMOS waveguides as well to reduce the carrier lifetime. Moreover, it is easier to implement doping profile and p-i-n diode structure in InP than in silicon. Doping can be done straightforwardly during epitaxial growth of InP material systems, without the need of ion implantation. Moreover, it is discovered that at the same n-dopant concentration, InP membrane waveguides experience three times lower absorption loss than SOI waveguides.[71] This is attributed to the higher electron mobility in InP than in silicon at the same n-dopant concentration.[71,79] A quantitative comparison is shown in Table 3. These evidences have shown high potential of creating low-optical-loss and highly compact p-i-n diode structure to reduce the free carrier lifetime in IMOS nanophotonic waveguides.

4.3. Ultralow Energy Optical Crossconnects

Optical micro-electro-mechanical system (MEMS) is regarded as a promising technology for large-scale optical crossconnects for the rapidly growing optical networks.[80] The optical MEMS (especially the NOEMS) has the advantage of high scalability and low energy consumption. The advantages of realizing MEMS and NOEMS devices on IMOS platform have been discussed in Section 2.

Recently, a NOEMS phase modulator has been demonstrated on IMOS platform,[32] based on a twin-guide layer structure similar to the one previously used for SOAs.[12] The p-InP layer and the passive InP (as well as n-InP layer) forms the top and bottom waveguides of the NOEMS phase modulator, respectively, whereas the original InGaAsP active layer in between is removed wet chemically. Based on it, a Mach–Zehnder interferometer (MZI) optical switch has been fabricated, as shown in **Figure 11**. Since the top and bottom waveguides are doped, an electrostatic force will be applied as the structure is biased. As a result, the top waveguide can be actuated and cause significant change in the mode effective index and phase shift (see Figure 11c). The first demonstration already showed promising results: maximum 4.8π phase shift with a phase modulator of only 140 μm long and a 15 dB extinction ratio of the MZI switch. Megahertz-level actuation frequency is expected. Such giant phase shift can find applications in switch networks and sensors which require low energy consumption.

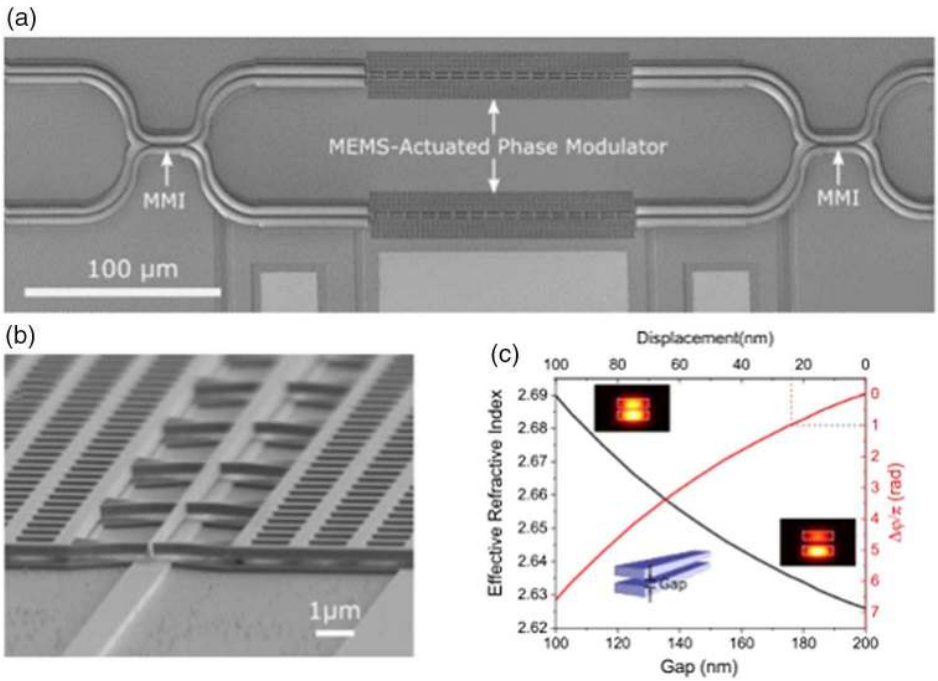

Figure 11. IMOS-based NOEMS: a) SEM picture of the fabricated MZI optical switch using NOEMS phase modulators, b) a NOEMS phase modulator, and c) calculated mode effective index and phase shift as a function of the actuated gap.[32]

5. Conclusion and Outlook

The IMOS platform has shown significant progress in recent years. It has enabled nanophotonic integrated circuits with intrinsic active functions. The twin-guide integration scheme offers an efficient and compact active–passive integration, which enabled various amplifiers and lasers. The double-sided processing on the membrane has opened up a new degree of freedom in device design for optical, optoelectronic, and RF optimizations. IMOS devices have shown promising performances in several novel applications, ranging from on-chip quantum photonics and nanomechanical optical crossconnects to off-chip free-space interfacing.

The IMOS platform has high potential of meeting the scaling trend in PIC development (the photonic Moore's law[2]), by providing sub-micrometer nanowire waveguides and ultrasharp bends[81] in the passives, as well as actives with reduced active–passive interfacing lengths (e.g., short transition tapers in the twin-guide SOAs). The reduced taper lengths contribute to the reduction of the total lengths of the active devices. The double-sided processing scheme opens up opportunities for diode structural innovation which can lead to complete elimination of the transition tapers (for instance, in butt-jointed membrane SOAs and UTC photodiodes).

In IMOS, the photonic layer is completely realized in an InP membrane, therefore, it is independent of the carrier beneath it. Instead of a silicon substrate, the membrane can be integrated vertically on top of a complementary metal oxide semiconductor wafer, which contains the electronics needed for the photonics. Such vertical integration (including the via interconnections) can overcome the scaling and speed bottlenecks in conventional PIC assemblies, and can be performed at full wafer scale. This opens up a promising route to significant cost reduction and mass manufacturing of photonic/electronic cointegrated circuits.[7,82]

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

indium phosphide, membranes, nanophotonics, photonic integration, photonic integrated circuits, semiconductor laser, waveguides

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