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Individual defects in InAs/InGaAsSb/GaSb Nanowire Tunnel Field-Effect-Transistors operating below 60- mV/decade

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Abstract: Tunneling Field-Effect Transistors (TunnelFET), a leading steep-slope transistor candidate, is still plagued by defect response and there is a large discrepancy between measured and simulated device performance. In this work, highly scaled InAs-$In_xGa_{1-x}As_ySb_{1-y}$-GaSb vertical nanowire TunnelFET with ability to operate well below 60 mV/decade at technically relevant currents are fabricated and characterized. The structure, composition, and strain is characterized using transmission electron microscopy with emphasis on the heterojunction. Using Technology Computer Aided Design (TCAD) simulations and Random Telegraph Signal (RTS) noise measurements, effects of different type of defects are studied. The study reveals that the bulk defects have the largest impact on the performance of these devices, although for these highly scaled devices interaction with even few oxide defects can have large impact on the performance. Understanding the contribution by individual defects, as outlined in this paper, is essential to verify the fundamental physics of device operation, and thus imperative for taking the III-V TunnelFETs to next level.

To address the power constraint and to augment the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) functionality for low-power applications, a novel device needs to operate well below the thermal limit (60 mV/decade), but also provide the same current levels although at lower drive voltages. Tunneling Field-Effect Transistor (TunnelFET) is a device that uses band pass filtering to remove high energy carriers and can be designed to operate below the thermal limit. [1-2] TunnelFETs fabricated from Si and III-V:s have demonstrated promising results.[3] Si TunnelFETs have shown the ability to operate well below 60 mV/decade, although not yet at any technically useful current levels.[4-6] III-V TunnelFETs have achieved high currents but without operation significantly below 60 mV/decade.[7-9] One of the main limitations to achieve a subthreshold swing (*S*) well below 60 mV/decade with III-V TunnelFETs are defects in the materials that enable defect-assisted tunneling [10,11], which have had a detrimental effect on the subthreshold swing and the off-state currents. Thereby, to fully explore the potential of the III-V TunnelFETs, there is a need to understand what influence the different types of defects have on the performance. In this work, we present highly scaled nanowire III-V TunnelFETs with competitive performance, and with a subthreshold swing well below the thermal limit of 60 mV/decade at room temperature. This outstanding performance shows that these devices have a comparably low defect density, that allows studies of individual defects. Using transmission electron microscopy (TEM), the structure is characterized, determining the composition, crystal structure, and strain. Modeling is performed to understand the impact of defects in the channel, as well as in the oxide, on the performance of these devices. Finally, using Random Telegraph Signal (RTS) noise measurements, the influence of oxide defects was studied experimentally. The findings presented here allow for TunnelFET optimization, which can increase the energy efficiency of electronic systems. It may also enable new applications in areas where the energy budget is limited, for instance in battery operated or energy harvesting applications related to the Internet of Things.

Nanowires were epitaxially grown using metal-organic vapor phase epitaxy (MOVPE) from Au seed particles patterned using electron beam lithography on a high resistivity Si(111) substrate

with a 260 nm highly n-doped InAs layer.[12] The InAs and InGaAsSb segments were grown at 460 °C while the GaSb segment was grown at 515 °C (see methods). The bottom part of the InAs segment was n-doped using Sn and the InGaAsSb and GaSb segments were p-doped using Zn leaving a 100-nm-long not intentionally doped InAs channel segment (Fig 1a). To study how a change in the band lineup at the tunnel junction affects the electrical characteristics, two different InGaAsSb compositions were grown, $In_{0.1}Ga_{0.9}As_{0.88}Sb_{0.12}$ for sample A and $In_{0.32}Ga_{0.68}As_{0.72}Sb_{0.28}$ for sample B. Fabrication of the devices began with digital etching of the nanowires to remove a parasitic GaSb-shell and to reduce the diameter of the InAs channel region down to 20 nm. A high-*k* layer was applied using atomic layer deposition followed by evaporation of a spacer layer to separate the drain and gate regions. The gate layer was formed by sputtering of a tungsten film, followed by definition of the physical length (L_g = 250 nm) using reactive ion etching and mask definition. A second spacer layer was applied to separate the gate and source regions followed by sputtering of Ni/Au top-metal and formation of probing pads. A detailed description of the fabrication process can be found in the methods section. A schematic image of a finished device is presented in Fig. 1b. The transfer characteristics of a device from sample A (device A) and B (device B) are shown in Fig. 1c and d, respectively. Both devices exhibit excellent electrostatics (low drain-induced barrier lowering), as expected for the gate-all-around geometry. Output characteristics for both devices shows good saturation (Fig. 1e and f). Device B shows a superlinear current onset, typical for TunnelFETs. The well-behaved output data for both devices confirms the proper material choice for TunnelFETs. For an I_{off} = 1 nA/μm (low power logic) and V_{DS} = 0.3 V, the I_{on} current for device A and B is 10.6 μA/μm and 3.9 μA/μm, respectively. Notably, both devices demonstrate a subthreshold swing below the thermal limit of 60 mV/decade, reaching 48 mV/decade for device A and 53 mV/decade for device B. Operation below 60 mV/decade occurs for both types of devices over a wide current range, close to three orders of magnitude for device A. This is exemplified by a record high I_{60} current (the current level at which the slope equals 60 mV/decade) of 0.31

μA/μm at 0.3 V for device A. These devices show a factor of almost 100 higher I_{60} as compared to other implementations approaching relevant current levels. [13] The high I_{60} originates from the use of a narrow bandgap channel, excellent electrostatics, as well as very low defect density in the InAs/InGaAsSb heterojunction. The TunnelFET operation is largely determined by the properties of the heterojunction. Consequently, the heterojunction of the nanowires, presented in Fig. 2a and b, was examined in detail using transmission electron microscopy. The composition was determined using energy dispersive X-ray spectroscopy and corroborated by measurements of the lattice plane differences from high resolution images. Most of the InAs segment has a wurtzite (WZ) crystal structure, but the final part before the introduction of Ga, approximately 3-5 nm in sample A and 10 nm in sample B, has a zincblende (ZB) structure most likely formed during the switching sequence. The transition from InAs to InGaAsSb is graded over ~25 nm and both the InGaAsSb and the GaSb segment have pure zincblende crystal structure without any observed stacking faults, which is typical for Sb-containing nanowires. [14] The local lattice distances are reduced after the structural change from WZ to ZB (Fig. 2c and 2d). Measurements are normalized to InAs(ZB) [15], d_{111} and d_{112} for the axial and radial measurements, respectively. The observed reduction is expected, since the large amount of Ga lowers the average atomic radii. However, on both samples this reduction starts at the WZ-ZB transition, (Fig. 2c and d) corresponding to 3-5 nm and 10 nm prior to the measured Ga increase in sample A and B, respectively. The InAs(ZB) is thereby compressed radially, which is expected since it tries to adapt to the smaller InGaAsSb lattice. However, Poisson's ratio would predict an expansion in the axial direction, which has not been observed. Exact strain is difficult to evaluate due to non-linearity of the resulting lattice for a given composition. However, assuming a linear relation between the composition and lattice distances, and comparing to the measured lattice spacing, the local axial strain can be estimated to about 3% for sample A and 2% for sample B, both compressive, with its maximum in the InAs(ZB) region closest to the WZ-ZB transition and extending into the InGaAsSb region. It is known for similar compounds that can exist in both

WZ and ZB polytypes, that the WZ structure is the radially stiffer of the two (given a growth direction of [111]B or [0001]). [16] Applying this to InAs imposes restrictions on the ideal way of relaxation, and since the stiffer WZ is less prone to deformation it retains its radial dimensions over a longer distance. This explains the steeper drop in axial lattice distance in the section immediately after the WZ-ZB interface for the sample B. The more graded introduction of Ga into sample A provides a smoother transition, which is closer to the ideal adaption of the lattice to the final composition.

Based on the knowledge of the material composition and the strain profile, simulations of the InAs/InGaAsSb/GaSb nanowire TunnelFET were performed using the semi-classical simulator Sentaurus-Device. The actual device geometry and estimated doping profiles were used to analyze the performance of device B. All band structure parameters were set to the experimentally extracted values taken from Ref. 17. The InGaAsSb segment is divided into sub-regions based on its composition (Fig 3a). The formation of a quantization level in the triangular well at the InAs WZ-ZB interface was modeled by introducing a pseudo-grading of the CB edge (Fig. 3a). The TEM images revealed a steep change of the mole fraction in the 3-nm-long InGaAsSb segment denoted by R-1. The device is most sensitive to defects within this region. Best fit to the measured data is acquired by choosing a defect density (Nt) of 1.6×10^{18} cm^{-3}, which would result in exactly one defect state in the segment R-1 on spatial integration. With so few defects, we would almost expect a digital like variation between devices. Data from four devices with one nanowire from the same sample presented in Fig. 3b, shows that the minimal value for the subthreshold swing occurs at approx. the same I_{DS} although the devices show a strong variation in the subthreshold swing vs I_{DS}. Some of the variations could depend on some variations generated during processing, but part could also be from variations among position and energy of the few defects. Donor-like defects were assumed at the InAs/oxide interface. The comparison of simulated temperature-dependent transfer characteristics with the experimental data (Fig. 3c) confirmed good agreement between the two, which validates the selected

parameter set and simulation set-up. Using a minimal number of fitting parameters allows to reliably analyze the impact of individual degradation mechanisms. The effect of each defect type on the transfer characteristics is shown in Fig. 3d. The simulations confirm that the subthreshold swing could be significantly improved if all defects were suppressed. Notably, introduction of defects at the oxide/semiconductor interface alone caused only a minor degradation of the sub-threshold swing. This is due to the absence of surface inversion at the oxide/semiconductor interface as consequence of the small diameter, which disables the formation of a strong enough normal field required for defect-assisted tunneling (DAT). Due to the low doping in the InAs segment and the small diameter, the channel region is under accumulation leading to flat band conditions. Yet, a small subthreshold-swing degradation is observed when defects at the oxide/semiconductor interface are included, which is due to screening of the gate charge resulting in a weaker gate coupling. Additionally, oxide interface defects cause surface Shockley-Read-Hall (SRH) generation of electron-hole pairs by multi-phonon excitation, which adds to the leakage current at very low current levels. Bulk defects present in region R-1 near the hetero-junction are found mainly responsible for the degradation of the sub-threshold swing. Therefore, suppressing these defects would have a stronger impact on the improvement of the TunnelFET performance compared with suppressing oxide interface defects. Nevertheless, suppressing oxide interface defects further would reduce the leakage current level. In the above analysis, the oxide interface defects were assumed to be uniformly distributed at the interface. Although a uniform distribution reliably models the average impact of these defects, a localized single defect may have a strong electrostatic effect, which can induce RTS type of effects on the I-V characteristics. Similar effects are also found in small area MOSFETs. [18] Transfer characteristics with and without a localized positive InAs/oxide interface charge located 50 nm away from the hetero-interface are compared in Fig. 3e. An acceptor defect at the InAs/oxide interface is positively charged in the off-state. At a certain gate bias, the charged defect captures an electron neutralizing this charge. This affects the electrostatics of the TunnelFET, and the on-

current is sharply reduced after the positive charge has been removed. This gives rise to a peak in the transfer characteristics as schematically shown in Fig. 3e.

To experimentally verify the role of individual defects within the gate oxide of the TunnelFETs with this small dimensions, the transfer characteristics of different transistors were scanned for RTS noise. Measuring the time constants and current step sizes provides information about the effect of single electron charges on the potential in the channel. Capture of an electron in an individual acceptor type defect within the gate oxide reduces the current level as the channel potential energy is increased; emission of the electron increases the current. Since the current in TunnelFETs is most sensitive to potential fluctuations when operating in the subthreshold region, we expect to detect the strongest RTS noise below V_T. Experimentally, we observe relative RTS amplitudes $\Delta I_{DS}/I_{DS}$ of about 20% for the device in Fig. 4 and even up to 50% for other devices not shown. The large RTS amplitude originates mainly from the small channel diameter, where a single defect can have a strong influence on the entire channel potential. Furthermore, the current through a TunnelFET is mainly limited by the potential variations close to the tunnel junction, which enhances RTS response from oxide defects in this region.[19] The effect of an individual defect on the subthreshold characteristics is presented in Fig. 4a. An excerpt of a two-level RTS measurement at a constant bias point close to the step in Fig. 4a is presented in Fig. 4b. To be able to reliably extract the time constants, at least a few hundred (and up to a few thousand) current transitions were recorded for each bias point. The residual noise in Fig. 4a could originate from 1/f-type noise from the channel region or from additional RTS noise too fast to resolve. The time constants, at a fixed bias, for capture and emission of an electron were determined by fitting an exponential distribution to the recorded capture/emission times as shown in Fig. 4d. When the channel Fermi level is aligned with the defect energy level, the capture and emission time constants are equal and are set by the depth z of the defect from the channel into the oxide: $\tau_{c/e} = \tau_0 \times \exp(z/\lambda)$. [20] Here, $\tau_{c/e}$ is the capture/emission time constant, the constant τ_0 corresponds to capture into defects right at the MOS interface, and λ is

the tunneling attenuation length $\lambda = [\frac{4\pi}{h} \times \sqrt{2m^* \Phi_B}]^{-1}$ according to the Wentzel-Kramers-Brillouin theory [20] with the Planck constant h, the oxide effective mass m* and the energy barrier height between the channel and the oxide Φ_B. With symmetrical time constants measured to range between 100 ms and 300 ms for different devices, the probed depth into the oxide amounts to approximately 2.8 nm for $\tau_0 = 10^{-10}$ s. [21] From the identified depths of the defects and with simplified electrostatic considerations it can be estimated that the change from a single defect within the gate oxide is in the order of a few meV. This agrees well with the corresponding change of a few mV of gate voltage around the RTS step in the transfer curves of Fig. 4a and 4f. The effect of how increase of the channel Fermi level above the oxide defect energy increases the probability of the defect to be occupied by an electron, which in turn increases the emission time constant and decreases the capture time constant (Fig. 4e). Reducing the channel Fermi level below the defect energy level favors the unoccupied defect state, which increases the capture time constant and decreases the emission time constant (Fig. 4e). Qualitatively, the strong effect of even individual oxide defects can be seen in Figs. 4f-h. With the resolution of individual oxide defects, Fig. 4g and h explain how these defects deteriorate the overall TunnelFET subthreshold swing. The slopes without current steps are well below or at 60 mV/decade, but any average over all individual defect current steps increases the overall slope significantly. A more detailed analysis of the slopes in Fig. 4h reveals that besides the dominant current steps, the change in electrostatic potential also slightly alters the tunneling dynamics, which can be seen from the deviation between the measured data in Fig. 4g and the adjusted, parallel lines in Fig. 4h. The overall impact of all effects on the average slope between $I_{DS} = 10^{-9}$ A and 10^{-8} A is an increase from 55 mV/decade to 70 mV/decade, as illustrated in Fig. 4g.

We have demonstrated vertical III-V nanowire TunnelFETs with ability to operate well below the thermal limit of 60 mV/decade with currents in technically relevant range. This performance is achieved based on due to high quality and excellent electrostatics, achieved due to high scaling

and gate-all-around geometry. Yet, bulk defects in the proximity of the heterojunction still limits the device from reaching even lower subthreshold swing. Although, the origin of the defect level at present is unknown and it may originate from several contributions, like shallow or deep impurities, structural defects, or process damage, the presence of a high strain field at the heterojunction and the limited knowledge about dopant atoms in nanowire geometries suggest that these causes will first need to be investigated to identify the origin. Furthermore, the necessary scaling makes these devices also sensitive to the individual oxide defects. Our detailed investigations show that there is room for further improvement in device performance.

Methods

Growth was performed using arrays of Au discs with a thickness of 15 nm and diameter of 44 nm which were patterned by EBL on high resistivity Si(111) substrates with a 260 nm highly doped InAs layer on top. The nanowires were grown using metalorganic vapor phase epitaxy (MOVPE) in an Aixtron CCS 18313 reactor with a total flow of 8000 sccm at a pressure of 100 mbar. After annealing at 550°C, a 200-nm-long InAs segment was grown at 460°C using trimethylindium (TMIn) and arsine (AsH_3) with a molar fraction of $X_{TMIn} = 6.1 \times 10^{-6}$ and $X_{AsH3} = 1.3 \times 10^{-4}$, respectively. The bottom part of the InAs segment was n-doped by triethyltin (TESn) ($X_{TESn} = 6.3 \times 10^{-6}$). The InAs segment was followed by a 100 nm (In)GaAsSb segment with different compostions for sample A and B using trimethylgallium (TMGa) ($X_{TMGa} = 4.9 \times 10^{-5}$), trimethylantimony (TMSb) ($X_{TMSb} = 1.2 \times 10^{-4}$) and AsH_3 (sample A: $X_{AsH3} = 2.7 \times 10^{-5}$, sample B: $X_{AsH3} = 1.3 \times 10^{-5}$) corresponding to a gas phase composition of $AsH_3/(AsH_3+TMSb)$ = 0.18 for sample A and 0.094 for sample B. A 300-nm-long GaSb segment was subsequently grown while heating to 515°C using (TMGa) ($X_{TMGa} = 4.9 \times 10^{-5}$), trimethylantimony (TMSb)

($X_{TMSb} = 7.1 \times 10^{-5}$). The GaAsSb and the GaSb segments were both p-doped during growth using diethylzinc (DEZn) ($X_{DEZn} = 3.5 \times 10^{-5}$).

Structural and compositional analysis were performed using a JEOL 3000F transmission electron microscope (TEM), operated at 300 kV, with emphasis on the InAs/InGaAsSb transition. The wires were transferred to lacy carbon covered Cu-grids by pressing these onto the substrate in order to break off the wires. Both high resolution TEM (HRTEM) and scanning TEM (STEM), employing a high angle annular dark-field (HAADF) detector, were used. For the HRTEM structural measurements, the wires were imaged in the <110>/<11-20> zone-axis. Compositional analysis was performed, using the STEM-HAADF mode in combination with the XEDS-detector to map the transition, data which were used for qualitative measurements such as length of transition and quantitative measurements for the composition along the wire. Small structural variation, such as axial and radial strain, can be measured directly in real space in HRTEM images [22], or, as used here, indirectly in Fourier space by geometric phase analysis (GPA) [23]. The latter is implemented as a script in Digital Micrograph (Gatan Inc.) and the former is done manually in the same software.

Fabrication of the devices started with digital etching of the nanowires using ozone plasma to oxidize the surface of the nanowires and citric acid to remove the oxide, reducing mainly the InAs diameter to 20 nm thereby improving the electrostatics of the devices. [24] The InGaAsSb segment was also thinned down although with a lower rate and no visible etching of the GaSb could be observed. Using atomic layer deposition (ALD), the nanowires were covered with a high-*k* bilayer using 5 cycles of Al_2O_3 and 36 cycles of HfO_2 at temperatures of 300 °C and 120 °C, respectively. Estimated oxide thickness (EOT) for the high-*k* material is 1.4 nm. A 15-nm-thick SiO_x drain-gate spacer was applied using thermal evaporation with rotation and zero tilt. The flakes of the SiO_x on the sidewalls of the nanowires where removed with diluted HF

followed by applying 12 cycles of HfO_2 at 120 °C to compensate the thinning. The gate was fabricated by first sputtering a 60-nm-thick tungsten (W) layer, followed by definition of the physical gate-length (L_g) using a resist etch-back process with O_2-plasma in a reactive ion etching (RIE) system. Tungsten was removed from the exposed sections with SF_6/Ar. Utilizing photoresist and UV-lithography followed by etching of W with RIE, the gate-pad was defined. A gate-source spacer was fabricated by a spin-on photoresist (S1800) followed by etch-back process in RIE to determine the final thickness. Gate-via and drain-via were fabricated using UV-photolithography and RIE. To realize drain and source contacts, the high-*k* was removed on top of the nanowires and in the drain-via using HF. The final step was fabrication of the top-metal, by sputtering of 10 nm Ni and 150 nm Au followed by UV-lithography and wet-etching to define the contact pads.

Modeling of band edge and defect profiles was carried out based on the knowledge on the material composition and the strain profile. The actual device geometry and estimated doping profiles were used to analyze the performance of device B. The diameter of the TunnelFET was set to 20 nm. As revealed from the TEM analysis, the channel consists of different segments of InGaAsSb with linearly varying compositions in the p+ doped source with a doping level of 10^{19} cm^{-3}. The unintentionally doped channel (background doping of 10^{17} cm^{-3}) consists of an InAs-WZ segment with an additional InAs-ZB segment adjacent to the hetero-interface. The InGaAsSb segment is divided into sub-regions based on its composition (Fig. 3a). In region R-1, alloy composition varies from InAs (to the left) to $In_{0.7}Ga_{0.3}As_{0.84}Sb_{0.16}$ (to the right), henceforth denoted as $In_{1\rightarrow 0.7}Ga_{0\rightarrow 0.3}As_{1\rightarrow 0.84}Sb_{0\rightarrow 0.16}$. Region R-2 consists of $In_{0.7\rightarrow 0.44}Ga_{0.3\rightarrow 0.56}As_{0.84\rightarrow 0.72}Sb_{0.16\rightarrow 0.28}$. Region R-3 is composed of $In_{0.44\rightarrow 0.32}Ga_{0.56\rightarrow 0.68}As_{0.72}Sb_{0.28}$ while R-4 consists of $In_{0.32}Ga_{0.68}As_{0.72}Sb_{0.28}$. The

composition is assumed to vary linearly within each segment. Various band structure quantities such as effective mass values, band gaps, and electron affinities are required for a meaningful simulation of the TunnelFET. All band structure parameters have been set to the experimentally extracted values taken from Ref. [17]. An interpolation formula suggested by Adachi [25] has been used to obtain the above quantities for the quaternary alloy $In_xGa_{1-x}As_ySb_{1-y}$ for all intermediate compositions. In this way, any explicit fitting of the band structure quantities and the band offsets have been avoided. As described in the previous section, uniaxial compressive strain is present at the hetero interface. The effect of strain on the band alignment has been modeled by the model-solid theoretical approach by Van de Walle. Simulations of the InAs/InGaAsSb nanowire TunnelFET were performed using the semi-classical simulator Sentaurus-Device. The inability to account for quantum confinement effects is a drawback of semi-classical simulations. The quantization of electronic states in the triangular-like potential well at the InAs WZ-ZB interface (Fig. 3a) results in the formation of discrete energy levels. Our calculations suggest that the triangular quantum well will form only one bound state whose energy level is very close to the top of the finite barrier. This will effectively smear out the otherwise steep valley at the interface. Simulations showed that ignoring this effect causes a serious discrepancy between simulated and experimental data. Therefore, the above effect has been modeled by introducing a pseudo-grading of the CB edge at the interface thus making it continuous (Fig. 3a). Effects related to geometrical confinement in radial direction start to emerge in III-V semiconductors when the diameter falls below 20 nm. Hence, they are not expected to significantly alter the band structure parameters (band gap, effective mass, etc.) in the source, channel, and drain segments and have been ignored. The analysis of the TEM images reveals a steep change of the mole fraction in the 3-nm-long InGaAsSb segment R-1. This may induce defect states in that segment. The degradation of the TunnelFET characteristics due to defect states has been taken into account by creating a nonlocal mesh adjacent to the hetero-interface and activating both direct and phonon-assisted nonlocal defect-assisted-tunneling (DAT) models. Choosing a peak N_t of 1.6×10^{18} cm^{-3} would result in exactly one defect state in

the segment R-1 on spatial integration. Since the exact position of a single defect within the segment R-1 is unknown and cannot be probed, in a first approximation the N_t was assumed to be constant in the whole segment. The variation of the defect energy level within the band gap then leads to best agreement with the experimental data when it is located 0.1 eV above the VB edge. A simulation parameter called *trap interaction volume*, which is a measure of the coupling strength of the tunneling process and plays the role of a scaling factor for the generation rate in the nonlocal DAT model, was adjusted to $10\ \text{Å}^3$ to match the simulated DAT current level to the experimental one. Note that this parameter is related, but not identical to the volume of the localized wave function. In addition to defects near the hetero-junction, defects at the oxide/semiconductor interface may degrade the TunnelFET performance. Donor-like defects were assumed and placed at the InAs/oxide interface. Their energetic distribution was adapted from an earlier study. [26] Defects at the InGaAsSb/oxide interface are screened by the central region of the nanowire due to its high doping concentration. Furthermore, the Fermi level in InGaAsSb is located below the VB edge which leaves the defects unfilled and electrostatically inactive. Hence, defects at the InGaAsSb/oxide interface were not considered in the TCAD analysis.

RTS noise was measured at temperatures of 11 K, 150 K and 300 K using a setup consisting of a Lake Shore Cryotronics CRX-4K probe station and an Agilent B2912A SMU. Data with time resolutions between 0.2 ms and 2 ms was collected at several different fixed gate and drain voltages using measurement times long enough to obtain at least several hundred and up to a few thousand transitions.

The transition time constants (τ) were determined from the measured data by fitting the exponential distribution (Eq. 1) to a histogram of the capture/emission times.

$$\boldsymbol{f(t) = \frac{1}{\tau} e^{-\frac{t}{\tau}}} \quad (1)$$

The distance z from the channel interface into the gate oxide was determined according to

$$z = \lambda \, ln\left(\frac{\tau}{\tau_0}\right) \quad (2)$$

where λ is the tunneling attenuation length, τ the measured time constant and τ_0 a constant. Here, we chose $\tau_0 = 10^{-10}$ s according to Ref. 21 as is often found in literature. We are aware, however, that there does not seem to be a consensus on what this constant should be and also e.g. $\tau_0 = 6.6 \times 10^{-14}$ can be found. [27] In any case, changing this number will not change the physical interpretation of our results but instead only shift the estimated depth of the defects in the gate oxide. The tunneling attenuation length λ is calculated according to

$$\lambda = \left(\frac{4\pi}{h}\sqrt{2m^{*}\phi_B}\right)^{-1} \quad (3)$$

where h is the Planck constant, m^* the effective electron mass in the gate oxide and Φ_B the barrier height from the channel material to the gate oxide. Here, we used $m^* = 0.23\ m_0$ with the electron rest mass m_0 and $\Phi_B = 2.3$ eV [28] which results in $\lambda = 0.13$ nm.

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Author Contributions

E.M fabricated the devices, performed DC characterization, did data analysis, wrote: abstract, introduction, fabrication section and conclusions. Produced Fig 1. M. H. performed the noise measurements, analyzed the noise characteristics, wrote most of the noise characterization text and produced Fig. 4. E. L. contributed to the analyzing of the data. A.R.P performed the TEM analysis, analyzed the TEM data, wrote material characterization section, and produced Fig 2. S.S. performed simulations of heterostructures, helped to analyze the data, wrote the modeling section and produced Fig. 3. A.S. supervised the modeling and helped to analyze the results. J.S. grew the nanowires and wrote the text about the growth. R.W. supervised the TEM characterization and helped to analyze the results. L.E.W. directed the project and contributed to the analyzing and writing of the manuscript. All authors discussed the data and commented on the manuscript.

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Captions

Fig. 1: Nanowire structure and electrical measurements (a) Schematic illustration of a nanowire with different sections marked with different colors. (Doping type and section lengths are indicated) (b) Schematic illustration of the vertical InAs/InGaAsSb/GaSb nanowire TunnelFET, showing all layers (left side) and regions (right side) of the transistor. High-κ is a bilayer of Al_2O_3/HfO_2 with EOT 1.4 nm, drain spacer is 15 nm SiO_x, gate metal is a 60-nm-thick tungsten layer, source spacer is an organic photoresist film and the top metal is 15/150 nm Ni/Au film. Relative thickness of the layers in the image is exaggerated to enhance visibility. (c,d) Transfer data for drive voltages 0.1- 0.5 V for device A and B, respectively. Devices show a small DIBL of 25/37 mV/V (A/B) and reaches

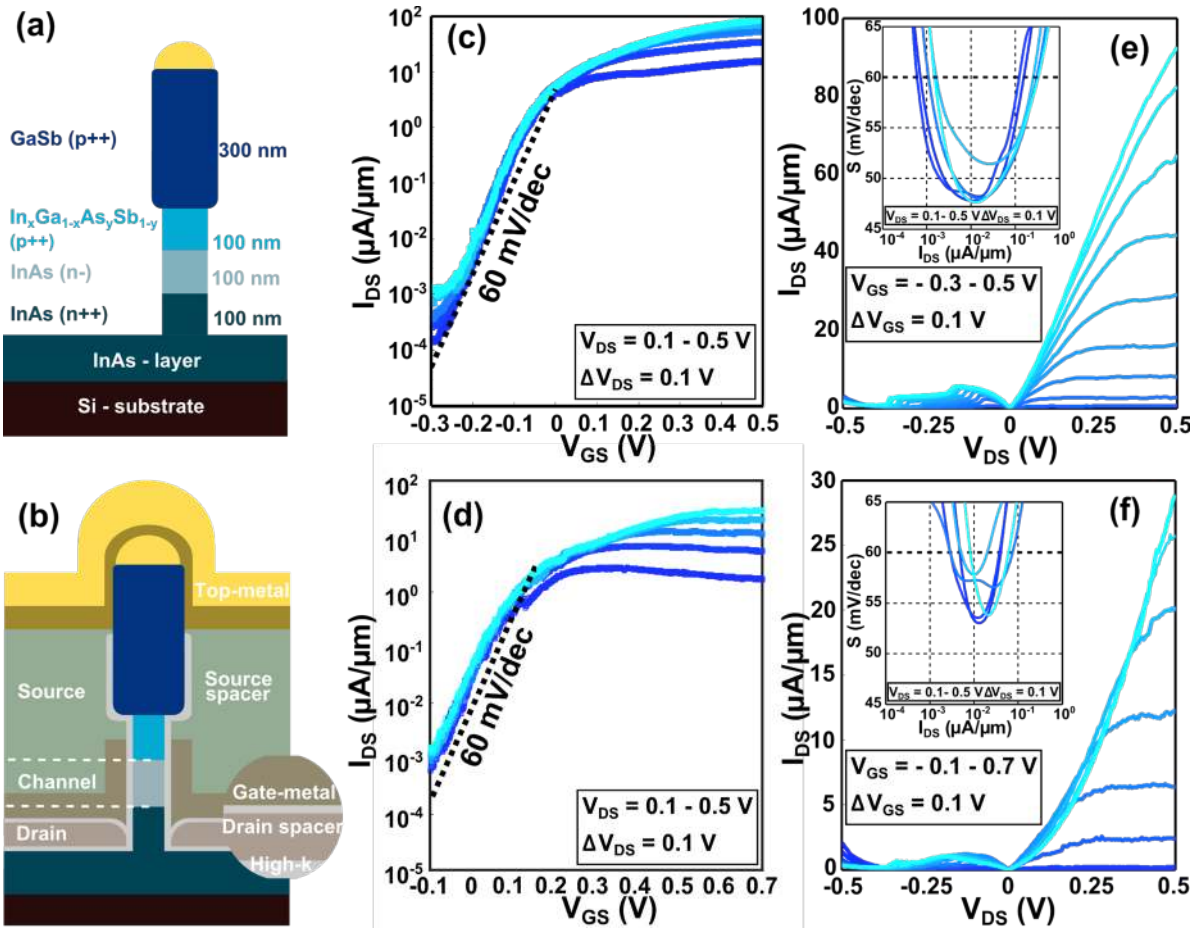
an on-current of 10.3/3.9 μA/μm (A/B) at V_{DS} = 0.3V and I_{off} = 1 nA/μm (e,f) Output data for device A and B, respectively. Device A shows larger on-currents than device B, reaching 92 μA/μm compared to the 29 μA/μm at V_{DS}=V_{GS}=0.5 V. This is mainly due to the source depletion observed in device B. Both devices have clear NDR peaks in backward direction reaching peak-to-valley-current-ratio of 14.6 and 14.2 for device A and B, respectively. Inserts in both figures shows a I_{DS} vs S graph, which confirms sub-60 mV/decade operation down to 48 mV/decade and 53 mV/decade for device A and B, respectively.

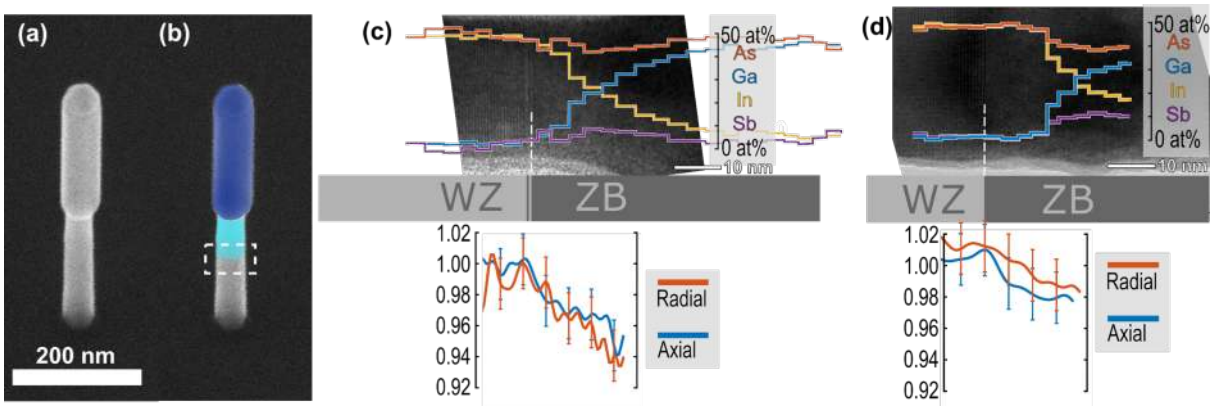
Fig. 2: Characterization of nanowires. (a) SEM image of one nanowire from sample A taken directly after growth, prior to digital etching. The diameter of the nanowire increase when the GaSb segment is grown due to increased solubility of the group III materials in the Au-particle. (b) The same nanowire as in image (a) with InGaAsSb and GaSb segments colored. The marked box shows the section of main interest for the TEM study. (c,d) Illustrates the compositional and structural changes for sample A and B respectively. The compositional changes in atomic% for respective element are shown in colored curves with legend and scale to the right, overlaying an HRTEM image of the transition. To ensure statistical significance, the curves represent the average of volume segments across the wire with a width of the individual steps. In the band across at the top, the crystal structure segments are indicated, and at the bottom, the lattice measurements are indicated along with error bars. The radial measurements are normalized to InAs d_{112},ZB (corresponding to InAs d_{-2110}, for WZ).

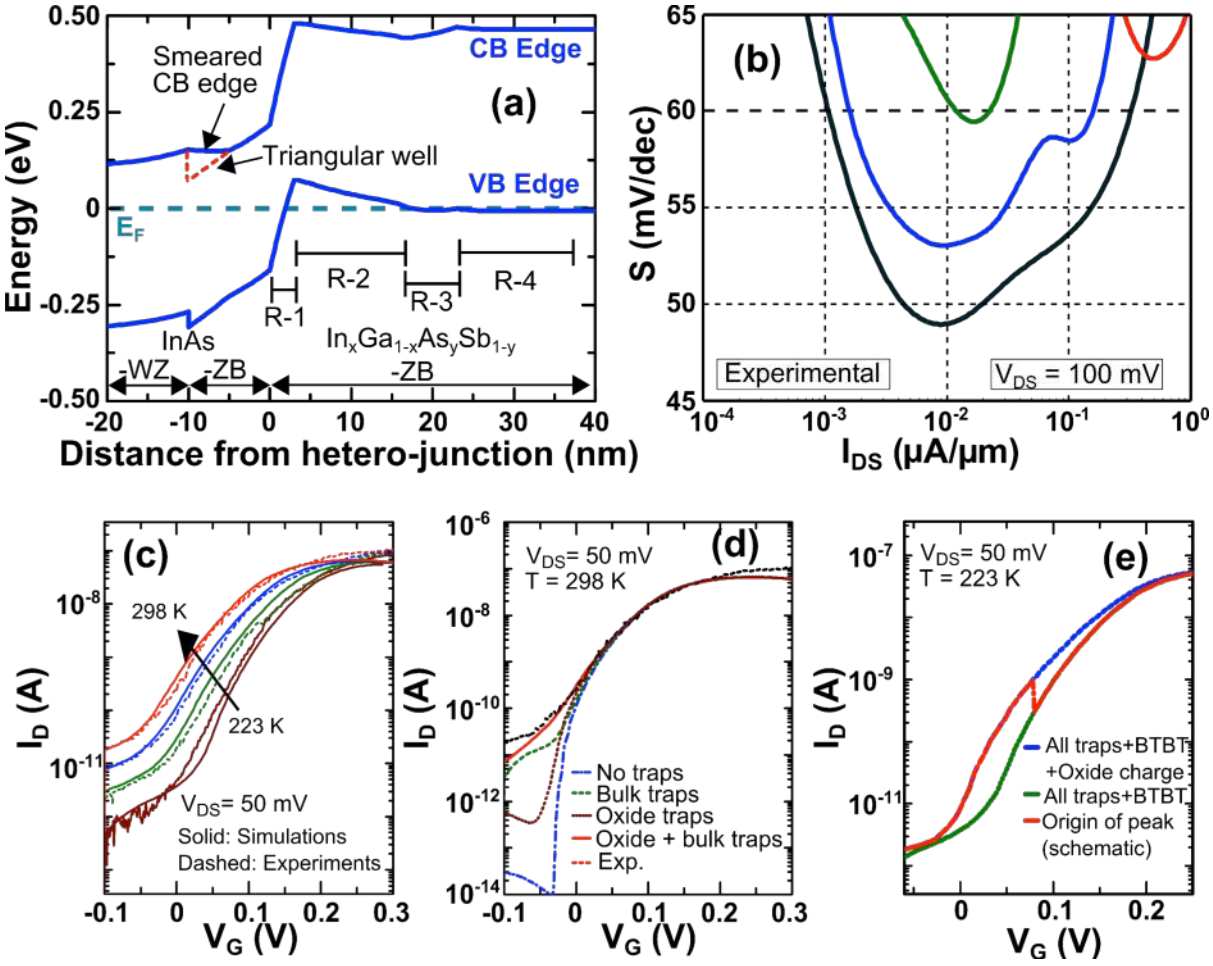
Fig. 3: Simulations of the band structure (a) Band edge diagram along the axis of the nanowire at V_{DS} = 0V and V_{GS} = 0V. A triangular-like quantum well is present at the InAs-ZB/InAs-WZ interface. (b) Current vs subthreshold swing for four different devices from same sample. All devices have one nanowire. (c) Comparison of experimental and simulated transfer characteristics for different temperatures. (d) Contribution for different type of the effects of InAs/oxide defects and bulk defects near the hetero-junction. (d) Comparison of transfer characteristics with and without a trapped positive charge at the InAs/oxide interface 50 nm away from the hetero-junction.

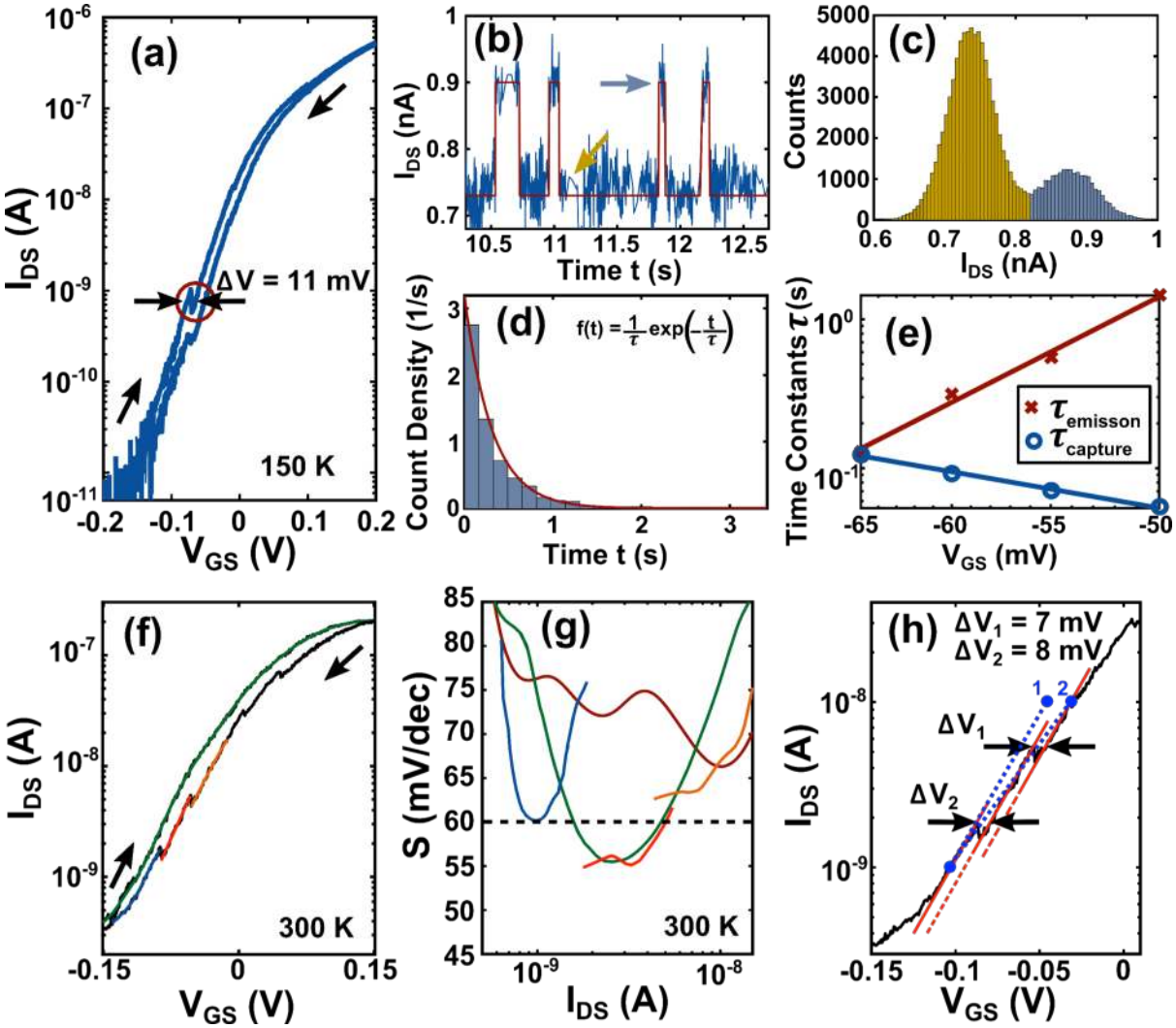
Fig. 4: RTS measurements (a) Transfer characteristic for a single nanowire transistor at 150 K. The effect of a single oxide defect is clearly visible as a distinct step. (b) Excerpt of an RTS measurement in time domain. Blue: measured signal, red: accentuation of RTS steps. The arrows indicate the upper and the lower current levels. (c) Representative histogram of the current for the entire measurement in (b). Two distinct current levels are clearly visible. The colors refer to the colors of the arrows in (b). (d) Representative histogram for the extraction of the emission time constant for the measurement in (b). The exponential distribution f(t) fitted to extract the time constant τ is indicated in red.

(e) Time constants varying close to the step indicated in (a). The same time constant for capture and emission of an electron occurs at exactly the step. (f) Transfer characteristics for a device with a number of distinct steeps in the backward sweep. (g) Subthreshold swings extracted in more detail for the different regions in (f). The individual slopes (blue, bright red, yellow) and the slope without visible steps (green) are at/below 60 mV/decade. Adding the influence of several individual defects results in an average slope (dark red), which is clearly degraded compared with the individual slopes. (h) The subthreshold region of the device presented in (f) where several distinct RTS steps are visible. Each step results from the discharge of an individual oxide defect. The individual slopes are almost parallel and any average across the individual steps will degrade the total device slope significantly. The average slope is increased from 55 mV/decade to 70 mV/decade.


(a)
GaSb (p++)
300 nm
InxGa1-xAsySb1-y (p++)
100 nm
InAs (n-)
100 nm
InAs (n++)
100 nm
InAs - layer
Si - substrate
(b)
Top-metal
Source
Source spacer
Channel
Gate-metal
Drain
Drain spacer
High-k
(c)
60 mV/dec
VDS = 0.1 - 0.5 V
ΔVDS = 0.1 V
IDS (μA/μm)
VGS (V)
(d)
60 mV/dec
VDS = 0.1 - 0.5 V
ΔVDS = 0.1 V
IDS (μA/μm)
VGS (V)
(e)
VGS = - 0.3 - 0.5 V
ΔVGS = 0.1 V
IDS (μA/μm)
VDS (V)
S (mV/dec)
VDS = 0.1- 0.5 V ΔVDS = 0.1 V
IDS (μA/μm)
(f)
VGS = - 0.1 - 0.7 V
ΔVGS = 0.1 V
IDS (μA/μm)
VDS (V)
S (mV/dec)
VDS = 0.1- 0.5 V ΔVDS = 0.1 V
IDS (μA/μm)


(a)
(b)
200 nm
(c)
50 at%
As
Ga
In
Sb
0 at%
10 nm
WZ
ZB
1.02
1.00
0.98
0.96
0.94
0.92
Radial
Axial
(d)
50 at%
As
Ga
In
Sb
0 at%
10 nm
WZ
ZB
1.02
1.00
0.98
0.96
0.94
0.92
Radial
Axial


(a)
Smeared
CB edge
CB Edge
Triangular well
VB Edge
E_F
R-1
R-2
R-3
R-4
InAs
-WZ
-ZB
$In_xGa_{1-x}As_ySb_{1-y}$
-ZB
Energy (eV)
Distance from hetero-junction (nm)
(b)
Experimental
V_{DS} = 100 mV
S (mV/dec)
I_{DS} (μA/μm)
(c)
298 K
223 K
V_{DS}= 50 mV
Solid: Simulations
Dashed: Experiments
I_D (A)
V_G (V)
(d)
V_{DS}= 50 mV
T = 298 K
No traps
Bulk traps
Oxide traps
Oxide + bulk traps
Exp.
I_D (A)
V_G (V)
(e)
V_{DS}= 50 mV
T = 223 K
All traps+BTBT
+Oxide charge
All traps+BTBT
Origin of peak
(schematic)
I_D (A)
V_G (V)


(a)
ΔV = 11 mV
150 K
I_{DS} (A)
V_{GS} (V)
(b)
I_{DS} (nA)
Time t (s)
(c)
Counts
I_{DS} (nA)
(d)
f(t) = $\frac{1}{\tau}\exp\left(-\frac{t}{\tau}\right)$
Count Density (1/s)
Time t (s)
(e)
$\tau_{emisson}$
$\tau_{capture}$
Time Constants τ(s)
V_{GS} (mV)
(f)
300 K
I_{DS} (A)
V_{GS} (V)
(g)
300 K
S (mV/dec)
I_{DS} (A)
(h)
ΔV$_1$ = 7 mV
ΔV$_2$ = 8 mV
ΔV$_1$
ΔV$_2$
I_{DS} (A)
V_{GS} (V)