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Induced strain mechanism of current collapse in AlGaN/GaN heterostructure field-effect transistors

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Gated transmission line model pattern measurements of the transient current–voltage characteristics of AlGaN/GaN heterostructure field-effect transistors (HFETs) and metal–oxide–semiconductor HFETs were made to develop a phenomenological model for current collapse. Our measurements show that, under pulsed gate bias, the current collapse results from increased source–gate and gate–drain resistances but not from the channel resistance under the gate. We propose a model linking this increase in series resistances (and, therefore, the current collapse) to a decrease in piezoelectric charge resulting from the gate bias-induced nonuniform strain in the AlGaN barrier layer. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1412282]

The so-called current collapse[1–4] and long-term stability are the most important problems preventing large-scale practical usage of nitride-based heterostructure field-effect transistors (HFETs) and metal–oxide–semiconductor HFETs (MOSHFETs) in ultra-high-power microwave systems. The current collapse manifests itself as a reduction of the device current when a large alternating signal is applied to the gate. This reduction is the main reason why the output power of AlGaN/GaN HFETs is considerably smaller than the value expected from steady-state $I-V$ characteristics. For example, a typical AlGaN/GaN HFET with a maximum saturation current about $I_{DS}\approx 1$ A/mm and the knee voltage $V_{KN}\approx 5$ V at a moderate drain bias of $V_D=35$ V, should deliver an output power

$$P_{\mathrm{OUT}}\approx I_0\times(V_D-V_{KN})/2\approx 7.5 \ \ \mathrm{W/mm}, \tag{1}$$

where $I_0\approx I_{DS}/2$ is the operating dc current. However, for such a device, even under pulsed drain bias and pulsed rf drive, conditions eliminating the device self-heating, the measured rf output power is, typically, about 2–4 W/mm. Of course, the maximum output power depends strongly on the input–output impedance matching. However, as we recently showed,[1] a precise load-pull tuning leads to the measured values of the output power that are very close to those given by Eq. (1) if one uses the actual value I_{00} of the device dc current measured under a rf drive on the gate. Hence, we conclude that the impedance mismatch is not the main reason for the difference between the expected and measured rf powers. We also showed that I_{00} differs from I_0 much more than might be expected from transistor transfer curve nonlinearity and that this difference is a direct manifestation of the current collapse.[1]

In spite of a large number of studies of the current collapse,[1–7] the physical mechanism of the effect has remained somewhat mysterious even though the phenomenon has been observed in almost all AlGaN/GaN HFETs and MOSHFETs. In this letter, we present the results of the experiments that allow us to locate the device active layer regions responsible for the current collapse. We used gated transmission line model (GTLM) measurements[8,9] [see Fig. 1(a)] under pulsed gate bias conditions in order to isolate the changes of the channel resistance under and outside the gate during the transient. The gate lengths in sequential sections of the GTLM varied from $L_G=10\ \mu$m to $L_G=100\ \mu$m, whereas the gate–source and gate–drain openings were kept constant at $L_{\mathrm{GS}}=L_{\mathrm{GD}}=10\ \mu$m. The width of all the sections was $W=200\ \mu$m. Gate voltage pulses (typically, 1–100 s long) were used to bias the devices from pinch-off to open channel conditions [Fig. 1(b)]. We used two levels of the drain bias: well below and well above the knee voltage in order to study the device behavior in both linear and saturation regimes.

The device epilayer structures were grown by low-pressure metal–organic chemical-vapor deposition (MOCVD) on insulating 4H–SiC substrates. The typical heterostructure consists of a 1–1.5 μm insulating GaN layer capped with a 25 nm $Al_{0.2}Ga_{0.8}N$ barrier layer. The measured room-temperature Hall mobility and sheet carrier concentration were 1100–1400 $\mathrm{cm^2/V\,s}$ and $(0.9–1.3)\times 10^{13}\,\mathrm{cm^{-2}}$, respectively. Source–drain Ohmic contacts were fabricated us-

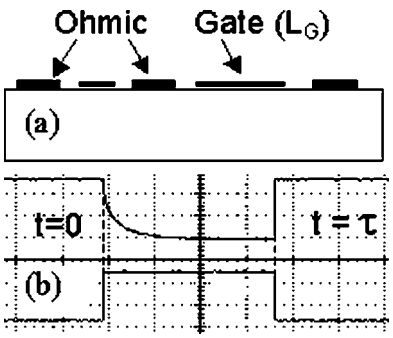

FIG. 1. (a) GTLM pattern (charge-coupled-device image) and (b) gate and drain voltage pulses used in transient measurements; 2.0 s/div; 2.0 V/div (the gate pulse); 0.5 V/div (the drain pulse).

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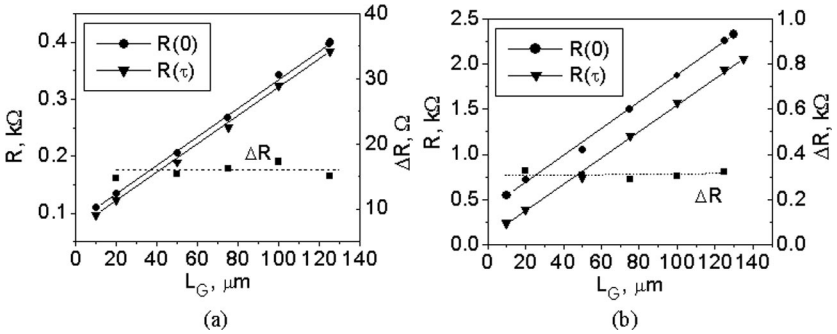

FIG. 2. Gate length dependencies of total resistance in the linear regime (a) and transfer resistance in the saturation regime (b). Circles and triangles show the data measured in the beginning and at the end of the transient, respectively. Dashed lines with squares show the gate length dependencies of the change in device resistances ΔR. Open circles show the results of the simulations based on the proposed induced strain model.

ing Ti/Al/Ti/Au electrodes annealed at 850 °C for 1 min in nitrogen ambient. Prior to the gate fabrication, a 15 nm SiO_2 layer was deposited on part of the heterostructure using plasma-enhanced chemical-vapor deposition. This SiO_2 layer was added to fabricate MOSHFETs on the same wafer, along with regular HFETs. Finally, a (Ni/Au) gate electrode was deposited using a standard lift-off technique. A reactive-ion-etched mesa was used for device-to-device isolation.

Let us first discuss the results obtained in the linear mode of device operation. In this case, the total resistance of the GTLM section measured at any moment of time t of the transient process is given by

$$R_T(t)=R_{GS}+R_{CH}(V_G)+R_{GD}, \tag{2}$$

where R_{GS} and R_{GD} are the resistances of gate–source and gate–drain openings, respectively, and R_{CH} is the gate voltage-dependent resistance of the channel under the gate. In principle, all three components of the resistance R_T might depend on time. Since the drain bias is well below the saturation voltage, the components of total resistance can be expressed as

$$R_{GS}=R_{GD}=\rho_{S0}\times L_{GS}/W, \tag{3a}$$

$$R_{CH}(L_G)=\rho_{SG}\times L_G/W, \tag{3b}$$

where the ρ_{S0} and ρ_{SG} are the sheet resistances of the two-dimensional (2D) channel outside and under the gate of the device, respectively. Here, we neglected the contribution from the contact resistances to the total resistance due to relatively large gate–source and gate–drain openings. The total resistance of the GTLM section can be then rewritten as

$$R_T(t)=2\rho_{S0}\times L_{GS}/W+(\rho_{SG}/W)\times L_G. \tag{3c}$$

The total resistances of the GTLM sections $R_T(0)$ and $R_T(\tau)$ were measured in the beginning of the transient process and at the end of the gate pulse (when the current is close to its steady-state value), respectively. The corresponding dependencies of $R_T(0)$ and $R_T(\tau)$ on the gate length are shown in Fig. 2(a). Figure 2(a) also shows the difference $\Delta R=R(\tau)-R(0)$ as a function of gate length L_G. The slope of the $R_T(L_G)$ line represents the channel resistance under the gate, while the intercept $R_T(L_G=0)$ gives the total resistance of the gate–source and gate–drain openings $R_{GS}+R_{GD}$ at a given moment during the transient. As can be seen from Fig. 2(a), both dependencies are linear and have very close slopes but different intercepts. Therefore, we conclude that the time dependence of device current in this linear regime of operation is caused by the transient variations of the gate–source and gate–drain resistances, while the channel resistance under the gate remains unaffected. Similar dependencies with equal slopes and different intercepts were measured for MOSHFET devices.

Figure 2(b) shows the GTLM measurement results for a high drain bias case corresponding to the current saturation regime. Since the gate length in our GTLM exceeds 10 μm, the velocity saturation effects do not determine the saturation current. Indeed, the effect of the saturation velocity is dominant when $\alpha=\mu(V_{GS}-V_T)/(\nu_S L_G)\gg 1$, where μ is the field-effect mobility, V_{GS} is the gate-to-source voltage, V_T is the threshold voltage, ν_S is the electron saturation velocity, and L_G is the gate length. For the measured GTLM, $\mu\sim 1000\,\mathrm{cm^2/V\,s}$, $L_G\geqslant 10\,\mu$m, $\nu_S\sim 2\times 10^5$ m/s, $V_T\sim -5$ V, and for $V_{GS}=0$, we have $\alpha\leqslant 0.25$. In this case and assuming that $g_{CH}\times R_{CH}\ll 1$, the saturation current of the HFET, I_{DS} is given by[10]

$$I_{DS}=\frac{g_{CH}(V_G-V_T)}{2(1+g_{CH}R_S)}, \tag{4}$$

where $g_{CH}=1/R_{CH}(L_G)$ is the channel conductance, V_G is the gate voltage, V_T is the threshold voltage, and R_S is the HFET series resistance. Equation (4) can be rewritten as

$$R_{TR}=\frac{V_G-V_T}{2I_{DS}}=R_S+\frac{1}{g_{CH}}=R_S+R_{CH}(L_G). \tag{5}$$

Equation (5) describes the same gate length dependence of the device "transfer resistance," $R_{TR}=(V_G-V_T)/(2I_{DS})$, for the saturation regime and is similar to Eq. (3c), which is valid for the linear regime. The GTLM results from Fig. 2(b) show that, in the saturation regime, the current transient process is again controlled by the variations of the source–gate and gate–drain resistances rather than by the channel resistance under the gate. Similar dependencies were also measured for the MOSHFET devices.

According to these results of the GTLM measurements, the source and drain series resistances are responsible for the current collapse. An increase in the source series resistance should result in a decrease of device current. An increase in both source and drain series resistances should result in an increased knee voltage. These are precisely the observations in the current collapse behavior. Therefore, our data of Fig. 2 clearly establish a linkage between gate pulsing, the resulting increase in the source–gate and gate–drain series resistances, and the current collapse. One possible explanation for the increase in series resistance values during the transient is the change in strain under and outside the gate region. When the gate bias changes from the starting point toward a more negative value, the electric field in the AlGaN barrier layer is increased. This electric field $F\approx V_T/d$, where d is the thick-

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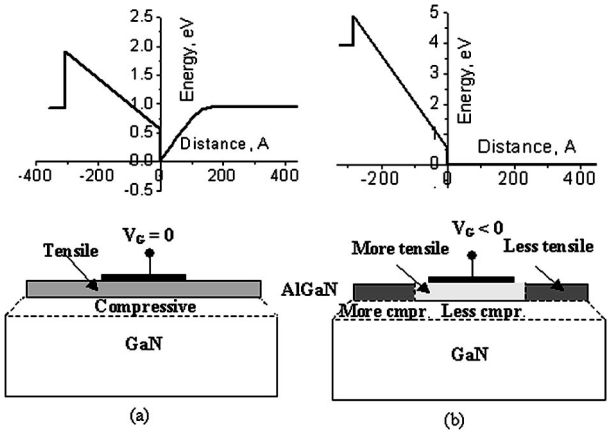

FIG. 3. Band diagrams and schematic illustration of strain in AlGaN and GaN layers induced by gate voltage. Under zero gate bias strain is tensile in the top AlGaN layer and compressive at the GaN layer surface. Negative gate bias increases tensile strain in the AlGaN layer under the gate and decreases strain outside the gate.

ness of AlGaN layer, is about $5\ \mathrm{V}/250\ \text{Å} \approx 2.5\ \mathrm{MV/cm}$, which is quite comparable to the built-in piezoelectric field. If the GaN layer is not strained then the AlGaN barrier layer simply adjusts its lattice constant to that of the underlying GaN layer.[11] Thus, the change in the electric field with gate biasing should not affect the strain. However, we believe that the surface region of the GaN layer is strained to a certain degree as well. Thus, the change in the electric field (comparable to the piezoelectric field) should affect the strain. Consequently, upon application of negative gate bias and due to the piezoelectric effect, the tensile strain in the AlGaN layer under the gate increases. This should push the AlGaN barrier layer sideways, thereby decreasing the tensile strain outside the gate near the gate edges and, hence, the piezoelectric charge in the AlGaN barrier material in these regions (see Fig. 3). This should result in increased source–gate and gate–drain resistances. Only slow processes of the piezoelectric charge adjustment and/or trapping affects are available to these regions to offset this piezoelectric charge reduction. Therefore, when the gate voltage swings back to its starting values the charges in the source–gate and gate–drain openings cannot instantly readjust to the original values. This should give rise to the observed current collapse. For the AlGaN layer under the gate, the gate metal provides a ready source of electrons to adjust the generated piezoelectric charge. Therefore, this region does not contribute to the current collapse.

In Fig. 4 we include the pulsed transfer characteristics (squares) and the transient drain current measured when the gate voltage pulse returned to zero (triangles) as a function of gate voltage amplitude for a conventional 1.5 μm gate AlGaN/GaN HFET. As seen from these data, at negative bias the current corresponding to zero pulsed gate voltage is smaller than the dc current. This is a clear manifestation of current collapse. Also from Fig. 4, the magnitude of this current collapse varies nearly linearly with the gate voltage. However, at positive gate voltage, the transient ''return'' current at $V_G = 0$ exceeds the dc current. These observations can be explained by our proposed model for current collapse. Due to gate biasing, the induced strain should vary nearly linearly with the voltage, giving rise to a monotonic increase in the electric field, induced strain, piezoelectric charge, and hence, the series resistance. A positive gate voltage pulse should change the sign of the induced strain in the barrier layer outside the gate, thereby resulting in induced accumulation charges. This should, in turn, decrease the series resistances, and hence, increase the current.

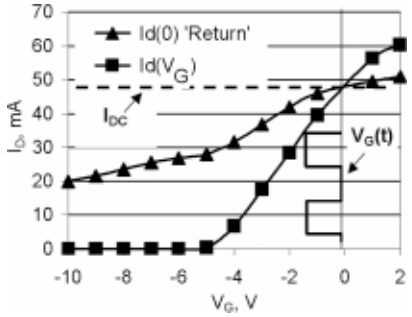

FIG. 4. Pulsed transfer characteristic (squares) and the dependencies of ''return'' current on gate pulsed bias (triangles). Applied pulsed gate voltage changes from zero to the V_G value. Dashed line shows the dc drain current also corresponding to a zero gate voltage pulse.

In conclusion, we reported on the gated transmission line model measurements of the transient current–voltage characteristics of AlGaN/GaN HFETs and MOSHFETs. Our data show that the source and drain series resistances are responsible for the current collapse. These resistances may increase from the induced strain due to gate voltage swing. Our proposed model based on the measured data for AlGaN/GaN HFETs and MOSHFETs explains nearly all the observations in the current collapse phenomenon.

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