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Inductively heated synthesized graphene with record transistor mobility on oxidized silicon substrates at room temperature

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We report chemical vapor-deposited (CVD) graphene field-effect transistors (GFETs) on conventional SiO_2/Si substrate with high-performance comparable to GFETs on boron nitride under practical ambient conditions. The fabricated GFET statistics reveal maximum carrier mobility of $\sim$17 800 cm^2/V-s. Intrinsic graphene features such as three-region output characteristics including soft current saturation have also been observed, in addition to over ten-fold gate modulation. Low-temperature studies indicate that impurity scattering is the limiting transport mechanism. Our results on graphene, synthesized by an inductively heated CVD system, suggest that the prospects of GFETs on oxidized silicon are comparable to those on ideal surfaces, e.g., *h*BN at room temperature. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4828501]

Charge transport in graphene on technological important interfaces such as oxidized silicon is of great importance owing to the maturity and widespread use of this interface as a gate oxide for solid-state transistors.[1,2] Compared to higher-k interfaces such as Al_2O_3 and HfO_2, graphene field-effect transistors on SiO_2 have higher FET mobility as a result of its relatively higher surface optical phonon energies (59 and 155 meV).[2,3] However, compared to hexagonal boron nitride (*h*BN) dielectric which offers even higher optical phonon energies (102 and 195 meV) and a flatter surface,[3,4] graphene on SiO_2/Si consistently shows inferior performance which becomes more pronounced at lower temperatures as impurity scattering obscures the expected improvement in mobility.[2] In addition, many important features of carrier transport in GFETs such as current saturation and strong electron-hole symmetry are rarely observed especially with CVD graphene transferred onto SiO_2/Si and tested under ambient conditions (the operating condition for virtually all practical device applications). Despite the outstanding GFET performance achievable on exfoliated *h*BN, the challenge of synthesizing high-quality large-area films of controlled thickness has limited its current prospects.[5] For these reasons, recent research has been increasingly focused on the transport properties of graphene on polar and non-polar interfaces, and many surface effect techniques have been reported including the use of hydrophobic, organic, and fluoropolymer thin film interfaces to enhance carrier mobility and reduce impurity doping on standard substrates.[6–9]

In this article, we report on the state-of-the-art transistors using large-area CVD graphene on standard SiO_2/Si under ambient conditions. The GFETs displayed mobilities as high as 17 800 cm^2/V-s, strong electron-hole symmetry, current saturation, and gate modulation of current that is greater than an order of magnitude. We attribute these outstanding transistor properties primarily to improvements in graphene synthesis based on our recently developed inductively-heated chemical vapor deposition,[10] and improvement in graphene transfer and fabrication that is largely free of residue. The achieved results using synthetic graphene on oxide are comparable to the leading results reported for exfoliated graphene on exfoliated *h*BN dielectric. This suggests that high-performance GFETs with all the desirable graphene properties are achievable on SiO_2/Si at room temperature without the need for interface engineering or 'ideal' dielectric materials.

The graphene used in this study was synthesized via inductively heated chemical vapor deposition, a method we recently developed.[10] Inductive heating uses magnetic fields to remotely heat the surface of conductive films and is widely used in industry.[10] This inductively heated CVD setup (Fig. 1(a)) allows rapid heating and cooling rates (up to 30 °C/s), and heating between room temperature and the growth temperature (1100 °C) can be achieved within 3 min. A typical two-step annealing and growth consumes 20–30 min. Consequently, the total processing time takes 23–33 min, compared to 60–100 min for conventional thermal CVD.[11,12] In addition, the magnetic induction heating occurs mostly on the surface of the sample via eddy currents localized to within a skin depth. As a result, it is a much more energy-efficient furnace that heats up only the desired growth surface compared to traditional cold-wall resistive heating that heats up the entire substrate. The synthesized graphene was then transferred onto 285 nm thermal oxide on silicon using a popular process, adapted from the conventional poly(methyl methacrylate) (PMMA) method[13] with 12 rinse cycles to obtain high-quality transfer.[10] Raman spectroscopy was employed to verify the quality of the monolayer graphene with the following characteristics (Fig.1(b)): (i) full width at half maximum (FWHM) of the 2D-peak is $\sim$30 cm^{-1}, (ii) the intensity ratio of the 2D/G is 3–4, and (iii) negligible D-peak.

Three-terminal back-gated GFETs were fabricated using a resist-free shadow mask process to define source and drain contacts. Device isolation was achieved by probe-tip

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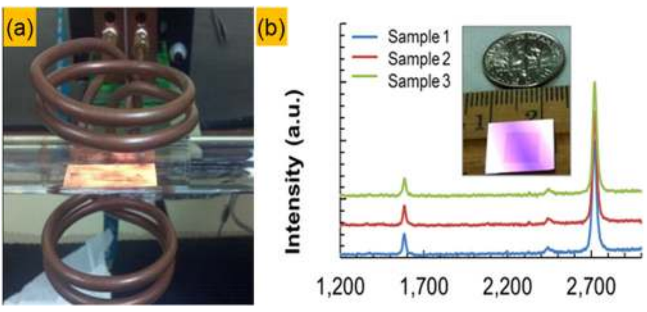

FIG. 1. (a) Image showing the center section of the inductively heated chemical vapor deposition system (operating frequency 240 kHz) for graphene synthesis; (b) representative Raman spectrum of synthesized graphene (inset is an optical image of transferred graphene onto SiO_2/Si substrate compared to a dime).

patterning. The GFET channel length varied in a doubling manner from 25 to 200 μm with a fixed channel width of 200 μm as shown in Fig. 2(a). A record mobility value of 17 800 was observed from these back-gated devices on SiO_2/Si as seen in Fig. 2(b).

Electrostatic measurements under ambient and low temperature conditions shown in Fig. 3(a) represent the electrical performance of GFETs from our synthesized graphene. A typical transfer curve as seen in Fig. 3(a) reveals an I_{ON}/I_{OFF} (or R_{MAX}/R_{MIN}) ratio over 12, which is one of the highest values reported so far for CVD graphene devices on SiO_2/Si under ambient conditions. The I_{OFF} (R_{MAX}) is defined here as the current (resistance) at the Dirac point, while the I_{ON} (R_{MIN}) is the current (resistance) at gate voltages sufficiently far from the Dirac point where the device resistance asymptotically approaches the contact resistance.[15,16] The slight positive shift of the Dirac voltage is attributed to unintentional p-type charge doping of graphene either from the polymer residue on graphene from the wet-transfer process or moisture adsorption from the ambient.[17–21] Low-temperature studies of the carrier mobility down to 6 K reveal little or no temperature dependence suggesting that impurity scattering is the dominant scattering mechanism.

Fig. 3(b) shows the statistics of the low-field carrier mobilities extracted from 22 different experimental devices using a widely accepted diffusive transport model.[14] The highest mobility obtained in our GFETs is ~17 800 cm^2/V-s and the statistical mobility data depict an average of 8400 and 10 700 cm^2/V-s for holes and electrons, respectively. These room-temperature values are significantly higher than

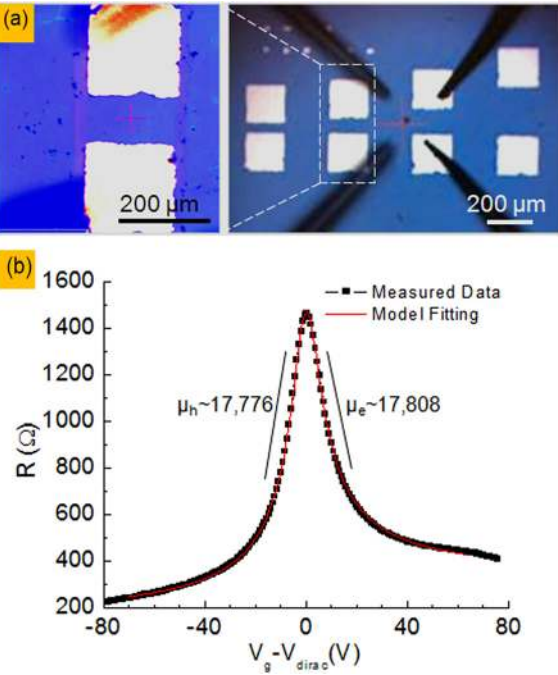

FIG. 2. Graphene field-effect transistor (GFET) made by shadow mask: (a) optical image of GFET devices (channel length varied from 25 to 200 μm). (b) Transfer curve (squares) measured at ambient condition in strong agreement with a diffusive model (line),[14] indicating outstanding mobility of ~17 800 cm^2/V-s.

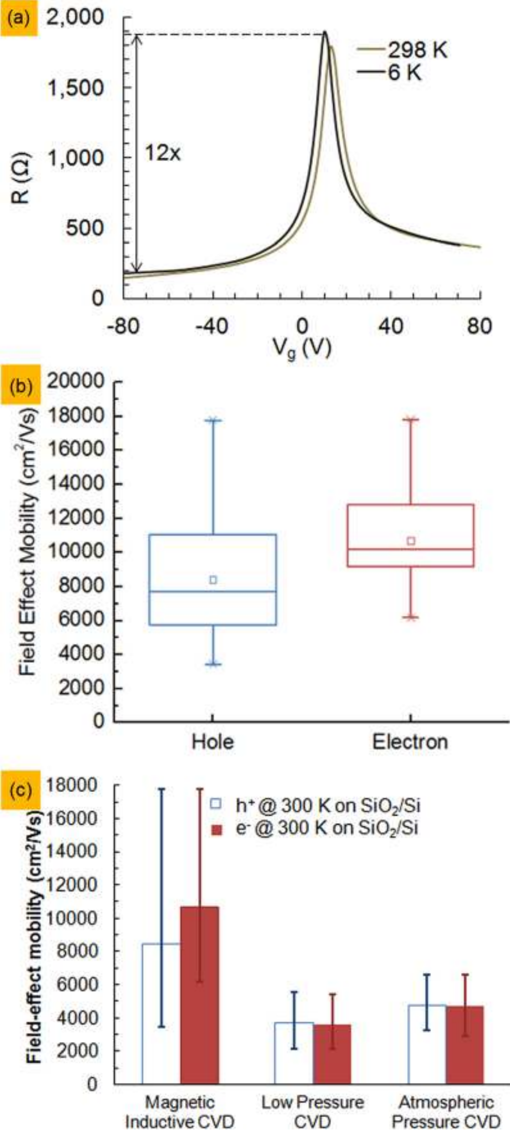

FIG. 3. Electrical characterization of fabricated graphene field effect transistors (GFET): (a) I_d versus V_g curve at 6 K and 298 K showing invariant mobility (~14 000 cm^2/V-s using the same aforementioned fitting model) with respect to the temperature. (b) Box statistical value of extracted field effect mobility from 22 GFET devices measured at ambient condition (notches from top to bottom: maximum ×, 75%, mean value □, 25%, and minimum × values) with maximum field-effect mobility up to 17 800 cm^2/V-s. (c) Comparison of field-effect mobility values from graphene transistors on SiO_2/Si sharing the same configuration, dimension, and transfer method: the inductive CVD graphene exhibited superior electrical performance than counterparts from conventional thermal chemical vapor deposition.

TABLE I. Comparison of the electrical properties of recently reported high mobility CVD and exfoliated graphene devices.

Reference	Graphene source/dielectric	Temperature for measurement	Field effect mobility (cm^2/V-s)	Impurity concentration (cm^{-2})
Cornell, 2011 (Ref. 23)	CVD-Gra/SiO_2	298 K	7300 ± 1100	N/A
UTD 2012 (Ref. 22)	CVD-Gra/SiO_2	77 K	7800–12700	$5–6 \times 10^{11}$
		298 K	5760 ± 680	$5.5–6.5 \times 10^{11}$
UT Austin 2010 (Ref. 24)	CVD-Gra/SiO_2	298 K	800–16 000	N/A
This work	CVD-Gra/SiO_2	298 K	**6000–17 800**	**$2–8 \times 10^{11}$**
Columbia U. 2010 (Ref. 26)	CVD-Gra/*h*BN	298 K	8579 or 10 713	$\sim 2 \times 10^{11}$
SKKU, 2012 (Ref. 27)	CVD-Gra/*h*BN	298 K	3000–6850	$\sim 0.5 \times 10^{11}$
UT Austin. 2010 (Ref. 30)	Exfoliated Gra/SiO_2	298 K	4000 ∼ 11 000	$5–15 \times 10^{11}$

the existing reported GFET mobilities from conventional CVD graphene on SiO_2 dielectric[22–25] and even comparable to GFETs on *h*BN[26–28] dielectric as well as the best samples of exfoliated graphene on SiO_2/Si[29,30] as summarized in Table I. Although high mobility values had been reported for conventional CVD graphene on SiO_2/Si,[24] graphene synthesized in this work exhibits more stable performance with much higher average mobility value and lower variation range. We note that the maximum GFET mobility achieved in this work is within a factor of two of the surface phonon-limited theoretical value in the absence of charge or neutral impurity scattering (∼25 900 cm^2/V-s),[3] indicating further progress is possible. Using the same device configuration and dimension, we conducted another comparison among different graphene synthesis methods to show that our developed synthesis route is the dominating factor for superior mobility of our GFETs. Fig. 3(c) shows the same batch of devices made using three different CVD methods, and the mobility of graphene synthesized via inductive heating is 2-3 times higher than counterparts from conventional low and atmospheric pressure CVD.

In addition to the high mobility and I_{ON}/I_{OFF}, the fabricated GFETs also demonstrated current saturation and the unique three-region response at room temperature. Although current saturation and the three-region response of graphene has been reported in 2008,[31] it had been limited to exfoliated graphene with top-gate configuration and measured at low temperature. Recent reports on this topic still employs top-gate,[32] or exfoliated graphene.[33] This is likely because back-gate structures with thick thermal oxide are considered a poor electrostatic media for observing these features.[31] However, our measurement in Fig. 4 shows that these features can be observed for the graphene studied here with thick gate oxides commonly used for basic post-transfer studies. Moreover, similar to the low temperature behavior (Fig. 4(a)), the I_d-V_d output curve exhibits a complete three-region response with kink-effect[31–33] at ambient condition (purple and green curves in Fig. 4(b)). Physics based drift-diffusive transport modeling,[34] including fundamental effects such as field-dependent quantum capacitance, fixed velocity saturation, and fixed contact resistance show good agreement with the experimental output characteristics (Fig. 4(c)). The model parameters are based on values similar to those extracted from the transfer characteristics with (the best fit) saturation velocity of $\sim 5 \times 10^7$ cm/s, which is close to the theoretical estimate for charge carriers in graphene on an oxidized Si substrate.[3] The high saturation velocity, which is about half of the Fermi velocity in graphene is further affirmation of the fast carrier properties of the high-quality graphene on SiO_2/Si.

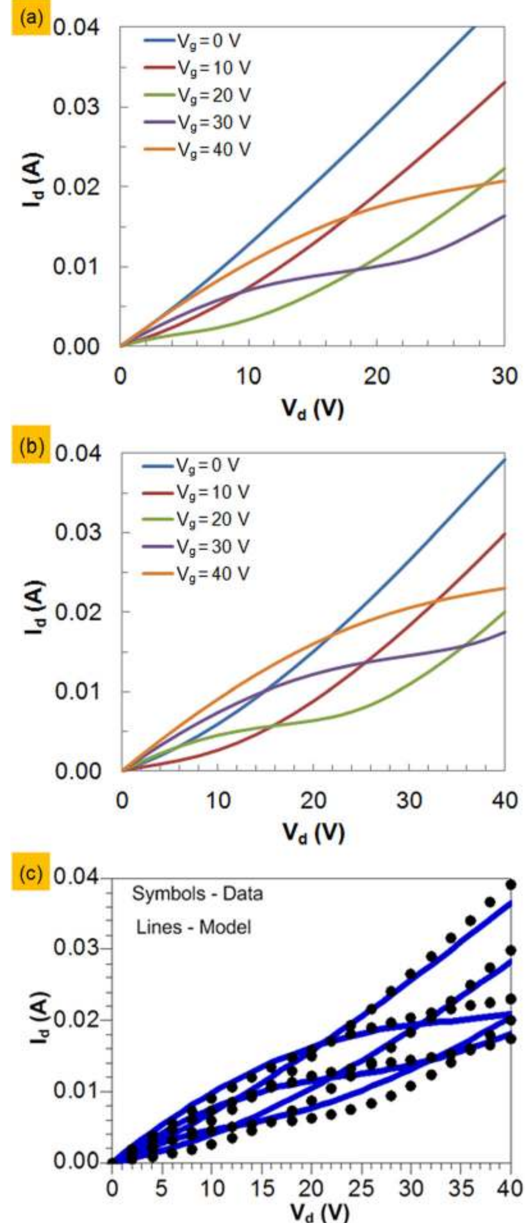

FIG. 4. Experimental I_d versus V_d with different gate bias showing saturation and the so-called second linear region (purple and brown curve) at (a) 6 K and (b) 298 K (room temperature); (c) drift-diffusive transport modeling exhibits a good agreement with experimental data in (b).

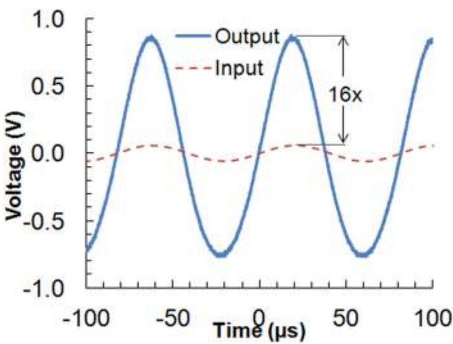

FIG. 5. Amplifier with 16× voltage gain achieved with the fabricated graphene field effect transistors.

Given the high mobility, high I_{ON}/I_{OFF} ratio and demonstrated current saturation, our high-performance GFETs are well suited for analogue applications such as room temperature terahertz devices and detectors.[35,36] For instance, a common-source amplifier shown in Fig. 5 yields a 16 × voltage gain between output (at the drain) and input (at the gate). The hole branch of the GFET was employed showing the expected non-inverting amplifier response.[35] The input source was provided by a function generator (12.2 kHz) with an oscilloscope serving as the load with a load impedance of 1 MΩ.

In conclusion, we have demonstrated GFETs from inductively heated CVD graphene transferred onto SiO_2/Si substrate with high carrier mobility comparable to those achieved on *h*BN under ambient conditions. Output characteristics indicate three-region response including soft current saturation, which is an intrinsic feature of GFETs. A GFET amplifier with voltage gain of about 16× was also realized. Our results suggest that the prospects of experimental GFETs on oxidized silicon are comparable to those on ideal surfaces at room temperature.

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