

Inductorless DC-AC Cascaded H-bridge Multilevel Boost Inverter for Electric/Hybrid Electric Vehicle Applications

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Abstract—This paper presents an inductorless cascaded H-bridge multilevel boost inverter for EV and HEV applications. Currently available power inverter systems for HEVs use a DC-DC boost converter to boost the battery voltage for a traditional 3-phase inverter. The present HEV traction drive inverters have low power density, are expensive, and have low efficiency because they need a bulky inductor. An inductorless cascaded H-bridge multilevel boost inverter for EV and HEV applications is proposed in this paper. Traditionally, each H-bridge needs a DC power supply. The proposed inductorless cascaded H-bridge multilevel boost inverter uses a standard 3-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg which uses a capacitor as the DC power source. Fundamental switching scheme is used to do modulation control and to produce a 5-level phase voltage. Experiments show that the proposed inductorless DC-AC cascaded H-bridge multilevel boost inverter can output a boosted AC voltage.

I. INTRODUCTION

Recently, because of increasing oil prices and environmental concerns, hybrid electric vehicles (HEV) and electric vehicles (EV) are gaining more attention because they have higher efficiency and lower emissions. An HEV typically combines a smaller internal combustion engine of a conventional vehicle with a battery pack and an electric motor to drive the vehicle. The combination offers lower emissions but with the power range and convenient fueling of conventional (gasoline and diesel) vehicles. An EV typically uses rechargeable batteries and an electric motor. The batteries need to be charged regularly.

Prepared by the Oak Ridge National Laboratory, Oak Ridge, Tennessee 37831, managed by UT-Battelle for the U.S. Department of Energy under contract DE-AC05-00OR22725.

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Both HEV and EV need a traction motor and a power inverter to drive the traction motor. The power inverter is the key part of a HEV or EV. The requirements of the power inverter include high peak power and low continuous power rating. Currently available power inverter systems for HEVs use a DC-DC boost converter to boost the battery voltage for a traditional 3-phase inverter. If the motor is running on low to medium power, the DC-DC boost converter is not needed and the battery voltage will be directly applied to the inverter to drive the traction motor. If the motor is running in high power mode, the DC-DC boost converter will boost the battery voltage to a higher voltage so that the inverter can provide higher power to the motor. The present HEV traction drive inverters have low power density, are expensive, and have low efficiency because they need bulky inductors for the DC-DC boost converters.

An inductorless cascaded H-bridge multilevel boost inverter shown in Fig. 1 for EV and HEV applications is described in this paper. Traditionally, each H-bridge needs a DC power supply [1-5]. The proposed inductorless cascaded H-bridge multilevel boost inverter uses a standard 3-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg which uses a capacitor as the DC power source [6][7]. Fundamental switching scheme is used to do modulation control and to output 5-level phase voltage. Experiments show that the proposed inductorless DC-AC cascaded H-bridge multilevel boost inverter can output a boosted AC voltage.

II. WORKING PRINCIPLE OF INDUCTORLESS CASCADED H-BRIDGE MULTILEVEL BOOST INVERTER

The topology of the proposed inductorless DC-AC cascaded H-bridge multilevel boost inverter is shown in Fig. 1. The inverter uses a standard 3-leg inverter (one leg for each phase) and an H-bridge with a capacitor as its DC source in series with each phase leg.

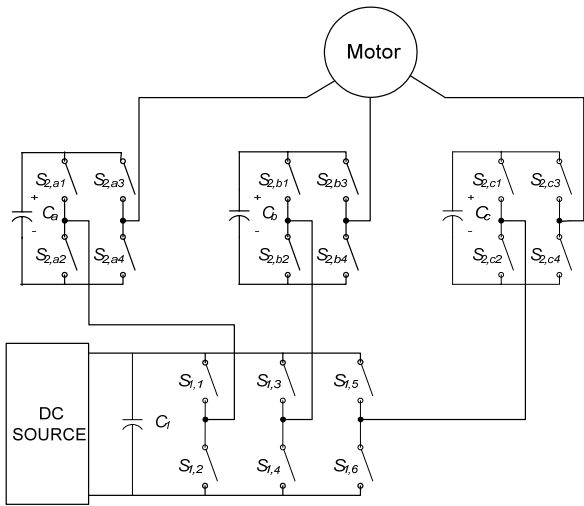


Fig. 1. Topology of the proposed inductorless DC-AC cascaded H-bridge multilevel boost inverter.

To see how the system works, a simplified single phase topology is shown in Fig. 2. The output voltage v_1 of this leg of the bottom inverter (with respect to the ground) is either $+V_{dc}/2$ (S_5 closed) or $-V_{dc}/2$ (S_6 closed). This leg is connected in series with a full H-bridge which in turn is supplied by a capacitor voltage. If the capacitor is kept charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S_1, S_4 closed), 0 (S_1, S_2 closed or S_3, S_4 closed), or $-V_{dc}/2$ (S_2, S_3 closed). An example output waveform that this topology can achieve is shown in Fig. 3(a). When the output voltage $v = v_1 + v_2$ is required to be zero, one can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ or $v_1 = -V_{dc}/2$ and $v_2 = +V_{dc}/2$.

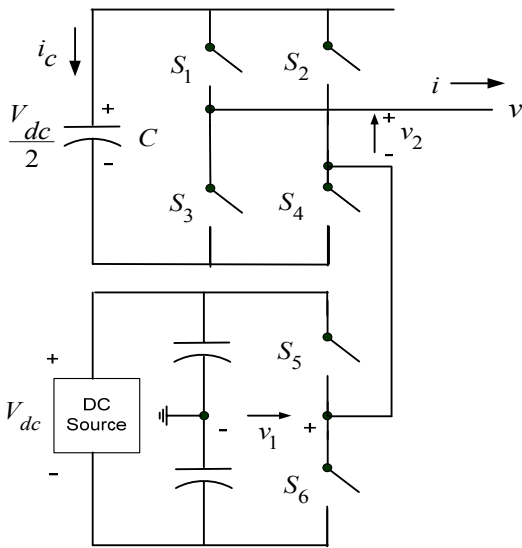


Fig. 2. Single phase of the proposed inductorless DC-AC cascaded H-bridge multilevel boost inverter.

Further capacitor's voltage regulation control detail is illustrated in Fig. 3. During $\theta_1 \leq \theta \leq \pi$, the output voltage in Fig. 3(a) is zero and the current $i > 0$. If S_1, S_4 are closed (so that $v_2 = +V_{dc}/2$) along with S_6 closed (so that $v_1 = -V_{dc}/2$), then the capacitor is discharging ($i_c = -i < 0$ see Fig. 3(b)) and

$v = v_1 + v_2 = 0$. On the other hand, if S_2, S_3 are closed (so that $v_2 = -V_{dc}/2$) and S_5 is also closed (so that $v_1 = +V_{dc}/2$), then the capacitor is charging ($i_c = i > 0$ see Fig. 3(c)) and $v = v_1 + v_2 = 0$. The case $i < 0$ is accomplished by simply reversing the switch positions of the $i > 0$ case for charging and discharging of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S_1, S_4 , and S_6 are closed or the switches S_2, S_3, S_5 are closed depending on whether it is necessary to charge or discharge the capacitor. Therefore, it is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage.

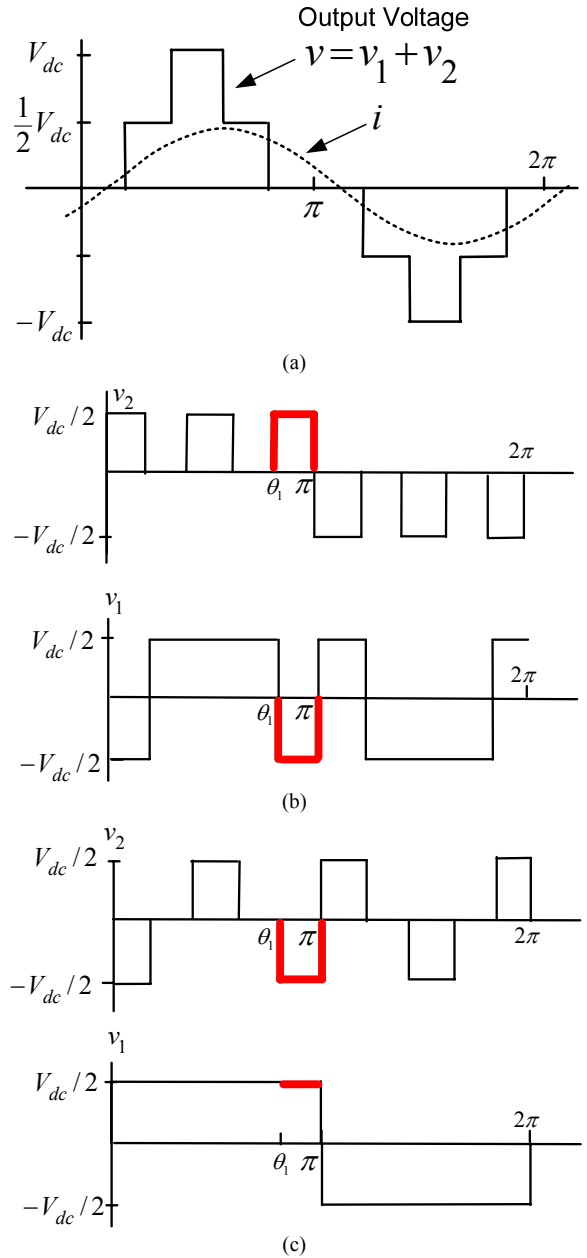


Fig. 3. Capacitor voltage regulation with capacitor charging and discharging (a) overall output voltage and load current; (b) capacitor discharging; (c) capacitor charging.

If fundamental frequency switching modulation control method is used, the goal of the switching control is to output a 5-level voltage waveform, and the load current is a sinusoidal waveform which is shown in Fig. 3(a). If the capacitor's voltage is higher than $V_{dc}/2$, control the switches S_5 and S_6 to output voltage waveform v_1 , and control the switches S_1, S_2, S_3 and S_4 to output voltage waveform v_2 shown in Fig. 3(b). The highlighted in Fig. 3(b) is the capacitor discharging period, and the inverter's output voltage is 0. If the capacitor's voltage is lower than $V_{dc}/2$, control the switches S_5 and S_6 to output voltage waveform v_1 , and control the switches S_1, S_2, S_3 and S_4 to output voltage waveform v_2 shown in Fig. 3(c). The highlighted in Fig. 3(c) is the capacitor charging period when the inverter's output voltage is 0. Therefore, the capacitors' voltage can be regulated by alternating the capacitor's charging and discharging control when the inverter output is 0.

This method of regulating the capacitor voltage depends on the voltage and current not being in phase. That is, one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current. In other words, the highest output AC voltage of the inverter depends on the displacement power factor of the load.

III. SWITCHING CONTROL OF INDUCTORLESS CASCADED H-BRIDGE MULTILEVEL BOOST INVERTER

There are several kinds of modulation control methods such as traditional sinusoidal PWM method (SPWM) [8-16], space vector PWM method, selective harmonic elimination method [17-22], and active harmonic elimination method [23], and they all can be used for inverter modulation control. For the proposed inductorless DC-AC boost inverter control, a practical modulation control method is the fundamental frequency switching control for high output voltage and SPWM control for low output voltage which only uses the bottom inverter. In this paper, fundamental frequency switching control is used.

The key issue of the fundamental frequency modulation control is to choose two switching angles. In this paper, the goal is to output the desired fundamental frequency voltage and to eliminate the 5th harmonic. Mathematically, this can be formulated as the solution to the following equations:

$$\begin{aligned} \cos(\theta_1) + \cos(\theta_2) &= m_a \\ \cos(5\theta_1) + \cos(5\theta_2) &= 0 \end{aligned} \quad (1)$$

This is a system of two transcendental equations with two unknowns θ_1 and θ_2 , and m_a is the output voltage index. Traditionally, the modulation index is defined as

$$m = \frac{V_1}{V_{dc}/2} \quad (2)$$

Therefore, the relationship between the modulation index m and the output voltage index m_a is

$$m = \frac{4}{\pi} m_a \quad (3)$$

There are many ways one can solve (1) for the angles. Here, the resultant method [17] is used to find the switching angles. A practical solution set is shown in Fig. 4 which is continuous from modulation index 0.75 to 2.42.

Although it can be seen from Fig. 4 that the modulation index range for the 5-level fundamental frequency switching control method can reach 2.42 which is double of the traditional power inverter, it requires the capacitors' voltage to be kept constant at $V_{dc}/2$.

Traditionally, the maximum modulation index for linear operation of a traditional full-bridge bi-level inverter using SPWM control method is 1 (without third harmonic compensation) and 1.15 (with third harmonic compensation, and the inverter output voltage waveform is SPWM waveform, not square waveform). With the cascaded H-bridge multilevel inverter, the maximum modulation index for linear operation can be as high as 2.42; however, the maximum modulation index depends on displacement power factor as will be shown in the next section.

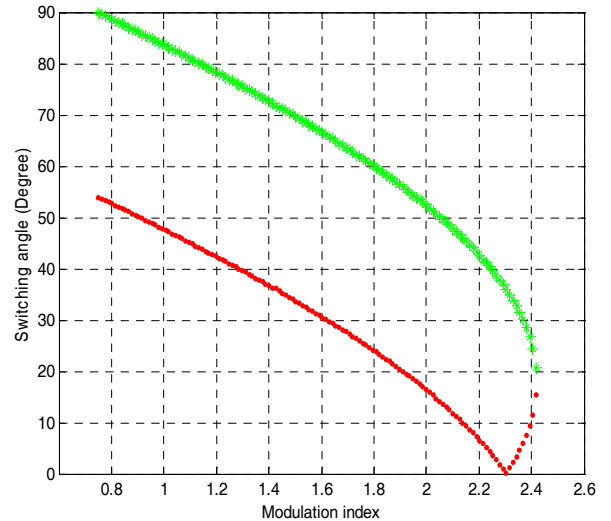


Fig. 4. Switching angle solutions for proposed inductorless DC-AC cascaded H-bridge multilevel boost inverter control.

IV. OUTPUT VOLTAGE BOOST

As previously mentioned, the cascaded H-bridge multilevel inverter can output a boosted AC voltage to increase the output power, and the output AC voltage depends on the displacement power factor of the load. Here, the relationship of boosted AC voltage and the displacement power factor is discussed.

It is assumed that the load current displacement angle is φ as shown in Fig. 5. To balance the capacitor voltage, the pure capacitor charging amount needs to be greater than the pure discharging amount. That is, to regulate the capacitor's voltage with fundamental frequency switching scheme, the following equation must be satisfied,

$$\int i_{\text{charging}} d\theta - \int i_{\text{discharging}} d\theta > 0 \quad (4)$$

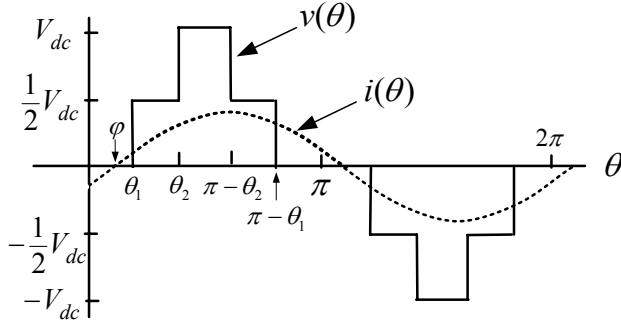


Fig. 5. Capacitor charging and discharging cases.

To see it in detail, the current charging and discharging with inductance load can be classified into three cases. For convenience of discussion of practical inductance load, it is reasonable to assume the inductance load current as:

$$i = I \sin(\omega t - \varphi) \quad (5)$$

and the displacement power factor

$$pf = \cos(\varphi) \quad (6)$$

The three cases are:

$$(1) 0 \leq \varphi \leq \theta_1$$

$$\int_0^{\varphi} |i| d\theta + \int_{\varphi}^{\theta_1} i d\theta + \int_{\pi - \theta_1}^{\pi} i d\theta - \int_{\theta_2}^{\pi - \theta_2} i d\theta > 0 \quad (7)$$

$$(2) \theta_1 < \varphi \leq \theta_2$$

$$\int_0^{\theta_1} |i| d\theta + \int_{\pi - \theta_1}^{\pi} i d\theta - \int_{\theta_2}^{\pi - \theta_2} i d\theta > 0 \quad (8)$$

$$(3) \theta_2 < \varphi \leq \pi/2$$

$$\int_0^{\theta_1} |i| d\theta + \int_{\pi - \theta_1}^{\pi} i d\theta - \int_{\theta_2}^{\pi - \theta_2} i d\theta > 0 \quad (9)$$

Combining (5), (6), (7), (8) and (9), it can be concluded that for $0 \leq \varphi \leq \theta_1$,

$$pf \leq \frac{\pi}{4m} \quad (10)$$

and for $\theta_1 < \varphi \leq \pi/2$,

$$pf \leq \cos \left[\tan^{-1} \left(\frac{\cos(\theta_2)}{\sin(\theta_1)} \right) \right] \quad (11)$$

Therefore, the conditions for the fundamental frequency switching scheme to eliminate the 5th harmonic and to regulate the capacitor's voltage are (10) and (11).

For practical applications, direct use of (10) and (11) is not convenient. A more convenient way to use (10) and (11) is to use minimum phase displacement angles. That means if the phase displacement angle is greater than the minimum angle, the voltage can be regulated anyway.

Fig. 6 shows the minimum phase displacement angle computed by (4)-(11). From the figure, it can be seen that for modulation index range $m < 1.27$ (the inverter output is 5-level

waveform, not bi-level waveform or square waveform), the minimum phase angle displacement is 0 which means the capacitor's voltage can be regulated for all displacement power factors in this modulation index range. For modulation index range $m > 1.27$, the required minimum phase displacement angle is shown in Fig. 6. Fig. 6 also shows the two switching angles.

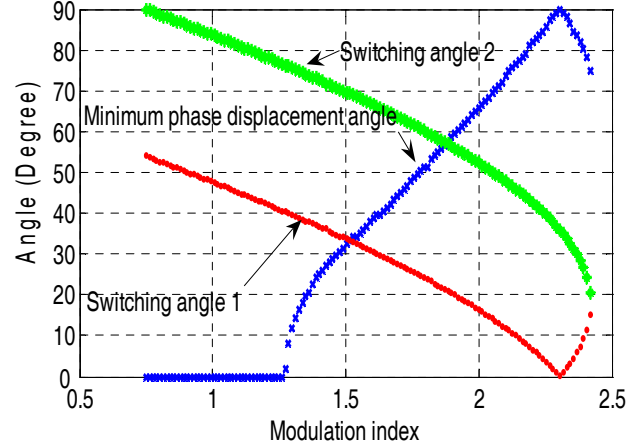


Fig. 6. Minimum phase displacement angle.

The phase displacement power factor vs. the output voltage modulation index is shown in Fig. 7.

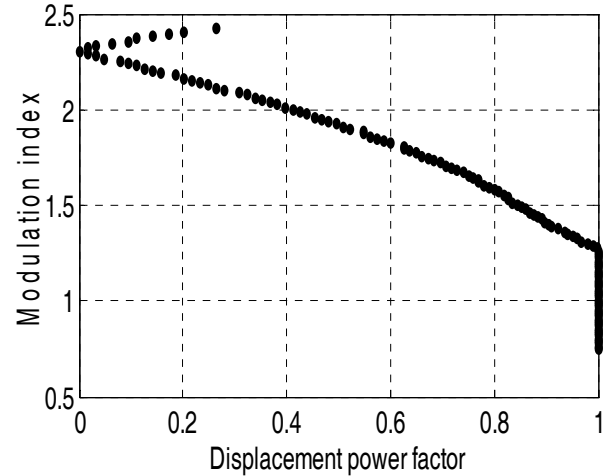


Fig. 7. Displacement power factor and output voltage modulation index.

It can be derived from Fig. 7 that the highest output voltage modulation index depends on the displacement power factor. The inverter can regulate the capacitor's voltage with displacement power factor 1 if modulation index is below 1.27; if modulation index is above 1.27, displacement power factor must be lower than a specified amount. For practical applications, the highest output voltage is determined when the load is determined.

V. EXPERIMENTAL IMPLEMENTATION AND VALIDATION

To experimentally validate the proposed inductorless DC-AC cascaded H-bridge multilevel boost inverter control

scheme, a prototype 5 kW three-phase cascaded H-bridge multilevel converter has been built using 100V, 180A MOSFETs as the switching devices which is shown in Fig. 8. A real-time variable output voltage, variable frequency three-phase motor drive controller based on Altera FLEX 10K field programmable gate array (FPGA) is used to implement the control algorithm. For convenience of operation, the FPGA controller is designed as a card to be plugged into a personal computer, which uses a peripheral component interconnect (PCI) bus to communicate with the microcomputer. To maintain the capacitors' voltage balance, a voltage sensor is used to detect the capacitors' voltage and feed the voltage signal into the FPGA controller. A 15 hp induction motor is used as the load of the inverter, and the motor was loaded to less than 5 kW in the experiments.

Fig. 9 shows the output phase voltage waveform, line-line voltage waveform, and phase current waveform with the output frequency 60 Hz. The modulation index of the output voltage is 2.03, and the capacitors' voltage is regulated to $V_{dc}/2$. The phase voltage waveform shows that the output voltage is 5 level, the line-line voltage is 9 level, and the phase current is a near-sinusoidal waveform.

Fig. 10 shows the normalized FFT analysis of the phase voltage, and that the 5th harmonic is very low (below 1%). Fig. 11 shows the normalized FFT analysis of the phase current which also has very low 5th harmonic current of 0.3%.

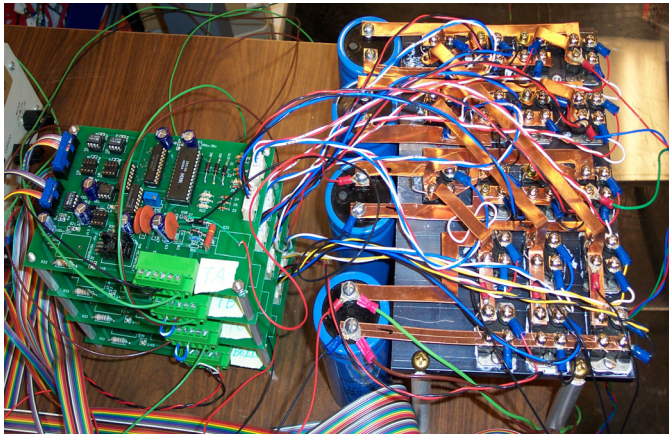


Fig. 8. 5 kW inductorless DC-AC cascaded H-bridge multilevel boost inverter prototype.

The experimental results and their FFT analysis all verified the fundamental frequency switching control. The modulation index in this experiment is from 0 to 2.03, which is much wider than the normal modulation index range 0~1.15 for traditional standard three-leg inverter.

A fixed R-L load is also used to confirm output voltage tests. First, the load was connected to the bottom traditional inverter to output its highest voltage; second, the load was connected to the cascaded H-bridge multilevel inverter with the same DC power supply voltage. The output voltages for the two cases are shown in Table I.

Table I shows that the highest output voltage of the cascaded H-bridge multilevel inverter is much higher than that of the traditional inverter. The voltage boost ratio is higher than 1.4 for the whole testing frequency range.

Table I also shows the highest output voltage of the inverter is decreasing when the frequency is decreasing; this is because the impedance of the inductor is decreasing. Another issue is the boost voltage ratio is decreasing when the frequency is decreasing; this is because the power factor is increasing for fixed R-L load.

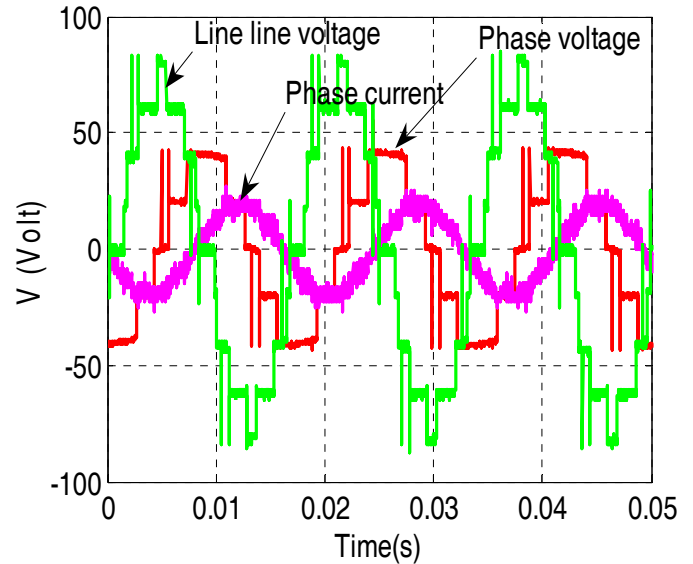


Fig. 9. Phase voltage waveform, line-line voltage waveform and current waveform with 15 hp induction motor load ($m=2.03$ and $f=60$ Hz).

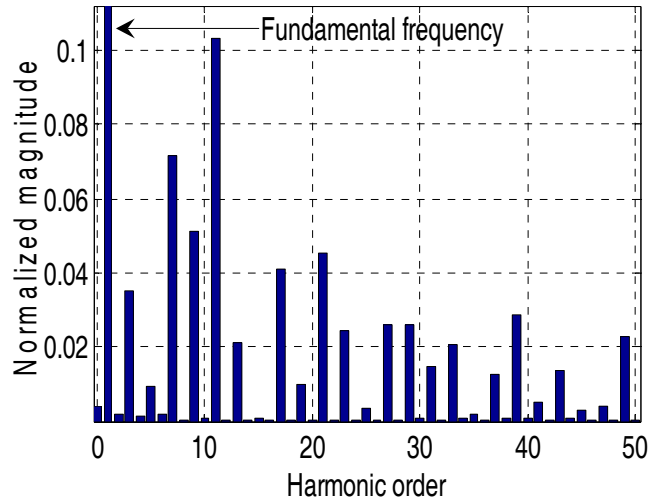


Fig. 10. Normalized FFT analysis of phase voltage.

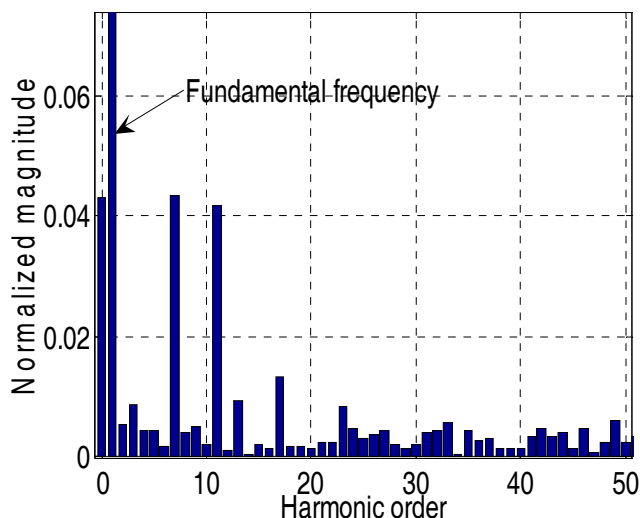


Fig. 11. Normalized FFT analysis of phase current.

Table I: Highest output voltage for traditional inverter and cascaded H-bridge multilevel inverter (DC Bus is 40 Volts)

Test frequency (Hz)	Traditional inverter output voltage (V)	Cascaded H-bridge multilevel inverter output voltage (V)	Boost ratio
200	23.1	42.8	1.85
150	23.1	42.2	1.82
100	23.1	41.2	1.78
60	23.1	37.7	1.63
40	23.1	33.1	1.43

VI. CONCLUSIONS

The proposed inductorless cascaded H-bridge multilevel boost inverter uses a standard three-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg. Fundamental switching scheme is used for modulation control, and to output 5-level phase voltage. Experiments show that the proposed inductorless DC-AC cascaded H-bridge multilevel boost inverter can output a boosted AC voltage with the same DC power supply which has wider modulation index range than the traditional inverter. The application of this DC-AC boost inverter on HEV and EV applications can remove the bulky inductor of the present DC-DC boost converter, increasing the power density possible.

REFERENCES

[1] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, Jan./Feb. 1999, pp. 36-44.
 [2] J. S. Lai and F. Z. Peng, "Multilevel converters – A new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no.3, May/June 1996, pp. 509-517.

[3] J. Rodríguez, J. Lai, and F. Peng, "Multilevel inverters: a survey of topologies, controls and applications," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, Aug. 2002, pp. 724-738.
 [4] Z. Du, L. M. Tolbert, J. N. Chiasson, "A Cascade Multilevel Inverter Using a Single DC Source," *IEEE Applied Power Electronics Conference*, March 19-23, 2006, Dallas, Texas, pp. 426-430.
 [5] K.A. Corzine, F.A. Hardrick, and Y.L. Familant, "A Cascaded Multilevel H-Bridge Inverter Utilizing Capacitor Voltages Sources," *Proceedings of the IASTED International Conference, Power and Energy Systems*, Feb. 24-26, 2003, Palm Springs, California, pp. 290-295.
 [6] J. N. Chiasson, B. Özpineci, and L. M. Tolbert, "Five-level three-phase hybrid cascade multilevel inverter using a single dc source," *IEEE Applied Power Electronics Conference*, February 25 - March 1, 2007, Anaheim CA, pp. 1504-1507.
 [7] J. N. Chiasson, B. Özpineci, Z. Du, and L. M. Tolbert, "Conditions for capacitor voltage regulation in a five-level cascade multilevel inverter: application to voltage-boost in a PM drive," *IEEE International Electric Machines and Drives Conference*, May 3 – 5, 2007, Antalya, Turkey, pp. 731-735.
 [8] J. K. Steinke, "Control strategy for a three phase AC traction drive with a 3-level GTO PWM inverter," *IEEE PESC*, 1988, pp. 431-438.
 [9] P. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Trans. Industry Applications*, vol. 33, Jan./Feb. 1997, pp. 202–208.
 [10] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel inverters," *IEEE Industry Applications Society Annual Meeting*, October 1999, Phoenix, AZ, pp. 1186–1192.
 [11] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, G. Sciuotto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electronics*, vol. 7, no. 3, July 1992, pp. 497-505.
 [12] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel PWM methods at low modulation indices," *IEEE Trans. Power Electronics*, vol. 15, no. 4, July 2000, pp. 719-725.
 [13] D. G. Holmes, "The significance of zero space vector placement for carrier based PWM schemes," *IEEE IAS Annual Meeting*, 1995, pp. 2451-2458.
 [14] J. Vassallo, J. C. Clare, P. W. Wheeler, "A power-equalized harmonic-elimination scheme for utility-connected cascaded H-bridge multilevel converters," *IEEE Industrial Electronics Society Annual Conference*, 2-6 Nov. 2003, pp. 1185–1190.
 [15] S. Sirisukprasert, J.-S. Lai, T.-H. Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," *IEEE Trans. Ind. Electronics*, vol. 49, no. 4, Aug. 2002, pp. 875-881.
 [16] P. C. Loh, D. G. Holmes, T. A. Lipo, "Implementation and control of distributed PWM cascaded multilevel inverters with minimum harmonic distortion and common-mode voltages," *IEEE Trans. on Power Electronics*, vol. 20, no. 1, Jan. 2005, pp. 90-99.
 [17] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, Z. Du, "Control of a multilevel converter using resultant theory," *IEEE Transactions on Control System Theory*, vol. 11, no. 3, May 2003, pp. 345-354.
 [18] Z. Du, L. M. Tolbert, J. N. Chiasson, "Modulation extension control for multilevel converters using triplen harmonic injection with low switching frequency," *IEEE Applied Power Electronics Conference*, March 6-10, 2005, Austin, Texas, pp. 419-423.
 [19] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: Part I –harmonic elimination," *IEEE Trans. Industry Applications*, vol. 9, May/June 1973, pp. 310-317.
 [20] H. S. Patel and R. G. Hoft, "Generalized harmonic elimination and voltage control in thyristor inverters: Part II –voltage control technique," *IEEE Trans. Ind. Applications*, vol. 10, Sept./Oct. 1974, pp. 666-673.
 [21] P. N. Enjeti, P. D. Ziogas, J. F. Lindsay, "Programmed PWM techniques to eliminate harmonics: A critical evaluation" *IEEE Transactions on Industry Applications*, vol. 26, no. 2, March/April 1990, pp. 302 – 316.
 [22] T. Kato, "Sequential homotopy-based computation of multiple solutions for selected harmonic elimination in PWM inverters," *IEEE Trans. Circuits and Systems I*, vol. 46, no. 5, May 1999, pp. 586-593.
 [23] Z. Du, L. M., Tolbert, J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, Mar. 2006, pp. 459-469.