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Influence of Bulk Doping and Halos on the TID Response of I/O and Core 150 nm nMOSFETs

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Abstract: The total ionizing dose sensitivity of planar 150 nm CMOS technology is evaluated by measuring the DC responses of nMOSFETs at several irradiation steps up to 125 krad(SiO_2). Different TID sensitivities are measured for transistors built with different channel dimensions and operating voltages (I/O and core). The experimental results evidence strong relations between TID sensitivity and the doping profiles in the channel. I/O transistors have the highest TID sensitivity due to their thicker gate oxide and lower bulk doping compared with core devices. In general, narrow-channel devices have the worst degradation with negative threshold voltage shifts, transconductance variations and increased subthreshold leakage currents, suggesting charge trapping in shallow trench isolation (STI). The enhanced TID tolerance of short-channel core devices is most likely related to the increased channel doping induced by the overlapping of halo implantations. Finally, transistors fabricated for low-leakage applications exhibit near insensitivity to TID due to higher bulk doping used during the fabrication to minimize the drain-to-source leakage current.

Keywords: total ionizing dose; TID; radiation effects; 150 nm technology; MOSFET; core transistors; I/O transistors; threshold voltage shift; leakage current

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1. Introduction

In space applications, integrated circuits (ICs) must overcome environmental hazards and at the same time keep their electric performance within the operational specification requirements [1]. Even if commercial devices are available in nodes lower than 5 nm, space systems require mixed signal electronics working with more consolidated technologies, such as the 150 nm CMOS node studied in this work [2]. Indeed, most modern CMOS technologies do not allow interfacing electronics with the standard of 3.3 V, which is still used in space applications. Furthermore, with the current semiconductor supply crisis, fabrication processes that are less stringent but more easily accessible are of interest when the performance requirements are not too high.

Ionizing radiation can affect the reliability of ICs by causing parametric shifts in transistor characteristics [3–5]. Trapped charges in the gate oxide of MOSFETs induce threshold voltage shifts, transconductance degradation and drive current variations [5]. In the last years, the shrinking of the gate oxide thickness of MOSFET technologies and new layouts with enhanced gate control, such as the FinFET and Gate-All-Around FET, have improved TID sensitivity [6–10]. Indeed, the buildup of a positive trapped charge scales with the dielectric thickness [3–5] also as a result of the increased probability of charge neutralization through the tunneling of electrons injected from adjacent semiconductor materials [11–13]. However, the downscaling of devices has brought new degradation mechanisms related to thick isolation oxides [5,14].

Several recent works about the TID effects of devices designed in the 180 nm MOSFET [15,16], 65 nm MOSFET [16], 28 nm MOSFET [7], 16 nm FinFETs [17,18] and other

channel materials [19–21] show strong radiation-induced degradation related to charge buildup in Shallow Trench Isolation (STI) oxide and its interface. The worst degradation is found in narrow-channel transistors [15,16], an effect known as the Radiation-Induced Narrow-Channel Effect (RINCE) [16]. RINCE induces large parametric drifts in narrow MOSFETs [15–18], with leakage current increases due to the activation of parasitic transistors in n-channel MOSFETs [22–25]. Another TID-related issue becoming important for modern transistors is the degradation of spacer oxides and of the overlying silicon nitride layers above Lightly Doped Drain (LDD) extensions [26–28]. Furthermore, recent studies [18,29] have demonstrated that the TID responses of 90 nm, 28 nm and 16 nm CMOS technologies have started to be influenced by halo implantations, which can deeply change the channel doping [29–33]. In [29], experimental measurements and TCAD simulations revealed the important role of halo implantations, which can enhance TID tolerance due to the increase in the overall bulk doping in short-channel devices [29]. Following works on 16 nm FinFETs showed similar improvements in the TID tolerance of short-channel devices, underlining the important role of halo implantations for the TID response of the devices [18,29].

In this work, irradiated nMOSFETs designed in 150 nm Si planar MOS technology are characterized by DC static measurements, evidencing TID sensitivities depending on transistor type and channel dimension with trends that differ from previous studies on 130 nm and 150 nm technologies. I/O transistors exhibit worse TID-induced degradation compared to core devices, and devices designed with short channels have enhanced TID tolerance. The experimental results evidence the important role of channel doping in the TID sensitivity of devices, which may be different between devices of the same technological node due to changes in the doping profiles of halo implantations and of bulk wells. The results provide guidelines for IC designers to facilitate circuit qualification, as these geometry dependencies can be used as a mitigation strategy, especially in analog parts, where the area requirements are typically relaxed.

2. Devices and Experiments

2.1. Test Structures

The devices under testing were fabricated in the Mixed-Signal 150 nm CMOS Process (LF15A) from LFoundry, Italy. This work focuses on n-channel MOSFETs, which are provided on Si wafers in a customized array structure, containing several types and several geometries of transistors with no ESD protections.

As shown in Table 1, four types of transistors were tested: I/O 5V, I/O 3.3V, core HS 1.8V (High Speed) and core LL 1.8V (Low Leakage). Gate oxide was fabricated in SiO_2 with an oxide thickness of <3 nm for 1.8 V devices. Compared with the 1.8 V transistors, the gate oxide thickness of 3.3 I/O devices was ~2.5×, and that of 5V I/O devices was ~6×. Moreover, the HS and LL devices had different doping profiles, which resulted in a lower threshold voltages for the HS type, as is discussed in Section 3.1.

Table 1. Device types and dimensions [1].

MOSFET Type	#1 Narrow/Short W/L [μm]	#2 Narrow/Long W/L [μm]	#3 Large/Long W/L [μm]
I/O 5V nMOSFET	0.8/0.8	0.8/10	10/10
I/O 3.3V nMOSFET	0.8/0.35	0.8/10	10/10
Core HS 1.8V nMOSFET	0.32/0.15	0.32/10	10/10
Core LL 1.8V nMOSFET	0.32/0.15	0.32/10	10/10

[1] Types and dimensions of MOSFETs under testing divided in three groups: narrow and short, narrow and long, and large and long.

Each array structure contained 12 different combinations of channel widths (0.32 μm < W < 10 μm) and channel lengths (0.15 μm < L < 10 μm). In this work, we

focused the analysis on nMOSFETs with three significant channel dimensions (see Table 1): narrow and short, narrow and long, and large and long. Transistors of the same type shared gate, source and bulk terminals, whereas separated drain terminals were dedicated to each transistor. Transistors were measured on wafers through a manual probe station.

2.2. Exposure Conditions and Measurement Details

The devices under testing were irradiated up to 125 krad(SiO_2) through irradiation steps of 25 krad(SiO_2) at room temperature (RT) at the University of Padova, Italy, using an X-ray irradiator composed of a tungsten tube with a peak energy deposition of 10 keV [34]. The dose rate was set to 36 krad(SiO_2)/hour within the ESCC 22900 standard rate [35], for a total exposure time of about 4 h. The X-ray spectra emitted from the tube was filtered with 150 µm Al foil in order to remove the low-energy spectra component (<8 keV). The devices under testing were biased and measured with the help of a wafer prober inside the irradiation cabinet. After exposure, annealing tests were performed, but, due to the constraints of wafer-level measurements, the annealing time was shortened with respect to the ESCC 22900 standard durations used with packaged devices [35]. The devices were first annealed at room temperature for 24 h and were then annealed for another 24 h at 100 °C by using a thermal chuck. According to previous studies [3–5,36–39], worst-case DC bias conditions were applied during irradiation and post-exposure annealing with the "ON" bias configuration ($V_{gs} = V_{dd}$ and $V_{ds} = 0$ V). At least two different devices of each type were evaluated for all experimental conditions with typical results, as shown below. The DC responses of the transistors were evaluated by measuring the main DC parameters with a semiconductor parameter analyzer (HP 4156) before exposure at several irradiation steps and after the annealing tests.

3. Experimental Results and Discussion

3.1. Bulk Doping

The I/O and core 150 nm nMOSFET structures are represented schematically in Figure 1. I/O devices are produced with a typical fabrication process for planar CMOS technologies with SiO_2 gate oxide and STI oxides. Core transistors are designed with an additional anti-punchthrough implantation and source/drain halos. The anti-punchthrough implantation is a highly doped region, which is implanted a few nanometers under the gate oxide along the entire channel length. In n-channel MOSFETs, the halos are highly p-doped bulk regions localized close to the source and the drain extensions [39–42]. Both the anti-punchthrough implantation and halos are introduced into the core transistors to overcome Short-Channel Effects (SCEs), such as threshold voltage roll-off and high leakage currents.

As a result, in core devices, bulk doping along the channel is not uniform due to halo implantations, and the average doping concentration depends on the channel length. In short-channel transistors, the drain halo implantation can overlap with the source one [40,42], causing an increase in the doping in the center of the channel, which increases the threshold voltage of the short transistors [33,40,42]. The rise in the threshold voltage with decreasing channel length is called the Reverse Short-Channel Effect (RSCE) [33,42] and is typical of scaled CMOS technologies with high halo doping concentrations.

Figure 2a shows the threshold voltage V_{th} of pristine nMOSFETs. V_{th} is plotted as a function of the channel length for transistors with a channel width of 0.3 µm (continuous) and 10 µm (dotted). The V_{th} of I/O devices is insensitive to the channel length, as the bulk doping is uniform with the channel length (no halos). On the contrary, the trend of V_{th}-L of core devices is strongly characterized by the RSCE, indicating highly doped halo implantations, which increase overall channel doping.

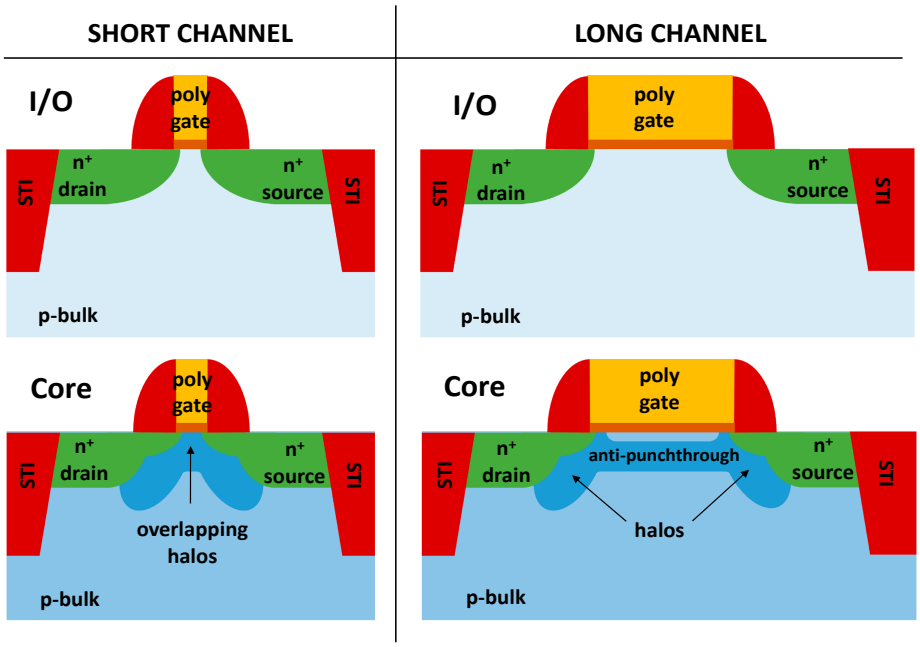

Figure 1. Schematic representation of I/O and core nMOSFETs designed in short and long-channel dimensions. I/O transistors are fabricated with the typical fabrication process of planar CMOS devices. Core transistors are fabricated by using LDD extensions, an anti-punchthrough implantation and source/drain halos. By decreasing the channel length, the drain halo overlaps with the source one, increasing the overall channel doping.

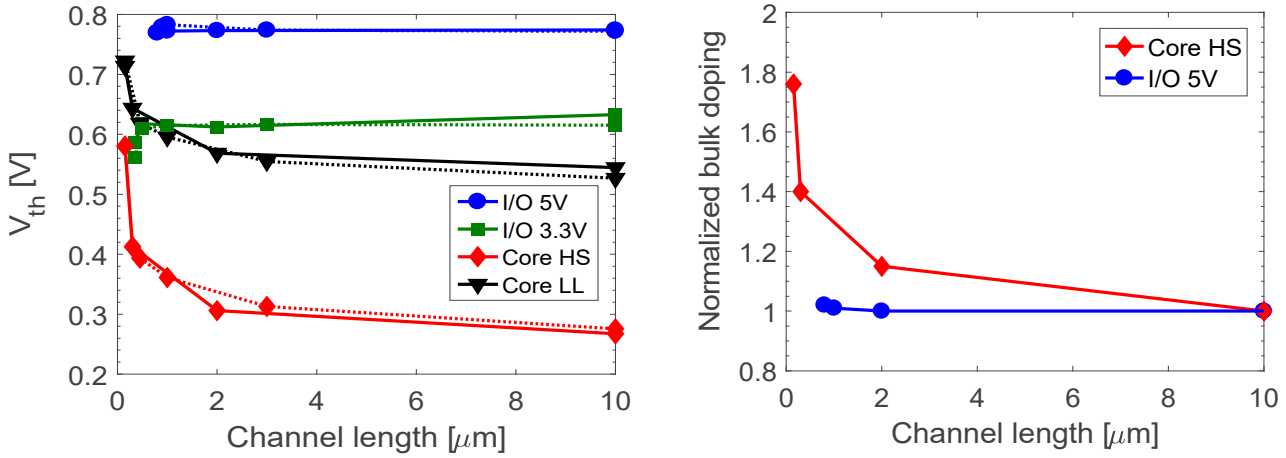

Figure 2. (**a**) Threshold voltage V_{th} as a function of the channel length for fresh nMOSFETs. Continuous lines refer to narrow transistors with W = 0.8 µm for I/O devices and W = 0.3 µm for core ones. Dotted lines refer to large transistors with W = 10 µm for I/O and core devices. Measurements carried out at room temperature in linear region (V_{ds} = 0.1 V). (**b**) Normalized bulk doping at the center of the channel as a function of the channel length of core HS and I/O 5V nMOSFETs. The bulk doping value is normalized by the bulk doping of the longest device (W = 10 µm).

Figure 2b highlights the channel length dependence of the bulk doping, which is retrieved at the center of the channel and 2 nm under the gate oxide. The value of the bulk doping of each transistor is normalized by the bulk doping of the longest channel transistor (L = 10 mm) of the same type. In core devices, the bulk doping increases by about 1.8× in the shortest channel length due to the overlap of halo implantations, which is consistent

with the increase in the V_{th} shown in Figure 2. On the contrary, different I/O transistors have similar V_{th} regardless of the channel length.

Finally, the doping channel profiles of core LL devices are higher than the bulk doping of core HS devices. Indeed, LL transistors require increased bulk/halo doping to improve the leakage current at the expense of speed, which, on the contrary, are essential parameters in HS devices. The increased bulk/halo of LL devices is evident by comparing the values of subthreshold leakage current and the threshold voltage of LL and HS devices having the same channel dimension. Considering the LL and HS transistors with W/L = 10/10 µm, the subthreshold leakage current of the LL device is in the order of 10^{-14} A vs. 10^{-11} of the core HS device, and V_{th} is 0.55 V for the LL device vs. 0.25 V for the core HS device. Therefore, the transistors are characterized by different channel doping, depending on the transistor type and on the channel length.

3.2. TID Effects on I/O and Core nMOSFETs

Figure 3 reports the I_d-V_{gs} in logarithmic and in linear scales for I/O and core nMOSFETs with narrow and long channel dimensions, as shown in Table 1. Transistors are measured in the linear region (V_{ds} = 0.1 V) at several irradiation steps up to 125 krad(SiO_2). The TID responses of I/O devices (a and b) degrade more than the core transistors (c and d). The increased subthreshold leakage current suggests charge trapping in the STI oxides, and the negative shift of the threshold voltage suggests positive charge generation in the gate oxide. At 125 krad(SiO_2), the transistor responses of I/O devices are dominated by a high leakage current, which degrades the I_{on}/I_{off} ratio from ~10^8 to ~10. The $I_{on\text{-}lin}$ current, defined as the drain-to-source current at V_{gs} = V_{dd} and V_{ds} = 0.1 V, increases by 28% in the 5V I/O devices and by 12% in the 3.3 V I/O ones. After exposure, transistors are annealed for 24 h at room temperature and for 24 h at 100 °C. Room temperature annealing causes negligible effects, whereas high-temperature annealing induces large recovery of I_{off} and an almost complete recovery of V_{th}, indicating the partial neutralization of the radiation-induced charge trapped in the gate oxide and STI.

Core devices are the most tolerant, with a negligible increase in the subthreshold leakage current, from 3 × 10^{-11} A pre-rad to 10^{-10} A after 125 krad(SiO_2) in HS core devices. Low leakage core devices are almost insensitive to TID with a variation in the $I_{on\text{-}lin}$ current of smaller than 2% after 125 krad(SiO_2). On the other hand, the TID response of HS core devices shows an evident increase in the transconductance with a cumulated dose and a negligible shift in the threshold voltage of less than 40 mV after 125 krad(SiO_2). The insensitivity of V_{th} suggests negligible effects related to charge trapping in the gate oxide. A slight recovery is visible after the annealing test at room temperature.

Figure 4 compares the TID sensitivity of the four different types of MOSFETs: I/O 5V, I/O 3.3V, core HS 1.8V and core LL 1.8V. The variation in the main DC parameters—$I_{on\text{-}lin}$, V_{th}, g_m and I_{off}—are plotted as a function of the dose in narrow and long-channel transistors (W/L = 0.8/10 mm for I/O devices and W/L = 0.32/10 mm for core devices). The worst-case response is found in I/O 5V transistors, and the core LL transistors exhibit the best TID tolerance. The I/O 5V transistor shows a ΔV_{th} shift of −0.6 V vs. −0.1 V for I/O 3.3V and <−0.05 V for core transistors. Room temperature annealing causes only marginal parametric shifts, whereas high-temperature annealing induces a large recovery of V_{th} for I/O 5V and I/O 3.3V.

Figure 4d shows the degradation of the subthreshold leakage current (I_{off}), which is defined as the drain current at V_{gs} = 0 V and V_{ds} = 0.1 V. When transistors are exposed to ionizing radiation, I/O transistors exhibit the largest increase in the I_{off} with the worst-case in the 5V nMOSFETs with I_{off} increasing from 8 × 10^{-15} A to 3.2 × 10^{-7} A. The leakage current of the I/O n-channel transistors exposed to TID flows from the drain to the source. This suggests TID-induced effects related to charge trapping in the STI, which may activate the parasitic channel close to the STI sidewalls [22–25]. On the contrary, LL and HS core nMOSFETs show modest increases in the leakage current with an increment of less than one order of magnitude after 125 krad(SiO_2). After the irradiation, the room temperature

annealing has very minor effects on the leakage current, with I_{off} values of 2.6×10^{-7} A vs. 3.2×10^{-7} A before annealing. The following 100°C annealing for 24 h induces visible I_{off} recoveries of about two orders of magnitude in 5V I/O transistors. However, the recovery of I_{off} is partial if compared to the almost complete recovery of I_{on}, shown in Figure 4a, suggesting effects related to charge trapping in different locations of the STI, as is discussed in Section 4.

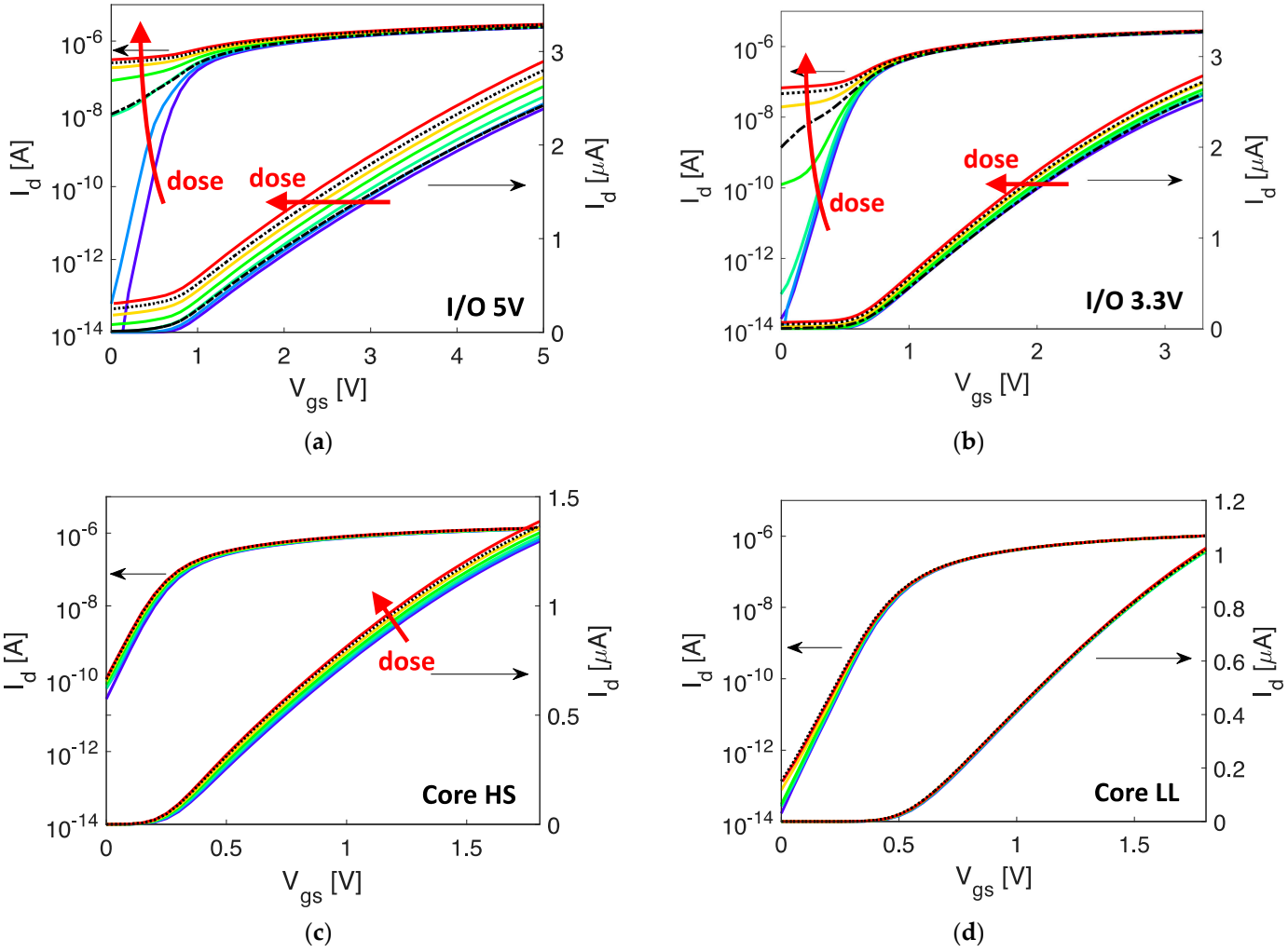

Figure 3. I_d-V_{gs} in the linear regime (V_{ds} = 0.1 V) at room temperature of nMOSFETs of different types with long and narrow channels (W/L = 0.8/10 µm for I/O devices and W/L = 0.32/10 µm for core devices). Transistors irradiated up to 125 krad(SiO_2), annealed at room temperature for 24 h, and finally annealed at 100 °C for 24 h (only I/O devices). (**a**) I/O 5V, (**b**) I/O 3.3V, (**c**) core HS and (**d**) core LL.

It is worth noting that the degradation mechanism in I/O devices and core devices is different. In I/O devices, the variation in the I_{on} current is caused first by a huge shift in V_{th} and secondly by the degradation of g_m. On the other hand, the relatively small I_{on} variation in HS core devices is mostly related to a decrease in g_m, as V_{th} is almost insensitive to TID effects. After 125 krad(SiO_2), ΔI_{on} is 10%, and Δg_m is 10%.

In conclusion, by comparing the TID response of I/O 5V, I/O 3.3V, core HS and core LL, the main visible effects are as follows:

- I/O transistors degrade more than core devices, mainly due to a large negative V_{th} shift and an increase in the subthreshold leakage current I_{off}.
- The TID degradation of core devices is modest and related to variations in g_m.

- Low-leakage (LL) core devices show a higher TID tolerance than that of high-speed (HS) core devices.

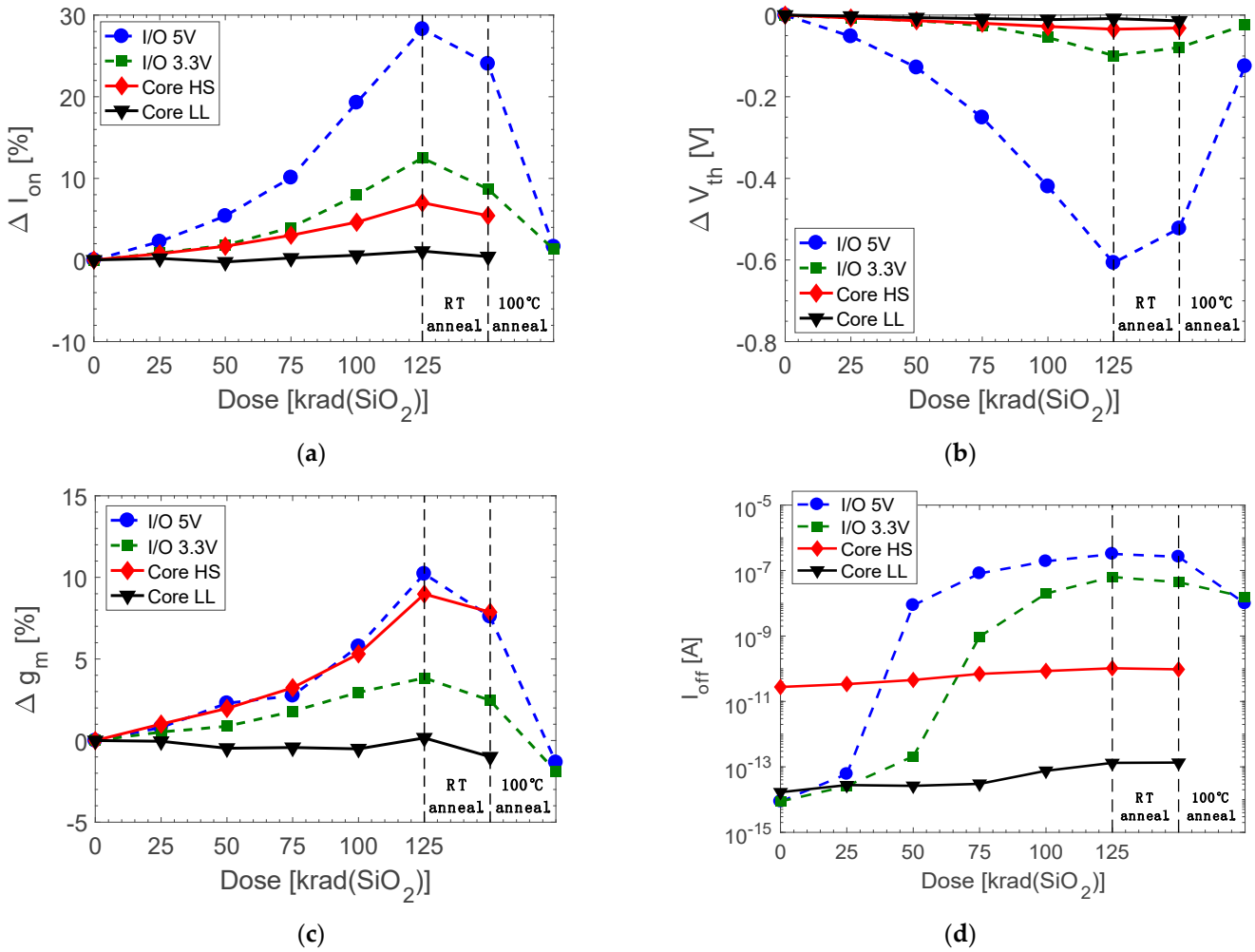

Figure 4. Variations in (**a**) maximum current ΔI_{on}, (**b**) threshold voltage ΔV_{th}, (**c**) transconductance Δg_m and (**d**) leakage current I_{off} as a function of dose for the four transistor types: I/O 5V, I/O 3.3V, core HS and core LL. The channel geometries are the narrowest and shortest: W/L = 0.8 µm/10 µm for I/O devices, and W/L = 0.35 µm/10 µm for core devices. The plots show the main DC parametric shifts at room temperature in nMOSFETs in the linear region (V_{ds} = 0.1 V). All transistors are irradiated up to 125 krad(SiO_2) and are then annealed for 24 h at RT and 100 °C.

3.3. Channel-Width-Dependent Effects

Figure 5 compares the V_{th} shift of several transistors with different channel widths and the same channel length (L = 10 µm). In both I/O and core devices, the worst-case response is found in narrow channel transistors, evidencing a clear channel-width-dependent effect. After 125 krad(SiO_2), the V_{th} shift of the narrow I/O 5V nMOSFET (blue curve) is −600 mV, whereas the largest nMOSFET (black curve) is −35 mV. The negative variation in V_{th} in the transistor is induced by the large increase in the leakage current visible in Figure 4 and partially by the charge trapping in the gate oxide. The negligible variation in g_m in the largest device, Δg_m < 2% after 125 krad(SiO_2), indicates that the charge trapping related to the gate oxide mainly occurs in the bulk of the oxide and not at the SiO_2/Si interface. The core HS transistors exhibit a V_{th} shift of −35 mV and <−1 mV for the narrowest and largest devices, respectively, showing a channel-width-dependent effect. However, the high tolerance of the largest device suggests modest charge trapping in the gate oxide and along its SiO_2/Si interface [3–5].

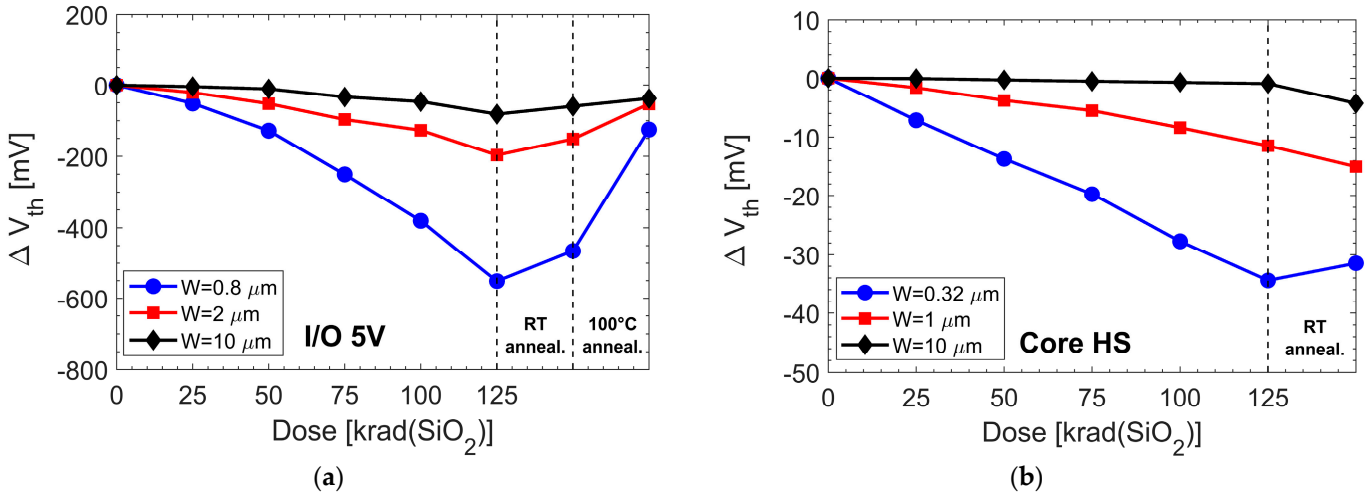

Figure 5. ΔV_{th} is plotted as a function of the dose for devices with different channel widths, and the channel length is constant at 10 µm. Transistors irradiated up to 125 krad(SiO_2), annealed at room temperature for 24 h and then annealed at 100 °C for 24 h (only I/O devices). All measurements are carried out at room temperature in linear regime (V_{ds} = 0.1 V). (**a**) I/O 5V devices and (**b**) core HS devices.

The channel width dependence of V_{th}, combined with the large increase in the I_{off} current, indicates that the TID-induced effects are mainly dominated by positive charge buildup in the STI oxides [15,16]. Indeed, when the channel is depleted at $V_{gs} < V_{th}$, the positive charge in the STI inverts the lateral regions of the channel close to the STI sidewalls, causing an increase in the leakage current [7,15,16]. When the channel is inverted at $V_{gs} > V_{th}$, the positive charges in the STI improve the conductivity of the lateral regions, incrementing the effective channel width and thus g_m and V_{th} (RINCE) [16,17]. Room temperature induces a slight recovery of the parametric shift due to recombination of trapped charges in the STI oxides. The largest recovery is visible during high-temperature annealing with the recovery of g_m and V_{th} in all transistors. The largest transistors exhibit slight positive ΔV_{th}, indicating the generation of interface traps at the SiO_2/Si channel interface along the gate oxide.

3.4. Channel-Length-Dependent Effects

Figure 6 shows the dc parametric shifts of several core HS nMOSFETs with different channel lengths. All devices have the same channel width of 0.32 µm, i.e., the narrowest width. The ΔI_{on} curves evidence a general increase in the I_{on} current, with the highest shift for transistors having the longest channel L = 10 µm (green line) of about 7% of ΔI_{on} after 125 krad(SiO_2). The shortest devices L = 0.15 µm (blue line) have the best TID tolerance, with ΔI_{on} < 0.5% after 125 krad(SiO_2). Δg_m increases as a function of the cumulated dose with similar trends to the ΔI_{on} curves, thus indicating that the I_{on} increase is induced by the enhancement of g_m vs. the dose. This is in agreement with the relatively small decrease in V_{th}, with the worst case in the longest device, having a ΔV_{th} of −33 mV after 125 krad(SiO_2).

On the other hand, Figure 7 shows parametric shifts in the I_{on}, g_m and V_{th} of the 3.3 V I/O nMOSFETs designed with different channel lengths and an identical channel width of 0.8 µm. The ΔI_{on} characteristics are relatively insensitive to the channel length, as all I/O transistors exhibit a ΔI_{on} enhancement of about 15% after 125 krad(SiO_2). In I/O transistors, the I_{on} degradation is induced by both negative V_{th} shifts and by the enhancement of g_m, as shown in Figure 7b,c. The enhancement of /**g_m indicates positive charge trapping in the STI.

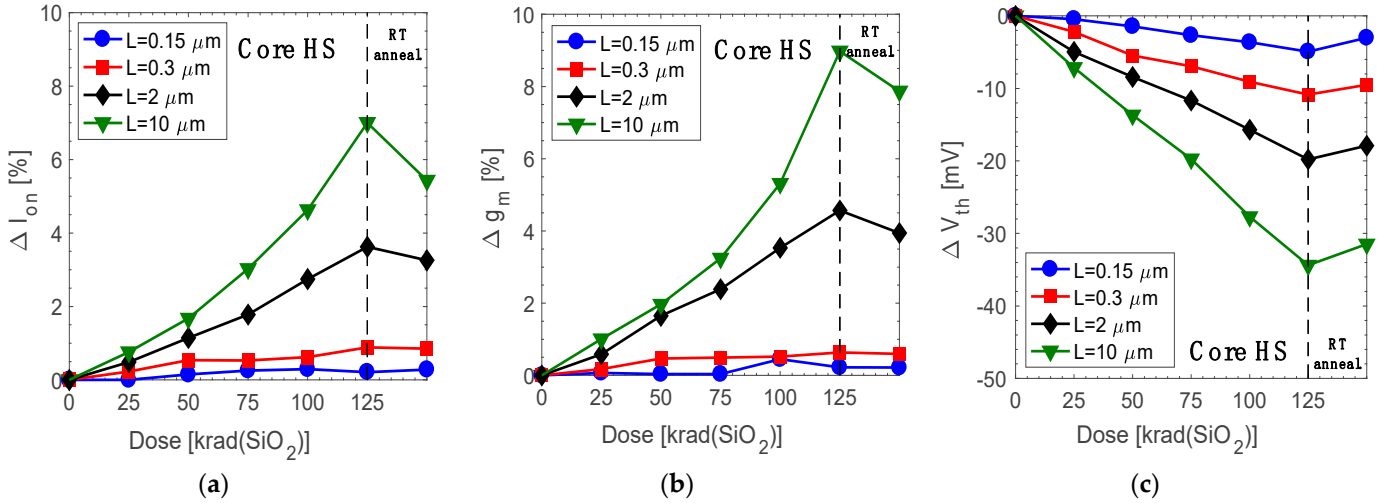

Figure 6. (**a**) Maximum current ΔI_{on}, (**b**) threshold voltage ΔV_{th} and (**c**) transconductance Δg_m as a function of dose for core HS nMOSFETs of different channel lengths. The channel width is the narrowest available (W = 0.32 mm). Transistors measured at room temperature in linear regime (V_{ds} = 0.1 V) during the irradiation up to 125 krad(SiO_2) and after annealing at room temperature for 24 h.

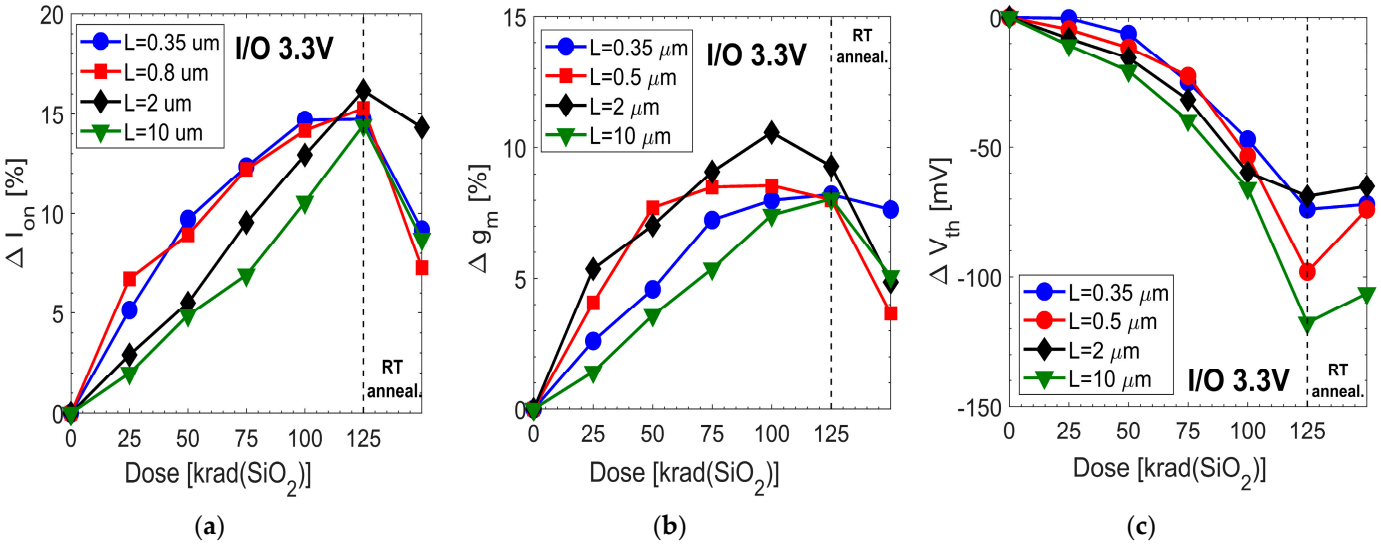

Figure 7. (**a**) Maximum current ΔI_{on}, (**b**) threshold voltage ΔV_{th} and (**c**) transconductance Δg_m as a function of dose for I/O 3.3V nMOSFETs of different channel lengths. The channel width is the narrowest available (W = 0.8 mm). Transistors measured at room temperature in linear regime (V_{ds} = 0.1 V) during the irradiation up to 125 krad(SiO_2) and after annealing at room temperature for 24 h.

Interestingly, the HS nMOSFETs with the shortest channel exhibit the highest TID tolerance, showing the lowest variations in g_m and V_{th}. This channel length dependence is related to the halo implantations, which is similar to the studies on 28 nm MOSFETs technologies [21]. In narrow and short-channel devices, halo implantations increase the overall bulk doping, thus requiring a larger amount of trapped charge in the STI to alter the carrier distribution in the channel [20,21] and consequently mitigating the radiation-induced effects in short-channel transistors. The higher channel doping in shorter transistors is in agreement with Figure 2a, where the V_{th} of fresh HS transistors is strongly dependent on the channel length, evidencing the highest V_{th} for the shortest channel transistor. On the contrary, halos are not implanted during the fabrication of I/O devices, in agreement with

the slightly reverse channel length dependance of V_{th} (see the blue and green curves of Figure 2a). The absence of the halo prevents the formation of channel-length-dependent TID effects. It is worth noting that the channel-length-dependent effect is related to the charge trapping in the STI, and it is visible only in irradiated narrow-channel devices (small W), whereas large devices (large W) are insensitive to it.

This channel length effect is strongly evident in HS core devices, whereas it is modest in LL core devices. Figure 8 reports the ΔI_{on} of core HS and LL devices as a function of the channel length when the devices are irradiated at 125 krad(SiO_2). The LL devices (black curve) are characterized by very modest ΔI_{on} degradation of <2%. This enhanced TID tolerance of LL devices is most likely associated with the high bulk doping used during fabrication for minimizing the leakage currents of LL devices. The higher channel doping attenuates the TID-induced effects related to the STI, thus completely deleting the dependence of the TID effects to the channel length.

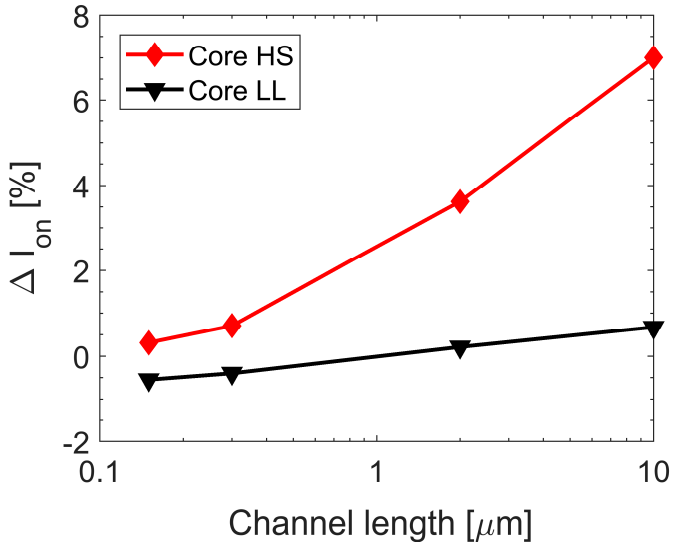

Figure 8. Evidence of the channel length dependence of the TID effects in core transistors. The changes in the drain current are plotted at 125 krad(SiO_2) as a function of channel length (L) in nMOSFETs with the same narrow channel W = 0.32 μm.

4. Interpretation of Experimental Results

The experimental results on 150 nm MOSFET highlight the high sensitivity of the TID response to channel width, channel length and type of transistors. In general, the experimental results show that the widest channel transistor evidences modest V_{th} shifts and modest subthreshold slope variations (see Figure 5). These results suggest a very small generation of interface traps along the channel interface and a very limited amount of charge buildup in the gate oxide, confirming the robustness of the SiO_2/Si interface and not highlighting dominant TID mechanisms related to the gate oxide.

The TID effects of 150 nm MOSFETs are dominated by charge buildup in STI, degrading narrow transistors (RINCE) [16], which is consistent with previous works on 180 nm, 130 nm and 65 nm technology nodes, where the narrow channel exhibits a large increase in g_m shifts and increased I_{off} currents [6–8,16–19]. During the high-temperature annealing, the almost complete recovery of the V_{th} of narrow transistors indicates the neutralization of positive trapped charges in the STI and/or the generation of interface negative traps close to the SiO_2/Si. Neutralization is likely limited to the upper region of the STI oxide close to the gate corner, as the I_{off} current does not completely recover like V_{th}, similar to the TID-induced degradation visible in the 28 nm and 16 nm technologies [7,8,18]. This is consistent with a model where the electrical field is applied to the nMOSFET gate during high-temperature annealing (V_{gs} = V_{dd} in nMOSFETs), and holes and the H^+ of the upper corner of the STI drift toward the SiO_2/Si interface [16,18,43]. At the SiO_2/Si interface of

the corner of the STI, holes can recombine with tunneling electrons, and H^+ can depassivate Si-H bonds, generating new interface traps, which are negatively charged [16,18,43].

Another interesting result is the channel length dependence of the TID degradation of nMOSFETs. Short-channel nMOSFETs show lower TID sensitivity than that of long-channel transistors. This effect can be related to halo implantations, which increase the average bulk doping in the channel region. Transistors with larger doping concentrations are less affected by radiation, because larger amounts of charge are required to alter the carrier distribution. The influence of halo implantations is not visible in core LL nMOSFETs, likely characterized by large halo doping to decrease the leakage current.

5. Conclusions

The TID sensitivities of 150 nm MOSFETs of different dimensions and types strongly depend on the bulk doping profile in the channel region. In I/O transistors, large negative shifts in the threshold voltage and high leakage currents indicate radiation-induced charge buildup in the gate oxide and STI. The TID degradation of I/O transistors is insensitive to the channel dimension and scales with the thickness of the gate.

On the other hand, core transistors are more TID-tolerant than I/O transistors, as a result of the scaled thickness of the gate dielectric and high bulk doping, caused by the use of anti-punchthrough implantations and halos. Core LL devices, which use highly doped bulk/halos, are the most tolerant. One of the most interesting results is an evident channel length dependence in the TID response of core transistors, where short-channel devices exhibit higher TID tolerance than that of long-channel ones. This channel-length-dependent effect is related to halo implantations, which can overlap in the shortest channel devices, increasing the overall channel doping of the core devices. The higher bulk doping of short-channel devices has also been confirmed by the doping profiles released by the manufacturer and is in agreement with the RISCE of V_{th} in pristine devices, confirming the high influence of bulk doping on the TID sensitivity of CMOS technology.

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