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2007

Liu, Y., Chen, T. P., Ding, L., Yang, M., Wong, J. I., Ng, C. Y., et al. (2007). Influence of charge trapping on electroluminescence from Si-nanocrystal light emitting structure. Journal of applied physics, 101, 1-4.

https://hdl.handle.net/10356/91942

https://doi.org/10.1063/1.2713946

JOURNAL OF APPLIED PHYSICS **101**, 104306 (2007)

Influence of charge trapping on electroluminescence from Si-nanocrystal light emitting structure

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(Received 30 October 2006; accepted 26 January 2007; published online 18 May 2007)

We report a study on the influence of charge trapping on electroluminescence (EL) from Si nanocrystal (nc-Si) distributed throughout a 30 nm SiO_2 thin film synthesized by Si^+ implantation into an oxide film thermally grown on a *p*-type Si substrate. The electron and hole trapping in the nc-Si located near the indium tin oxide gate and the Si substrate, respectively, cause a reduction in the EL intensity. The reduced EL intensity can be recovered after the trapped charges are released. A partial recovery can be easily achieved by the application of a positive gate voltage or thermal annealing at hot temperatures (e.g., 120 °C) for a short duration. The present study highlights the impact of charging in the nc-Si on the light emission efficiency and its stability of nc-Si light-emitting devices. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2713946]

I. INTRODUCTION

Since silicon is the core material for microelectronic devices, there is intensive interest in the integration of silicon optical/optoelectronic devices for the emission, modulation, and detection on one chip based on the mainstream Si technology. One of the main bottlenecks in working toward a photonic integration compatible with the Si technology is the lack of an efficient Si-based light source. In recent years, Si-nanocrystal structures provide the possibility of Si-based light emitting devices.[1–9] One of the promising methods to synthesize the Si nanocrystals (nc-Si) embedded in SiO_2 dielectric films for the light emitting structures is Si ion implantation into SiO_2 thin films. Electroluminescence (EL) at room temperature from such structures has been observed by different researchers,[10–12] which represents a very important step towards the development of Si-based optoelectronics. However, there are still many problems and difficulties such as the low efficiency and efficiency degradation of the EL. In this work we will show that the efficiency degradation is due to the charge trapping in the Si nanocrystals. We have observed that the EL intensity can be modulated by the charging/discharging in the nc-Si, i.e., the EL intensity is reduced by the charge trapping in the nc-Si while it is recovered by the release of the trapped charges from the nc-Si.

II. EXPERIMENTAL

SiO_2 films with the thickness of 30 nm were thermally grown on (100) oriented, *p*-type Si substrates at 950 °C. Si^+ ions were implanted into the oxide films at 8 keV with a dose of 2×10^{15} cm^{-2}. After the ion implantation, thermal annealing was carried out at 1000 °C for 100 min to induce the formation of nc-Si. Light-emitting structures were fabricated using a 130 nm indium tin oxide (ITO) layer and a 500 nm Al layer to form the top and bottom electrodes, respectively. For the capacitance-voltage (*C-V*) measurement, the structure with aluminum top electrode instead of the ITO electrode was also prepared. The area of the top electrodes varies from 7.9×10^3 to 4.5×10^6 μm^2. The as-deposited ITO layer has a sheet resistance of 25 Ω/sq, a surface rms <1.0 nm, and an average transmittance of above 85% over the visible wavelengths of 400–800 nm. The stopping and range of ions in matter (SRIM) simulation shows that the implanted Si ions distribute throughout the entire 30 nm oxide with the peak concentration of excess Si atoms located at around 15 nm underneath the oxide surface, as illustrated in Fig. 1(a). Figure 1(b) shows the transmission electron microscopy (TEM) image of nc-Si with the sizes of ~3–4 nm embedded in the SiO_2 matrix. Photoluminescence (PL) measurement was performed at an excitation wavelength of 325 nm, but no PL was observed in the as-fabricated sample. The *C-V* measurement was performed with a HP 4284A *LCR* meter, while the current measurement was carried out with a Keithley 4200 semiconductor characterization system.

III. RESULT AND DISCUSSION

Figure 2(a) shows the experimental setup of the EL measurement. Under a negative bias applied to the ITO gate and with the substrate grounded, electrons and holes are injected from the ITO gate and the Si substrate, respectively, and radiative recombination of the injected electrons and holes leads to light emission. At the same time, some of the injected charges are trapped in the nc-Si as shown in Fig. 2(a), affecting the carrier injections and thus the EL. The EL from

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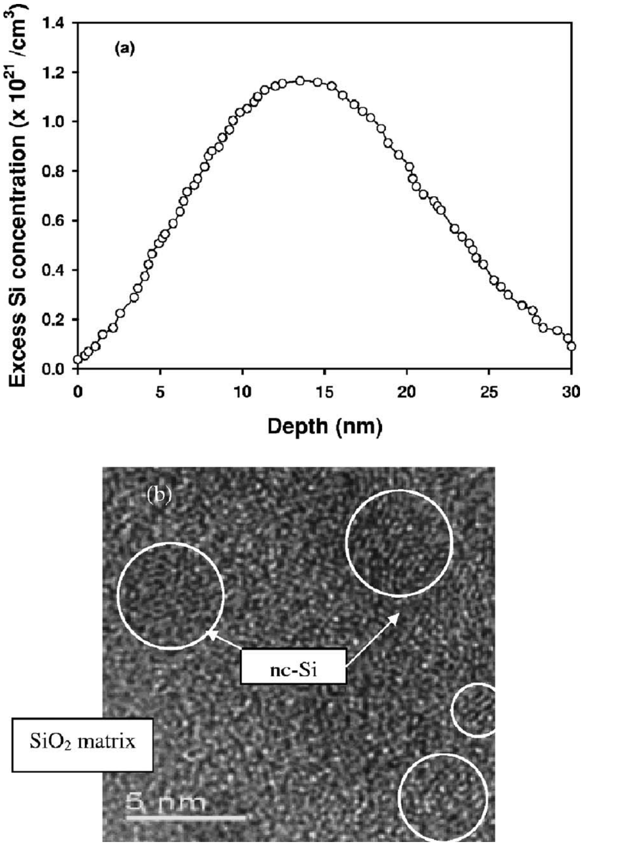

FIG. 1. (a) Depth distribution of the excess Si concentration in the 30 nm SiO_2 layer obtained from SRIM simulation, and (b) TEM image of the nc-Si embedded in SiO_2 matrix. The implantation energy is 8 keV.

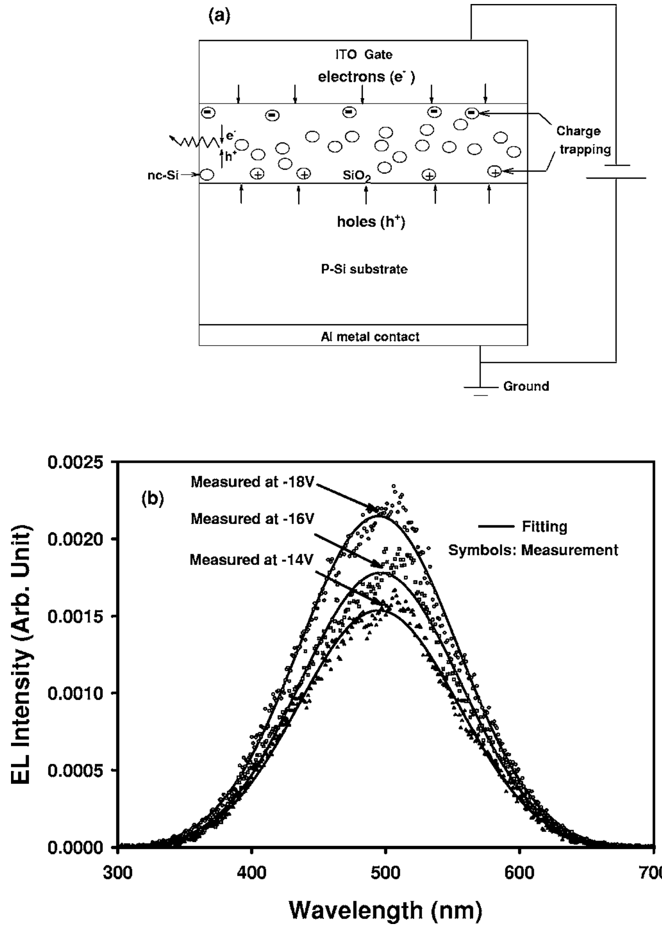

FIG. 2. (a) Experimental setup for the EL measurement and illustration of charging in the nc-Si, and (b) EL spectra under various measurement voltages.

the light-emitting structure can be observed with naked eyes in a dark environment. Figure 2(b) shows EL spectra measured under the voltages of −14, −16, and −18 V, respectively. The EL exhibits a broad spectrum peaked at ~500 nm (~2.5 eV). The EL intensity increases with the injection current. No photoluminescence (PL) from the same Si^+ implanted SiO_2 film was observed, which could be due to the fact that the nanocrystals were still not fully stabilized to exhibit PL after the annealing at the slightly lower temperature (i.e., 1000 °C). Indeed, it was reported that the annealing at 1100 °C shows the PL related to the formation of Si nanocrystal.[13] On the other hand, as the energy (~2.5 eV) of the EL peak is significantly larger than the band gap (~1.8–2.1 eV) of the nc-Si with a size of ~3–4 nm,[14] it seems that the EL cannot be simply attributed to the quantum confinement effect. It is believed that the defects in the Si^+-implanted SiO_2 film, which serve as the luminescent centers,[10,15–17] play an important role in the light emission.

As EL intensity is determined by the numbers of the injected electrons and holes available for the radiative recombination, charge trapping in the nc-Si,[18] which affects the carrier injection, should have an impact on the light emission. This has been confirmed in our experiment. As can be observed in Fig. 3(a), the application of −25 V for 1 s leads to a drastic reduction in the light emission intensity as compared to the virgin case, which is attributed to the charge trapping in nc-Si. The large negative flatband voltage shift ($\Delta V_{FB}=-1.7$ V) after the application of −25 V for 1 s in the *C-V* characteristic shown in Fig. 3(b) indicates a large amount of hole trapping in the nc-Si located near the interface of SiO_2/Si substrate. The equivalent areal density (ΔQ) of trapped holes corresponding to the negative flatband voltage shift can be estimated with

$$\Delta Q = -\Delta V_{FB} C_{ox}, \tag{1}$$

where C_{ox} ($=\varepsilon_0\, \varepsilon_{SiO_2}/d$, where ε_0 is permittivity in vacuum, ε_{SiO_2} is the dielectric constant of SiO_2, and the oxide thickness $d=30$ nm) is the oxide capacitance per unit area. For the application of −25 V for 1 s, ΔQ is 1.2×10^{12} holes/cm^2. The hole trapping is due to the hole injection from the substrate under the negative gate bias. The injected holes can be trapped in any nc-Si distributed in the oxide, but most of the hole trapping should occur in the interface region as the injected holes can be easily trapped in the nc-Si located near the injection interface. The hole trapping will lead to a reduction in the electric field for the hole injection from the substrate. Similarly, some of the injected electrons from the ITO gate may also be trapped in the nc-Si with most of the electron trapping occurring near the gate, and thus the electric field for the electron injection from the ITO gate is also reduced. Note that the electron trapping near the gate cannot be readily revealed from the *C-V* measurement because the trapped electrons are far away from the SiO_2/Si substrate

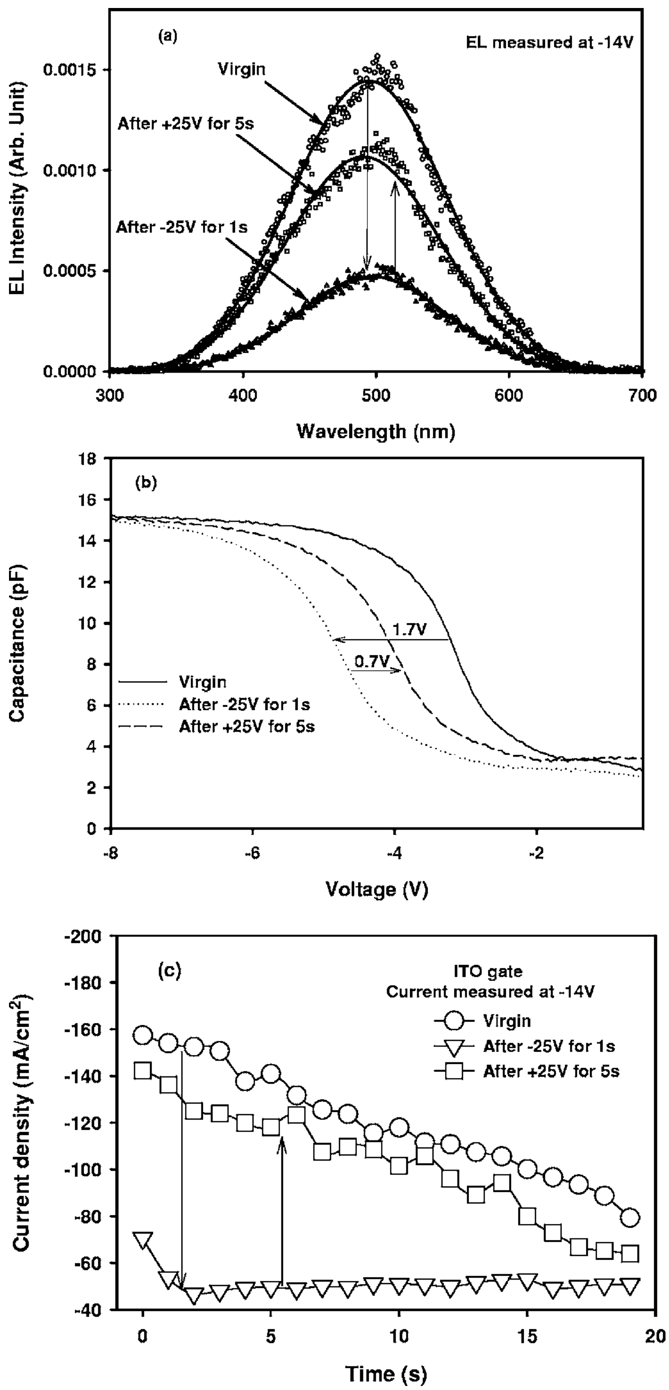

FIG. 3. Influence of trapping and detrapping of charges in nc-Si due to the application of −25 V for 1 s and +25 V for 5 s, respectively, on the EL (a), the *C*-*V* characteristic (b), and the injection current (c). Both the EL and the time-domain current measurements were carried out at −14 V.

interface. With reductions in the electric fields for both hole and electron injections, the injection current decreases. Indeed, as shown in Fig. 3(c), the current at the voltage of −14 V (note that the EL measurements shown in Fig. 3(a) were carried out at −14 V) for the virgin case is much larger than that after the application of −25 V for 1 s. With the reduction of the injection current, the number of injected holes and electrons for the radiative recombination decreases, and thus the EL intensity decreases. It should be pointed out that the charge trapping occurs not only at the higher voltage of −25 V but also at the relatively low voltage of −14 V. As shown in Fig. 3(c), the current measured at −14 V for both the virgin case and after the application of −25 V for 1 s decreases with the biasing time, indicating the accumulation of charges trapped in the nc-Si. This means that the EL intensity would degrade during the EL operation.

On the other hand, as can be seen in Fig. 3(a), the reduced EL intensity is partially recovered by the application of +25 V for 5 s. The recovery is due to the release of some of the charges trapped in the nc-Si under the influence of the positive gate voltage. As shown in Fig. 3(b), the application of +25 V for 5 s leads to a partial recovery in the flatband voltage shift, i.e., the ΔV_{FB} is partially recovered from −1.7 V for the case of application of −25 V for 1 s to −1 V now. The reduction in the flatband voltage shift indicates that some of the trapped holes have been released by the application of the positive voltage (41% of the trapped holes have been released). Under a positive gate voltage, some of the trapped holes can tunnel out from the nc-Si or recombine with the electrons injected from the substrate. After the release of some of the trapped holes, for an EL or current measurement at a negative gate voltage, the electric field at the SiO_2/Si substrate interface increases, and thus the hole injection from the substrate increases. On the other hand, some of the trapped electrons near the gate can also be released under the influence of a positive gate voltage, and then the electron injection from the gate also increases in the EL or current measurement. Therefore, with the release of some of the trapped holes and electrons, a partial recovery in the current is achieved as shown in Fig. 3(c). This explains the above-mentioned partial recovery in the EL intensity. The trapped charges can also be released by a hot temperature annealing for a short period. Figure 4 shows the effect of the annealing at 120 °C for 40 s. As can be seen in this figure, the annealing leads to a partial recovery in the EL intensity, the flatband voltage shift, and the injection current, and the situation is very similar to that of the application of the positive bias discussed above. The relatively low temperature and short duration of the hot-temperature annealing indicates that some of the trapped charges are easily released when they gain the thermal energy. This could suggest that only those nc-Si located near the Si substrate and the ITO gate are involved in the process as the charges trapped in them can easily tunnel out to the gate or escape to the substrate at an elevated temperature.

Also it should be pointed out that with the accumulation of trapped charges (i.e., the trapped electrons near the gate and the trapped holes near the substrate) under a negative bias, the injection current would degrade with time. Indeed, as can be seen in Fig. 3(c), the injection current at −14 V decreases with time. The decay of injection current is also observed on the structures with Al gate, as shown in Fig. 5. This indicates that the current degradation is not related to the ITO gate, and it further supports the argument that the charge trapping in the nc-Si leads to decrease in the injection current.[18] The current decay means degradation in the EL intensity as a result of the accumulation of trapped charges in the nc-Si. As discussed above, the trapped charges could be released under a positive gate bias. This suggests that bipolar pulses (i.e., the pulses change between negative and positive

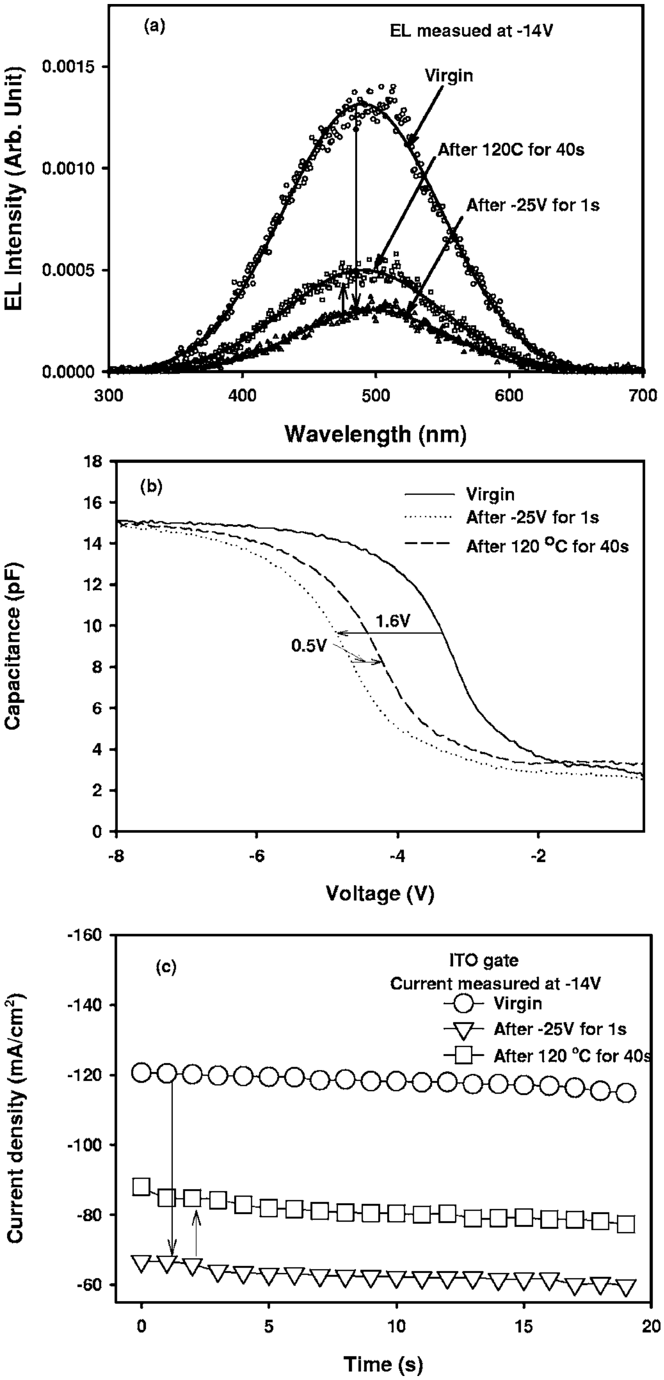

FIG. 4. Influence of trapping and detrapping of charges in nc-Si due to the application of −25 V for 1 s and the annealing at 120 °C for 40 s, respectively, on the EL (a), the *C-V* characteristic (b), and the injection current (c). Both the EL and the time-domain current measurements were carried out at −14 V.

voltages alternately) could eliminate the charging effect and thus maintain the EL efficiency as reported in Ref. 19.

IV. CONCLUSION

In conclusion, the influence of charge trapping on the EL emission from ITO/Si^+ implanted SiO_2 layer/Si structure has been studied. It is shown that the charge trapping in the nc-Si near the gate and the substrate can cause a large reduction in the EL intensity due to the decrease of the electric fields for both the electron injection from the gate and the hole injection from the substrate. However, the reduced EL intensity can be recovered after the trapped charges are released. A partial recovery can be easily achieved by the application of a positive gate voltage or thermal annealing at hot temperatures (e.g., 120 °C) for a short duration. The results suggest that bipolar pulses (i.e., the pulses change between negative and positive voltages alternately) could eliminate the charging effect and thus maintain the EL efficiency.

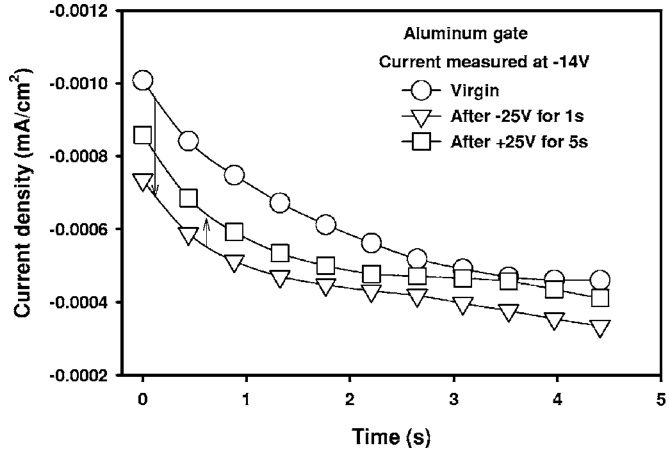

FIG. 5. Degradation of the injection current measured at −14 V for the structure with Al gate.

ACKNOWLEDGMENT

This work has been financially supported by the Academic Research Fund of the Ministry of Education, Singapore, under Project No. ARC 1/04 and by the Singapore Millennium Fund.

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