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Influence of contact effect on the performance of microcrystalline silicon thin-film transistors

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Microcrystalline silicon thin-film transistors were prepared by plasma-enhanced chemical vapor deposition at substrate temperatures below 200 °C. The transistors exhibit electron mobilities of 38 $cm^2/V\,s$, threshold voltages in the range of 2 V, and subthreshold slopes of 0.3 V/decade. Despite the realization of transistors with high carrier mobility, contact effects limit the performance of the transistors. The influence of the drain and source contacts on device parameters including the mobility, the threshold voltage, and the subthreshold slope will be discussed in detail. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2390634]

With the advance of flat-panel display technologies thin-film transistors (TFTs) based on amorphous silicon (*a*-Si:H) have established themselves as an inexpensive and reliable technology for display back panels. The electron mobility of *a*-Si:H TFTs allows for operation of liquid crystal flat-panel displays at video rate. However, the performance of *a*-Si:H TFTs does not enable the operation of organic light-emitting diode (OLED) displays or radio-frequency identification tags. In order to provide stable operation of large-area OLED displays at video rate, the carrier mobility has to be in the range of 5 $cm^2/V\,s$ or higher.[1] Furthermore, the threshold voltage of the TFTs has to be stable during device operation. As the threshold voltage of *a*-Si:H TFTs is not stable due to the creation of electronic defects during operation,[2] *a*-Si:H TFTs are not suitable for such applications. So far only polycrystalline silicon (poly-Si) TFTs provide sufficiently high carrier mobilities and stable threshold voltages.

An alternative material that exhibits high carrier mobilities is hydrogenated microcrystalline silicon (μc-Si:H). The material mainly consists of amorphous and crystalline phase. μc-Si:H TFTs combine two worlds of low temperatures processing with the performance of poly-Si TFTs. So far device mobilities of $>40\ cm^2/V\,s$ were reported by Cheng and Wagner,[3] Lee *et al.*,[4] and Saboundji *et al.*[5] Despite the realization of transistors with high carrier mobility, the electronic transport in such TFTs is not fully understood. In particular, the influence of the drain and source contacts on the device performance is still under investigation. In the following, μc-Si:H TFTs with channel lengths ranging from 2 to 200 μm were characterized and analyzed. The short channel TFTs with channel length below 10 μm enable a detailed discussion of the influence of contacts on the device properties.

A schematic cross section of the realized TFT is shown in Fig. 1. Top-gate staggered TFT structures were used in this study to take full advantage of the high crystalline volume fraction of bulk μc-Si:H.[6] The drain and source contacts of the TFTs were realized by chromium with 30 nm thickness. Afterwards, a highly doped *n*-type μc-Si:H film is deposited by plasma-enhanced chemical vapor deposition (PECVD) to form Ohmic contacts between the drain and source electrodes and the channel material. An intrinsic (i) μc-Si:H layer with 100 nm thickness, which acts as channel, and gate dielectric of 300 nm, were prepared by PECVD. The dielectric was realized by silicon dioxide (SiO_2). SiO_2 was used as a gate dielectric to minimize the defect density at the channel/dielectric interface.[7,8]

The microcrystalline *n* and *i* layers were prepared at radio frequencies of 13.56 MHz and substrate temperatures of 190 and 160 °C, respectively. The microcrystalline material was grown in the high pressure and high power regime, which facilitates the deposition at high deposition rates.[9,10] The deposition pressure of the *i* layer was 1330 Pa and the power density was 0.3 W/cm^2. For these parameters a deposition rate of 0.3 nm/s was achieved. The *i* layer exhibits a dark conductivity in the order of 10^{-6} S/cm and a crystalline volume fraction of 55%. The SiO_2 was prepared at 150 °C. To clean and hydrogenate the *i*-layer surface the samples were subjected to a hydrofluoric acid dip prior to the deposition of SiO_2. Finally, the gate electrode is formed by an aluminum film. The devices were fabricated on Corning 1737 glass. Transistors with channel length and width rang-

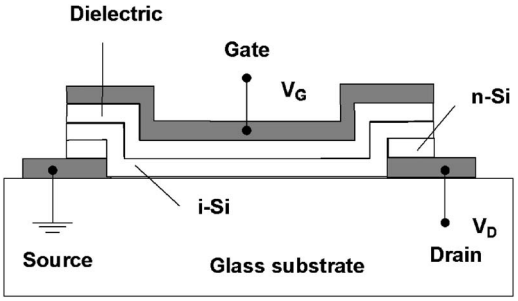

FIG. 1. Schematic cross section of a top-gate staggered μc-Si:H TFT. The transistor was fabricated by using a two-mask photolithographic process.

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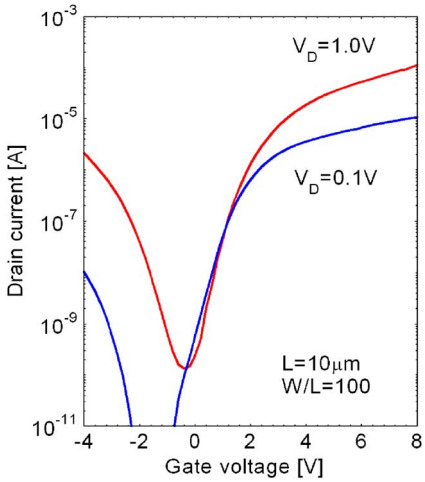

FIG. 2. (Color online) Transfer characteristics of a μc-Si:H TFT (annealed at 150 °C for 30 min) with W=1000 μm and L=10 μm. The transfer curves were measured for V_D=0.1 and 1 V.

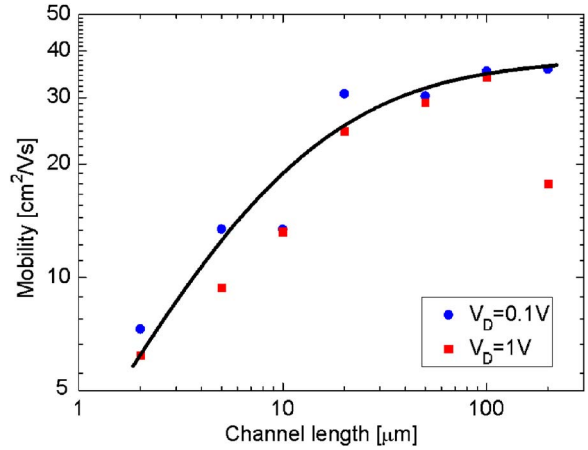

FIG. 3. (Color online) Measured device mobility as a function of channel length for annealed μc-Si:H TFTs.

ing from 2 to 200 μm and from 200 to 1000 μm were fabricated, respectively. To allow for the fast evaluation of the materials and the device properties, a simple two-mask photolithography process was developed.

In order to improve the device behavior all transistors were annealed at an elevated temperature of 150 °C for 30 min under ambient conditions. The annealing temperature was selected to be close to the deposition temperature of *i* layer to avoid the degradation of the device and the effusion of hydrogen out of the film.[11] A detailed discussion of the influence of thermal annealing on the device characteristics is given elsewhere.[12]

The device characterization was performed at room temperature under dark conditions. In this letter, typical device data of TFTs after several measurements are presented, since the initial measurement significantly deviates from their stable device performance.

The device mobility μ of the transistors was extracted using following equation for the drain current I_D in linear region from the measured transfer characteristics:

$$I_D = \mu C_G \frac{W}{L}\left(V_G - V_T - \frac{V_D}{2}\right)V_D, \tag{1}$$

where W and L is the channel width and length of the TFT, respectively, C_G is the gate capacitance per unit area, V_G, V_T, and V_D are the gate voltage, threshold voltage, and drain voltage, respectively. A device mobility of 13 cm^2/V s was extracted from the transfer characteristics in Fig. 2. The on/off ratio of the TFT for low drain voltages is larger than 10^6. The gate leakage current of the transistor is four orders of magnitude lower than the corresponding drain current at high gate voltages (not shown).

Measurements of devices with different device geometries were performed. The extracted device mobility as a function of the channel length is shown in Fig. 3. The obtained values strongly depend on the channel length. For long channel devices (L=200 μm) a device mobility of 35 cm^2/V s is extracted, whereas for short channel devices (L=2 μm) the determined value is reduced to 7 cm^2/V s for V_D=0.1 V. Similar data were published by other group for the channel length dependence of the device mobility of μc-Si:H TFTs.[4]

The reduction of the device mobility for short channel transistors can be explained by the influence of the drain and source contacts on the potential distribution across the channel. The nonideal contact behavior causes a voltage drop at the drain and source contacts, which leads to a reduction in the channel potential. In the following it is assumed that the contacts can be described by Ohmic contacts, so that the drain voltage in Eq. (1) can be replaced by $V_D - I_D R_C$, where $V_D - I_D R_C = V_{D0}$ represents the voltage drop across the channel. R_C is the resistance of the drain and source contacts. The influence of the contacts on the device behavior is more pronounced for short channel devices, since the drain current is proportional to V_{D0}/L.

Considering the nonideal contact behavior, the following expression for the mobility can be derived:

$$\mu \approx \mu_0 \frac{L}{L + \mu_0 W C_G R_C (V_G - V_T)}, \tag{2}$$

where μ_0 is the electron mobility of the microcrystalline channel material and μ is the device mobility extracted from the measured transistors, which is affected by the influence of the drain and source contacts. Equation (2) was employed to fit the experimental data in Fig. 3. We extracted a μ_0 of 38 cm^2/V s and a R_C of 5.6 kΩ. A good agreement between the experimental data and the fit was achieved, nearly independent from V_D (0.1 V $< V_D <$ 1 V). Furthermore the transmission line model[13] was used to extract the contact resistance of the transistors. Both methods exhibit very similar values for the contact resistance.

The device threshold voltage V_T extracted from Eq. (1) as a function of the channel length is shown in Fig. 4(a). The data were extracted from the transfer curves measured at V_D=0.1 and 1 V. The device threshold voltage apparently increases for longer channel transistors. The channel length dependent device threshold voltage can again be explained by the influence of the drain and source contacts on the threshold voltage. Taking the influence of the contact effects into account the following expression for the device threshold voltage which is the extrapolation of the drain current to I_D=0 can be derived from Eq. (1) by substituting $V_D - I_D R_C$ for V_D:

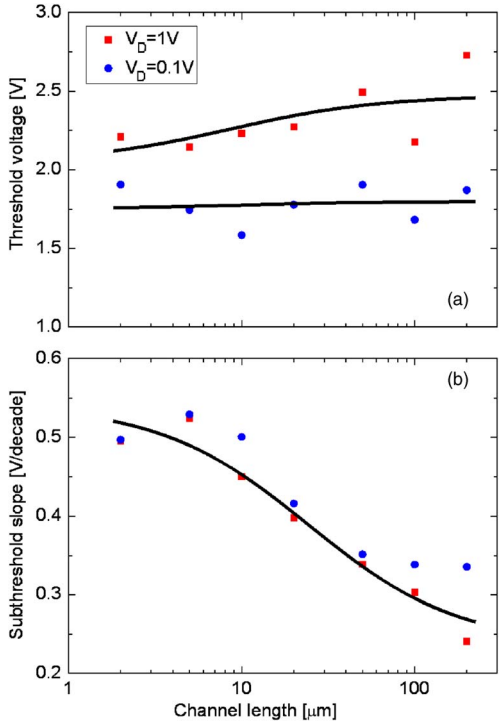

FIG. 4. (Color online) Measured device threshold voltage (a) and subthreshold slope (b) for annealed μc-Si:H TFTs as a function of channel length.

$$V_T = V_{T0} - \frac{I_D R_C}{2}, \tag{3}$$

where V_{T0} is the threshold voltage of the μc-Si:H TFT, which is not affected by the influence of the contacts. The V_T is close to V_{T0} for long channel transistors. For short channel devices the contact effects are more pronounced, which leads to a reduction of the V_T. Equation (3) was used to fit the extracted device threshold voltages in Fig. 4(a). A good agreement between the experimental data and fit was achieved, which underlines that the channel length dependence of the device threshold voltage can also be explained by the drain and source contact effects. From the fit of the device threshold voltage, we extracted a V_{T0} value of 2.5 V. The extracted R_C is identical with the value extracted from the fit of the channel length dependence of the device mobility.

The device threshold voltage of the transistors is closely related to the subthreshold slope. The device subthreshold slope S as a function of the channel length is shown in Fig. 4(b) for V_D=0.1 and 1 V. As expected the subthreshold slope is nearly independent of the drain voltage. Investigating the channel length dependence, a decrease of the device subthreshold slope with increasing channel length is observed. The device subthreshold slope is determined by

$$S = \frac{\partial V_G}{\partial(\log(I_{D\text{sub}}))}, \tag{4}$$

where $I_{D\text{sub}}$ is the drain current in the subthreshold region, which is described by following relationship:[14]

$$I_{D\text{sub}} \propto \frac{W}{L}\mu \exp\left(\frac{C_G V_G}{q N_T d_S k_B T}\right), \tag{5}$$

where q, N_T, d_S, k_B, and T is the electron charge, the defect density in the μc-Si:H, the μc-Si:H channel layer thickness, the Boltzmann constant, and the temperature, respectively. The determined defect density (3.5×10^{16} cm^{-3} is in the range of the values obtained from the electron spin resonance and detailed device analysis.[15] This underlines that Eq. (5) can be applied to describe the subthreshold current of the μc-Si:H TFTs. The device mobility was used in Eq. (5) to account for the contact effects on the subthreshold current. By substituting Eq. (2) into Eq. (5), the device subthreshold slope

$$S = S_0 \frac{L + W\mu_0 C_G R_C (V_G - V_T)}{L + W\mu_0 R_C [C_G (V_G - V_T) - q N_T d_s k_B T]}, \tag{6}$$

where S_0 is the subthreshold slope of the μc-Si:H TFT, which is not affected by the influence of the contacts, while S is influenced by the contacts. Equation (6) shows that the device subthreshold slope increases for short channel devices, which is consistent with the experimental data in Fig. 4(b).

The realized μc-Si:H TFTs exhibit electron mobilities of 38 cm^2/V s, threshold voltages in the range of 2 V, and subthreshold slopes of 0.3 V/decade. The experimental results reveal that the channel length has a distinct influence on extracted device parameters such as mobility, threshold voltage, and subthreshold slope. The device mobility decreases for short channel transistors. A detailed analysis reveals that the reduced device mobility can be attributed to the influence of the drain and source contacts. The device threshold voltage decreases and the subthreshold slope increases with decreasing channel length, which is attributed to the similar contact effects.

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