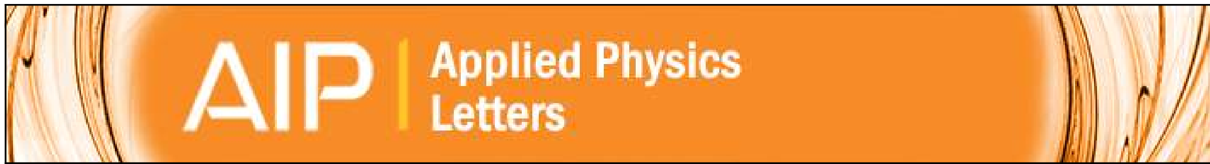

Influence of grain size at first monolayer on bias-stress effect in pentacene-based thin film transistors

Yiwei Zhang, Dexing Li, and Chao Jiang

Citation: Applied Physics Letters **103**, 213304 (2013); doi: 10.1063/1.4833251
View online: http://dx.doi.org/10.1063/1.4833251
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/103/21?ver=pdfcov
Published by the AIP Publishing

Re-register for Table of Content Alerts

Create a profile.

Sign up today!

This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 124.16.156.254 On: Fri, 29 Nov 2013 08:50:40

CrossMark

Influence of grain size at first monolayer on bias-stress effect in pentacene-based thin film transistors

Yiwei Zhang, Dexing Li, and Chao Jiang[a)]
CAS Key Laboratory of Standardization and Measurement for Nanotechnology, National Center for Nanoscience and Technology, No. 11 Beiyitiao Zhongguancun, Beijing 100190, China

(Received 7 October 2013; accepted 10 November 2013; published online 22 November 2013)

Threshold voltage shift under applied gate voltage is a key factor characterizing stability of organic thin-film transistors (OTFTs), while the physical mechanism is still controversial. In this study, we systematically examined the initial growth of pentacene polycrystalline films under different growth rates. Bias stress performance of the fabricated pentacene-based OTFTs was found to be highly related to the initial gain size of the pentacene films. Larger grain size at the first deposition layer led to smaller threshold voltage shift. The quantitative correlation can be described by a two-dimensional microscopic mobility model relating to the grains and grain boundaries. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4833251]

Organic thin film transistors (OTFTs) have attracted considerable attention because of the potential to be utilized as electronic switching elements in flexible, low-cost, and large area devices such as active-matrix display,[1,2] organic sensors,[3] nonvolatile memory devices.[4] Among various organic semiconductors, pentacene is an excellent candidate to study the physics mechanisms of OTFTs for its high mobility and relatively simple chemical structure.[5,6] During last decade, significant progress has been made and the charge-carrier mobilities have reached above $10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$.[7] However, the stability of OTFTs should also be considered for commercial application besides the high mobility.[8] Bias-stress effect is the phenomenon that threshold voltage (V_T) at which the transistor switches on shifts gradually to the gate bias voltage that is applied to the device, as has been one of the most attractive research fields of OTFTs.[9–11] Bias stress effect is attributed to trapping states in the dielectric layer, semiconductor layer, and/or semiconductor/dielectric interface.[12–14] However, the mechanism of bias-stress effect remains a concern since the microscopic understanding of charge trapping in organic materials remains elusive.

In the case of the polycrystalline thin film transistors, the grain boundaries play crucial role in the bias stress effect.[15,16] In pentacene-based OTFTs, the charge trapping was found to occur preferentially in intergrain regions of organic thin film by using scanning Kelvin probe microscope (SKPM).[17] The molecular packing morphology, which can be controlled by growth parameters, was also found to remarkably influence the performance of copper phthalocyanine (CuPc) OTFTs.[18] Simeone *et al*. studied the environmental stability of top contact pentacene OTFTs with different grain sizes of pentacene active layer with a thickness of 30 nm.[19] They concluded the morphology difference influences the hysteresis of transfer characteristics induced by water absorption. The grain boundaries served as channels for water diffusion.

Many previous studies have been done on the topic of influence of the grain size on bias stress effect in OTFTs. However, they usually related to grain sizes on the surface of the films instead of the ones at the first deposited molecular layer. Consequently, the obtained results are often obscured by the fact that the first monolayer of pentacene on dielectric, where the conducting channel locates, generally has morphology difference from that of the film with the thickness of several tens of nanometers.[20,21]

In our former reports, the mobility dependence on the pentacene film morphology was successfully related to a transport model involving two-dimensional single-layered grains and grain boundaries at the first monolayer in polycrystalline pentacene OTFTs.[21–23] It is noted that for OTFTs the channel forms in a very few layers close to the semiconductor/dielectric interface,[21–24] which means that the properties of grains and grain boundaries at the first monolayer indeed have great effect on the performance of organic films.

In this research, we utilized the mentioned phenomenological model based on two-dimensional grains and grain boundaries at the first monolayer to interpret the gate bias related stability. First, we studied the film growth mode of pentacene films deposited with different deposition rates and extracted the grain size at the first monolayer according to the two-dimensional grain boundary model. Then, we systematically characterized the threshold voltage shift in the pentacene-based OTFTs, and applied the model to clarify the influence of the grain size at the first monolayer on the gate bias effect.

Top contact thin film transistors were fabricated. Heavily P-doped n-type silicon wafers with thermally grown oxide layer of 300 nm serve as the substrates (gate electrode). Before pentacene deposition, a buffer layer of polystyrene (PS) with the thickness of 70 nm was spin-coated onto the substrate to modify the dielectric. Then 50 nm pentacene (Aldrich Co.) film was deposited through thermal evaporation (Auto-306 BOC-Edwards Co.) under a vacuum pressure of 5×10^{-5} Pa with deposition rates of $R = 0.798$, 1.55, 5.00, and 7.56 nm min^{-1}, respectively. The substrate temperature was kept at room temperature (25 °C) for all the experiments. Then 50 nm Au was deposited onto the pentacene film through a shadow mask to form the source and drain electrodes with a channel length $L = 50\,\mu$m and width

a)Author to whom correspondence should be addressed. Electronic mail: jiangch@nanoctr.cn

This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 124.16.156.254 On: Fri, 29 Nov 2013 08:50:40

W = 2000 μm. The gold films were evaporated with a same depositing rate of 12 nm/min. To investigate the grain sizes at the first layer of the pentacene film, 1 nm (nominal thickness) pentacene film (about 2/3 monolayer) was deposited also with the four different deposition rates mentioned above. In this research, except the pentacene depositing rates, all other experimental conditions kept even to ensure the comparability.

The morphology of the pentacene monolayer film was characterized by Nanoscope III atomic force microscope (AFM, Vecco Co.) using tapping mode. The bias stress effect measurements of OTFTs were carried out with a Keithley 4200 semiconductor analyzer in a homemade four probe testing system. The stress conditions were set the same for all the devices, keeping the drain voltage without bias to the source voltage and the difference between the applied gate-source voltage and the origin threshold voltage as a constant of −30 V. All the measurements were carried out in vacuum at room temperature (25 °C), so that the influence of water and oxygen molecules could be ignored.[19]

To investigate the initial growth process, the pentacene monolayer film with nominal thickness of 1 nm was characterized. As shown in Fig. 1(a), larger deposition rate results in smaller grain size at the first pentacene monolayer. Assuming that the further growth of extra pentacene molecules will heal the gaps among the existing grains before one complete monolayer forms,[20] the grain sizes at the first monolayer can be extracted from the initial nucleation densities shown in Fig. 1(a). The total length of grain boundaries per unit area (i.e., grain boundary density) can be obtained by the simple model of Voronoi polygons,[20,25] as shown in Fig. 1(b).

The nucleation density can be fitted through Eq. (1) which relates deposition rate as follows:[26]

$$N \propto R^p \exp\left(\frac{E_N}{k_B T_S}\right), \tag{1}$$

where N is the nucleation density, R is the deposition rate, p is a parameter related with the critical nucleus size which is a constant in our experiments, E_N is the characteristic energy related with the surface character of the substrate, k_B is Boltzmann constant, and T_S is the temperature of the substrate. In our experiments, all the properties of the substrate, including T_S, are kept invariable, which means only R is a variable in Eq. (1). The satisfying fitting result between the nucleation density and the deposition rate indicates that using different depositing rates to control the grain sizes at the first monolayer of pentacene films is effective, as shown in Fig. 1(c). But as a phenomenological model, it is still difficult to extract the grain boundary density through the nucleation density, so further simplification about the grain shape is necessary. It is noted that the grain boundary densities fitted with Voronoi polygon model are well equal to those with square grain model assuming all the grains are uniform squares, as evidenced in Fig. 1(d). Accordingly, it is then reasonable to assume the initial polycrystalline film layer can be divided into square grains with average lengths L_G, connected by grain boundaries with average length L_{GB} between them. We further suppose that within each single grain the pentacene molecular packing is ordered in high order, as leads to a low trap density there, while the grain boundaries are thought to be where much more traps are located than in grains.

Figure 2 illustrates the transfer characteristics of OTFTs with different pentacene depositing rates before and after the gate bias stress for 1200 s, 2400 s, 3600 s, and 4800 s, respectively. The source-drain currents gradually decrease with bias time, and the threshold voltages gradually negatively

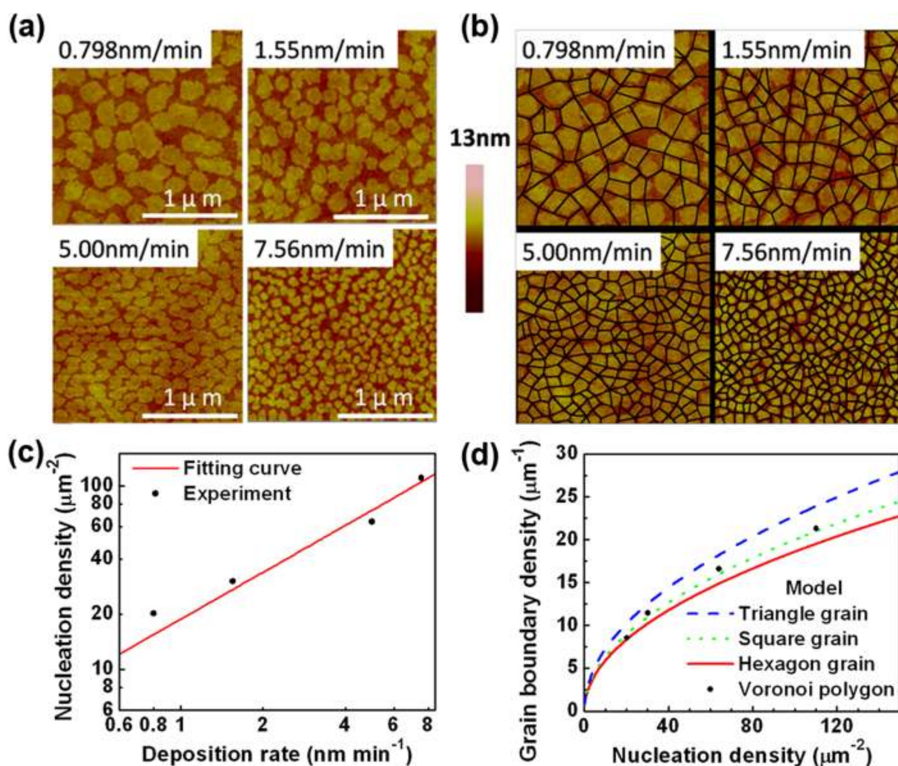

FIG. 1. (a) $2 \times 2\,\mu m^2$ AFM images of pentacene films with nominal 1 nm deposited with four different deposition rates. (b) Illustration of the grain boundaries at the first monolayer using Voronoi polygon model. (c) Experiment (dot) and fitted relationship (curve) between nucleation density and deposition rate of the pentacene monolayer. (d) Grain boundary density versus nucleation density for Voronoi polygon model with three curves deduced from uniform triangle, square, or hexagon grain assumptions.

This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 124.16.156.254 On: Fri, 29 Nov 2013 08:50:40

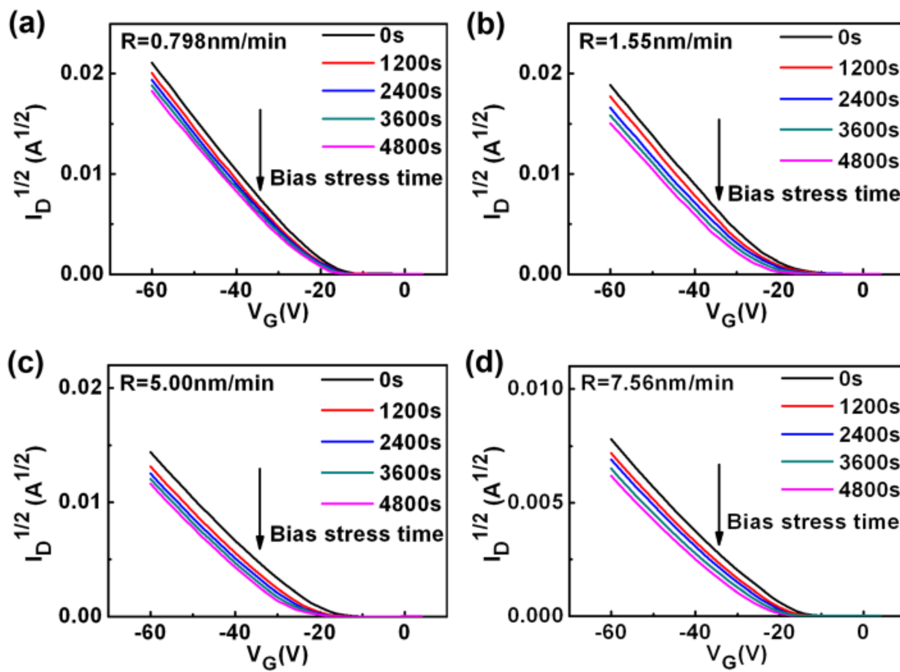

FIG. 2. Transfer characteristics of OTFTs with different pentacene deposition rates of (a) 0.798 nm/min, (b) 1.55 nm/min, (c) 5.00 nm/min, and (d) 7.56 nm/min for origin, and four bias stress times of 1200 s, 2400 s, 3600 s, and 4800 s, respectively.

shift for all series samples. The origin saturation mobilities for the increasing deposition rates are 1.58, 1.31, 0.80, and 0.40 $cm^2\ V^{-1}\ s^{-1}$, respectively. During gate bias stress measurement in the vacuum chamber, the mobility degradation is barely visible as evidenced in Fig. 2. The good field-effect mobility and the weak degradation indicate that the gradual negative shift of the threshold voltages during bias stress is the intrinsic property of the OTFTs.

To establish an analytic correlation between V_T shift and grain sizes at the first monolayer, we suppose the traps causing bias stress effect can be attributed into two parts: (1) *Traps in grain boundaries* at the first pentacene monolayer, where trapping density is higher because of the disordered molecular stacking. The V_T shift induced by this part is denoted as ΔV_{TGB}. (2) *Traps inside grains and in dielectric layers*. In grains, the molecules stack in so highly ordered way that all these grains can be treated as single crystals with a same trap density. And in dielectric layer, there is no difference between different experiment series. As a result, the V_T shift induced by this part is denoted as ΔV_{TGD}, which can be supposed the same for all the transistors under the same bias conditions.

The ΔV_{TGB} shift induced by traps in grain boundaries can be expressed as follows:

$$\Delta V_{TGB} = \frac{S_{GB} \times n}{C_i \times W \times L} = \frac{W \times L \times \dfrac{2L_{GB}}{(L_G + L_{GB})} \times n}{C_i \times W \times L} = \frac{2L_{GB} \times n}{(L_G + L_{GB}) \times C_i}, \tag{2}$$

where L and W are the channel length and width, respectively, S_{GB} is the total area of the two-dimensional grain boundaries located at the first monolayer of pentacene film, n is the trapped carrier concentration per unit area within the grain boundaries during bias stress, C_i is the capacitance of the dielectric layer per unit area, L_G and L_{GB} are the width of grains and grain boundaries, respectively. The value C_i applied in our experiments is 10.61 nF cm^{-2} which has a slight fluctuation between different samples, while it is quite small as can be ignored in the trap density assumption.

Then, we get the relationship between the total ΔV_T shift and the grain size at the first monolayer, which is expressed as

$$\Delta V_T = \Delta V_{TGD} + \frac{2L_{GB} \times n}{(L_G + L_{GB}) \times C_i}. \tag{3}$$

For our pentacene-based OTFTs, both the experimental and the fitted total ΔV_T shift through Eq. (3) versus grain

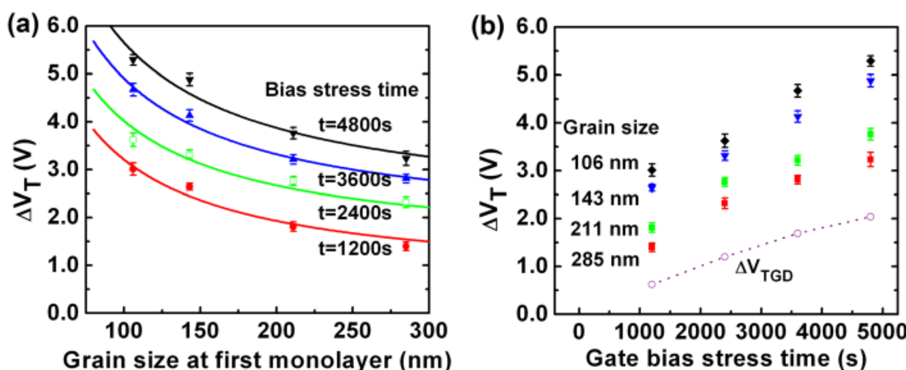

FIG. 3. Threshold voltage shift ΔV_T for the pentacene-based OTFTs with different grain sizes at the first monolayers under four bias stress times. (a) Experimental (symbol) and fitted relationship (line) between ΔV_T and grain size for bias stress times of 1200 s, 2400 s, 3600 s, and 4800 s, respectively. (b) ΔV_T and the fitting parameter of ΔV_{TGD} versus gate bias stress time using the same data with (a) for grain sizes of 106 nm, 143 nm, 211 nm, and 285 nm, respectively. The dot line is a guideline for the eye.

This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 124.16.156.254 On: Fri, 29 Nov 2013 08:50:40

size at the first monolayer are shown in Fig. 3. It is noted that the threshold voltage shift does decrease with larger grain size or smaller nucleation density. The fitting parameter of L_{GB} is 2.99 nm. Under different bias conditions, the fitting parameter of n is $2.78 \times 10^{12}\,cm^{-2}$ for bias stress time $t = 1200\,s$, $3.06 \times 10^{12}\,cm^{-2}$ for $t = 2400\,s$, $3.45 \times 10^{12}\,cm^{-2}$ for $t = 3600\,s$, and $3.88 \times 10^{12}\,cm^{-2}$ for $t = 4800\,s$, as are supported by the reported ones.[6,11] The ΔV_{TGD}, contribution other than grain boundary, are also depicted in Fig. 3(b). These fitting parameters are consisting with our former reported values obtained from mobility fitting by two-dimensional grain boundary model.[20,21]

It is noticeable, when the amount of grain boundaries at the first monolayer is large; the ΔV_{TGD} is a rather small proportion comparing the total ΔV_T shift, while for transistors with larger grain size at first monolayer, the contribution of ΔV_{TGD} becomes significant. In our investigated deposition rate range which covers the common deposition rate of pentacene films grown in S-K growth mode in literatures,[18] the traps in first layer grain boundaries do play a major role in the total ΔV_T shift behaviors. The presented model captures the main factors causing the threshold voltage shift under gate bias stress and produces a quantitative description of the phenomena.

Moreover, the changes of ΔV_T and ΔV_{TGD} with time show different characters. ΔV_{TGD} increases gradually with bias stress time in our time scale, while ΔV_T increases more quickly at the beginning stage (the first 1200 s), especially for transistors with more first layer grain boundaries, then increases gradually with a similar slope to that of ΔV_{TGD}. This means that the trapping states located in grain boundaries at the first monolayer are filled up with a much higher speed, while other trapping states in grains or dielectrics are occupied with a slower speed. We guess that the difference comes from the trapping barriers distribution, although further evidence is still essential to confirm this point.

It is difficult to indicate the microscopic process of the charge trapping, but we can confirm that grain boundaries at the first monolayer of pentacene film have great influence on the process. And the analytic expression based on the two-dimensional grain boundary model is effective to illustrate the relationship between the morphology of the first monolayer and the bias-stress induced threshold voltage shift. The fitting parameter of n, representing charge trapping caused by all the physical processes in grain boundaries could help deepen our understanding of the device physics of small molecular OTFTs.

To conclude, we carried out a series of experimental and theoretical work to investigate the threshold voltage shift under gate bias stress in pentacene-based OTFTs. Through the study of the film growth modes and the charge trapping process, we utilized a phenomenological model to quantitatively describe the correlation between the shift of threshold voltage and the change of grain sizes at the first monolayer in the polycrystalline OTFTs. The fitting parameters based on the model are reasonable and practically illustrate the microstructure of the pentacene first monolayer. This may strengthen our understanding on the charge trapping behavior in polycrystalline OTFTs and may be helpful to optimize the design of the OTFTs.

This work was supported by the National Basic Research Program of China (Grant No. 2011CB932800) and the National Natural Science Foundation of China (Grant Nos. 11074056, 11374070, and 11104042).

[1] H. Sirringhaus, Adv. Mater. **17**, 2411 (2005).
[2] R. A. Street, Adv. Mater. **21**, 2007 (2009).
[3] T. Someya, T. Sekitani, S. Iba, Y. Kato, H. Kawaguchi, and T. Sakurai, Proc. Natl. Acad. Sci. U.S.A. **101**, 9966 (2004).
[4] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, and T. Someya, Science **326**, 1516 (2009).
[5] G. Horowitz, Adv. Mater. **10**, 365 (1998).
[6] G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga, and M. Hajlaoui, Adv. Mater. **10**, 923 (1998).
[7] J. Zaumseil and H. Sirringhaus, Chem. Rev. **107**, 1296 (2007).
[8] H. Sirringhaus, Adv. Mater. **21**, 3859 (2009).
[9] K. Fukuda, T. Suzuki, T. Kobayashi, D. Kumaki, and S. Tokito, Phys. Status Solidi A **210**, 839 (2013).
[10] K. Suemori, S. Uemura, M. Yoshida, S. Hoshino, N. Takada, T. Kodzasa, and T. Kamata, Appl. Phys. Lett. **91**, 192112 (2007).
[11] D. Knipp, R. A. Street, A. Volkel, and J. Ho, J. Appl. Phys. **93**, 347 (2003).
[12] P. A. Bobbert, A. Sharma, S. G. J. Mathijssen, M. Kemerink, and D. M. de Leeuw, Adv. Mater. **24**, 1146 (2012).
[13] A. Sharma, S. G. J. Mathijssen, M. Kemerink, D. M. de Leeuw, and P. A. Bobbert, Appl. Phys. Lett. **95**, 253305 (2009).
[14] F. Gholamrezaie, A. M. Andringa, W. S. Roelofs, A. Neuhold, M. Kemerink, P. W. M. Blom, and D. M. de Leeuw, Small **8**, 241 (2012).
[15] R. Hausermann and B. Batlogg, Appl. Phys. Lett. **99**, 083303 (2011).
[16] D. W. Li, E. J. Borkent, R. Nortrup, H. Moon, H. Katz, and Z. N. Bao, Appl. Phys. Lett. **86**, 042105 (2005).
[17] M. Tello, M. Chiesa, C. M. Duffy, and H. Sirringhaus, Adv. Funct. Mater. **18**, 3907 (2008).
[18] P. Kumar, A. Sharma, S. Yadav, and S. Ghosh, Org. Electron. **14**, 1663 (2013).
[19] D. Simeone, M. Rapisarda, G. Fortunato, A. Valletta, and L. Mariucci, Org. Electron. **12**, 447 (2011).
[20] B. Stadlober, U. Haas, H. Maresch, and A. Haase, Phys. Rev. B **74**, 165302 (2006).
[21] Y. Y. Hu, Q. Qi, and C. Jiang, Appl. Phys. Lett. **96**, 133311 (2010).
[22] Y. Y. Hu, L. M. Wang, Q. Qi, D. X. Li, and C. Jiang, J. Phys. Chem. C **115**, 23568 (2011).
[23] Q. Qi, A. F. Yu, L. M. Wang, and C. Jiang, J. Nanosci. Nanotechnol. **10**, 7103 (2010).
[24] R. Matsubara, N. Ohashi, M. Sakai, K. Kudo, and M. Nakamura, Appl. Phys. Lett. **92**, 242108 (2008).
[25] M. C. Bartelt and J. W. Evans, Phys. Rev. B **54**, R17359 (1996).
[26] J. A. Venables, G. D. T. Spiller, and M. Hanbucken, Rep. Prog. Phys. **47**, 399 (1984).

This article is copyrighted as indicated in the abstract. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 124.16.156.254 On: Fri, 29 Nov 2013 08:50:40