Influence of Interfacial Mixing on Thermal Boundary Conductance Across a Chromium/Silicon Interface

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The thermal conductance at solid-solid interfaces is becoming increasingly important in thermal considerations dealing with devices on nanometer length scales. Specifically, interdiffusion or mixing around the interface, which is generally ignored, must be taken into account when the characteristic lengths of the devices are on the order of the thickness of this mixing region. To study the effect of this interfacial mixing on thermal conductance, a series of Cr films is grown on Si substrates subject to various deposition conditions to control the growth around the Cr/Si boundary. The Cr/Si interfaces are characterized with Auger electron spectroscopy. The thermal boundary conductance (h_{BD}) is measured with the transient thermoreflectance technique. Values of h_{BD} are found to vary with both the thickness of the mixing region and the rate of compositional change in the mixing region. The effects of the varying mixing regions in each sample on h_{BD} are discussed, and the results are compared to the diffuse mismatch model (DMM) and the virtual crystal DMM (VCDMM), which takes into account the effects of a two-phase region of finite thickness around the interface on h_{BD}. An excellent agreement is shown between the measured h_{BD} and that predicted by the VCDMM for a change in thickness of the two-phase region around the interface. [DOI: 10.1115/1.2897344]

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Introduction

Thermal management has played a critical role in the development of micro- and optoelectronic devices over the past several decades. Much of the theory used in thermal management design has relied on macroscopic principles where feature sizes and times are larger than the mean free path and scattering time of the energy carriers. Only recently, with the advent of smaller devices and structures, have we had to develop models and theories based on microscopic principles. This is particularly the case with the growing interest in nanoscale and superlattice devices. For this reason, there has been a growing interest in the determination of the thermophysical properties, but perhaps more critical to thermal transport in nanoscale and superlattice devices is the thermal boundary conductance (h_{BD}), which is frequently approximated or neglected, leading to significant uncertainties in design and performance. The thermal boundary conductance between materials is becoming increasingly critical to both the design and selection of innovative materials. Indeed, as the nanorevolution continues, our focus turns toward the manipulation of material systems to enhance/restrict thermal transport, but much fundamental work remains before significant advances can be made in the area of interface engineering.

Heat conduction across solid-solid interfaces is a controlling factor for thermal transport in thermoelectrics [1,2], thin-film high temperature superconductors [3,4], vertical cavity surface emitting lasers [5], and optical data storage media [6]. The properties of the interfaces in these devices lead to varying levels of h_{BD}, creating a temperature difference between the two solids. Kapitza was the first to observe a finite temperature drop across an interface between two different materials [7]. This work was at low temperatures where the mean free paths of the primary energy carriers (acoustic phonons) are large. Unlike at low temperatures, at room temperature, the energy carriers' mean free paths are quite small ($\sim$10–100 nm) and h_{BD} is typically neglected. With the advent of nanoscale devices with dimensions on the order of the mean free paths, h_{BD} has become significant in thermal management at room temperature. This is especially the case for devices with multiple interfaces, such as superlattices [8] and very large scale integrated (VLSI) circuits [8].

Thermal boundary conductance across nanomaterial interfaces has been the focus of several computational and experimental studies. An extensive review of thermal boundary conductance experiments and theory until 1989 is presented by Swartz and Pohl [9]. Since then, much progress has been made in numerical studies of h_{BD} [10]. Several groups have numerically examined the effects that lattice mismatch and the type of phonon scattering—elastic, inelastic, specular, or diffuse—have on h_{BD} [11–22]. The dependence of h_{BD} on lattice mismatch and phonon scattering has also been examined experimentally [23–26]. These analyses have mainly focused on perfect interfaces between nanomaterials (i.e., no interatomic mixing or disorder around the interface). However, in realistic nanodevices, pronounced interdiffusion or reactions can occur on the order of the characteristic length of the device, even at room temperature [27]. This interdiffusion results in the presence of a disordered and two-phase region at the interface of two materials, which contributes to the

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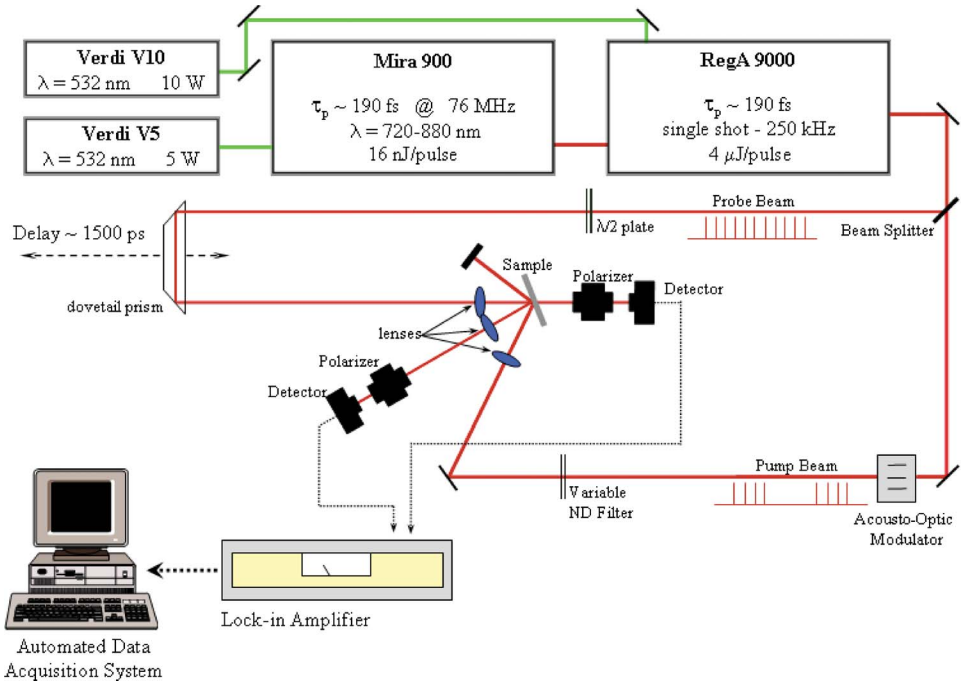

Fig. 1 TTR experimental setup used in this study

overall h_{BD} [9]. The effects of disorder or a two-phase region on h_{BD} has been the focus of many numerical studies [28–32] but, experimentally, has only been qualitatively observed [33]. The lack of experimental observation has led to conflicting theoretical results for h_{BD} as a result of multiphase and diffusion regions. For example, the scattering-mediated acoustic mismatch model (SMAMM) predicts a decrease in h_{BD} [20], while calculations by Kozorezov et al. indicate an increase [34]. However, these results are based on purely theoretical calculations, and, as previously mentioned, there have not been many experimental studies on the effects of interfacial mixing on h_{BD}; clearly, an in-depth experimental examination of interfacial diffusion effects on h_{BD} in thin-film systems would make a large contribution to the current understanding of h_{BD}.

This study examines h_{BD} at the interfaces of Cr films on Si substrates fabricated by various deposition procedures in an attempt to systematically vary the properties of the Cr/Si interface. Chromium is of particular interest since Cr films are often used as adhesion layers for more conductive materials in interconnects [35,36], in metal-dielectric mixtures (cermets) [37], and in high powered laser systems [38]. The thermal boundary conductance in the Cr/Si systems is measured with the transient thermoreflectance (TTR) technique. In the TTR technique, a short-pulsed laser beam is used to heat a thin metal film. The transient reflectance of the thin metal film is then probed with a weaker laser pulse after a known time delay. This technique has been used by several groups to measure h_{BD} at metal-dielectric interfaces [23,24,39]. The change in elemental composition near the interfaces is characterized with Auger electron spectroscopy (AES). Since this study is focused on the elemental change of Cr and Si in the interfacial region, AES is sufficient to resolve the major constituents. The experimental results show an excellent agreement with the virtual crystal diffuse mismatch model (VCDMM) [40,41], a model based on the diffuse mismatch model (DMM) [9] that takes into account the effect of mixing around the interface of two materials on h_{BD}.

Experimental Setup

The TTR data were taken with the pump-probe experimental setup shown in Fig. 1. The primary output of the laser system emanates from a Coherent RegA 9000 amplifier operating at a 250 kHz repetition rate with about 4 μJ/pulse and a 150 fs pulse width at 800 nm. The pulses were split at a 9:1 pump to probe ratio. The pump beam, modulated at 125 kHz, was focused down to a 100 μm radius spot size to achieve a 10 J m^{-2} fluence. The radii of the pump and probe beams were measured with a sweeping knife edge [42]. Although the low repetition rate of the RegA system and the "one shot on–one shot off" modulation rate of the pump beam ensures minimal residual heating between pump pulses, the phase of the signal must still be taken into account. The phase correction was performed by the procedures for signal phase adjustment outlined by Stevens et al. [42].

For long scans, the alignment of the pump and probe spots may become an issue [24,43]. To avoid misalignment problems, the probe beam was collimated before the probe delay stage and was profiled with a sweeping knife edge at all time delays. In this study, a pump to probe radius ratio of 10:1 was used, and the probe was aligned with the delay stage, resulting in less than 1.5 μm and 4.0 μm drift along the horizontal and vertical axes perpendicular to the surface, respectively. These spot characteristics result in less than 1% error due to misalignment of the beams [42].

The TTR technique produces some excitation of the metal film followed by a cooling of the film due to the film's thermal connection to the substrate. To simplify data reduction, the temperature response is ideally influenced only by conductance across the interface and not by diffusion within the metal film. If the film is too thick or has a low thermal conductivity, however, there will be two free parameters (film thermal conductivity k_f and h_{BD}) when fitting experimental data to a thermal model. To avoid this situation, the Biot number Bi for the interface should be significantly

less than 1 (typically less than 0.1), so that the film can be treated as a lumped thermal capacitance [44]. Therefore, the film thickness should be restricted to

$$\mathrm{Bi} = \frac{h_{\mathrm{BD}} d}{k_f} < 0.1 \Rightarrow d < \frac{0.1 k_f}{h_{\mathrm{BD}}} \tag{1}$$

where d is the film thickness. For Cr/Si interfaces, $h_{\mathrm{BD}} \sim 2.0 \times 10^8$ W m^{-2} K^{-1} and k_f=94 W m^{-1} K^{-1} [24,45]. Therefore, the film thickness should be no more than 50 nm. This is a reasonable thickness from the microscopic prospective since it is approximately three times larger than the mean free path, therefore reducing the probability of ballistic electron scattering at the interface [46,47].

For the case when the metal film is treated as a lumped capacitance, the thermal model for the film and substrate system is

$$\rho d C_f \frac{dT_f(t)}{dt} = h_{\mathrm{BD}}[T_s(0,t) - T_f(t)] \tag{2}$$

$$\frac{\partial T_s(x,t)}{\partial t} = \alpha_s \frac{\partial^2 T_s(x,t)}{\partial x^2} \tag{3}$$

where T_f is the temperature of the film that is measured using the TTR technique, T_s is the substrate temperature and is a function of time and space, and ρ, C_f, and α_s are the film density, film specific heat, and substrate diffusivity, respectively. Radiative and convective losses at the front of the film surface are negligible compared to typical interface conductances of 10^6–10^8 W m^{-2} K^{-1} and are therefore neglected. The temperature in Eqs. (2) and (3) can be nondimensionalized by

$$\varphi_{f,s} = \frac{T_{f,s} - T_0}{T_f(0) - T_0} \tag{4}$$

where T_0 is the ambient temperature and $T_f(0)$ is the temperature of the film immediately after excitation. Therefore, the thermal model can be expressed as

$$\frac{d\varphi_f(t)}{dt} = \frac{h_{\mathrm{BD}}}{\rho d C_f}[\varphi_s(0,t) - \varphi_f(t)] \tag{5}$$

$$\frac{\partial \varphi_s(x,t)}{\partial t} = \alpha_s \frac{\partial^2 \varphi_s(x,t)}{\partial x^2} \tag{6}$$

subject to the following initial conditions:

$$\varphi_f(0) = 1 \tag{7}$$

$$\varphi_s(x,0) = 0 \tag{8}$$

and the following boundary conditions:

$$-k_s \frac{\partial \varphi_s(0,t)}{\partial x} = h_{\mathrm{BD}}[\varphi_f(t) - \varphi_s(0,t)] \tag{9}$$

$$\frac{\partial \varphi_s(\infty,t)}{\partial x} = 0 \tag{10}$$

The semi-infinite assumption made in Eq. (10) is reasonable for the time scale of interest, ~1–5 ns. The thermal penetration depth for most substrates at this time scale is $(\alpha_s t)^{1/2} < 1$ μm, which is significantly less than the thickness of the Si substrate used in this study.

Table 1 Thermophysical parameters used in the study [56]

Lattice heat capacity of Cr film, C_f	3.3×10^6 J m^{-3} K^{-1}
Lattice heat capacity of Si substrate, C_s	1.65×10^6 J m^{-3} K^{-1}
Thermal conductivity of Si substrate, k_s	148 W m^{-1} K^{-1}
Ambient temperature, T_0	300 K

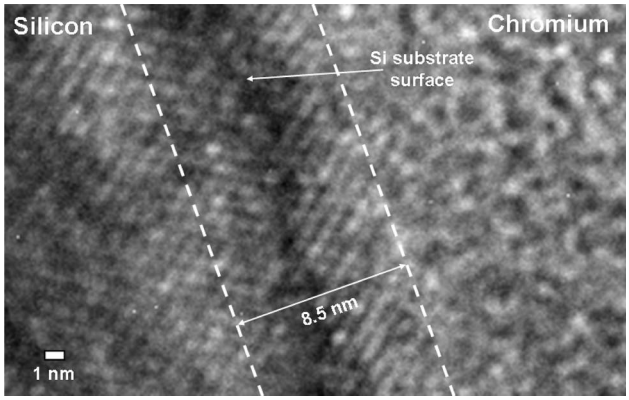

Fig. 2 TEM image of the Cr/Si interface. The observable mixing from the TEM analysis is based on the Si crystallographic planes, yielding a 8.5 nm mixing layer. However, the actual Cr/Si elemental mixing may not be completely crystalline; therefore, AES is used for interfacial chemical analysis.

Equations (5) and (6) subject to Eqs. (7)–(10) were numerically solved using the Crank–Nicolson method, which has only a second order truncation error in both time and space. The thermal boundary conductance was determined by fitting the TTR data to the model using the material constants listed in Table 1. The specifics of the fitting procedure are discussed in a later section.

Sample Preparation and Interface Characterization

The purpose of changing the conditions during deposition was to try to control the amount of interdiffusion between the Cr and Si. When in contact with Si at room temperature, Cr has been shown to form an intermixed region ~10 ML thick [48]. However, when in contact with thick oxide layers (such as SiO_2, an oxide layer that naturally forms on Si), Cr will develop a strong adhesive bond to the oxide, creating a diffusion barrier for further reaction between the Cr and SiO_2 [36]. In addition, Cr is known to form silicides on oxide-free surfaces at elevated temperatures ($CrSi_2$ at 720 K) [49]. An example of Cr/Si mixing is shown in the transmission electron micrograph in Fig. 2, which is focused on the interface between the Cr film and the Si substrate of sample Cr-4 (see Tables 1 and 2). The surface of the Si substrate exhibits some degree of roughness, which is apparent by the dark region labeled "Si substrate surface" in Fig. 2. Note that the thickness of interatomic mixing determined from the transmission electron microscopy (TEM) analysis was quantified by examining the interference lines from the Si[110] crystallographic planes. Therefore, the mixing region, which is determined from the TEM as 8.5 nm

Table 2 Fabrication details of Cr/Si samples

Sample ID	Backsputter etch (min)	Heat treatment prior to deposition	Deposition notes
Cr-1	None	None	50 cm Cr at 300 K
Cr-2	5	None	50 nm Cr at 300 K
Cr-3	5	20 min at 873 K	50 nm Cr at 300 K
Cr-4	5	50 min at 873 K	50 nm Cr at 300 K
Cr-5	5	20 min at 873 K	50 nm Cr at 573 K
Cr-6	5	None	10 nm Cr at 300 K; Heat treatment to 770 K; deposition of 40 nm Cr at 300 K

thick, only represents the Cr/Si mixing when the Si diamond structure is still present. There is still some atomic mixing between the Cr/Si that results in a noncrystalline structure; therefore, the chemical mixing between Cr and Si could be slightly larger than the structural quantification from the TEM image. This elucidates the importance of a chemical analysis for an accurate determination of Cr/Si elemental mixing.

The Cr films were grown on Si ⟨100⟩ substrates in a multisource, high vacuum thin-film sputter deposition system, a Supersystem III manufactured by the Kurt J. Lesker company capable of pumping down to 10^{-7} Torr. This specific system is equipped with a chamber heater capable of reaching temperatures greater than 900 K and a vibrating quartz crystal to monitor deposition rate. The Cr deposition rate is about 17 nm/min with 37 SCCM Ar flow rate and 300 W power to the target gun. All substrates were spin cleaned with reagent alcohol (90.7% ethyl alcohol, 4.8% isopropyl alcohol, 4.5% methyl alcohol, and 0.12% water), trichloroethylene, and methanol, and were then subsequently baked for 5 min at 400 K to remove any residual water that may have formed at the substrate surface as a result of spin cleaning. Once in the chamber, various in situ deposition procedures were performed including backsputter etching followed by chamber heating up to 873 K before deposition. While fabricating some samples, the chamber temperature was elevated during or after Cr deposition. During any type of chamber heating, a ramp rate of 20 K/min was maintained until the target temperature was reached. Therefore, if a certain deposition requires the chamber to maintain 873 K for 20 min, the chamber is actually at an elevated temperature for a much longer time due to the slow temperature rise to reach the target temperature and the slow radiative cooling processes of the vacuum chamber back to room temperature. The procedures used during fabrication for each of the 50 nm Cr/Si samples are summarized in Table 2. A total of 50 nm of Cr was deposited during any given deposition and was verified with the in situ vibrating quartz crystal. Films of this thickness ensure that h_{BD} across the Cr/Si interface can be accurately resolved, given the 1.5 ns maximum delay of the probe path in the TTR experimental setup [24].

A number of differently composed interface regions were expected, as the Cr/Si fabrication parameters were systematically modified. The interfaces were characterized by AES, used in conjunction with an argon ion beam to provide quantitative compositional information as a function of depth into the material. Data were taken on a commercial X-ray photoemission spectroscopy (XPS)/scanning Auger system (Physical Electronics 560), equipped with a double-pass, cylindrical mirror electron energy analyzer (CMA). To minimize the adsorption of contaminants on the sample surface, the chamber is maintained at ultrahigh vacuum (at a base pressure of 10^{-9} Torr) with a 200 Hz ion pump, assisted by a small sublimation pump. These pumps allow the vacuum chamber to remain virtually free of hydrocarbon contamination. The electron gun is mounted coaxially inside the electron energy analyzer for efficient data collection and to reduce shadowing effects. A 3 keV electron beam was used for AES analysis, and depth profiling was conducted by atomically sputtering away the material using a 240 nA Ar ion beam current and a 2×2 mm^2 raster, which resulted in a Cr sputtering yield of 4.12 nm/min. A typical AES depth profile of the Cr/Si samples is shown in Fig. 3. It should be noted that the vacuum in the sputtering chamber during Cr deposition was low (10^{-6} Torr), so the relatively low levels of O_2 and C contamination found in the films is expected. Also, note that the O_2 and C percentages in the Cr film depth are slightly higher than the actual composition since contaminants from the film surface are pushed into the depth of the film as a result of the Ar ion bombardment for the depth profile. The beginning and end of the Cr/Si mixing region is defined as the depth at which Si reaches 10% of the total film composition and Cr reaches 10% of the film composition, respectively. This threshold was chosen since C levels were slightly less than 10% of the total film composition near the interface.

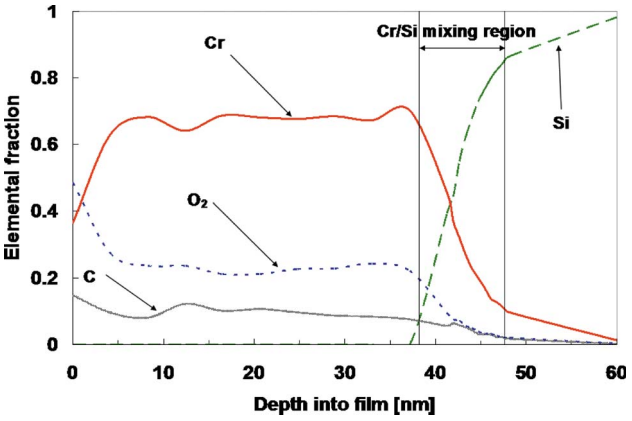

Fig. 3 Example of a full AES spectrum of one of the Cr/Si films examined, Cr-1. Note the relatively high concentrations of O_2 and C at the sample surface, about 100% more than those in the film. These elements were sputtered away from the surface with the ion gun during the depth profiling procedure. The mixing layer is depicted by the vertical lines at the 10% mark of the Si and Cr.

The AES spectra around the mixing region for all six samples are shown in the Appendix. The ID's of each sample corresponding to the ID's in Table 2 are shown in the upper left of each plot. The line types in the Appendix represent different elements and correspond to the same designation as in Fig. 3. Due to the controlled deposition conditions, varying mixing layer thicknesses and spatial gradients are expected at the sample interfaces. Since Cr is expected to form a diffusion barrier when in contact with an oxide layer, the O_2 levels at the beginning of the mixing layer must also be considered to explain the different compositional changes among the samples. The O_2 levels at the beginning of the defined mixing layer range from 12% to 21%. Examining only the samples that were deposited at room temperature (Cr-1–Cr-4), Cr-1 has about 19% O_2 at the beginning of the mixing layer while the other room temperature samples have about 14%. The backsputter etch procedure performed on Cr-2–Cr-4 is most likely responsible for this since bombarding the substrate with Ar atoms prior to deposition is a common method to remove the native oxide layer.

Substrate etching can physically roughen the substrate, which could lead to Cr atoms being deposited into craters beneath the substrate surface introduced by the backsputter process. This is evident from the differing mixing layer thicknesses among the samples deposited at room temperature. In an attempt to smooth the substrate surface after backsputtering, the chamber temperature was increased to 873 K prior to Cr deposition. When only backsputtered (Cr-2), the mixing layer depth is almost 15 nm compared to a 9.5 nm two-phase region seen in Cr-1, which was not backsputtered prior to deposition (however, since only ETM spin cleaning was performed on Cr-1, it is assumed that the surface was relatively smooth from factory polishing and the oxide layer). The annealing for different times (20 min and 50 min for Cr-3 and Cr-4, respectively) results in a smaller mixing layer depth with increased annealing times. Notice that annealing for 50 min (Cr-4) results in a two-phase region of 10 nm, almost the same thickness as Cr-1 (9.5 nm) in which there was no in situ substrate preparation.

The thermal model used in this study is extremely sensitive to film thickness [24]. Although 50 nm of Cr was deposited during fabrication due to the varying levels of Cr/Si mixing, the portion of the film that can be modeled with the Cr heat capacity is actually less than 50 nm. To accurately model this system, the thick-

Table 3 Summary of results from the AES and TTR data

Sample ID	Cr film thickness (nm)	Mixing layer (nm)	O_2 (%)	Slope of Si in mixing layer (%/nm)	Av. h_{BD} (GW m^{-2} K^{-1})
Cr-1	38	9.5	19	9.7	0.178
Cr-2	37	14.8	14	16.4	0.113
Cr-3	35	11.5	14.2	16.6	0.139
Cr-4	35	10.1	14.6	7.4	0.15
Cr-5	39	5.8	21.5	24.1	0.134
Cr-6	45	7	12.3	28.1	0.124

ness used in Eq. (5) was determined from the AES scans, and the thickness of the film in this study is defined as the distance from the film surface to the beginning of the mixing layer. The thicknesses used for each film are listed in Table 3.

To quantify the spatial change of the elements in the mixing layer, the Si data points in the first ~3 nm after the beginning of the mixing layer were fitted with a linear trend. The slope of this line represents the rate of change of the Si concentration during the first few nanometers of Cr/Si mixing. Since the elemental concentrations of Cr, C, and O_2 all decrease as Si increases, monitoring the change in Si with distance into the mixing layer gives a good indication of the spatial gradient in the mixing region. As previously mentioned, a total of 50 nm of Cr was deposited during the fabrication of each sample. The defined mixing layers all terminate at or before 50 nm in the AES profiles, indicating that Si diffusion into the deposited Cr is the primary diffusion element causing the two-phase mixing layer. Again, examining the room temperature depositions, Cr-1 and Cr-4 have similar Si gradients and Cr-2 and Cr-3 have similar gradients. This is probably a result of different interdiffusion rates of the Cr and Si during deposition, resulting from O_2 layers or various degrees of roughness on the substrate surface. The higher O_2 levels on the surface of Cr-1 limited interdiffusion, resulting in a slower diffusion of the Si into the Cr. This is consistent with past studies indicating that Cr and O_2 form a diffusion barrier [36]. However, we see the same type of gradient in Cr-4, indicating that the Si diffusion could be dictated by the smoothness of the surface. Substrate roughening is assumed in Cr-2 from the backsputter procedure, and perhaps a similar degree of roughness is present in Cr-3 since the attempt to anneal the substrate only lasted for 20 min, as opposed to Cr-4, which maintained a high chamber temperature for 50 min. A summary of the mixing layer depth, O_2 concentration at the beginning of the interfacial mixing layer, and slopes of the Si in the AES profiles is given in Table 3.

Samples Cr-5 and Cr-6 were subjected to higher deposition temperatures. 50 nm of Cr was deposited on a backsputtered and annealed substrate at 573 K in Cr-5. Notice that the Si diffusion is much smoother throughout the mixing layer, and the defined mixing layer is much thinner than the room temperature samples. The higher temperature and smooth surface probably resulted in much faster Si diffusion, which would lead to the thinner mixing layer. This also explains the profile for Cr-6, which exhibits the same thin mixing layer. This sample was only backsputtered before 10 nm of Cr was deposited; then, the chamber was heated above the $CrSi_2$ formation temperature. This explains the mixing layer ending slightly after 50 nm from the Cr film surface (similar to Cr-2). However, the chamber was heated and maintained above the $CrSi_2$ formation temperature for 5 min. So, theoretically, this could have resulted in silicide formation that would not have been detected in the AES depth profile presented in the Appendix. This sample (Cr-6) was additionally characterized with XPS [50], and no evidence of Cr silicide formation was detected.

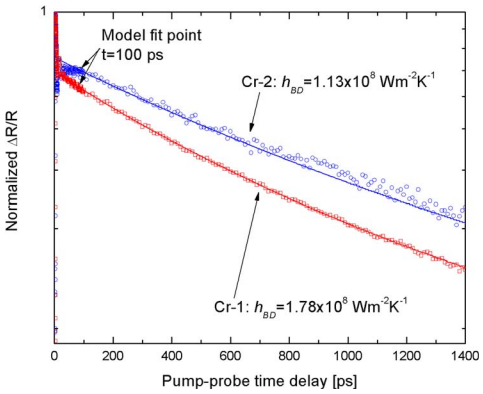

Fig. 4 TTR data of Cr-1 and Cr-2 fits with the model described with Eqs. (5)–(10). A 40% decrease in the best fit h_{BD} from Cr-1 to Cr-2 is observed, with the only change in the experiment occurring in the deposition conditions (see Table 1).

Thermal Boundary Conductance at Various Cr/Si Interfaces

Several TTR scans were taken on each sample, and the average of the resulting h_{BD} for these scans is reported in Table 3. A consistent deviation of less than 7% from the mean was calculated for all the data on each sample. The thermal boundary conductance of each was determined by scaling the model (Eqs. (5)–(10)) to the TTR data at 100 ps and fitting the model to the data [24]. This method assumes that the reflectance varies linearly with temperature [24,39,51]. At 100 ps, the temperature gradient in the metal film is negligible, and the electrons and lattice are in thermal equilibrium. The thermal boundary conductance was treated as a free parameter and was adjusted to minimize the sum of squares between the thermal model and the TTR data. Minimization was performed using an inverse parabolic interpolation technique, which normally required less then ten iterations to converge.

To ensure that the TTR data taken with the 10 J m^{-2} pump can be linearly related to electron temperature, h_{BD} of Cr-3 was measured at a variety of pump fluences ranging from 0.5 J m^{-2} to 10 J m^{-2}. The average h_{BD} measured with varying pump fluence was 0.139 GW m^{-2} K^{-1}, which is the same h_{BD} determined from the various measurements on Cr-3 with 10 J m^{-2}. The deviation among the measurements was less than 4% from the mean, which is less than the ~7% deviation among the samples from repeated measurements at one fluence, as previously mentioned. This indicates that for the fluence used in this study (10 J m^{-2}), the assumption that the reflectance varies linearly with temperature is valid.

Figure 4 shows the normalized TTR data taken on Cr-1 and Cr-2 and the best fit of the thermal model to the data using the thermophysical constants listed in Table 1 and h_{BD} as the fitting parameter. A best fit h_{BD} of 0.178 GW m^{-2} K^{-1} was found for Cr-1, where Cr-2 showed a 40% reduction in h_{BD} with 0.113 GW m^{-2} K^{-1}. Examining the corresponding AES profiles of Cr-1 and Cr-2 (Appendix), it is apparent that the thickness of the mixing layer and spatial change of the Si content in the mixing layer can both contribute to varying levels of h_{BD}.

The thermal boundary conductance measured in Cr-1 is consistent with the 0.2 GW m^{-2} K^{-1} h_{BD} measurement of a 30 nm Cr film deposited on a lightly backsputtered Si substrate by Stevens et al. [24]. However, Cr-1 was not subject to backsputtering, where Cr-2 was deposited after backsputtering at relatively high powers for a long time. This is evidence of the extreme sensitivity

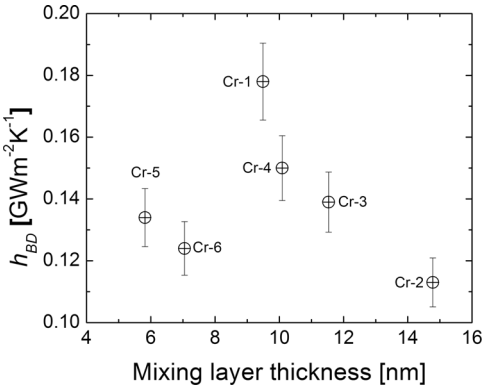

Fig. 5 Average of the measured h_{BD} of each sample as a function of mixing layer thickness. The room temperature samples display a linear decrease in h_{BD} with increasing mixing layer thickness. The samples deposited at higher temperatures (Cr-5 and Cr-6) do not follow this trend, which could be due to defects of a change in the microstructure relative to the room temperature deposited samples. The error bars represent the 7% deviation from the mean calculated from the data from each sample, which are the calculated errors associated with the repeatability of the data from the experiment.

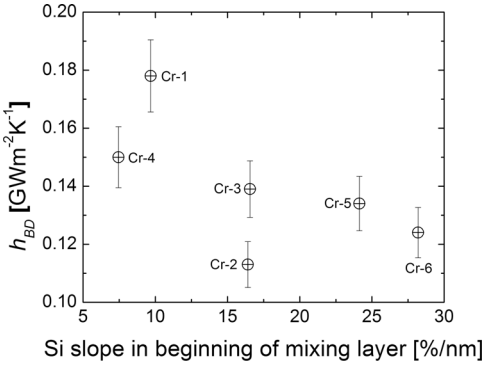

Fig. 6 Average of the measured h_{BD} of each sample as a function of rate of Si increase at the beginning of the interfacial layer. An increase in h_{BD} is observed as the Si spatial change in the film becomes more gradual. The error bars represent the 7% deviation from the mean calculated from the data from each sample, which are the calculated errors associated with the repeatability of the data from the experiment.

of h_{BD} to interfacial conditions and is indicative of the variability in the fabrication processes.

The sensitivity of the model to film thickness also needs to be considered. Since the model assumes a lumped capacitance, a change in film thickness would change the thermal mass of the system, affecting the predicted change in temperature. For example, assuming that the Cr film thicknesses were actually 50 nm, the amount of Cr deposited onto the Si substrates during deposition, the values of h_{BD} determined from the fitting routine could increase as much as 50%. However, this increase would be common on all samples maintaining the same trends reported in this study. As previously mentioned, the Cr film thicknesses were determined from the AES profiles and are listed in Table 3. This thickness sensitivity also gives more evidence of the effect of fabrication variability and interfacial conditions on the measured thermal boundary conductance since h_{BD} measured by Stevens et al. was slightly higher for a thinner film.

Figure 5 shows the measured h_{BD} of the six Cr samples as a function of mixing layer thickness. The thermal boundary conductance in the room temperature samples (Cr-1–Cr-4) decreased with increasing mixing layer thickness. In these samples, the h_{BD} ranged from 0.178 GW m^{-2} K^{-1} in the sample with a 9.5 nm mixing thickness to 0.113 GW m^{-2} K^{-1} in the sample with 14.8 nm of mixing. In these room temperature samples, the smallest amount of mixing occurred in Cr-1, which was not subject to any in situ substrate cleaning. The other room temperature samples, Cr-2–Cr-4, were subject to backsputter etching, which reduced the oxygen on the Si surface from ~19% to ~14% (see Table 3) and also roughened the substrate prior to Cr deposition. The largest mixing layer thickness and lowest h_{BD} were measured in Cr-2, which could be a result of the Si substrate being rougher than the other room temperature samples. When the substrate was heated after etching, presumably smoothing the surface and reducing surface defects before room temperature Cr deposition (Cr-3 and Cr-4), the mixing layer thickness decreased, resulting in a linear increase in h_{BD}. The measured h_{BD} in Cr-1 deviated from the linear trend in Cr-2–Cr-4, which could be partly due to the increased O_2 concentration.

The samples that were subject to non-room-temperature depositions, Cr-5 and Cr-6, did not demonstrate the same relationship between h_{BD} and mixing layer. Both samples had much smaller mixing layer thicknesses. The elevated temperatures imposed on the Cr during deposition could have introduced impurities or changed the material structure around the interface or in the film that was not detectable by AES, therefore introducing another variable between the high temperature deposited samples and the room temperature deposited samples.

Figure 6 shows the relationship between measured h_{BD} and the interface "abruptness" (the slope of the Si content changes with depth, as previously described). Note that the slope of the spatial increase of Si is quantified by only considering the first 3 nm in the mixing layer defined in the AES data. In addition, a very abrupt interface does not necessarily relate to a small mixing layer thickness. The apparent trend is a decrease in h_{BD} with an increasingly abrupt interface. The highest h_{BD} values in the room temperature samples (Cr-1–Cr-4) are measured on the samples in which the Cr was deposited on a smooth Si surface, which created a more gradual increase in Si content near the interface compared to the samples in which Cr was deposited at elevated temperatures (Cr-5 and Cr-6). Chromium and Si represent acoustically matched materials with nearly identical Debye temperatures (Θ_{D_Cr} =630 K and Θ_{D_Si}=640 K) and, therefore, have similar Debye cutoff frequencies [45]. By calculating the phonon radiation limit (PRL) of the Cr/Si system, an upper limit of the h_{BD} is established as 1.38 GW m^{-2} K^{-1} [23,52]. Any contribution to thermal boundary conductance by phonons resulting in a value above this limit would indicate occurring inelastic phonon scattering processes [25,26]. The calculated PRL is higher than the measured h_{BD}; so, elastic scattering is assumed in this analysis.

The DMM, which assumes elastic phonon scattering [9], can therefore be applied to the system. In its simplest form, the DMM can be calculated with

$$h_{BD} = h_{1\to 2} = \frac{1}{4}\sum_j \nu_{1,j}\int_0^{\omega_{\max}} \tau_{1\to 2}\hbar\omega\frac{\partial N_{1,j}}{\partial T}d\omega \qquad (11)$$

where $\nu_{1,j}$ is the speed of phonon mode j (longitudinal or transverse) in side 1 (acoustically softer material—here, the Cr film), $\tau_{1\to 2}$ is the probability of phonon transmission from side 1 into side 2, and $N_{1,j}$ is the product of the phonon occupation function and density of states of mode j on side 1. Assuming that the diffuse scattering from the rough boundary equilibrates the phonon system, the Bose-Einstein distribution function can be implemented and h_{BD} of 0.855 GW m^{-2} K^{-1} is calculated using a Debye approximation. The DMM, like the PRL, also overpredicts the measured h_{BD}. This has often been associated with poor interface quality and substrate damage [9,23,24,33]. As shown in this study,

this could result in varying degrees of mixing, which is most likely the direct cause for differences between the measured h_{BD} and that calculated from the DMM. The DMM does not take into account an interfacial mixing layer. Although the SMAMM has been proposed to partially account for this [20], it is not applied in this study since it assumes specular phonon reflection, which is clearly not a valid assumption in this case since the interfacial region is shown to be significantly disordered [4].

At an ideal interface with no mixing, a phonon from the Cr film scatters at the Cr/Si interface and is either transmitted into the Si or reflected back into the Cr. Assuming diffuse scattering and using equations in the references based on the phonon speeds of the different modes (longitudinal and transverse), the phonon transmission probability can be calculated [9]. For a Cr/Si interface, the phonon transmission probability is $\alpha_{Cr-Si}=37\%$ under the Debye solid model, meaning that at the ideal interface, 37% of the phonons are transmitted from the Cr side to the Si side (or from Si to Cr since the phonon loses its "memory" when it is scattered). This transmission can be assumed constant over the energy spectrum if we assume that Cr and Si are isotropic Debye solids, an assumption that is made in the derivation of the form of the DMM and PRL that is used in this study [9]. This scattering can also be explained as 37% of the incident phonon energy is transmitted into the substrate.

In the event of interfacial mixing, the phonons must propagate across a finite amount of space to conduct energy into the substrate. When these phonons scatter with Si at the beginning of the mixing layer, a certain percentage is transmitted deeper into the mixing layer. As the thickness of interfacial mixing layer increases, the probability that a phonon will scatter more than once increases, thereby decreasing h_{BD}, which is expected with increased diffuse scattering in well matched materials [9]. Reduced transmission can also occur from defects or a change in the microstructure around the interface, which could explain the further reduction of h_{BD} observed in Cr-5 and Cr-6, assuming that the elevated temperature during deposition changed the microstructure of the two-phase region compared to the room temperature deposited samples.

VCDMM to Predict h_{BD} as a Function of Mixing Region Thickness

The functionality of h_{BD} with mixing region thickness and composition can be predicted with the VCDMM [40,41]. This model introduces a simple correction to the DMM through the use of a virtual crystal to account for the manner by which energy propagates through the interfacial region. In this manner, multiple scattering events occurring at the interface can be quantified, allowing for a more accurate prediction of h_{BD} as well as insight into the effect of interfacial quality on an overall heat transfer.

In calculations of the traditional DMM (Eq. (11)), the estimation of a perfect interface is assumed; however, as shown in the previous sections, interfacial thickness indeed affects h_{BD}. To account for this thickness, the VCDMM replaces the interfacial region with a third material, the virtual crystal, which has properties that are a blend of the bulk materials [53] and a thickness equal to the length of disorder. Incorporating the virtual crystal modifies the DMM by necessitating the need to account for both the interaction between each of the bulk materials and interface as well as the now finite thickness of the interface.

The interaction between the two materials and the disordered region is investigated by estimating the h_{BD} between each of the bulk materials and the virtual crystal. This is accomplished using Eq. (11) for each of the now two interfaces with a modification of the transmission coefficient α to account for the virtual crystal. This modification is shown below where the subscript i designates the bulk material of interest, and VC the virtual crystal,

Table 4 Comparison of VCDMM to DMM and experimental data on samples deposited at room temperature

Sample ID	Measured h_{BD} ($GW/m^2 K$)	VCDMM ($GW/m^2 K$)	DMM ($GW/m^2 K$)
Cr-1	0.178	0.147	0.855
Cr-2	0.113	0.118	0.855
Cr-3	0.139	0.146	0.855
Cr-4	0.15	0.131	0.855

$$\tau_{i\to VC} = \frac{\sum_j \nu_{VC,j}^{-2}}{\sum_j (\nu_{i,j}^{-2} + \nu_{VC,j}^{-2})} \tag{12}$$

Again, this calculation treats all solids as Debye solids. To calculate the phonon propagation speed in the virtual crystal, a rule of mixture estimation is used where b_1 is the percentage by mass of material 1 in the disordered region,

$$\nu_{VC,j} = b_1 \nu_{1,j} + (1 - b_1)\nu_{2,j} \tag{13}$$

To accurately calculate the percentage b_1 for the Cr/Si interfaces presented here, the depth profiles of Cr-1–Cr-4 were analyzed. These interfaces were chosen for this analysis because the temperature of these samples during Cr deposition was consistent. Therefore, any interfacial structural changes occurring from heat treatments to the Cr/Si system post-Cr deposition do not have to be taken into account, and only the effects of the mixing layer on h_{BD} can be examined. By fitting a functional form using shape preserving interpolants through the silicon profile, a mean value of the elemental percentage was obtained. This value was then used to calculate the virtual crystal properties and hence the h_{BD} for the two interface system according to

$$h_{BD} = \left[\left\{ \sum_j h_{1\to VC,j} \right\}^{-1} + \left\{ \sum_j h_{2\to VC,j} \right\}^{-1} \right]^{-1} \tag{14}$$

The above relation accounts for only the efficiency by which

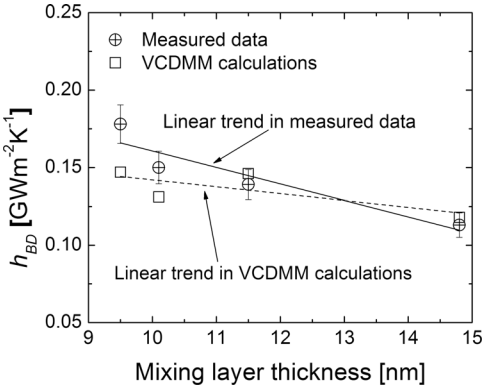

Fig. 7 Comparison of the VCDMM to the experimental data on samples Cr-1–Cr-4. Added electron-phonon coupling resistance is taken into account in these calculations since Cr and Si are acoustically matched solids. Where as the DMM predicts h_{BD} that is almost eight times larger than that measured on the samples with no dependence on mixing layer thickness or compositions, the VCDMM calculations are within 18% of the measured values and show similar trends with mixing layer thickness when taking into account the change in Si composition in the mixing region.

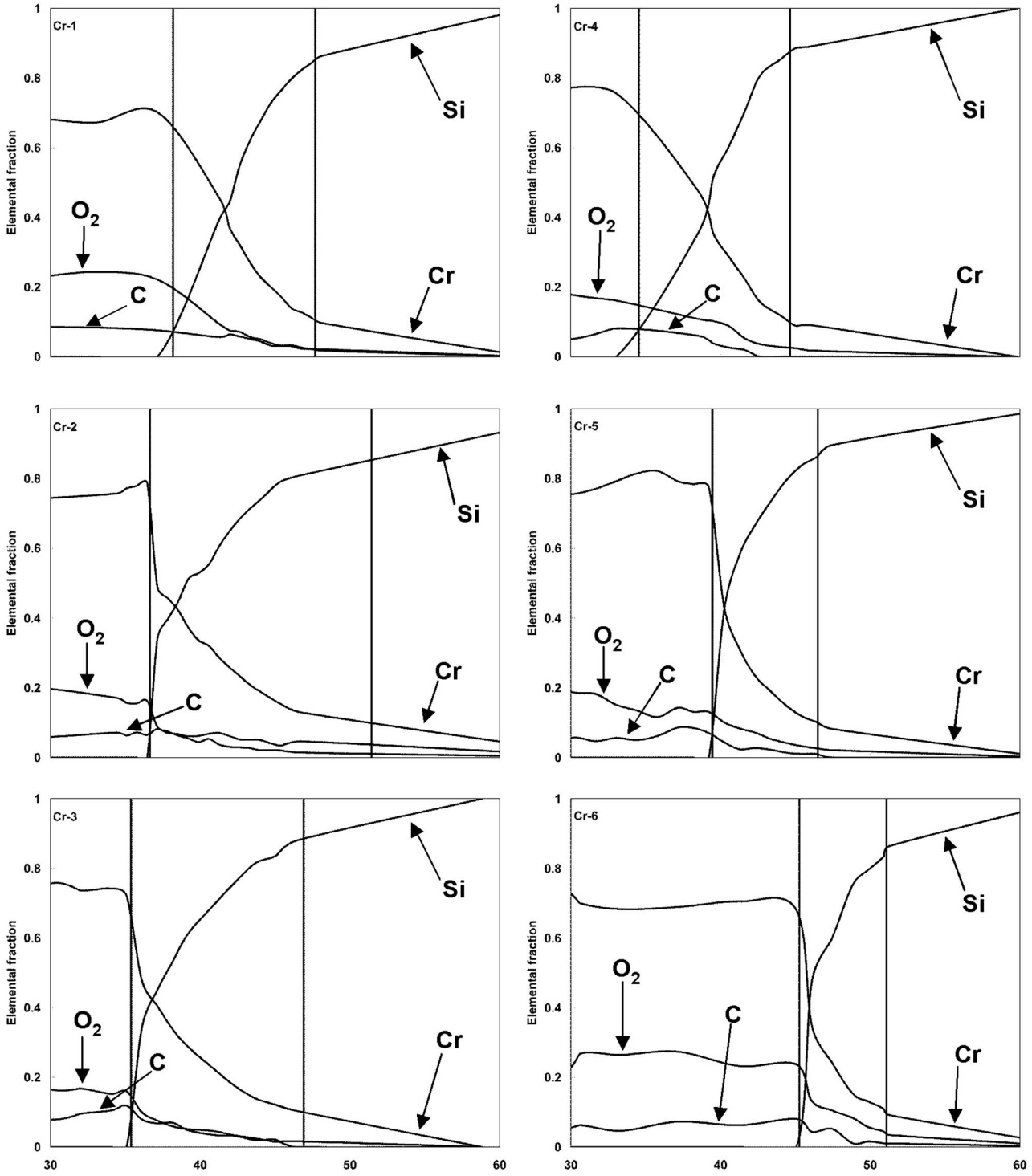

Fig. 8 Auger electron spectroscopy depth profiles

energy transfers from the bulk to the interface but does not analyze the ease by which energy propagates through the interfacial region. To examine this effect, the results of Eq. (14) are scaled according to the depth factor δ, which is a ratio of the interfacial thickness D to the mean free path of the virtual crystal Λ_{VC}. Using kinetic theory to estimate the mean free path along with the measured thickness of the Cr/Si interface, the depth factor was calculated, allowing for the estimation of the h_{BD} from the VCDMM approach, as shown in

$$h_{BD} = \left[\left\{ \frac{\sum_j h_{1\to VC,j}}{\delta_j} \right\}^{-1} + \left\{ \frac{\sum_j h_{2\to VC,j}}{\delta_j} \right\}^{-1} \right]^{-1} \quad (15)$$

Finally, to completely model the system, the electron-phonon coupling was incorporated by using the value reported by Hostetler et al. [54] for chromium and the methodology of Majumdar and Reddy [55] in order to obtain the final prediction for h_{BD}.

Table 4 and Fig. 7 show a comparison of the virtual crystal model to the experimental data. The virtual crystal approach is within 18% of the measured values, whereas the predicted h_{BD} of the DMM is about eight times these values. In both prediction and measurement, there is a distinct trend of decreasing thermal boundary conductance with increasing interfacial thickness. This results from the additional scattering, which occurs as the phonons must propagate through the disordered region. The additional scattering, reduces the rate at which energy flows, thus decreasing the overall conductance and illuminating the role of interfacial quality on performance.

Conclusions

The thermal boundary conductance at the Cr/Si interface was studied for a variety of interfacial conditions. The deposition conditions for the 50 nm Cr films were systematically varied to change various aspects of the Cr/Si mixing, and h_{BD} was measured with the TTR technique. The range of h_{BD} values across the six Cr/Si interfaces show that slight changes in interfacial properties can significantly affect thermal boundary conductance. By different in situ substrate preparation techniques, h_{BD} was reduced by as much as 40%. Results showed a dependence of h_{BD} on both mixing layer thickness and the abruptness of Si change at the interface. The trend in h_{BD} values follows with diffuse scattering assumptions, and it is apparent that in well matched systems such as Cr/Si, phonons that scatter more than once can decrease h_{BD}, which is not taken into account in traditional models such as the DMM. A recently developed model, the VCDMM, was applied to the room temperature deposited data, and a close agreement in both value and trend with mixing layer thickness was observed, offering new insight into the dependence of thermal boundary conductance on disorder around solid interfaces.

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Nomenclature

b = percentage by mass
Bi = Biot number
C = heat capacity, J m^{-3} K^{-1}
d = film thickness, m
h_{BD} = thermal boundary conductance, W m^{-2} K^{-1}
k = thermal conductivity, W m^{-1} K^{-1}
N = total number of phonons per frequency per volume at temperature T, m^{-3}(s^{-1})$^{-1}$
T = temperature, K
v = phonon velocity, m s^{-1}

Greek Symbols

α = thermal diffusivity, m^2 s^{-1}
δ = depth factor in virtual crystal
φ = nondimensionalized temperature
Θ_D = Debye temperature, K
ρ = mass density, kg m^{-3}
τ = probability of phonon transmission across the interface

Subscripts

f = film
$i \rightarrow 2$ = from side i to the virtual crystal
j = phonon mode (longitudinal or transverse)
s = substrate
VC = virtual crystal
0 = initial
1 = material on side 1
2 = material on side 2
$1 \rightarrow 2$ = from side 1 to side 2

Appendix

The Auger electron spectroscopy depth profiles of the six Cr/Si samples are shown in Fig. 8. Note the variation among samples of the mixing layer thickness, Si rate of change at the beginning of the mixing layer, and O_2 concentrations, which are summarized in Table 3.

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