Influence of Lucky Defect Distributions on Early TDDB Failures in SiC Power MOSFETs

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***Abstract*— In this work, we explore the effect of different defect profiles on the occurrence of early time-dependent-dielectric-breakdown (TDDB) to forecast the defect profile present in commercial grade SiC/SiO_2 DMOSFETs. Early failure simulations are performed using the recently developed "lucky defect" model. The model shows that the bulk defects in the gate oxide are the likely culprit for early TDDB failures through an increase in tunneling current via trap-assisted-tunneling (TAT). We show that an exponential distribution of "lucky defects" in the oxide bulk affects the failure distribution in a similar fashion to what we observe experimentally. We also identify the implications of under-sampling the population in these extrinsically dominated failure distributions. Armed with these tools, we show that, the speculated carbon rich transition layer at or near the interface is not likely present in the measured DMOSFETs.**

Keywords—Reliability Testing; SiC; TDDB; Extrinsic Failures; Lucky Defect Model;

I. INTRODUCTION

Silicon Carbide (SiC) DMOSFET production is reaching a maturity level that allows it to replace conventional silicon devices in the power market [1, 2]. Recent studies have shown that the bias temperature instability (BTI) risk for such devices is diminishing due to recent advances in annealing and interface passivation [2, 3]. The intrinsic TDDB performance was also shown to be comparable, if not better than, that of similar SiO_2/Si devices [4]. However, the transition to large volume production requires better control of extrinsic defects and a low level of early failures which is what dictates the overall product reliability. Unfortunately, extrinsic reliability in SiO_2/SiC has received little to no attention. This study greatly extends earlier efforts [5] to identify the origin of these early failures by establishing a correlation between the extrinsic tails of measured failure distributions and user defined lucky defect profiles for arbitrarily chosen device populations.

II. EARLY FAILURES IN SILICON CARBIDE DEVICES

Figure 1 shows the collective TDDB failure distribution collected from over 430 SiC DMOSFETs with 50 nm thick thermal oxide SiO_2 at different fields and different temperatures. Typically, SiC DMOSFET TDDB distributions suffer from a tail similar to what is shown in fig. 1. This tail is frequently *ignored* to focus on the intrinsic reliability. Since the oxide and area are identical for all tested devices, and assuming the breakdown mechanism is the same for all stress fields and temperatures, all groups have the same intrinsic β but a different $T_{63\%}$. Thus, we can normalize the different failure distributions to increase the sample size. The main observation from fig.1 is a distribution tail of around 7.5%. In this paper, we will examine the possible source of such a distribution tail and its connection to the presence of traps in the oxide.

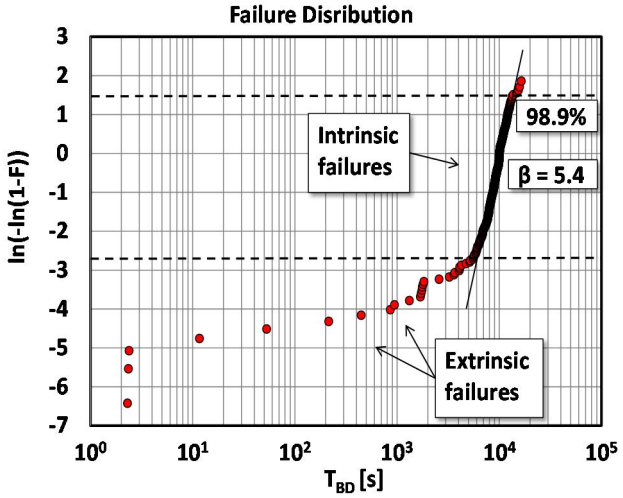

Fig. 1. TDDB results on a total of 432 SiC DMOSFET (200 µm x 200 µm) with a 50 nm thick oxide SiO_2/SiC. The collective data from several TDDB test fields (6.8 MV cm^{-1} to 10 MV cm^{-1}) and temperatures (25 °C to 275 °C) were normalized to a breakdown time of 10^4 s.

III. LUCKY DEFECT MODEL

A newly developed model has attributed the occurrence of early defects in SiO_2/SiC to the presence of "lucky defects" in the oxide bulk [5]. In this model, a "lucky" defect with the appropriate energy level and spatial location (fig. 2) will locally enhance the gate leakage current through trap-assisted-tunneling (TAT) during high-field TDDB stress (fig. 3) where the tunneling current is normally in the Fowler-Nordheim (FN) regime.

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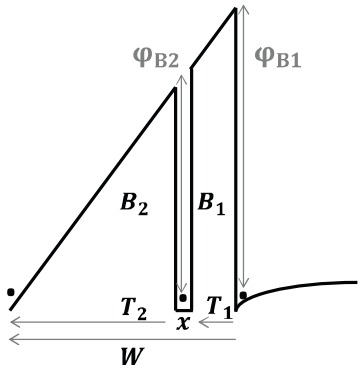

Fig. 2. TAT probability is controlled by the probability to tunnel into the defect (T1), and the probability to tunnel out to the oxide conduction band (T2). The total tunneling current resulting from TAT is at its maximum when T1 = T2.

The increased leakage current leads to an increase in oxide wear-out rate and therefore a shorter lifetime. This effect reaches its maximum when the defect is located at a "sweet spot", $x(E_{OX})$, defined as:

$$x(E_{ox}) = W(E_{ox}) * [1 - \sqrt{2}/2] \quad (1)$$

where W is the total width of the FN barrier at the stress field E_{OX}. Thus, the lifetime reduction depends on the physical location of the "lucky defect" in the dielectric and the corresponding amount of gate leakage enhancement due to TAT. Hence the reduced lifetime in the presence of a "lucky defect":

$$T_{BD}^{*} = T_{BD} \bullet \left(\frac{J_{FN}}{J_{FN}+J_{TAT}}\right)\left(\frac{A}{A_{DF}}\right)^{\frac{1}{\beta}} \quad (2)$$

where J_{FN} is the FN component of the leakage, J_{TAT} the TAT component of the leakage, A the area of the device and A_{DF} the area of the "lucky defect" assumed to be ~1 nm^2 [5].

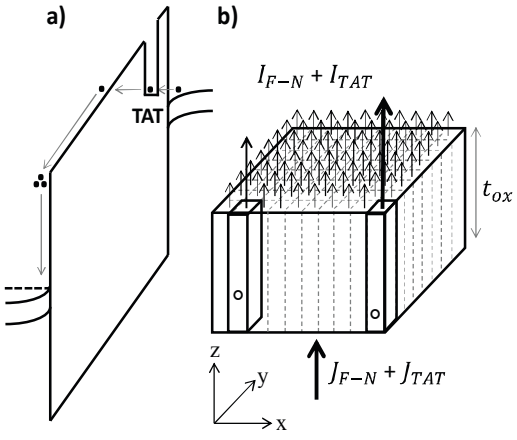

Fig. 3. Tunneling current in the presence of traps: a) traps at the "lucky energy" resulting in b) local increase in current.

Using this model, we examine the effect of different "lucky defects" profiles on the TDDB performance.

IV. MODEL IMPLICATIONS ON FAILURE DISTRIBUTIONS

The defect density of the oxide (10^8 cm^{-3}) and the different distributions considered are related to the oxide process and can be considered as a by-product of the SiO_2 oxide growth on SiC. To simplify the simulation, we assume all defects have the appropriate energy to enhance tunneling. Thus, we consider a wafer area of (2 cm x 2 cm) containing ten thousand DMOSFETs, each with the same area as the one used experimentally (200 µm x 200 µm) and the same 50 nm thick SiO_2 dielectric, as shown in fig. 4.

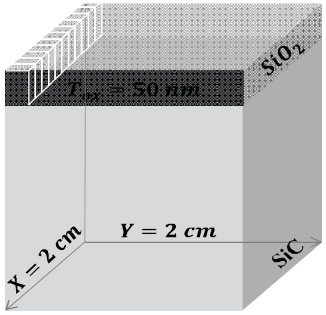

Fig. 4. Dimensions of DMOSFETS considered.

Fig. 5 shows a uniform distribution of "lucky defects" which would be similar to a uniform contamination during oxide growth.

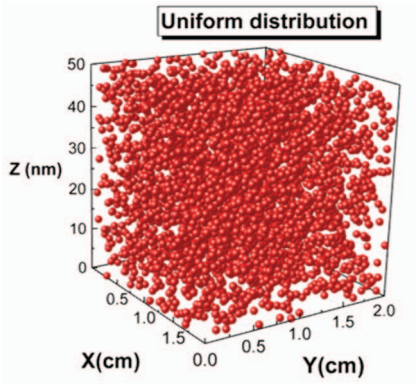

Fig. 5. Uniform lucky defect distribution with a density of defect of 10^8 cm^{-3}

As mentioned earlier, the most lifetime reduction is caused by defects that are at or close to a sweet-spot (Eq. 1), but the current enhancement decreases exponentially as the defect is placed further away from the sweet-spot (Eq. 2). Thus, for the uniform distribution of defect shown in fig. 5, only a small fraction of defects located closer to the SiO_2/SiC interface result in early fails. This is evident in fig. 6a where a tail of 1.18 % "extrinsic" fails is obtained. However, if we consider 50 randomly selected devices out of the distribution, which is a similar statistical sample to a usual wafer level TDDB test, we would not observe any early fails (fig. 6c). This early TDDB assessment would lead to conclusions that no further screening is needed. However, if we consider a sample size of 400 (fig. 6b) which is similar to high temperature operating life (HTOL) qualification tests at the package level, we would observe a few

outliers and an apparent inconsistency with the wafer-level data.

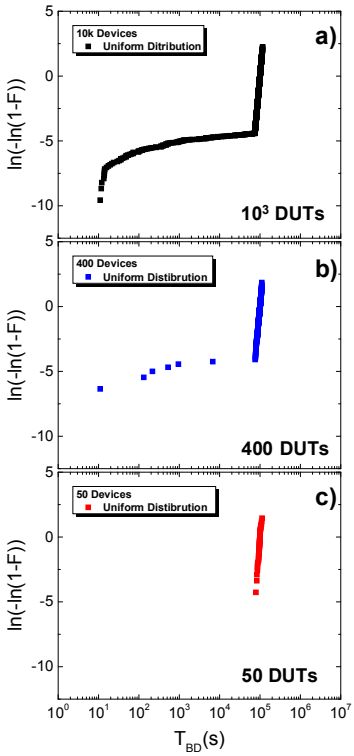

Fig. 6. Uniform distribution of lucky defects. a) shows the TDDB failure distribution of 10000 devices showing tails of early failures, b) shows the resulting TDDB distribution for 400 devices sample size which is similar to an HTOL stress, and c) shows the TDDB distribution with 50 devices sample size which is similar to a routine TDDB test at wafer level.

Fig. 7 shows a normal distribution of defects mostly contained within 10 nm of the interface. This distribution is often cited in the SiC literature as a few nanometers thick carbon rich transition layer has been observed at the SiO_2/SiC interface using electron microscopy [6,7].

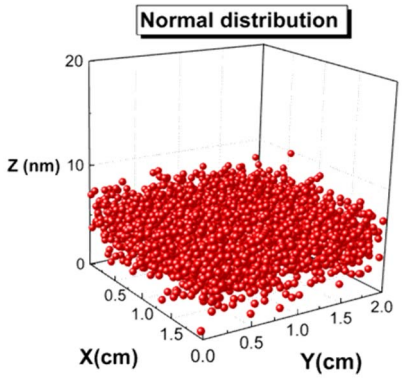

Fig. 7. Normal lucky defect distribution mostly contained within 10 nm of the interface with a density of defect of 10^8 cm^{-3}.

Similar to a uniform distribution, this defect profile only results in a 0.83 % tail which might not be captured during a wafer level test (fig. 8c).

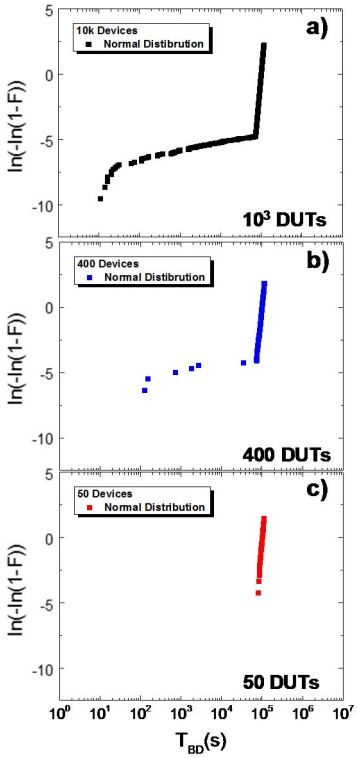

Fig. 8. Normal distribution of lucky defects mostly contained within 10 nm of the interface. a) shows the TDDB failure distribution of 10000 devices showing tails of early failures, b) shows the resulting TDDB distribution for 400 devices sample size which is similar to an HTOL stress, and c) shows the TDDB distribution with 50 devices sample size which is similar to a routine TDDB test at wafer level.

However, if we consider a narrower transition layer, only a nanometer from the interface (fig. 9), we see a large increase in early failures and the tail reaches 31.95 % of the population (fig. 10c). This tail is much higher than the 7.5 % tail that was observed experimentally (fig. 1).

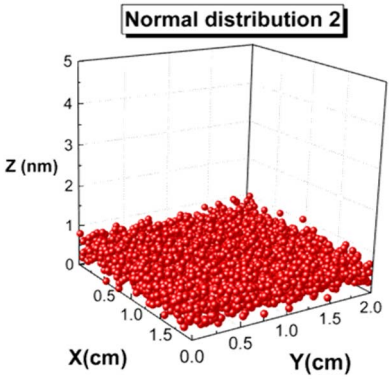

Fig. 9. Normal lucky defect distribution mostly contained within 1 nm with a density of defect of 10^8 cm^{-3}.

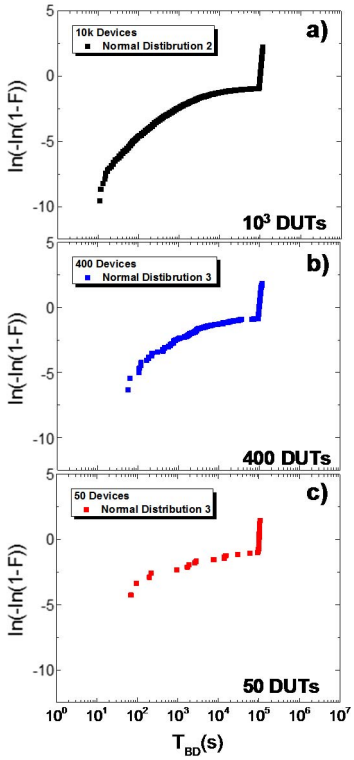

Fig. 10. Normal distribution of lucky defects mostly contained within 1 nm of the interface. a) shows the TDDB failure distribution of 10000 devices showing tails of early failures, b) shows the resulting TDDB distribution for 400 devices sample size which is similar to an HTOL stress, and c) shows the TDDB distribution with 50 devices sample size which is similar to a routine TDDB test at wafer level.

Finally, we consider an exponential distribution with the highest concentration closest to the interface (fig. 11). The resulting tail observed in (fig. 12a) is of 10.95 % which is similar to what was measured experimentally. This distribution is the most physically sound, since carbon related species are created as a byproduct of the thermal growth. At the initial phase of growth, the SiO_2 is thin enough that the carbon related species escape easily. However, as the oxide grows thicker, the carbon species cannot escape and lead to a larger concentration of defects closer to the interface.

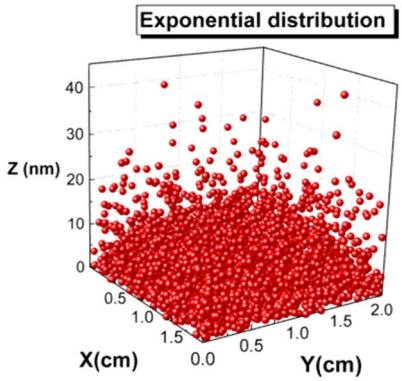

Fig. 11. Exponential lucky defect distribution with a density of defect of 10^8 cm^{-3}.

Fig. 12c shows that a 50 samples TDDB early assessment would lead to the conclusion that a moderate screening is a viable option since only 2-4 fails were observed. However, a screening criteria based on that test would not solve the early failure tail for the total population and fails would still be observed, even at HTOL.

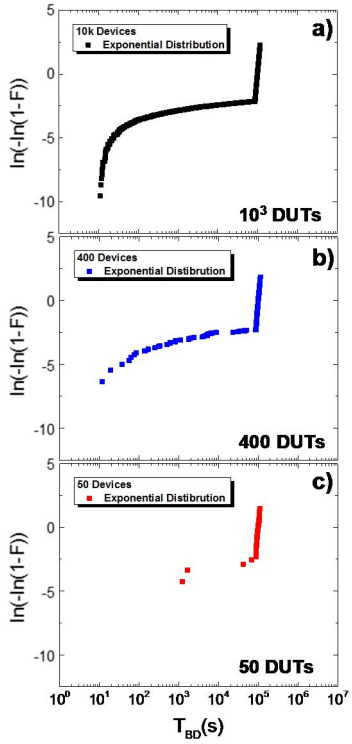

Fig. 12. Exponential distribution of lucky defects. a) shows the TDDB failure distribution of 10000 devices showing tails of early failures, b) shows the resulting TDDB distribution for 400 devices sample size which is similar to an HTOL stress, and c) shows the TDDB distribution with 50 devices sample size which is similar to a routine TDDB test at wafer level.

V. Conclusion

Despite the SiC community's efforts to improve contamination and processing, the products are still plagued with extrinsic-like fails. The observations reported here recommend a shift in focus from contamination control to oxide growth process improvements. Moreover, the simulations show that the sample size of the TDDB failure distributions is crucial to the TDDB assessment and the screening process can be destructive rendering the data meaningless.

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