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# Influence of Process Flow on the Characteristics of Strained-Si nMOSFETs

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We developed a process design that uses epitaxial growth of strained-Si layers after shallow trench isolation (STI) and well implantation to improve the drive current of n-type metal-oxide-semiconductor field effect transistors (nMOSFETs). Due to the significantly reduced thermal budget, we can minimize the degree of partial relaxation in strained-Si layers based on state-of-the-art MOSFET integration technique. Experimental results show that strained-Si devices fabricated by this flow exhibit enhanced saturated drive currents, up to 12% higher than that of strained-Si device with epitaxial growth of strained-Si layers before STI and well implantation.
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Methods of optimizing channel mobility need to be explored in order to overcome the limitations on the scaling down of devices and further improve the speed of complementary metal-oxide-semiconductor (CMOS) circuits. A promising candidate to reach this demand is to exploit the strain-induced band-structure modification. The use of a strained-Si channel for n-type metal-oxide-semiconductor field effect transistors (nMOSFETs)[1-3] has made great improvements on dc characteristics due to its potentially higher electron mobility. Enhanced carrier mobility using a tensile strained Si results principally from a reduction of the in-plane carrier effective mass and a reduction of intervalley scattering. Therefore, by fabricating MOSFET devices on the strained-Si layer, faster CMOS devices and performance enhancements are predicted without the high costs associated with aggressive geometric scaling. However, currently most studies[4-6] use a simplified standard MOS fabrication process based on reduced thermal budgets during the various processing steps to implement strained-Si nMOSFETs, particularly to avoid high-temperature shallow trench isolation (STI) commonly used in advanced integration processes, which leads to restriction in device implementation. Therefore, how to introduce the STI technology into strained-Si nMOSFET and make this flow useful for nanoscale transistors in advanced logic technologies are currently important issues. In this paper, strained-Si nMOSFETs prepared by process integration flows (selective growth of Si layer on SiGe virtual substrate post-STI and well implantation) has been fabricated. Compared to devices with epitaxial strained-Si layer before STI and well implantation, this process technology seems to efficiently reduce thermal budgets and provide an additional enhancement (up to 15%) in long-channel mobility. This additional increased mobility behavior is translated into a 12% higher on-state current for the long-channel devices and a 6% higher on-state current ($V_{GS} - V_{TH} = 1$ V and $V_{DS} = 1$ V) for devices down to 0.24 μm. Obviously, applying the modified STI technology flow to strained-Si nMOSFET fabricated is very suitable for state-of-the-art CMOS process.

## Experimental

The epitaxy structures investigated in this work were fabricated by a commercially available multi-wafer ultrahigh vacuum chemical vapor deposition (CVD) system on Si(100) 10–15 Ω cm substrate. Silane and germane were used as the Si and Ge precurors, respectively. The Si substrates were subjected to a precleaned process with HF-dip solution to reduce the accumulation of contamination by removing the surface native oxide and forming hydrogen passivated surface. After the precleaning step, the wafers were loaded into the loading chamber and then transferred to the reaction chamber for epitaxial growth. Structures first consist of a linearly graded $Si_{1-x}Ge_x$ buffers layers with the $x$ content increased from 0 to 20% over the thickness of 2 μm, followed by an undoped 1-μm-thick relaxed $Si_{0.8}Ge_{0.2}$ virtual substrate. The SiGe epitaxial layers were grown at 675°C. After that, same structure parameters with different process flows are adopted to identify the impact of high-temperature STI technology on the device characteristics. Herein, a 20 nm thick strained-Si layer was grown on relaxed $Si_{0.8}Ge_{0.2}$ virtual substrate. Then, the active areas were sequentially defined by the shallow trench isolation (STI), well implantation for the A sample. For the sample B, after STI and well implantation, selective epitaxy of strained-Si layer was then grown on the virtual substrate. The STI process included linear oxide deposition (920°C, 20 s), linear oxide postannealing (990°C, 30 min) and high density plasma (HDP)-CVD oxide rapid thermal annealing (RTA) (1000°C, 20 s). The p-well formation was implanted with $5 \times 10^{13}$ atoms/cm$^2$ boron and well-implant annealing was done at 1000°C for 12 s. Figure 1 shows the schematic diagram of different process flow sequences.

After that, all samples, including a Si control, were processed to produce nMOSFETs using the same Si CMOS process flow for comparison. Gate oxide of 2.2 nm was formed by wet, atmospheric pressure oxidation at 800°C for 30 min to minimize interdiffusion of the as-grown layer structure. Afterward, poly-Si gate was deposited and etched. This was followed by source/drain extensions and halos implants, spacer formation. After the gate spacer etching, a thin Si layer was grown in the source/drain region by a selective epitaxy growth process to reduce the contact resistance. After source/drain rapid thermal annealing (RTA) at 1050°C for 6 s was used to activate the implantations. Co silicides were formed in successive rapid thermal anneals at 480°C for 35 s and 830°C for 25 s. The other procedures were based on standard backend process.

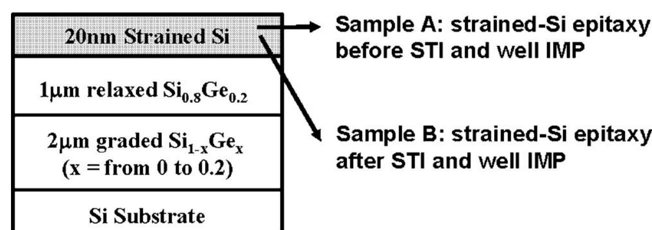


**Figure 1.** The schematic diagram of the strained-Si transistors process sequences.

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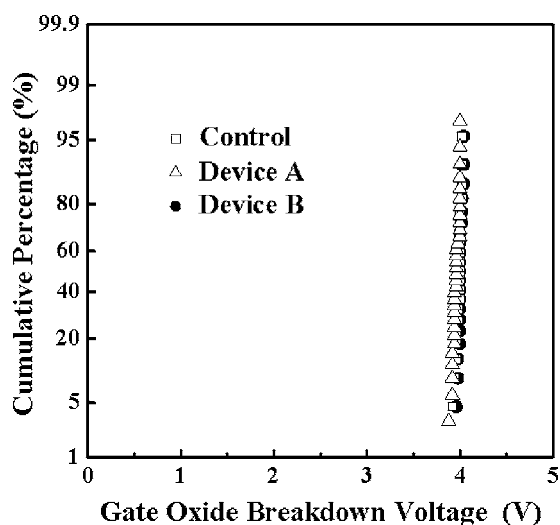


**Figure 2.** Comparison of the nMOSFETs gate oxide breakdown voltage distribution in strained-Si and Si control.

### Results and Discussion

It is noted that the high-temperature thermal processing not only enhanced Ge up-diffusion into the Si[6] but also induced partially strained-Si relaxation,[7] which are responsible for the mobility degradation. Ge up-diffusion becomes severe when strained-Si layer is less than 10 nm.[8] This is attributed to that at high-temperature process Ge from the underlying SiGe diffuse up into the strained-Si channel and segregated at the strained-Si/oxide interface. Consequently, it will lead to an increased fixed oxide charge and high trap density at $SiO_2$/Si interface, which result in a reduced gate-oxide breakdown voltage. However, strained-Si layer chosen at 20 nm thickness in our devices is enough immunity against Ge out-diffusion to gate oxide and is confirmed by comparable oxide breakdown voltage distribution (Fig. 2). Therefore, the effect of the Ge up-diffusion can be neglected in these devices.

The output current-voltage characteristics of strained-Si nMOSFET with the STI process are shown in Fig. 3. Evidently, both strained-Si nMOSFETs exhibit larger enhancement in driving current at a given degree of gate overdrive, which are responsible for the "high mobility" of the stained-Si channel (Fig. 4). Moreover, as compared to device A with pre-STI and well implantation, device B provides an effective enhancement in driving current of 12% for the long-channel length ($L = 10\ \mu m$) and of 6 % for the channel length down to 0.24 μm, at the same gate overdrive ($V_{gs} - V_{th} = 1$ V). We believe that such an improvement in device performance is attributed to the elimination of the effects of high-temperature STI process and well implantation on sample B. On the other hand, 15% degradation of channel mobility in sample A, as experimentally observed in Fig. 4, revealed that the strained-Si layer undergoes the additional high-temperature STI and well implantation process which leads to a decreased stress level in the Si cap layer. Consequently, an increase in the degree of strained-Si relaxation is accompanied by more misfit and threading dislocations formation which not only reduced the carrier mobility by scattering but also caused an increase in the leakage currents, as mentioned by the previous report.[7] Moreover, inefficient strain-induced energy band splitting also degrades mobility enhancement.

To further investigate the influence of different STI process sequences in this paper on the electrical characteristics of the strained-Si device, the threshold voltage ($V_{TH}$) roll-off as a function of gate length for the strained-Si with gate width of 10 μm is shown in Fig. 5. Noted that the $V_{TH}$ roll-off characteristics for sample B is compared to Si control. However, observed a lower $V_{TH}$ and sharper roll-off curve in sample A, especially at such wider gate width,

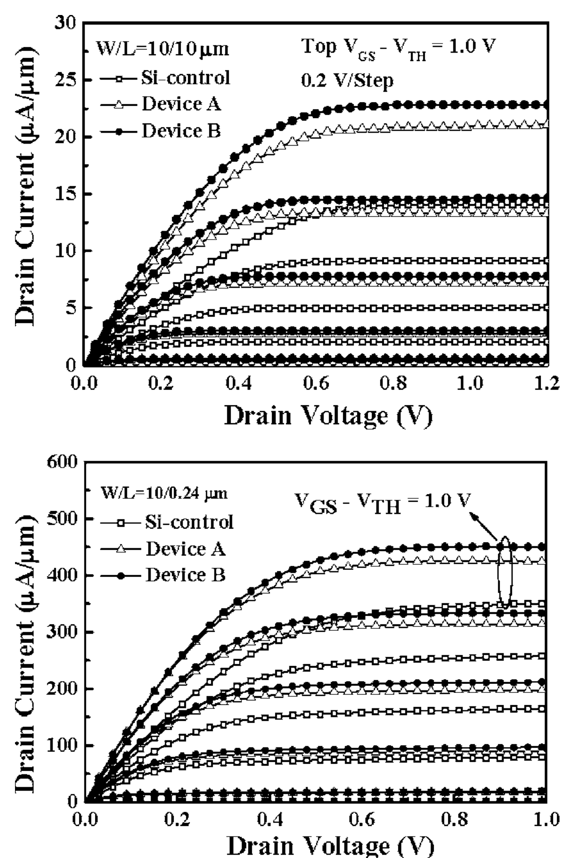


**Figure 3.** $I_{DS}$-$V_{DS}$ characteristics of the fabricated strained-Si and Si control devices with channel lengths of (a) 10 μm and (b) 0.24 μm, respectively.

indicates that the post-STI induces partial relaxation of strained-Si layers, resulting in more misfit dislocations between source and drain, which serve as a rapid diffusion path. Therefore, the more localized diffusion along these misfit dislocations cores is responsible for the larger leakage current mechanism for sample A.

### Conclusion

Strained-Si nMOSFET structures prepared by different STI process were fabricated. By appropriately modifying the STI process

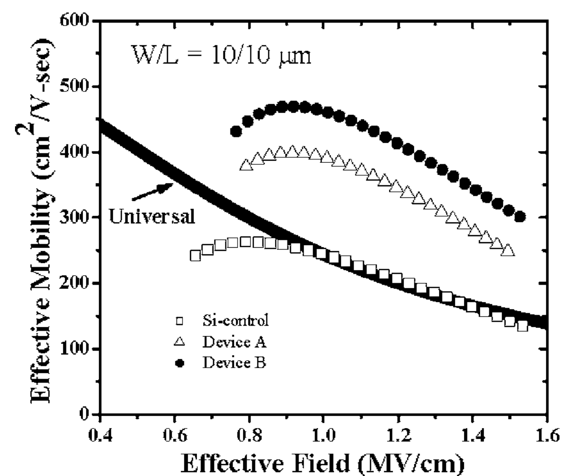


**Figure 4.** Effective mobility for strained-Si nMOSFETs as a function of effective field.

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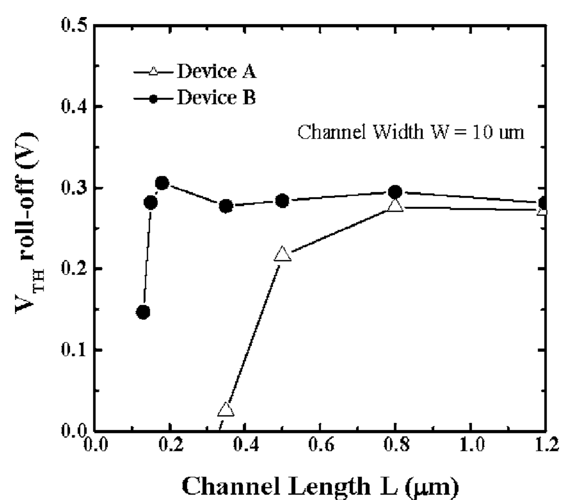


**Figure 5.** Threshold voltage as a function of gate length for the strained-Si with gate width of 10 μm.

sequences, the significant drive current and mobility enhancement has been obtained. Improved characteristics in sample B indicate that devices with new process sequences exhibit the controlled misfit dislocations in strained-Si layers and show a great flexibility for developing high-performance strained-Si CMOS.

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