Influence of the channel width on the threshold voltage modulation in MOSFETs

INFLUENCE OF THE CHANNEL WIDTH ON THE THRESHOLD VOLTAGE MODULATION IN M.O.S.F.E.T.S

Indexing term. Field-effect transistors

The threshold voltage of an m.o.s. field-effect transistor is modulated by the source-to-substrate reverse bias. In the letter. the theory for long- and short-channel transistors is extended to include the influence of the channel width. The result is an analytical expression for the threshold voltage as a function of geometry and bias that agrees well with experimental data.

The substrate doping under the gate of an m.o.s. transistor may be experimentally determined from measurements of the threshold voltage modulation due to the substrate bias. By plotting the threshold voltage shift with applied bias V_{BG} against $\sqrt{(V_{BG}+2\phi_F)}-\sqrt{(2\phi_F)}$, where ϕ_F is the bulk Fermi level, the substrate doping may be determined from the slope of the straight line.[1,2] However, this only applies if the channel length and channel width are much larger than the depth of the depletion layer under the gate. Several authors[3-6] have presented theories for short-channel transistors using simple geometrical approximations. In this letter, the influence of the channel width on the threshold voltage is also shown to be of great importance.

The straight-line theory presented in the introduction is a long-channel theory, because it neglects the influence of the source and drain. In a short-channel device, a large fraction of the field lines from the bulk charge under the gate will be terminated on the source and drain, giving less threshold voltage modulation. Cheney and Kotch[3] were the first to modify the theory to fit short-channel devices, but only for large substrate biases. Varschney[4] and Yau[5] extended the theory to low substrate biases by using two simple, 2-dimensional approximations in conjunction with a charge-conservation analysis to explain the influence of the channel length.

The most extensive work on short-channel devices has been done by Lee.[6] He refined the model of Cheney and Kotch, and, from a piecewise 1-dimensional analysis, he obtained a closed-form expression, which, however, is rather complicated (Reference 6, eqns. 14*a–e*). It will be shown here that this expression may be simplified if some of the simplifying assumptions used by Varschney and Yau are used. If the influence of the drain bias is neglected and if the built-in potential of the source and drain junctions is assumed to be $2\phi_F$, Lee's expression for the threshold voltage modulation ΔV_T may be reduced to

$$\Delta V_{T\,short} = \frac{qN}{C_{ox}}\left[\left(1-\frac{2\xi r}{L}\right)(x_n-x_{n0})+\frac{2\xi r^2}{L}\ln\left(\frac{r+x_n}{r+x_{n0}}\right)\right] \quad . \quad . \quad . \quad (1)$$

where

q = electronic charge

N = substrate doping

C_{ox} = oxide capacitance per unit area

r = source and drain diffusion depth

L = channel length

x_n, x_{n0} = depletion depth with and without applied substrate bias

ξ = weighting factor ($\simeq 1$)

For depletion depths $x_n < r/2$, this expression (with $\xi = 1$), as well as that of Yau, may be reduced by series expansion to that of Varschney. In this region all three theories agree well with experimental data. For $r/2 < x_n < L/2\xi$, Lee's theory agrees much better with experiment than the other two, which makes the simplified expression in eqn. 1 very useful. Now, when a useful expression for the influence of the channel length is found, the theory may be extended to include the influence of the channel width. As will be seen later in this letter, the channel width has an important influence on the threshold voltage modulation.

So far, it has been assumed that the width of the depletion layer is the same as the channel width. This assumption is good for wide transistors, but not for narrow ones. Since the gate oxide is very thin compared with the depletion layer, this layer will extend outside the metal gate.[7] This can be seen in Fig. 1, where the depletion layer is shown looking from the source towards the drain. In *a* the circular approximation of Copeland[8] is shown and *b* shows a linearised approximation similar to that of Lee. From Fig. 1 it may be seen that the threshold voltage must be adjusted, owing to the extra charge Q outside the metal gate. To the threshold voltage shift must be added a term $\Delta Q/C_{ox}$ that roughly equals

$$\frac{qN}{C_{ox}}\frac{\delta}{W}(x_n^2-x_{n0}^2)$$

where W is the channel width and δ is a width weighting factor. Copeland's approximation gives $\delta = 1{\cdot}5$, but δ may also be

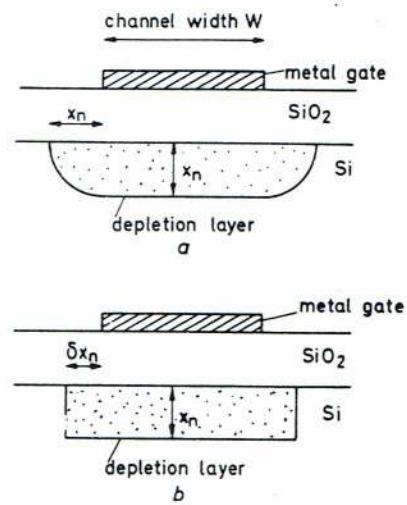

Fig. 1 *Width effect*
A cross-section of an m.o.s. transistor is shown looking from the source towards the drain. The depletion layer is shown to extend outside the gatewidth with two different approximations

affected by the substrate doping and by charges in the oxide.

If the piecewise linear approximation of Lee is extended in more detail to include the channel-width effect, a useful expression for the threshold voltage modulation may be obtained. This is done in the Appendix and gives

$$\Delta V_T = \frac{qN}{C_{ox}}\left[\left(1-\frac{2\xi r}{L}\right)(x_n-x_{n0})+\frac{2\xi r^2}{L}\ln\left(\frac{r+x_n}{r+x_{n0}}\right)\right.$$

$$+\frac{\delta}{W}(x_n^2-x_{n0}^2)+\frac{4\delta\xi r}{LW}\left[r(x_n-x_{n0})\right.$$

$$\left.\left.-\left(\frac{x_n^2}{2}-\frac{x_{n0}^2}{2}\right)-r^2\ln\left(\frac{r+x_n}{r+x_{n0}}\right)\right]\right] \quad . \quad . \quad . \quad (2)$$

For small depletion depths $x_n < r/2$ this equation may be reduced by series expansion to

$$\Delta V_T = \frac{qN}{C_{ox}}\left[x_n-x_{n0}+\left(\frac{\delta}{W}-\frac{\xi}{L}\right)(x_n^2-x_{n0}^2)\right] \quad (3)$$

However, in this letter, the complete expression in eqn. 2 will be used, since it gives the best approximation in the range $x_n < L/2\xi$.

For experimental verification of this extended threshold-voltage-modulation theory, a series of test transistors with different channel widths and lengths were used. These devices were adjacent to each other on a test chip. The source and drain diffusion depths for all devices were 3 μm. Measurements were done with a drain voltage of 100 mV, using the

device in the nonsaturated region. At such a small bias, the drain-current/gate-voltage curve shows a region of constant slope. The threshold voltage is usually defined as the gate voltage obtained if this region is extrapolated to zero current. However, the shift of the threshold voltage with substrate bias may be easily determined from only one measurement. It may be taken as the shift of the gate voltage needed to give a certain constant current in this region of constant slope. First, the substrate doping was obtained from measurements on a large device with a channel width by channel length of 50×50 μm. The effect of a short channel length was then obtained from measurements on a $400 \times 4{\cdot}1$ μm device. The $\xi = 1$ was used, since it gives the best agreement with the theories of Varschney and Yau. Measurements on a device with the same channel length, but with a channel width of only 10 μm, show the predicted influence of a narrow channel. The experimental data were fitted with the theoretical expression given in eqn. 2, using $\delta = 1{\cdot}2$. Additional tests of the theory were obtained from measurements on $10 \times 2{\cdot}9$ μm and $10 \times 1{\cdot}6$ μm devices. The results are shown in Fig. 2 and show excellent agreement between theory and experiments.

In conclusion, it has been shown that the threshold voltage modulation of an m.o.s.f.e.t. is affected not only by the channel length of the transistor, but also by its channel width. The influence of the channel width is determined in this letter and the theory is extended to include devices with arbitrary channel dimensions.

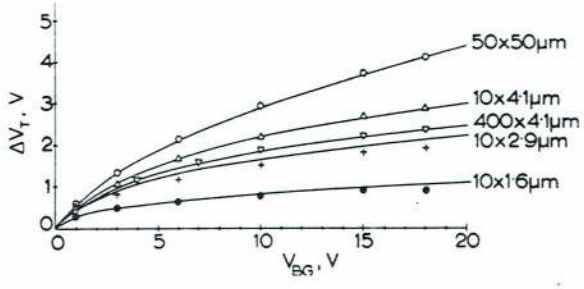

Fig. 2 *Results of measurements of threshold voltage modulation with bias on devices with different channel widths and channel lengths*

The channel dimensions are given as channel widtn × channel length. Theory is shown as solid lines and experimental data are given by symbols: ○ 50×50 μm, ▽ $400 \times 4{\cdot}1$ μm, △ $10 \times 4{\cdot}1$ μm, + $10 \times 2{\cdot}9$ μm, ● $10 \times 1{\cdot}6$ μm
$\xi = 1{\cdot}0$, $\delta = 1{\cdot}2$

Appendix: According to Lee, the total charge in the channel depletion region may be written as

$$Q_{Si} = \int_{area} \int \int_{\Psi_1}^{\Psi_2} C_{Si}(x_n)\, d\Psi\, dA$$

where A = area = effective gate area, Ψ_1, Ψ_2 = potential in the silicon in the bulk and at the surface, respectively, and $C_{Si}(x)$ = depletion-layer capacitance per unit area as a function of depletion depth x_n. The threshold voltage modulation may then be written as

$$\Delta V_T = \frac{\Delta Q_{Si}}{C_{ox} - LW}$$

Analysing the expression for Q_{Si} in detail, using the piecewise linear approximation of Lee and integrating over an effective depletion area $L(W + 2\delta x_n)$, gives

$$Q_{Si} = \int_0^{\xi x_n} \int_{-\delta x_n}^{W+\delta x_n} \int_0^{V+2\phi_F} \frac{\varepsilon_{Si}}{r + x_n}\, dx\, dy\, d\Psi + \int_{\xi x_n}^{L-\xi x_n} \int_{-\delta x_n}^{W+\delta x_n} \int_0^{V+2\phi_F} \frac{\varepsilon_{Si}}{x_n}\, dx\, dy\, d\Psi - \int_{L-\xi x_n}^{L} \int_{-\delta x_n}^{W+\delta x_n} \int_0^{V+2\phi_F} \frac{\varepsilon_{Si}}{r + x_n}\, dx\, dy\, d\Psi$$

$$= Q_{SiLee} + \int_0^{V+2\phi} \frac{\xi x_n\, 2\delta x_n\, 2\varepsilon_{Si}}{r + x_n}\, d\Psi + \int_0^{V+2\phi} \frac{(L - 2\xi x_n)\, 2\delta x_n}{x_n}\, d\Psi$$

where Q_{SiLee} is the simplified expression obtained from Lee and the two last integrals are due to the channel-width effect and extend the theory of Lee. Using

$$x_n = \sqrt{\left\{\frac{2\varepsilon_{Si}}{qN}(V + 2\phi_F)\right\}}$$

the first integral is found to be

$$Q_1 = 4qN\xi\delta\left[\frac{x_n^3}{3} - \frac{x_{n0}^3}{3} - r\left[\left(\frac{x_n^2}{2} - \frac{x_{n0}^2}{2}\right) - r(x_n - x_{n0}) + r^2 \ln\left(\frac{r + x_n}{r + x_{n0}}\right)\right]\right]$$

and the second integral is

$$Q_2 = 2qN\delta\left[L\left(\frac{x_n^2}{2} - \frac{x_{n0}^2}{2}\right) - 2\xi\left(\frac{x_n^3}{3} - \frac{x_{n0}^3}{3}\right)\right]$$

Inserting into eqn. 2 gives the extra contribution to the threshold voltage modulation due to the limited channel width as written in eqn. 1.

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References

1 CRAWFORD, R. H.: 'MOSFET in circuit design' (McGraw-Hill, 1967), pp. 40–45
2 AKIRA WADA: 'Estimation of the impurity redistribution in silicon substrates from MOSFET characteristics', *IEEE Trans.*, 1973, **20**, pp. 602–603
3 CHENEY, G. T., and KOTCH, R. A.: 'A simple theory for threshold voltage modulation in IGFET's', *Proc. Inst, Elec. Electron. Eng.*, 1968, **56**, pp. 887–888
4 VARSCHNEY, R. C.: 'Simple theory for threshold voltage modulation in short-channel m.o.s. transistor', *Electron. Lett.*, 1973, **9**, pp. 600–602
5 YAU, L. D.: 'A simple theory to predict the threshold voltage of short-channel IGFET's', *Solid-State Electron.*, 1974, **17**, pp. 1059–1063
6 LEE, H. S.: 'An analysis of the threshold voltage for short-channel IGFET's', *ibid.*, 1973, **16**, pp. 1407–1417
7 WASSERSTROM, E., and MCKENNA, J.: 'The potential due to a charged metallic strip on a semiconductor surface', *Bell Syst. Tech. J.*, 1970, **49**, pp. 853–877
8 COPELAND, A. J.: 'Diode edge effect on doping profile measurements', *IEEE Trans.*, 1970, **17**, pp. 404–407