InGaAs FinFET Modeling Using Industry Standard Compact Model BSIM-CMG

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ABSTRACT

In this paper, we present modeling results for InGaAs FinFETs using the industry standard compact model BSIM-CMG. We show that BSIM-CMG produces excellent fits to the measured I-V data of these devices. The difference seen in carrier mobility behavior of InGaAs FinFETs compared to silicon devices can be accounted for in the model. Furthermore, the calibrated model is used for performance projection in these devices. It is found that parasitic resistance and mobility reduction with vertical field limit the performance of these devices.

Keywords: InGaAs FinFETs, Compact Models, BSIM-CMG

1 INTRODUCTION

InGaAs-based FinFETs are seen as very promising devices for future generation CMOS technologies [1]. InGaAs offers higher carrier mobility whereas the multi-gate structure of FinFET offers better electrostatic control of the channel charge and hence better short-channel behavior. Experimental demonstrations of these devices showing increasingly improved performances are being made [1-3]. With the device level performance looking promising, circuit design with these devices will soon commence. Optimized circuit design and simulation with these devices need accurate and robust compact model. BSIM models [4] are extensively used in the semiconductor industry today for silicon-based devices. Among the BSIM family of models [4], BSIM-CMG [5] is a recently accepted industry standard model for multi-gate silicon devices. Here, we show that BSIM-CMG produces excellent results for InGaAs-based FinFETs also. To the best of the authors' knowledge this is the first time a compact model with excellent agreement to the experimental data for InGaAs FinFETs is presented. We found that the behavior of carrier mobility in InGaAs FinFETs is quite different from silicon devices and BSIM-CMG can be adjusted to account for this difference. Moreover, the calibrated model serves as a useful tool to analyze the physical phenomena which limit the performance of InGaAs FinFETs and compare it with better understood silicon devices. In addition, we use our model to project the performance which can be expected from these devices as this technology matures.

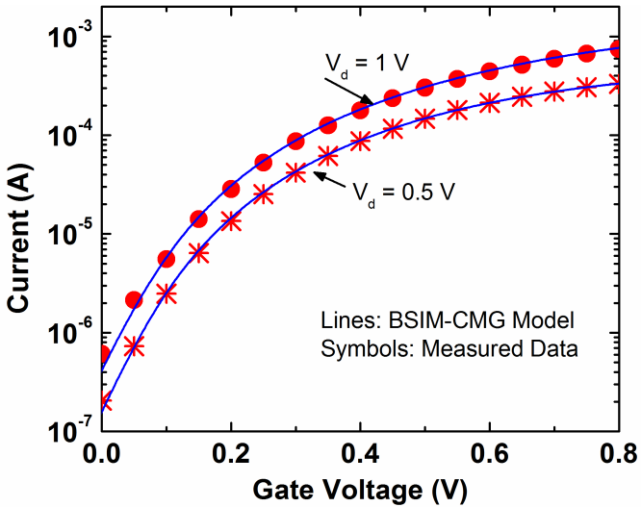

Fig. 1. Transfer characteristics of InGaAs FinFET modeled with BSIM-CMG model in semi-log scale showing the sub-threshold current model. L = 20 nm, H = 30 nm, W = 20 nm and N_f = 4.

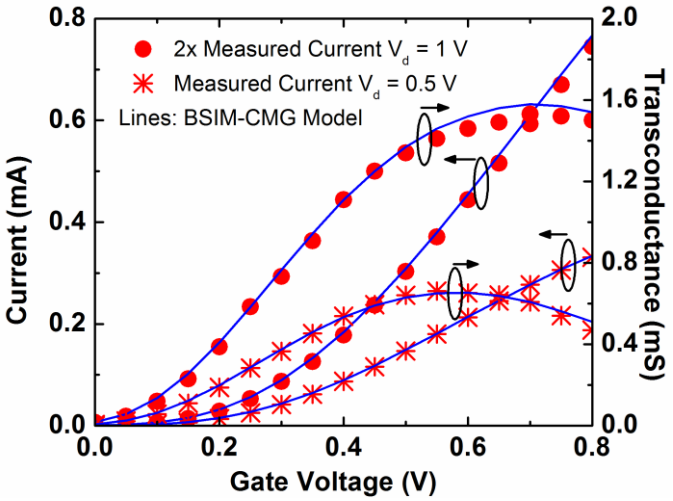

Fig. 2. Transfer characteristics of InGaAs FinFET modeled with BSIM-CMG model. Current for V_d = 1 V is doubled in the plot for better visibility. L = 20 nm, H = 30 nm, W = 20 nm and N_f = 4.

This paper is arranged as follows. In Section II, we briefly describe the important features of the BSIM-CMG

model which are pertinent to this work. In Section III, we present the model results by comparing it with experimental data. An analysis on device trans-conductance along-with a projection for its expected improvement is also presented in this section.

2 MODEL DESCRIPTION

BSIM-CMG is an industry standard surface-potential-based compact model for various flavors of multi-gate devices. The model consists of two important parts: 1) Core calculations, where device electrostatics is solved and the surface-potential is calculated. The surface-potential calculation depends on important parameters like band-gap, density of states etc. These material specific parameters have been set to appropriate values for simulation of InGaAs devices for this work. 2) Second part consist of the models for plethora of real device effects. These effects include: mobility-field dependence, series resistance, current saturation, channel-length modulation, drain-induced barrier lowering etc. The parameters introduced in real device effects model are extracted from experimental data and their values are indicative of the magnitude of the corresponding physical effect. The models of the real device effects are a very big part of a complete compact model. The real device effects models are especially important in advanced technology nodes as the devices suffer from extrinsic effects more and more in these nodes. More details about BSIM-CMG model can be found in [5]. The model results for InGaAs FinFETs are shown in the next section demonstrating that BSIM-CMG can account for important differences seen in InGaAs FinFETs as compared to the silicon devices.

3 RESULTS AND DISCUSSIONS

We present the modeling results for InGaAs FinFETs described in [2] with gate-length L = 20 nm, number of fins N_f = 4, fin-width W = 20 nm and fin-height H = 30 nm. The model results for transfer characteristics at drain voltage V_d = 0.5 V and V_d = 1 V are shown in Fig. 1 and Fig. 2. These figures show excellent model agreement with measured data. In Fig. 1, current is shown in log-scale to highlight the modeling of the sub-threshold region. It is clear that BSIM-CMG provides excellent fits to the measured data in this region with an accurate prediction of the sub-threshold slope.

In Fig. 2 we show the modeling of the current and trans-conductance (g_m) of the device in linear scale. It is important here to note that the parasitic resistances at the source (R_s) and at the drain (R_d) should be set prior to the extraction of mobility related parameters from transfer characteristics. We use the method described in [6] to extract the values of R_s and R_d. Mobility degradation effect (MDE) which is the consequence of various

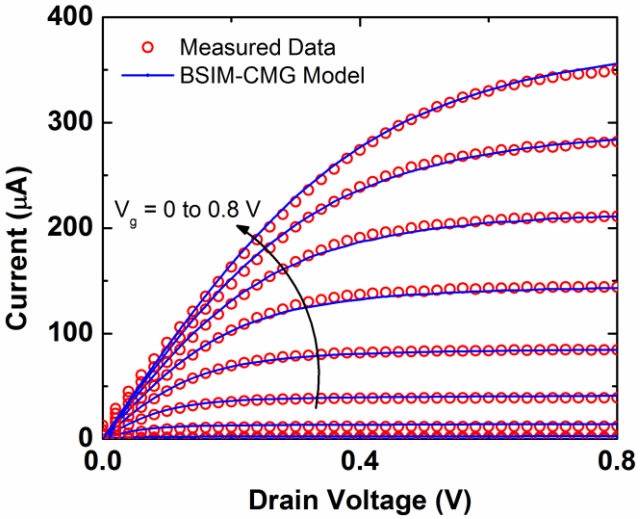

Fig. 3. Output characteristics of InGaAs FinFETs modeled with BSIM-CMG model. L = 20 nm, H = 30 nm, W = 20 nm and N_f = 4.

scattering mechanisms in the channel is found to be significantly larger in InGaAs FinFETs as compared to silicon devices. Excellent fits to the trans-conductance data in Fig. 2 shows that the mobility degradation effect is modeled very well. BSIM-CMG can handle significantly different MDE in InGaAs as compared to silicon devices via its MDE model which is given by,

$$\mu_{eff} = \frac{\mu_0}{1 + UA\left(E_{eff}\right)^{EU} + UD\left(\frac{1}{2}\left(1 + q_{ia}C_{ox}\right)\right)^{-UCS}} \quad (1)$$

where μ_0 is the low-field mobility, E_{eff} is the vertical electric field, q_{ia} is the normalized average inversion charge, C_{ox} is the oxide capacitance. UA, UD, UCS and EU are model parameters which are extracted from measurement data. (1) is derived using Matthiessen's rule,

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{ph}} \quad (2)$$

where μ_{sr} is the surface-roughness limited mobility and μ_{ph} is the phonon-scattering limited mobility. BSIM-CMG model parameter UA is indicative of the mobility limitation by surface roughness with a larger value corresponding to a smaller μ_{sr}. We found that for the InGaAs FinFETs the effective mobility is limited by the surface roughness mobility. The value of UA parameter obtained after fitting the full set of device characteristics for InGaAs FinFETs is around 8, which is considerably larger as compared to the values seen in case of silicon devices. This clearly indicates severe penalty in effective mobility at high vertical fields due to the surface roughness. Other authors have also reported similar findings about mobility of InGaAs FinFETs [7]. The main reason for the large degradation of

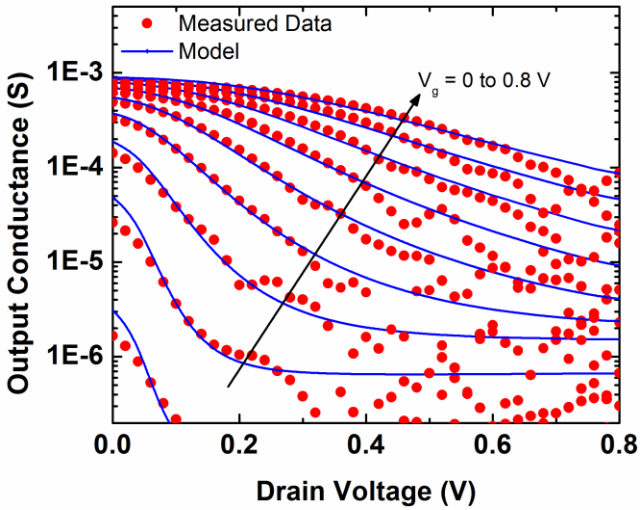

Fig. 4. Output conductance of InGaAs FinFET modeled with BSIM-CMG model. L = 20 nm, H = 30 nm, W = 20 nm and N_f = 4.

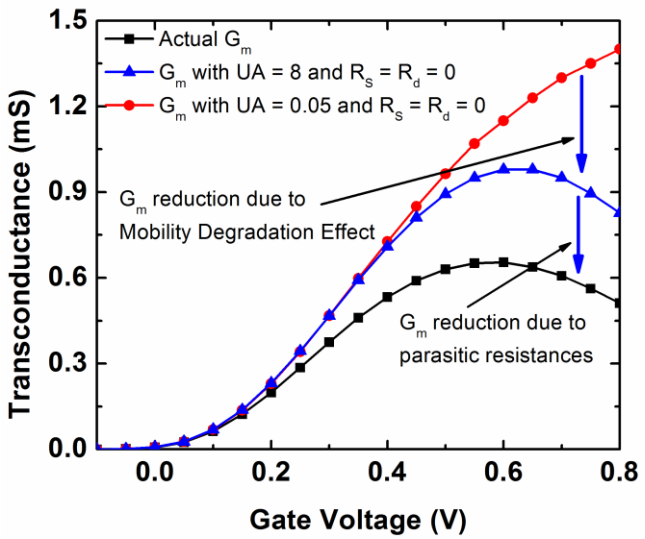

Fig. 5. Impact of mobility degradation effect and series resistance on trans-conductance of InGaAs device. UA = 0.05 is used in BSIM-CMG model to simulate MDE as seen in silicon FinFETs. UA = 8 is found for the InGaAs FinFETs in this paper. L = 20 nm, H = 30 nm, W = 20 nm and N_f = 4.

mobility is the higher surface-roughness scattering due to the poor interface quality between channel and the dielectric in these devices.

Next, we show the output characteristics of InGaAs FinFETs in Fig. 3, which demonstrate good correlation between BSIM-CMG model and experimental data. Current saturation is accounted properly by using the VSAT parameter in BSIM-CMG model. This again shows that BSIM-CMG model can be clearly adjusted via its parameters to model devices with significantly different carrier behavior as compared to silicon devices. Along with the current, output conductance (g_d) is also very important to model, especially for analog circuits, and BSIM-CMG produces excellent results for g_d as shown in Fig. 4.

We use the model to project the future performance which can be expected from these devices. We found that in addition to the parasitic resistances (R_s and R_d), surface roughness mobility degradation effect limits the device performance. The actual trans-conductance of the device is compared with a device where mobility degradation effect is reduced to the levels seen in silicon devices in Fig. 5. It can be seen that the peak-g_m can be improved by approximately 40% if surface roughness mobility degradation effect in these devices can be reduced to levels seen in silicon FinFETs with UA parameter values around 0.05. In Fig. 5 we also show g_m when the parasitic resistances are set to zero g_m further improves by 40%. Hence both parasitic resistances and surface roughness mobility degradation effects severely limit the device performance of InGaAs FinFETs.

As InGaAs FinFET technology advances, L and dielectric thickness T_{ox} will be scaled further. We analyze the variation of g_m as L and T_{ox} are scaled in Fig. 6. We found that if MDE remains the same, reducing T_{ox} will decrease gm since it increases vertical electric field. A

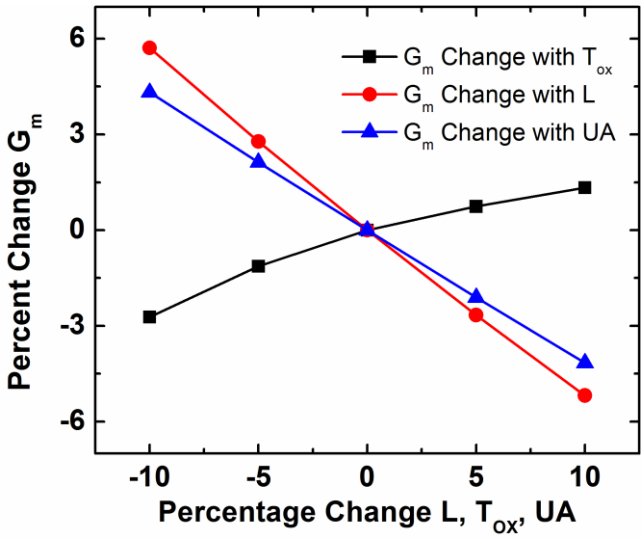

Fig. 6. Percentage change in g_m as technology parameters L and T_{ox} are scaled. MDE parameter UA produces similar changes in g_m as L indicating the significance of MDE in these devices.

reduction in L produces expected rise in g_m, however, it is interesting to see that a reduction in MDE effect (simulated via UA parameter) produces similar increment in g_m as the decrease in L. This underlines the importance of reducing MDE to achieve improved performances from InGaAs FinFETs. MDE as discussed earlier originates from surface-roughness scattering and technology solution to improve the di-electric channel interface will improve device performance considerably.

4 CONCLUSIONS

We show that the industry standard BSIM-CMG model produces excellent modeling results for InGaAs-based FinFETs and can be used for circuit-design with these devices. BSIM-CMG model parameters can be adjusted to account for the differences seen in InGaAs-based devices as compared to silicon devices. Further, extracted model parameter values indicate the strength of particular physical effects and are used for performance projection of these devices. It is found that along- with parasitic resistances, mobility degradation effect is very severe in InGaAs based FinFETs and improving MDE can improve the device trans-conductance substantially.

5 ACKNOWLEDGEMENTS

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