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InGaAs tunnel diodes for the calibration of semi-classical and quantum mechanical band-to-band tunneling models

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Promising predictions are made for III-V tunnel-field-effect transistor (FET), but there is still uncertainty on the parameters used in the band-to-band tunneling models. Therefore, two simulators are calibrated in this paper; the first one uses a semi-classical tunneling model based on Kane's formalism, and the second one is a quantum mechanical simulator implemented with an envelope function formalism. The calibration is done for $In_{0.53}Ga_{0.47}As$ using several p+/intrinsic/n+ diodes with different intrinsic region thicknesses. The dopant profile is determined by SIMS and capacitance-voltage measurements. Error bars are used based on statistical and systematic uncertainties in the measurement techniques. The obtained parameters are in close agreement with theoretically predicted values and validate the semi-classical and quantum mechanical models. Finally, the models are applied to predict the input characteristics of $In_{0.53}Ga_{0.47}As$ n- and p-lineTFET, with the n-lineTFET showing competitive performance compared to MOSFET. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4875535]

I. INTRODUCTION

The Tunnel Field-Effect Transistor (TFET) is a promising candidate for future low-power logic applications because of its steep turn-on capabilities. To be competitive with MOSFET, the Band-To-Band Tunneling (BTBT) rate determining the on-current must be sufficiently high. Semi-classical[1–4] and Quantum Mechanical (QM)[5–11] simulations predict that direct bandgap III-V compounds can provide these high BTBT rates. However, there is still uncertainty on the input parameters used in the BTBT models, and hence on the resulting III-V TFET performance predictions. Likewise, BTBT leakage predictions in MOSFET[12] suffer from the same uncertainty. The focus of our paper is the verification of these models and the calibration of their parameters.

Most semi-classical simulators implement the formalism by Keldysh and Kane.[13] In the uniform field limit, the BTBT rate for direct bandgap materials is given by

$$G_{\mathrm{BTBT}} = A_{\mathrm{BTBT}} \left(\frac{E}{E_0}\right)^2 \exp\left(\frac{-B_{\mathrm{BTBT}}}{E}\right), \qquad (1)$$

where E is the electric field, $E_0 = 1$ V/cm, and A_{BTBT} and B_{BTBT} are material-dependent input parameters.

Multiband QM simulators are often based on the Non-Equilibrium Green's Function formalism, combined with either a tight-binding[6–8] or a $\mathbf{k}\cdot\mathbf{p}$ (Refs. 5 and 11) basis set, the latter being computationally less demanding.[11] Others take a wavefunction approach, based on the $\mathbf{k}\cdot\mathbf{p}$ envelope function formalism.[14–17] Our paper focuses on the latter with a two-band model implementation. The input parameter is an interband momentum matrix element which indicates the coupling between the different bands.

In the past, researchers have proceeded to the calibration using highly doped p-n junctions[18] or complete TFET.[2,19,20] However, in highly doped p-n junctions, the tunneling is strongly affected by dopant induced bandgap narrowing (BGN).[21] Furthermore, the electrostatic potential is highly sensitive to the dopant concentration at the tunnel junction, and it is not possible to verify this potential with Capacitance-Voltage (C-V) measurements due to high conductive leakage. In a TFET, the potential profile is two dimensional and therefore more complicated to model accurately. Quantum confinement effects cannot be captured by semi-classical simulators,[19] and large devices cannot be modeled by atomistic simulators due to computational requirements.[20] Since BTBT is highly sensitive to the bandgap and the potential profile, these devices are not well suited for accurate calibration of the BTBT models.

In this work, p+/intrinsic/n+ (p-i-n) diodes are used to calibrate the BTBT models for InGaAs, both for a semi-classical simulator[22] and a recently developed QM simulator.[15–17] P-i-n diodes allow a more accurate calibration, since the potential profile is mainly determined by the dopant concentration in the highly doped regions. BTBT happens in the intrinsic region, which is unaffected by BGN. It will be shown that the potential in p-i-n diodes can be determined accurately, since it is possible to verify it with C-V measurements. To further validate the calibration and extend the range of electric field, simulations and experiments are compared using stacks with different intrinsic region thicknesses.

This paper is organized in the same way as the calibration procedure, shown in Fig. 1. Section II contains the details of the p-i-n diode fabrication using a novel process

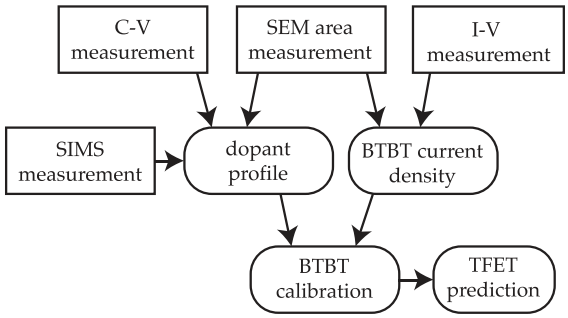

FIG. 1. Different electrical and physical characterization techniques are combined to obtain accurate BTBT calibration and make a prediction of the TFET performance.

flow. In Sec. III, dominant BTBT is confirmed with temperature-dependent current-voltage (I-V) measurements, and the scaling of the BTBT current with the junction area is discussed. In Sec. IV the dopant profiles are determined. The potential is then calculated using this dopant profile, and the BTBT models are calibrated by comparing the calculated BTBT current with the experimentally measured BTBT current. This is done for the semi-classical model in Sec. V and the QM model in Sec. VI. Finally, in Sec. VII, the performance of n-type and p-type InGaAs line-TFET[23] is predicted using the calibrated semi-classical simulator.

II. FABRICATION

The InGaAs p-i-n diodes are fabricated using a novel process flow. It features e-beam lithography to define diodes with small junction areas as shown by Pawlik *et al.*,[24] but the wet etching is metal-free. The large contact pads to p-InGaAs and n-InGaAs are deposited self-aligned using a basic back-end-of-line, as proposed by Demir *et al.*[25] The junction areas (A_j) range from 0.1 μm^2 to 216 μm^2. Such small A_j are needed to avoid series resistance problems. Self-aligned deposition of both metal contacts further decreases the series resistance, as the distance from the junction to n+ and p+ metal contacts is small, 50 nm and 250 nm, respectively (Fig. 2(a)).

In the first step of the process flow, four different n+/intrinsic/p+ InGaAs stacks are epitaxially grown by MBE on 2 in. InP (001) substrates (p-type doped $5 \times 10^{17}\,cm^{-3}$) from AXT.[26] The n-type impurity is silicon and the p-type impurity is beryllium. Three stacks have different intrinsic region thicknesses $T_i = 9$, 18, and 46 nm and one stack has no intrinsic region ($T_i = 0$ nm). After removing the InGaAs native oxide, a SiO_2 hard mask is deposited by CVD at 350 °C. This hard mask is patterned with round and square shapes by e-beam lithography and reactive ion etching (Fig. 3(a)). The diodes are wet etched according to this pattern using a diluted citric acid-peroxide solution (Fig. 3(b)). This process step determines the junction area A_j of the tunnel diodes. A_j is not equal to the area defined by e-beam lithography, since the wet etching undercuts the SiO_2 hard mask and InGaAs is etched anisotropically. To determine A_j, part of the diodes is removed from the process flow, the SiO_2 is removed with buffered HF, and the different A_j are measured directly using SEM. The next step in the process flow is a self aligned deposition of a metal contact on the exposed

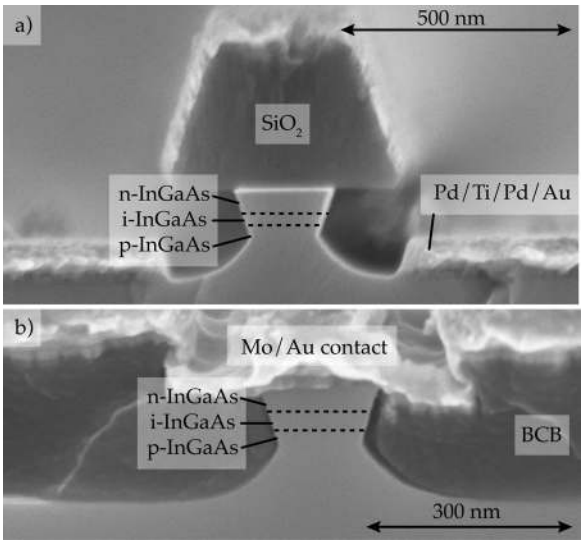

FIG. 2. (a) The metal contact to p-InGaAs is deposited self-aligned, close to the junction. (b) After the planarization with BCB and the removal of the SiO_2 hard mask, the contact to n-InGaAs is deposited self-aligned. On the device shown here, the metal contact to p-InGaAs was not present. The delamination of BCB at the sidewall occurs during the electron bombardment by the SEM.

p-InGaAs (Figs. 3(c) and 2(a)). The metal stack consists of Pd/Ti/Pd/Au and is deposited by evaporation. This metal contact is not deposited on the sidewalls of the diodes due to the shadowing effect of the SiO_2 hard mask. In a split experiment, AuZn/Au is deposited as a backside contact. An inter-layer dielectric of Benzocyclobutene (BCB) is then spun, cured, and recessed to 300 nm thickness with SF_6/O_2 reactive ion etching, exposing the top part of the metal and the SiO_2 (Fig. 3(d)). These two layers are removed with a sputter etch and buffered HF dip, respectively (Fig. 3(e)). This reveals the n-InGaAs, which is then contacted with sputtered Mo/Au (Fig. 2(b)). The contact is patterned into probing pads with i-line lithography and sputter etching. Finally, the exposed BCB is removed by SF_6/O_2 reactive ion etching (Fig. 3(f)).

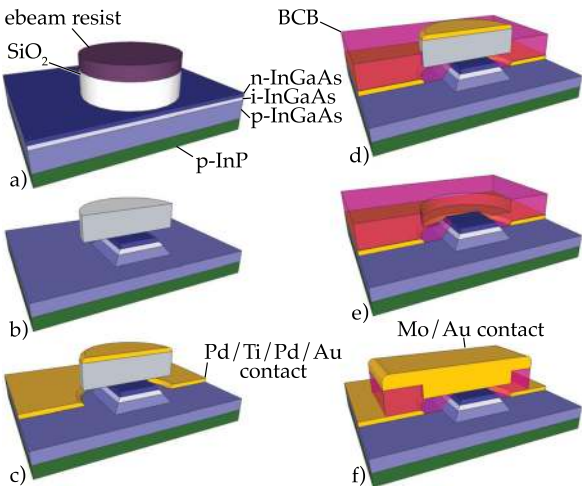

FIG. 3. Device schematics depicting the process flow, which includes (a) the MBE growth of InGaAs and SiO_2 patterning with e-beam resist, (b) wet etch of the diode mesa, (c) self aligned deposition of the p+ contact, (d) planarization with BCB, (e) opening of the contact hole, (f) deposition and patterning of the n+ contact pads and BCB recess.

III. BTBT CURRENT DENSITY MEASUREMENTS

In this section, the I-V characteristics of the diodes are analyzed. First, the external series resistance is determined to decouple its effect. Then, the voltage range of dominant BTBT is extracted with temperature-dependent I-V measurements. The scaling of the BTBT current with the area is then analyzed to allow the extraction of the BTBT current density. Additionally, the scaling of trap-dominated current and the peak-to-valley current ratio are discussed.

A. Impact of series resistance

The I-V characteristics are measured with an *Agilent 4156C precision parameter analyzer*. The series resistance is 250 Ω, both for diodes with a back contact to the InP substrate and diodes with a Pd/Ti/Pd/Au contact directly to the p-InGaAs. This places an upper limit on the current range where BTBT can be determined accurately. In the following figures considered for BTBT calibration, the I-V curves are trimmed such that the impact of series resistance is negligible.

B. Temperature dependent I-V to verify BTBT

For direct semiconductors, BTBT is nearly constant when changing the temperature. For InGaAs, the decrease in bandgap with rising temperature leads to a measured activation energy E_A typically lower than 0.1 eV. Diffusion, Shockley-Read-Hall (SRH) generation/recombination and Trap Assisted Tunneling (TAT) have typical activation energies of $E_A = E_g$, $E_A = E_g/2$, and $0.1\,\text{eV} < E_A < E_g/2$, respectively,[27,28] with E_g being the bandgap of the material. Therefore, temperature dependent measurements are used to verify in which bias range BTBT is dominant over the other current components.

The results in Fig. 4(a) show that for $T_i = 9$ nm, BTBT dominates in reverse bias (positive V_{np}) and small forward bias. At larger forward bias, trap-related recombination mechanisms dominate. The same behaviour is observed for $T_i = 18$ nm. For $T_i = 46$ nm, the BTBT generation/recombination rate is much lower due to the longer intrinsic region, and at high temperature diffusion current can be observed for small reverse bias and forward bias (Fig. 4(b)). The

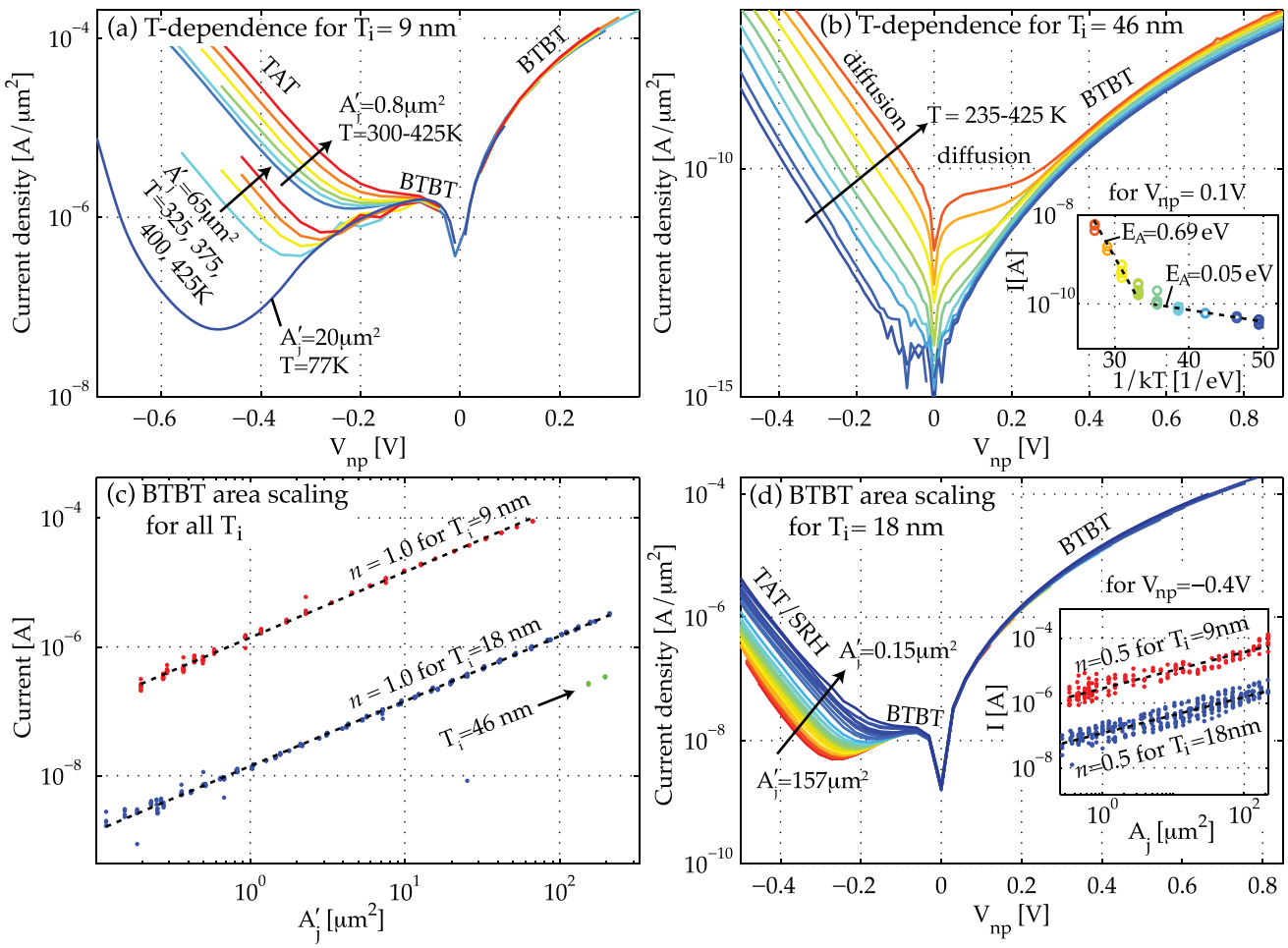

FIG. 4. Temperature-dependent I-V characteristics (the direction of the arrow indicates higher temperature) identify (a) BTBT and TAT regimes for $T_i = 9$ nm ($A'_j = 0.8$, 20, 65μm^2, T = 77, 300, 325, 350, 375, 400, and 425 K). For TAT, the activation energy $E_A = 0.2$ eV for $V_{np} = -0.4$ V. (b) For $T_i = 46$ nm, BTBT and diffusion regimes are identified ($A'_j = 197\mu m^2$, T = 235, 250, 275, 300, 325, 350, 375, 400, and 425 K). In the inset, E_a is small at low temperature, implying BTBT ($E_a = 0.06$ eV at T = 235–325 K, $V_{np} = 0.1$ V), and larger at high temperature, implying diffusion current (E_a=0.69 eV at T = 350–425 K, for both $V_{np} = 0.1$ V and $V_{np} = -0.2$ V). (c) The BTBT current scales with A'_j. $T_i = 9$ and 18 nm are biased at their peak voltage $V_{np} = -0.06$ V, and $T_i = 46$ nm is biased at $V_{np} = 0.5$ V. Due to difficulties during the processing of the contact pads for $T_i = 46$ nm, only the largest devices could be measured. (d) As shown for $T_i = 18$ nm, the current normalized with A'_j is constant in the BTBT region (reverse bias and small forward bias). In the inset, it is shown that the current scales with the perimeter ($I \sim A_j^{1/2}$) when the diodes are biased in the TAT/SRH regime ($V_{np} = -0.4$ V).

voltage range where BTBT dominates is thus confirmed for all diode types.

C. BTBT perimeter effects

In order to extract the BTBT current density, the current scaling is verified by considering diodes with different junction areas. Each area is measured individually by SEM. At a certain bias, the current of each diode is measured and plotted versus its area in a log-log plot (Fig. 4(c)). If the current I scales with the junction area A_j of the diode ($I \sim A_j^1$), the slope n of a linear fit through these points is 1. If I scales with the perimeter of the diode ($I \sim A_j^{1/2}$), $n = 1/2$. For the diodes biased in the BTBT region and with A_j measured by SEM, $n = 1.1$ is obtained. This means the BTBT generation does not happen over the full measured junction area, but only in the center part. This could be due to an electrostatic effect of interface traps or dopant deactivation at the sidewalls of the diodes. When the A_j are modified to A_j' by removing the area along the outer perimeter, and with a width of 100 nm, the results in Fig. 4(c) are obtained. The slope of the linear fit is $n = 1.0$, both for reverse bias and small forward bias (Fig. 4(d)). These modified A_j' are used throughout this paper when BTBT is discussed.

D. Defect related perimeter effects in forward bias

As shown in Figs. 4(a) and 4(d), the current at more negative V_{np} does not scale with A_j for $T_i = 9$ and 18 nm. When the current of differently sized diodes is mapped against the respective A_j, $n = 0.5$ (inset of Fig. 4(d)) is obtained. This indicates scaling with the perimeter, and the recombination current mainly originates from defects at the sidewalls of the diodes. For $T_i = 9$ nm, the ideality factor is 3, and the extracted activation energy $E_A = 0.2$ eV (Fig. 4(a)), suggesting recombination by TAT.[28] Furthermore, this recombination current is more than 10 times higher for $T_i = 9$ nm, where a strong electric field is present, compared to $T_i = 18$ nm (inset of Fig. 4(d)). For $T_i = 18$ nm, the ideality factor between 1.5 and 2, suggests perimeter recombination by TAT or SRH.

E. Peak-to-valley current ratio (PVCR)

The PVCR is an important figure of merit for tunnel diodes, since it captures information about the band-to-band tunneling recombination (peak current) and TAT/SRH recombination (valley current). Negative differential resistance can be observed for $T_i = 0$, 9, and 18 nm. For the largest available devices with $T_i = 9$ and 18 nm, the PVCR is 6 for square diodes and 3 for round diodes. A possible explanation is that for square diodes the sidewall planes align with the InGaAs crystal planes, contrary to round diodes. Therefore, wet etching may create more sidewall defects in the round diodes. When cooled down to 77 K, sidewall defects are deactived (Fig. 4(a)), and PVCR = 40 for large devices of all geometries. For the largest available devices with $T_i = 0$ nm, the maximum PVCR is 16 at room temperature (Fig. 5), which is a record for $In_{0.53}Ga_{0.47}As$ homojunctions.[24]

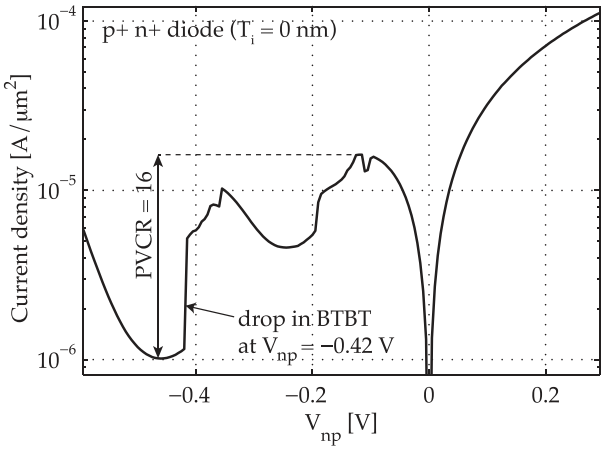

FIG. 5. Diodes without intrinsic region have a maximum PVCR = 16. The sharp drop in BTBT current at $V_{np} = -0.42 \pm 0.01$ V, indicates the total degeneracy in p- and n-type region. The additional current peaks are still under investigation.

IV. EXTRACTION OF THE DIODE DOPANT PROFILES

In Sec. III, the BTBT current density was determined accurately for all three p-i-n diodes types. Before the corresponding simulations can be ran to calibrate the models, the three dopant profiles need to be extracted, and realistic error bars need to be determined for these profiles. This is done with complementary SIMS and CV measurements.

A. Dopant profiles for T_i = 18 and 46 nm

The dopant concentration is determined with SIMS (Figs. 6(a) and 6(b)). The primary beam is a 250 eV oxygen beam and the mass separation is performed by a magnetic sector. Both measurements are performed two times. The silicon concentration is $N_{Si} = 2.2 \times 10^{19}\,cm^{-3}$ (n-type dopants) and the Beryllium concentration is $N_{Be} = 1.7(\pm 0.1) \times 10^{19}\,cm^{-3}$ (p-type dopants) in the respective neutral regions. Concerning the silicon background concentration, measurements on previous samples from this MBE tool have resulted in values about $1 \times 10^{16}\,cm^{-3}$, but since the SIMS detection limit is $N_{min} = 2 \times 10^{17}$, it cannot be determined accurately for these samples. However, simulations have shown that the diode potential is not sensitive variations in concentration around $N_{Si} = 1 \times 10^{16}\,cm^{-3}$, so this value is taken. Concerning the beryllium background concentration, all SIMS measurements show it is higher ($1 \times 10^{18}\,cm^{-3}$) at the edge of the silicon-rich region than in the intrinsic region.

Since the n- and p-type dopant concentrations are not excessively high, activation is assumed 100%. Furthermore, simulations have shown that even if the activation in the neutral regions is 70%, the change in electric field at the tunnel junction is negligible.

B. Dopant profile for T_i = 9 nm

In the intrinsic region, the dopant concentrations decrease exponentially with depth. The intrinsic region thickness T_i is defined as the distance between the two points where the concentration has decreased to 50% of its original value. T_i matches exactly with the designed values of the

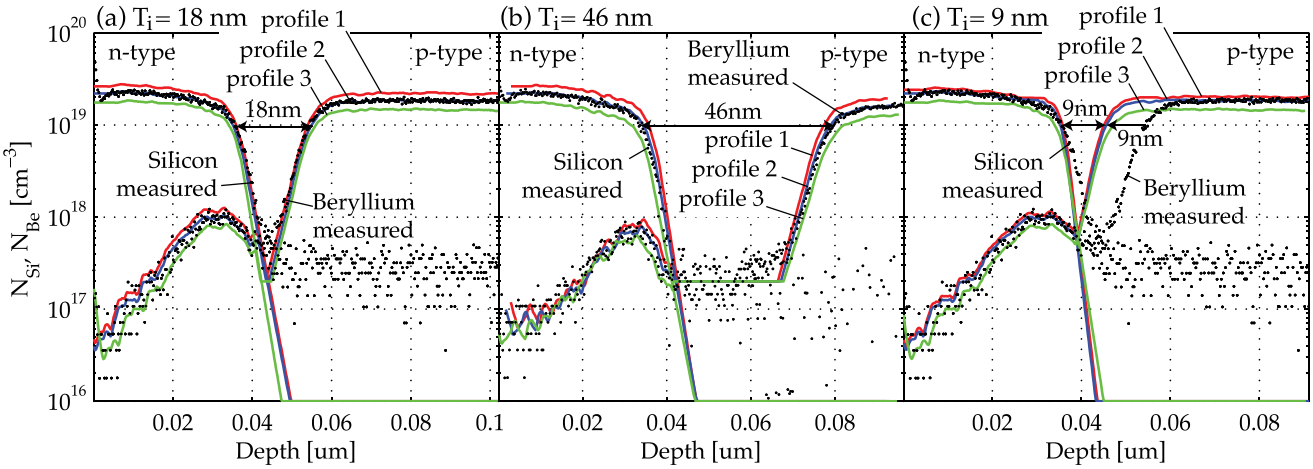

FIG. 6. The SIMS dopant profiles for (a) $T_i = 18$ nm and (b) $T_i = 46$ nm are shown by the black dots. For (c) $T_i = 9$ nm, since no SIMS measurement is available, the possible dopant profiles are obtained by modifying the $T_i = 18$ nm SIMS profile (dotted line): the Beryllium profile in the p-type region is shifted 9 nm towards to n-type region, but the Beryllium peak in the n-type region is kept identical. Using C-V measurements (Secs. IV D and IV E), the possible dopant profiles 1, 2, and 3 for (a) $T_i = 18$ nm are obtained by scaling the dopant concentration by 1.2, 1, and 0.8, scaling the depth values by 1.05, 1.05, and 1, and reducing the dopant downslopes to 90%, 90%, and 80% of their original value, respectively. For (b) $T_i = 46$ nm, the concentration is scaled by 1.2, 1, and 0.8, the depth by 0.95, 0.97, and 1.02, and the dopant downslopes are kept identical. For (c) $T_i = 46$ nm, the concentration is scaled by 1.1, 1, and 0.8, the depth by 1.05, 1.05, and 1.02, and the downslopes to 50%, 50%, and 65% of their original value, respectively.

MBE growth, for both $T_i = 18$ and 46 nm. Since no SIMS measurement was made for $T_i = 9$ nm, the SIMS data are extrapolated and a new dopant profile is created by shifting the Beryllium profile of $T_i = 18$ nm $\times$ 9 nm towards the silicon-doped region (Fig. 6(c)).

C. Sources of uncertainty on the dopant profiles

Uncertainties on the width of the intrinsic region and the dopants at the edge of the intrinsic region have the largest impact on the electric field and must be taken into account. Only a small degradation of dopant downslopes is possible, given the low surface roughness of the samples (RMS = 0.2 nm, as measured by AFM). There is also some uncertainty on the depth scale ($\pm 5\%$) and the absolute number of dopants measured ($\pm 20\%$).

D. CV measurements

Due to the uncertainties mentioned above, CV measurements are used as a complementary technique to determine the width of the depletion region. These measurements are carried out on the same devices for which the BTBT current density is extracted and thus provide information on the local dopant profile. The CV measurements are compared to Sentaurus Device AC simulations with imported SIMS dopant profiles. The band structure models and parameters of these simulations are discussed in Sec. V.

The impedance of the diodes is measured with an *Agilent 4284A precision LRC meter*. A parallel capacitance-parallel conductance $C_p - G_p$ equivalent circuit is used to reflect the high conductive component. The complex admittance $Y = G_p + j\omega C_p$ is then measured. C_p can only be extracted accurately, if ωC_p is about the same order of magnitude or higher than G_p. To increase ωC_p, the frequency range $f = \omega/2\pi$ is taken sufficiently high; 100 kHz–630 kHz for devices with $T_i = 18$ and 46 nm, and 400 kHz–640 kHz for $T_i = 9$ nm. To decrease the conductive leakage G_p, the diodes are biased in the valley region where BTBT and other recombination currents are low. The range where C_p can be extracted is shown in Fig. 7 for $T_i = 18$ nm. For $T_i = 9$ nm, G_p is too high at room temperature, and the CV measurements are done at T = 77 K to decrease conductance by TAT recombination. Under these conditions, C_p is frequency independent and varies slightly with the applied bias. C_p increases with more negative V_{np} (forward bias) as the depletion region becomes thinner.

All CV characteristics are measured on devices with $A_j = 216\ \mu m^2$. For easier probing, most CV measurements are done on devices encapsulated in BCB, with a 2900 μm^2 contact pad on top of the device and surrounding BCB, as shown in Fig. 3(f). Because of this, the measured capacitance

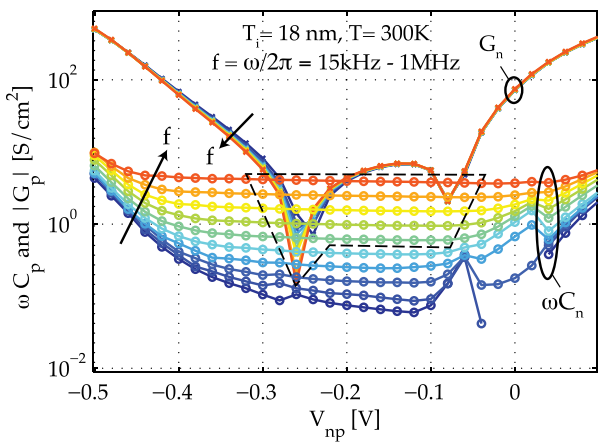

FIG. 7. The susceptance ωC_p and conductance G_p are shown at different frequencies $f = 15$ kHz to 1 MHz. The direction of the arrows indicates higher frequencies. C_p can be extracted if ωC_p is larger than or comparable to G_p. These conditions are met in the valley region $V_{np} = -0.1$ to -0.3 V and at sufficiently high frequencies ($f = 100$–630 kHz), indicated by the dashed region.

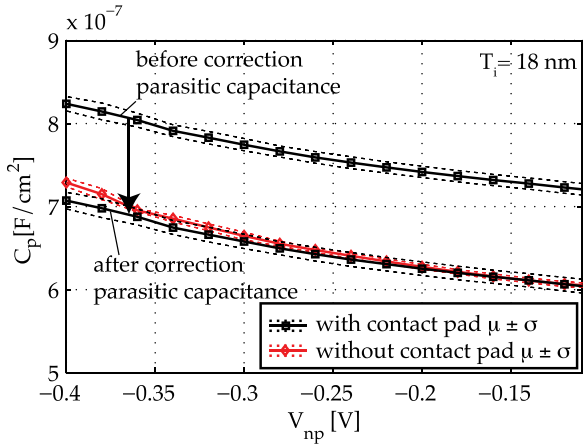

FIG. 8. The capacitance of devices with and without contact pad matches when the measured capacitance is corrected by subtracting the parasitic contact pad capacitance. The average μ (full lines) and standard deviation σ (dotted lines) are taken over 6 devices.

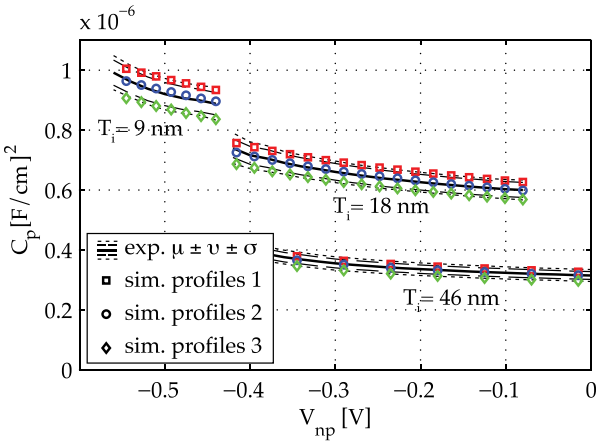

FIG. 9. The average measured capacitance (μ, full lines), the additional systematic error ($\mu \pm \nu$, broken lines) and additional standard deviation ($\mu \pm \nu \pm \sigma$, dashed lines) are shown for $T_i = 9$, 18, and 46 nm. Simulations of C-V using profiles 1, 2, and 3 reflect the uncertainty on the measured C-V. $T_i = 9$ nm are measured using contact pads at $T = 77$ K. $T_i = 18$ nm are measured both with and without pads at $T = 300$ K (Fig. 8). For $T_i = 46$ nm, the junction capacitance is comparable to the parasitic pad capacitance, and only devices without contact pads are considered ($T = 300$ K).

is a parallel circuit of the junction capacitance and a parasitic pad capacitance. The parasitic pad capacitance is determined on contact pads where no diodes are present. It is measured separately on every chip, since it depends on the thickness of the underlying BCB. The pad capacitance varies between 2.5×10^{-13} F and 3.1×10^{-13} F. The junction capacitance of the diodes is then determined by subtracting the pad capacitance from the total measured capacitance. In order to validate this approach, the junction capacitance for $T_i = 18$ nm was extracted from devices with and without contact pad. After the correction for the parasitic pad capacitance, the capacitances of both device types match, as shown in Fig. 8.

As with the SIMS measurements, the CV measurements also have some uncertainty. Measured over 10 devices, the standard deviation on the capacitance is about 1% of its average value. Possible systematic errors on the extraction of the diode area with SEM are $\pm 2\%$ uncertainty on the SEM calibration, $\pm 0.5\%$ uncertainty due to the resolution of the images, and $\pm 0.2\%$ uncertainty on the estimation of the junction location. The possible systematic error of the capacitance measurement is[29] $\pm 1.5\%$, given the 2 m cable length, $C = 1 \times 10^{-12}$ F and $f = 600$ kHz. Fig. 9 shows the measured junction capacitance for $T_i = 9$, 18, and 46 nm with systematic uncertainty ν and statistical uncertainty σ.

E. Combining CV measurements with SIMS measurements

Three dopant profile sets (1, 2, and 3) are generated to match the experimentally measured capacitance. Each set includes three profiles for the different T_i. Profile sets 1, 2, and 3 are based on the SIMS profiles and lie within the range of SIMS uncertainties, as described previously. As shown in Fig. 9, profiles 1 match the highest possible capacitance values and would give the highest possible BTBT current. Profiles 2 match the capacitance values in the case of zero systematic and statistical error. Profiles 3 match the lowest possible capacitance values and would give the lowest possible BTBT current. The simulated and measured capacitance values match over the full voltage range where they can be extracted. The values measured by SIMS, and the derived profile sets 1, 2, and 3 reflecting the total uncertainty, are shown in Fig. 6. The details of the adjustments are given in the respective figure captions. A remarkable conclusion of these simulations is that dopant profiles with different adjustments but resulting in the same simulated capacitance also give a very similar band-to-band tunneling current. In other words, the band-to-band tunneling calibration is not sensitive to which types of adjustments are made to the dopant profiles, as long as the capacitance simulated with these profiles matches the measured capacitance.

V. SEMI-CLASSICAL BAND-TO-BAND TUNNELING CALIBRATION

In this section, the band structure models and parameters of the semi-classical simulator are first discussed. Then, the BTBT parameters are calibrated using the previously discussed dopant profiles and the measured BTBT current density. Finally, the error bars of the calibration are discussed, and the calibrated parameters are compared to their theoretical prediction.

A. Band structure models and parameters

The bandgap (E_g) of InGaAs is taken 0.74 eV at $T = 300$ K. For CV simulations at $T = 77$ K, $E_g = 0.81$ eV.[30] Dopant-dependent bandgap narrowing is implemented with the Jain-Roulston model.[21,31] Multiple conduction band valleys (Γ, L, and X) are considered,[32] with a respective non-parabolicity correction[33] $\alpha = 1.35$, 0.42, and 0.077 eV^{-1}.

The position of the Fermi level is discussed and experimentally verified in the following paragraph. In the neutral regions, the distance between the majority carrier band edge and the Fermi level is calculated using Fermi-Dirac statistics, the density of states, and the carrier concentration. For the n-InGaAs region with $n = 2.2 \times 10^{19}$ cm^{-3}, the Fermi level is predicted to be 0.40 eV above the conduction band edge. For

the p-InGaAs region with $p = 1.7 \times 10^{19}\,\mathrm{cm}^{-3}$, the Fermi level is predicted to be 0.04 eV below the valence band edge. At small forward bias, this causes overlap of the valence and conduction bands and recombination by BTBT occurs. This recombination current drops to zero when the bands no longer overlap, for $V_{np} < -(0.04\mathrm{V} + 0.40\mathrm{V}) = -0.44\mathrm{V}$. This drop in BTBT current is experimentally observed for the diodes without intrinsic region (Fig. 5), where recombination by BTBT is very high compared to diffusion and recombination by SRH or TAT. The drop in BTBT current is located at $V_{np} = -0.42 \pm 0.01$ V, close to the predicted value. The average value and standard deviation are obtained by measuring 10 devices. This experimental verification of the Fermi level position gives additional confidence in the calculated potential profile.

B. Calibration of the BTBT parameters

In Sentaurus device, BTBT is implemented with a dynamic nonlocal BTBT model.[22] The input parameters A_{BTBT} and B_{BTBT} are calibrated by comparing the results of the simulator with the measured BTBT current density. The voltage range considered for calibration is reverse bias. This is because in forward bias, the BTBT recombination rate is also determined by the available density of states close to valence band edge and the Fermi level, which is not well known for degenerate doping. For $T_i = 46$ nm, the calibration starts from $V_{np} > 0.1$ V, since diffusion current is not negligible at lower V_{np} (Fig. 4(b)).

First, the dopant profile set 1 (for $T_i = 9$, 18, and 46 nm) is imported in the simulator. The parameters A_{BTBT} and B_{BTBT} are then modified to obtain a best fit of the BTBT current for the three diode types at the same time (Fig. 10). This determines the lower boundary for the parameters. This process is then repeated for profiles 2 and 3. The results of the calibration are shown in Table I. With these calibrated parameters, an excellent agreement is obtained between the measured and simulated current density (Fig. 10), with a maximum difference of 20%.

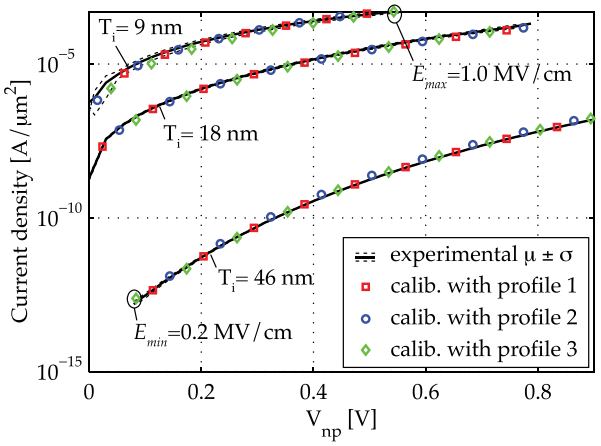

FIG. 10. With the calibrated parameters A_{BTBT} and B_{BTBT} shown in Table I, the simulated and experimental BTBT current match over the full range of electric fields (E = 0.2–1 MV/cm). The dotted lines indicate the standard deviation of 64, 32, and 9 devices for $T_i = 9$, 18, and 46 nm, respectively.

TABLE I. The lower limit, recommended values, and upper limit for the calibrated BTBT parameters are determined with dopant profile sets 1, 2, and 3, respectively.

	Lower limit	Recommended	Upper limit
A_{BTBT} [$\mathrm{cm}^{-3}\,\mathrm{s}^{-1}$]	1.1×10^{20}	1.3×10^{20}	1.6×10^{20}
B_{BTBT} [$\mathrm{V\,cm}^{-1}$]	6.0×10^{6}	5.7×10^{6}	5.4×10^{6}

The uncertainty on the BTBT generation rate is not only determined by the difference between the upper limit and lower limit in Table I but also depends on the electric field E at the junction; Eq. (1) shows that G_{BTBT} depends exponentially on B_{BTBT} when $E \ll B_{BTBT}$, but scales linearly with A_{BTBT} when $E \gg B_{BTBT}$. For TFET, the uncertainty is only ±30% at typical electric fields of $E = 4$ MV/cm. For MOSFET, the uncertainty on BTBT leakage in the off-state is ±50% at a typical drain junction field of $E = 1$ MV/cm.[34]

The calibrated parameters are now compared to their theoretically predicted values. According to the formalism by Keldysh and Kane[13]

$$A_{BTBT} = \frac{g\pi m_r^{1/2}(qE_0)^2}{9h^2\sqrt{E_g}}, \tag{2}$$

$$B_{BTBT} = \frac{\pi^2 m_r^{1/2} E_g^{3/2}}{qh}, \tag{3}$$

where g is the degeneracy factor, q is the elementary charge, and h is Planck's constant. The reduced tunnel mass m_r is given by $(m_e^{-1} + m_{lh}^{-1})^{-1}$. Using the electron effective mass $m_e = 0.043\ m_0$ (Ref. 35) and hole effective mass $m_{lh} = 0.052\ m_0$ (Ref. 36) with m_0 is the free electron mass, we obtain $A_{BTBT} = 1.6 \times 10^{20}\,\mathrm{cm}^{-3}\,\mathrm{s}^{-1}$, $B_{BTBT} = 5.6 \times 10^{6}\,\mathrm{V\,cm}^{-1}$, which are within the range of calibrated values.

VI. QUANTUM MECHANICAL BAND-TO-BAND TUNNELING CALIBRATION

In this section, the input parameter of a QM simulator is calibrated using the values obtained in Table I and compared to the theoretically predicted value. Finally, the diode I-V characteristics of the QM simulator and semi-classical simulator are compared.

The QM simulator used is based on the envelope function formalism, applying quantum transmitting boundary conditions[37] at the contacts. Since the current implementation only considers two bands, there is only coupling between these bands in the transport direction, and an effective mass approximation is applied in the orthogonal direction. The only input parameters for this simulator are the $\mathbf{k}\cdot\mathbf{p}$ interband momentum matrix element $\mathbf{P}$ between conduction and valence band, the bandgap, and the effective mass for the orthogonal direction. $\mathbf{P}$ is a measure for the coupling strength between the respective bands and is usually listed in units of energy as E_P (Ref. 35)

$$E_P = \frac{8\pi^2 m_0}{h^2}\mathbf{P}^2. \tag{4}$$

E_P is calibrated from B_{BTBT} with the relation

$$B_{BTBT} = \frac{\pi^2 E_g^2 m_0}{2h\sqrt{E_P m_0/2}} \quad (5)$$

derived from calculations by Kane.[13] Using the values from Table I, the range of calibrated values $E_P = 13.5$, 15, and 16.5 eV is obtained, with the lower limit, recommended value, and upper limit, respectively.

From theory, we can calculate the expected value of E_P in a 2-band description with no perturbation from other bands or spin-orbit interaction from[35]

$$\frac{m_0}{m_e} = 1 + \frac{E_P}{E_g}. \quad (6)$$

We then obtain the theoretical prediction $E_P = 16.5$ eV, which is within the range of calibrated E_P.

It should be noted that E_P differs from that in Ref. 35, where a value of 25.3 eV is recommended. This larger value is a result of the higher band perturbations included in the 8-band model, which necessitate an increase in E_P to retain the same effective mass (compare Eq. (2.15) in Ref. 35 to Eq. (6)). E_P obtained in this work is therefore valid for models which do not perturbatively include the effects of higher bands.

In order to validate this calibration method using Eq. (5), the diode potential profile calculated by the semi-classical simulator is imported in the QM simulator. Then, the BTBT current calculated by both simulators is compared. BGN is deactivated since this is not supported by the QM simulator. Fig. 11 indeed shows a very good agreement between both I-V curves. This agreement is expected, as the minimum diameter of the working diodes is about 200 nm, which is large enough not to observe quantum confinement effects.

VII. TFET PERFORMANCE PREDICTION

In this section, the input characteristics of n-type and p-type InGaAs homojunction TFET are predicted. The adopted configuration is a line-TFET, where the gate covers

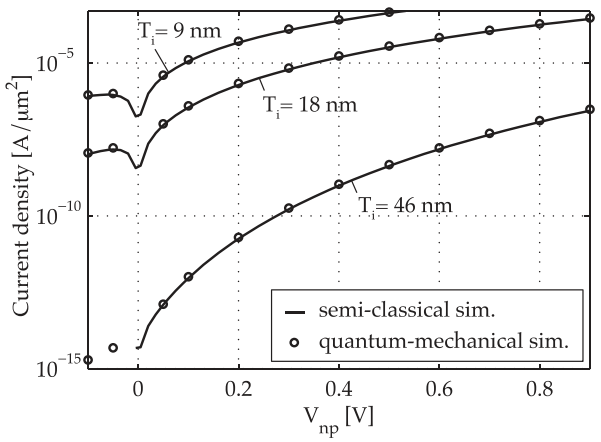

FIG. 11. The BTBT current calculated by the QM and semi-classical simulators are in good agreement. For the former, $E_P = 15$ eV and a light hole effective mass approximation is used in the transverse direction. The latter uses the recommended parameters in Table I. The potential is calculated with dopant profile set 2.

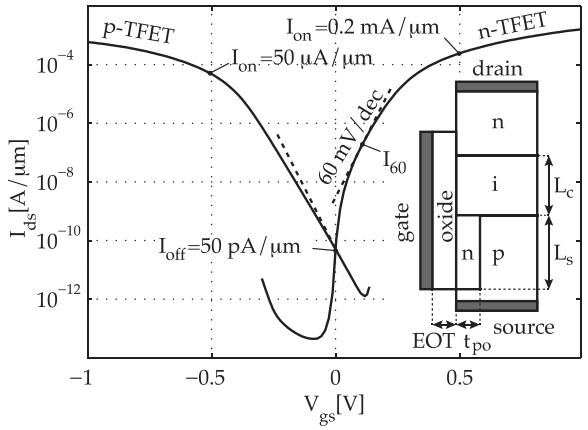

FIG. 12. The input characteristics are shown for n-lineTFET (inset) and p-lineTFET. For n-TFET, $t_{po} = 3$ nm and the gate workfunction WF = 4 eV. The source and pocket dopant concentrations are $N_s = N_p = 1 \times 10^{20}$ cm^{-3}. For p-TFET, $t_{po} = 5$ nm, WF = 5 eV, all dopant types shown in the inset are reversed and $N_s = N_p = 5 \times 10^{19}$ cm^{-3}. For both TFET, EOT = 0.6 nm and the drain voltage is $V_{ds} = 0.5$ V. The source and channel length are $L_s = 30$ nm and $L_c = 50$ nm, respectively.

the source and a counterdoped pocket (inset of Fig. 12). This results in tunneling perpendicular to the gate. After the tunneling event, the current flows underneath the gate dielectric towards the drain. Because the tunneling is uniform over the whole source-pocket junction, this configuration provides a steeper subthreshold swing compared to point-TFET.[23,38] For this TFET configuration, the semi-classical simulator[22] is used, since the QM simulator currently only considers coupling in the direction parallel to the gate. The band structure models are described in Sec. V, and for the nonlocal BTBT model the recommended values from Table I are used. BGN is not considered in these simulations.

The semi-classical simulator does not consider field-induced quantum confinement (FIQC). FIQC results in shifted input characteristics and a slightly lower on-current.[39] The shift is determined by the first quantized energy level in the source near the gate. In order to account for this, this energy is calculated quantum mechanically using an effective mass approximation with nonparabolic correction. The input characteristics are then shifted accordingly and shown in Fig. 12.

The n-type TFET has a sub-60 mV/dec subthreshold swing, and the transition point[40] from sub-60 mV/dec to super-60 mV/dec is $I_{60} = 0.2\ \mu$A μm^{-1}. The p-type TFET does not reach a sub-60 mV/dec subthreshold swing due to the low density-of-states in the conduction band of InGaAs.[41] Compared to MOSFET,[42] the pocketed InGaAs n-lineTFET shows competitive performance with $I_{on} = 0.2$ mA μm^{-1} in a supply voltage window $V_{dd} = 0.5$ V. The p-type TFET does not reach sufficiently high I_{on}.

VIII. CONCLUSIONS

We calibrated BTBT for a semi-classical simulator and a QM simulator using InGaAs p-i-n diodes. The recommended input parameters are $A_{BTBT} = 1.3 \times 10^{20}$ cm^{-3} s^{-1}, $B_{BTBT} = 5.7 \times 10^6$ V cm^{-1} for the former, and $E_P = 15$ eV for the latter. This value of E_P correctly describes BTBT, unlike values recommended for $\mathbf{k} \cdot \mathbf{p}$ implementations with

perturbative inclusion of higher bands. We determined the uncertainty on the BTBT rate, resulting in ±30% at electric fields typical for TFET and ±50% at electric fields typical for MOSFET. This low uncertainty was accomplished by determining the dopant profile with complementary SIMS and C-V measurements. The range of calibrated parameters encompasses the theoretically predicted values, confirming the validity of direct BTBT models for InGaAs. Our result suggests that reliable predictions can be made for other direct bandgap materials with the existing model.

We predicted the input characteristics of InGaAs homojunction TFET using the calibrated semi-classical simulator. The nTFET shows competitive performance with $I_{on} = 0.2\,mA\ \mu m^{-1}$ at $V_{dd} = 0.5\,V$, but the p-type TFET is underperforming. The performance of TFET can further be boosted with the use of heterojunctions, where materials with high density of states and high tunneling rates are combined.[43] However, it is still unknown whether BTBT models can accurate describe tunneling in these configurations, especially for a staggered or broken gap alignment where reflections can occur.[16] Therefore, the calibration of heterostructure tunneling is a topic of great interest.

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