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*Input-Current-Shaper Based on a Modified SEPIC Converter with Low Voltage Stress

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Abstract-The boost topology is often the designer's first choice when dealing with PFC front-ends. This topology is well documented in the literature and has obvious advantages like continuous input current and low voltage- and current-stress compared to other PFC topologies. The PFC SEPIC converter also has the advantage of the continuous input current but suffers from high voltage- and current stress. In this paper a Modified SEPIC converter is presented with reduced voltage stress, comparable to that of the boost converter. Experimental result of a 200W prototype for 185-270 V line voltage will also be presented.

I. INTRODUCTION

By January 2001 the European standard, EN61000-3-2, will be a reality. The limits on the current harmonics imposed by EN61000-3-2 have been one of the driving forces in the past decade concerning research in the field of Power Factor Correction (PFC) and Input Current Shaping (ICS). For many applications, the main goal is not to achieve unity Power Factor (PF) but just to stay within the harmonic current-limits by minimum effort concerning circuit-complexity, cost and loss of efficiency. Therefore researchers have put a lot effort into developing power converters that could achieve PFC together with fast regulation of the output voltage ([1], [2]) (Single-stage topologies). The most commonly used topology for PFC, is the boost-converter. The distinct advantage of this topology is the continuous input current making EMI-filtering less of a problem compared to buck, buck-boost topologies. By using a boost-converter the output voltage has to be higher than the line peak voltage, which is not necessarily the optimal operating point for the following DC/DC-stage.

The SEPIC converters input current is continuous and the output voltage can be lower than the line peak voltage. The major drawback of the SEPIC converter is the high current and voltage stress of the components [3].

In [4] it is shown how the SEPIC-converter in Discontinuous Conduction Mode (DCM) with a simple voltage loop achieves good PF. The voltage loop bandwidth has to be low in order not to regulate on voltage fluctuations caused by the pulsating power drawn from the line.

Because of the voltage stress the use of IGBTs instead of MOSTETs are preferable. Since the switching abilities of IGBTs can be a problem concerning the efficiency, soft switching techniques are often employed ([4], [5]) further increasing the circuit complexity. In [6] the Sheppard-Taylor topology is used as a PFC converter with the ability of creating a voltage lower than the line peak voltage with continuous input current but with increased circuit complexity as a result. In [7]-[9] buck topologies are used. A way to increase the PF for the buck converters is shown in [8] and [9], where a buck-boost converter is operated in parallel with the buck converter, so that current is flowing from the line even though the output voltage is above the instantaneous line voltage.

When considering the different PFC topologies that are able to produce a voltage below the line peak voltage, the SEPIC converter seems to be an attractive alternative; mainly because of the continuous input current. In this paper a converter based on the SEPIC converter will be proposed as a PFC front-end. The voltage stress in the proposed converter is comparable with the voltage stress in the boost converter.

In section II the proposed Modified SEPIC converter will be introduced. In section III, two different operation modes will be described and in section IV the theoretical calculations of section III will be experimentally verified with two different prototypes for line voltages in the range of 185Vac-270Vac.
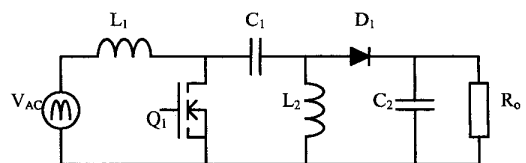
II. THE MODIFIED SEPIC CONVERTER

Fig. 1. Classical PFC SEPIC converter

The proposed converter is based on the classical SEPIC converter shown in Fig. 1, and compared to this converter, the proposed Modified SEPIC converter differs in two ways. The capacitor C_1 is a large bulk capacitor; a diode is placed in series with the inductor L_2. The bulk capacitor serves to decouple the pulsating input power, and the diode insures that the inductor L_2 can be operated in discontinuous mode (DCM) without the capacitor C_1 being charged to above the peak line voltage.
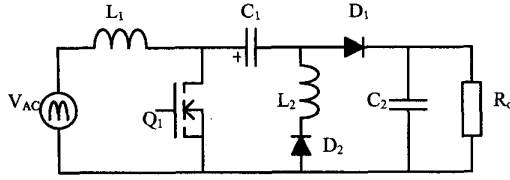
Fig. 2. Modified PFC SEPIC converter.

The inductor L_2 does not necessarily have to be operated in DCM but by insuring that no current can flow in the "off" direction of D_2, the voltage V_{C1} can arbitrarily be controlled by the ratio of L_1 to L_2, as long as the sum of the output voltage and V_{C1} is higher than the line peak voltage.

The drawback of adding D_2 in series with L_2, is not so much the power loss, since only part of the total power flows through D_2, but the inherent galvanic isolation possibility is lost.

III. OPERATION MODES

The modes described in this section, are all with the Modified SEPIC converter in DCM. The DCM operation is often used in low-power applications. The advantage of this mode is small magnetics, no reverse recovery problems with the rectifiers and reduced turn-on losses in the switch. The downside is higher rms-currents and more HF noise.

A. Fast regulation of the output

When regulating the boost PFC converter, a slow outer control loop is always applied in order not to regulate the pulsating input-power. This is not necessary with the Modified SEPIC converter because that the input-power is internally decoupled by the series bulk capacitor. The output is thereby decoupled from the input, and a fast loop can be implemented.

The output power consists of two contributions; the direct transferred power from the input through L1 and the contribution from the series bulk capacitor, C1, through L2 to the output.

Because of the fast regulation loop the output power will be kept constant and the duty-cycle, d(t), will be adjusted accordingly.

$$d(t) = \sqrt{\frac{P_{OUT}}{\dfrac{T_{Switch} \cdot V_{OUT} \cdot \hat{V}_{IN}^2 \cdot \sin^2(\omega t)}{2 \cdot L_1 \cdot (V_{C1} + V_{OUT} - \hat{V}_{IN} \cdot \sin(\omega t))} + \dfrac{T_{Switch} \cdot V_{C1}^2}{2 \cdot L_2}}} \quad (1)$$

, where T_{Switch} is the high-frequency switching period.

In the denominator of (1) the first fraction is related to the direct power transferred through L_1 and the second fraction is related to the power transferred through L_2.

It is assumed that the bulk capacitor voltage, V_{C1}, is constant during one half line period and therefore also during one switching cycle. The assumption that V_{C1} is constant during one half of the line period is not entirely correct. Twice the line frequency voltage-variation will be present on the capacitor C_1.

The input power to the converter is given by:

$$P_{IN} = \frac{1}{N} \cdot \sum_{n=1}^{N} \frac{T_{Switch} \cdot d(n)^2 \cdot \hat{V}_{IN}^2 \cdot \sin^2\left(\frac{n \cdot \pi}{N}\right) \cdot (V_{C1} + V_{OUT})}{2 \cdot L_1 \cdot \left(V_{C1} + V_{OUT} - \hat{V}_{IN} \cdot \sin\left(\frac{n \cdot \pi}{N}\right)\right)} \quad (2)$$

In (2), N is the number of switch cycles during one half line period, and n is a running integer.

It has been shown in numerous papers (e.g. [2], [3] and [10]) how V_{C1} can be determined numerically. By using (1) and (2) one can determine V_{C1} as a function of the ratio L_1 to L_2, the input voltage and a given output voltage. The ratio of L_1 to L_2 should be chosen so that the maximum voltage level applied to C_1 and Q_1 in Fig.2 is below the desired level.

In order to demonstrate the input current shaping a 200V output Modified SEPIC converter will be used. The use of 500V MOSFETs is desirable, so the ratio of L_1 to L_2 will be adjusted according to a maximum voltage stress on Q_1 of 450V. The capacitor C_1 should then be able to withstand 250V. With a ratio $L_1/L_2 = 1.25$, the voltage at the drain of Q_1 will stay below 450V.

Calculating the input current waveforms for a design of a 100W converter operated from 185-270 Vac, results in the waveforms shown in Fig. 3.
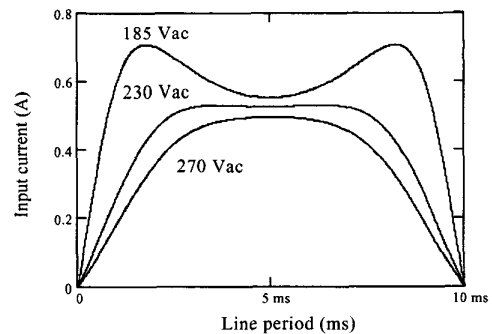

Fig. 3. Input current waveforms with line voltages of 185Vac, 230Vac and 270Vac for the Modified SEPIC converter with fast output regulation. P_{OUT}=100W.
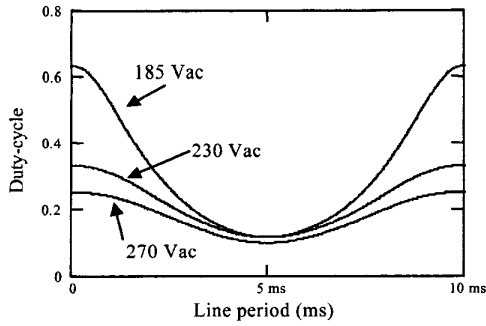
667

Fig. 4. Duty-cycle variations given by (1) for 185Vac, 230Vac and 270Vac. L_1 = 250 uH.

Figure 4 shows the time varying duty-cycle. The increasing duty-cycle when the line voltage drops from the peak value, is responsible for the current shaping.

Designing the fast outer voltage loop becomes increasingly difficult the larger the output capacity becomes. In the standard boost converter the output capacitor has to be large enough to decouple the pulsating input-power to meet the required ripple-voltage specifications. For the Modified SEPIC converter C_1 serves as the decoupling capacitor, so small polyester capacitors can be used at the output. If hold-up time is required, the main energy storage is then the series bulk capacitor, C1.

The amount of energy stored is given by:

$$E_{Cap.} = \tfrac{1}{2} \cdot C \cdot V_{CB}^2 \qquad (3)$$

At low line, the voltage on V_{C1} is at its minimum and it is therefore in this situation, the value of the capacitor must be chosen to secure the hold-up capability. In case of a line failure the converter performs an active energy transferring from V_{C1} to the output. With the input cut-off, the converter is reduced to a buck-boost converter.

For converters with passive energy-storage (e.g. boost, buck-boost) the useable energy can be determined by:

$$E_{Hold-up} = \tfrac{1}{2} \cdot C_O \cdot \left(V_O^2 - V_{min}^2 \right) \qquad (4)$$

In (4) C_O and V_O is the capacitance and voltage at the output, and V_{min} is the minimum voltage that can be accepted at the output.

Using (3) and (4) a comparison of the energy storage capability can be made:

$$\frac{C_B}{C_O} = \frac{V_O^2 - V_{min}^2}{V_{CB}^2} \qquad (5)$$

The Modified SEPIC converter with a maximum voltage stress of 450V at 270Vac, will have a minimum storage capacitor voltage of 100V at 185Vac. If the same size capacitor where to be used in a PFC buck-boost converter with an output voltage of 200V, using (5), the minimum voltage that the buck-boost converter should be able to handle is 173V, or a voltage drop of 13.5% of the output voltage. If the following DC/DC-stage can handle a larger voltage drop, the hold-up capabilities are better for the buck-boost converter and vice versa.

B. Constant peak-current control

By using fast regulation of the output, the resulting duty-cycle was seen to have a good current shaping quality. Using peak-current control with a slow voltage loop will also provide inherent high-quality input-current shaping.

When keeping the switch peak-current constant over one half line period, the duty-cycle function can be described as:

$$d(t) = \frac{I_{ref}}{T_{Switch} \cdot \left(\dfrac{\hat{V}_{IN} \cdot \sin(\omega t)}{L_1} + \dfrac{V_{C1}}{L_2} \right)} \qquad (6)$$

In (6) Iref is the demand peak-current set by the voltage loop. Since the voltage loop is slow, this reference current can be regarded as a constant, also with regard to the line period.

By inserting (6) into (1) and (2), the bulk capacitor voltage V_{C1} can be calculated in the same manner as before.

The duty-cycle function for a 200W, 200V Modified SEPIC converter is shown in Fig. 5, and the resulting input current is shown in Fig. 6. The values of L_1 and L_2 are 220 uH and 160 uH.
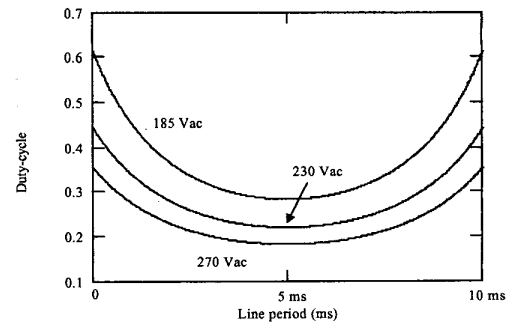

Fig. 5. The duty-cycle variation for the Modified SEPIC converter with constant peak-current control. P_{OUT} = 200W.
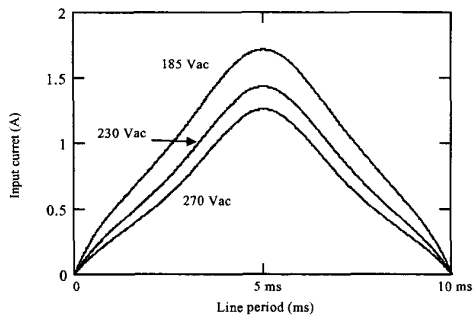
668

Fig. 6. Input-current waveform for the Modified SEPIC converter with constant peak-current control.

The resulting current waveforms shown in Fig. 6, is not far from being sinusoidal.

In the constant peak-current controlled converter, the energy storage can be placed at the output without creating stability problems. But in order to keep the voltage relatively constant on C_1, a certain amount of capacitance should make up this capacitor.

With respect to the hold-up capability, it is not indifferent where the capacitance is located. The total energy storage to be used in case of a line failure is now, for the Modified SEPIC converter with a bulk capacitor at the output, the sum of (3) and (4). This means, that if the left side of (5) is larger than 1, the capacitance is more useful at the output and vice versa.

C. Alternative control strategies

The simple voltage follower approach can also be used. The input current will exhibit the same properties as a boost converter operated in the same way.

A dedicated PFC control scheme is of course always a possibility if unity PF is the goal.

IV. EXPERIMENTAL RESULTS

To verify the two operation modes, two prototypes have been tested. From a Power Factor point of view, the constant peak-current approach offers the most consistent high-quality current and the attention will therefore mainly be on the constant peak-current controlled converter (prototype 2).

A. Prototype 1

The first prototype with the fast-regulated output voltage was tested with a simple voltage feedback loop. A 100W 200V output for 185-270Vac input voltage were build. The following component values were used: L_1 = 250uH, L_2 =

200uH, C_1 = 680uF/250V, C_2 = 2.2uF/250V, Q_1 = IRF830 (500V). Fig. 7 shows the resulting input current for line voltages of 185Vac, 230Vac and 270Vac.
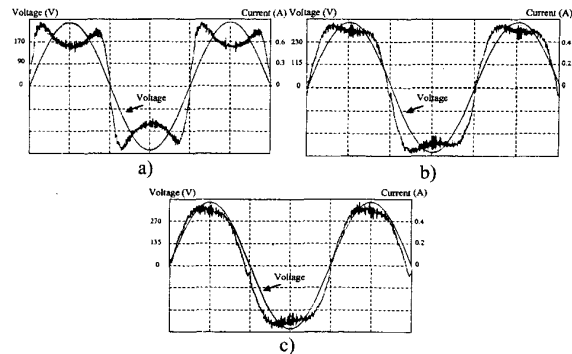

Fig. 7. Input-current of the Modified SEPIC converter with fast output regulation a) Vin = 185Vac, PF=0.89. b) Vin = 230Vac, PF=0.97. c) Vin = 270Vac, PF=0.98.
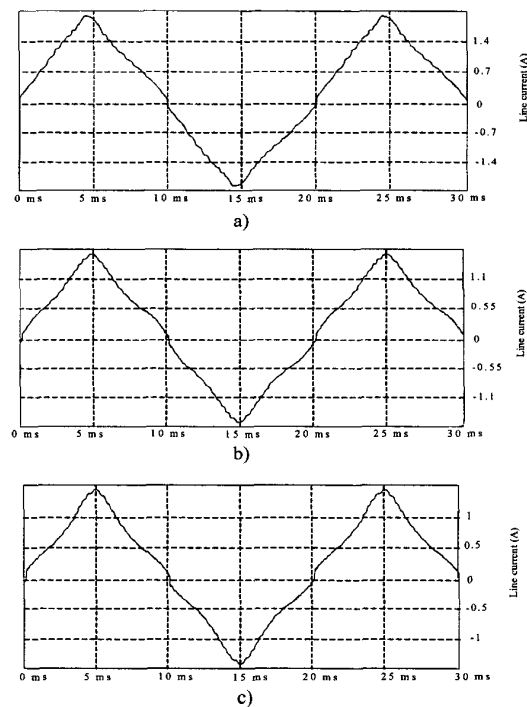

Figure 8. Input current for prototype 2 of the Modified SEPIC converter with constant peak-current control. a) Vac=185, PF = 0.992. b) Vac=230, PF =0.990. c) Vac=270, PF = 0.986

There is very god correlation with the predicted input-current waveforms of Fig. 3. The asymmetry of the waveforms of Fig. 7 is caused by the 100Hz voltage variation

669

on the bulk capacitor C_1. Even though the PF drops rapidly when the line voltage decreases, the harmonic content of the current (not shown), is well below the limits of EN61000-3-2, both class D and class A.

B. Prototype 2

The second prototype was realized with the constant peak-current control. The experimental results were taken from a 200W, 200V output for 185Vac-270Vac. The following component values were used for this prototype: $L_1 = 220uH$, $L_2 = 160uH$, $C_1 = 680uF/250V$, $C_2 = 680uF/250V$, $Q_1 = IRFBX10N50A (500V)$.

The input-current of the Modified SEPIC converter with the constant peak-current control is shown in Fig. 8. Again, the correlation between the predicted current waveforms of Fig. 6 and the experimental obtained is very good.

Fig. 9 shows the efficiency for the nominal line voltage of 230Vac as a function of the output-power, and Fig. 10 shows the efficiency as a function of the line voltage (185Vac-270Vac) at 200W.
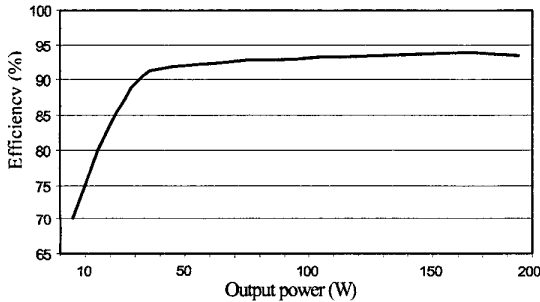

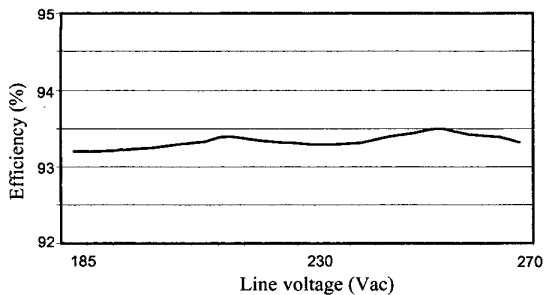Fig.9. Efficiency as a function of output-power for 230Vac line voltage (prototype 2).

Fig. 10. Efficiency as a function of the line voltage at P_{OUT}=200W for prototype 2.

The efficiency at maximum output power over the line voltage variation is above 93%. The line variation has very little effect on the efficiency, below 0.5% percent. Compared to a boost converter, the high-line efficiency of the Modified SEPIC converter is relatively far away from what can be expected from a boost converter, but at the low line, this relation improves. Since a 400VDC link-voltage not necessarily is the optimal operation point for the following DC/DC stage, the total system efficiency could be as good, or better than a standard approach with a boost converter.

V. FUTURE WORK

The Modified SEPIC converter is not restricted to operate in DCM, even though this paper has only dealt with this operation mode. Ongoing work shows, that CCM operation is possible using the constant peak-current control. A working 200W prototype for universal mains (90Vac – 270Vac) is being investigated and the results obtained in this work, will be presented in a future paper.

VI. CONCLUSSION

The task of shaping the input current to comply with EN61000-3-2 can be achieved using standard DC/DC control IC's. Reducing the voltage stress to a level where the range of components is larger makes the design easier to dedicate to a specific application.

For the Modified SEPIC converter the most important pros and cons are:

Pros
  • Component voltage stress comparable with boost converters
  • High quality input-current shaping
  • Current limiting capabilities
  • Uses standard current-mode control ICs

Cons
  • High current stress in the switch
  • High current stress in the series bulk capacitor
  • Inrush current limiting and galvanic isolation is lost (compared to the classical SEPIC)

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670

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