

Input-parallel Output-series DC-DC Boost Converter with a Wide Input Voltage Range, for Fuel Cell Vehicles

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ABSTRACT: An input-parallel, output-series DC-DC Boost converter with a wide input voltage range is proposed in this paper. An interleaved structure is adopted in the input side of this converter to reduce input current ripple. Two capacitors are connected in series on the output side to achieve a high voltage-gain. The operating principles and steady-state characteristics of the converter are presented and analyzed in this paper. A 400V/1.6kW prototype has been created which demonstrates that a wide range of voltage-gain can be achieved by this converter and it is shown that the maximum efficiency of the converter is 96.62%, and minimum efficiency is 94.14%. The experimental results validate the feasibility of the proposed topology and its suitability for fuel cell vehicles.

KEY WORDS: Input-parallel output-series; Wide voltage-gain range; Current ripple; Voltage stress; Fuel cell vehicles.

I. INTRODUCTION

Traditional fossil fuel resources are depleting quickly, but their continued use contributes to increasing pollution [1]-[3]. Development of clean energy systems is essential. Photovoltaic power generation, wind power generation and fuel cell power generation are important clean energy technologies [4]-[6]. With regard to transport, clean-energy vehicles which include fuel cell vehicles, pure electric vehicles, and hybrid energy source vehicles can be considered one of the most essential applications for clean-energy [7]-[8]. Fuel cell vehicles can provide clean propulsion power with zero emission, as well as higher energy utilization [9]. However, the use of fuel cells brings challenges, particularly with their low output voltage and high output current [10]. The main DC link bus of fuel cell vehicles has a high voltage level (400V), making it difficult to directly match voltages between the fuel cell stack and the main DC link bus. The fuel cell also has a “soft” output characteristic [11] –

its output voltage varies with load – and it must be interfaced to the main DC link bus through a step-up DC-DC converter with a wide range of voltage-gain. In addition the input current ripple of the converter for fuel cells must be low enough to prevent accelerated reduction of the life time of the fuel cell [12].

The conventional DC-DC Boost converter is employed due to its simple structure, but it suffers from disadvantages including limited voltage-gain due to parasitic parameters and the extreme duty cycle, and high voltage stress for its power semiconductors. The conventional interleaved Boost DC-DC converter can obtain low input current ripple, but this converter still has certain disadvantages including limited voltage-gain and high voltage stress for power semiconductors. The voltage stress for power semiconductors in the three-level DC-DC Boost converter in [13] can be reduced by half, but its voltage-gain is still limited. What's more, the output and input sides of this converter are connected by a diode; the potential difference between the two sides is a high frequency PWM voltage, which may result in additional maintenance requirements and increased EMI. The output and input sides of the Boost three-level DC-DC converter in [14] share a common ground, but the voltage-gain of this converter is still restricted. In addition, this converter requires a complicated control scheme to balance the flying-capacitor voltage. The multilevel DC-DC Boost converter in [15] obtains a high voltage-gain, and low voltage stress for the power semiconductors. However, this converter is too complex for automotive applications and requires reductions in cost and size. The converter proposed in [16] uses a Z source network to achieve a higher voltage-gain, but the output and the input sides do not share a common ground, which may result in

maintenance safety issues and additional EMI. The Quasi-Z source network is applied to the conventional Boost DC-DC converter in [17]. This converter, with high voltage gain also has a high voltage stress for the power semiconductors. The converter in [18] which applied a switched-inductor structure, can achieve a high voltage-gain, but a diode in the converter suffers high voltage stress. Non-isolated DC-DC converters with coupled inductors can obtain a high voltage-gain, low voltage stress for power semiconductors and high efficiency. There are many types of DC-DC converters with coupled inductors discussed in [19]-[22]. The converter with coupled inductors in [19] can obtain a high voltage-gain and low voltage stress for power semiconductors, but it suffers high ripple of input current. Interleaved boost converters with coupled inductors discussed in [20] have advantages of high voltage-gain and low input current ripple. However, these converters have high voltage stress for power semiconductors. Stacked high step-up coupled-inductor boost converters discussed in [21] can obtain a very high voltage-gain and low voltage stress for power semiconductors, but the input current ripple of these converters are higher. The interleaved boost converters with winding-cross-coupling mentioned in [21] obtain a high voltage-gain, low voltage stress for power semiconductors and low input current ripple. The Cascaded boost converters [22] can also obtain a high voltage-gain, but these converters have high input current ripple. In addition, their efficiencies are the product of the efficiency of each stage.

Some of the DC-DC converters described do not provide low input current ripple, high voltage-gain, and low voltage stress for power semiconductors at the same time. In this paper, an input-parallel output-series DC-DC Boost converter with a wide input voltage range is proposed as a solution. Compared with the conventional interleaved DC-DC Boost converter and the three-level DC-DC Boost converter, this converter has advantages including low input current ripple, low voltage stress for power semiconductors, and high voltage-gain. In addition, the potential difference between the output and the input sides of this converter

is a capacitor voltage rather than a high frequency PWM voltage. This paper is organized as follows: in *Section II*, the topology of the input-parallel output-series Boost DC-DC converter is presented. The operating principles of the converter topology are discussed in *Section III*. In *Section IV*, the steady-state characteristics of the converter are analyzed. The experimental results and analysis are given in *Section V*. Finally, the conclusions are presented in *Section VI*.

II. TOPOLOGY OF PROPOSED CONVERTER

The proposed input-parallel output-series DC-DC Boost converter is shown in Fig. 1. The conventional DC-DC Boost converter topology can be formed by inductor L_1 , power switch Q_1 , diode D_1 and capacitor C_2 . Similarly, inductor L_2 , power switch Q_2 , and capacitors C_1 and C_3 constitute a Boost DC-DC converter whose output voltage polarity is opposite to the input voltage polarity. These two converters are connected in parallel at the input side and in series at the output side: this arrangement forms the input-parallel output-series DC-DC Boost converter.

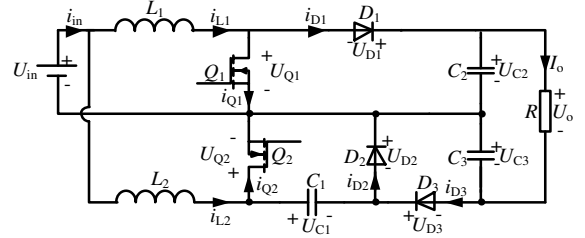


Fig. 1 The topology of the input-parallel output-series DC-DC Boost converter.

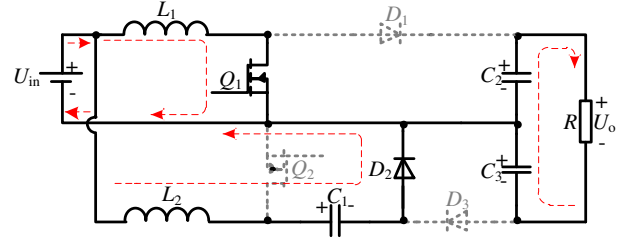
The topology of the converter comprises 2 inductors, 2 active power switches and 3 diodes. It is assumed that $L_1=L_2$, $C_1=C_2=C_3$, U_{in} is the input voltage, and i_{in} is the input current. i_{L1} and i_{L2} are the currents flowing through L_1 and L_2 respectively. The currents of Q_1 , Q_2 , D_1 , D_2 , and D_3 are i_{Q1} , i_{Q2} , i_{D1} , i_{D2} , and i_{D3} respectively. In addition, U_{D1} , U_{D2} , U_{D3} , U_{C1} , U_{C2} , and U_{C3} are the voltage stress of D_1 , D_2 , D_3 , C_1 , C_2 , and C_3 respectively. U_o is the output voltage, and I_o is the output current. An interleaved structure is adopted in the input side of this converter to reduce input current ripple. In addition, the two capacitors at the output side are connected in series to obtain a high voltage-gain.

III. OPERATING PRINCIPLES

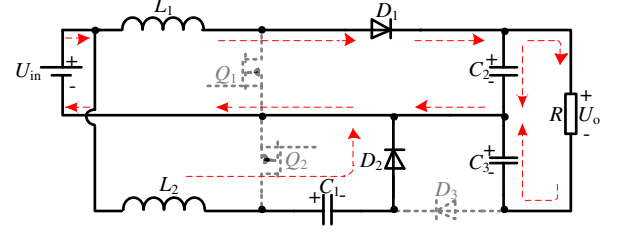
In order to analyze the steady-state characteristics of the proposed converter, the operation conditions are assumed to be as follows: (a) all the power semiconductors and energy storage components are ideal, which means the on-state resistances of power semiconductors, the forward voltage drop of the diodes, and the equivalent series resistances (ESRs) of the inductors and capacitors are ignored. (b) all the capacitances are large enough such that each capacitor voltage can be treated as constant. An interleaved structure is used in the input side of this converter. In this case, the relationship between d_1 and d_2 can be written as $d_1=d_2=d$, where d_1 and d_2 are the duty cycles of Q_1 and Q_2 respectively. The phase difference between the gate driving signals of Q_1 and Q_2 is 180° .

According to the operation of Q_1 and Q_2 , when the proposed converter operates in the continuous conduction mode (CCM), there are four switching states described as " S_1S_2 " in a switching period, $S_1S_2=\{00,01,10,11\}$. In addition, the sequence of the switching states in a switching period is related to the duty cycle ranges of Q_1 and Q_2 . *Sequence I* "10-00-01-00-10" appears within the range of $0<d<0.5$, while *Sequence II* "11-10-11-01-11" is obtained within the range of $0.5<d<1$.

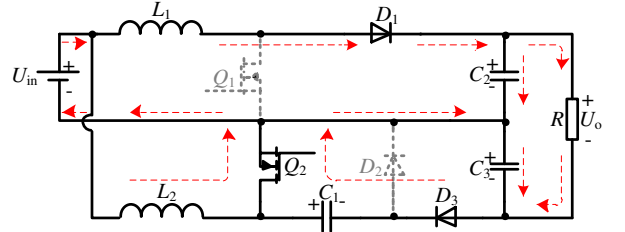
When the proposed converter operated in the discontinuous conduction mode (DCM), there are seven switching states in each switching period, $S_1S_2=\{01, 10, 11, 10_D, 01_D, 00_{D1}, 00_{D2}\}$. "10_D" represents the conditions of Q_1 is turned on, Q_2 is turned off, and $i_{L2}=0$. "01_D" means that Q_1 is turned off, Q_2 is turned on, and $i_{L1}=0$. "00_{D1}" represents that Q_1 and Q_2 are turned off, and $i_{L1}=0$. "00_{D2}" means that Q_1 and Q_2 are turned off, and $i_{L2}=0$. In addition, *Sequence I* "10-10_D-00_{D2}-01-01_D-00_{D1}-10" appears within the range of $0<d<0.5$, while *Sequence II* "11-10-10_D-11-01-01_D-11" can be obtained within the range of $0.5<d<1$. Tab. 1 shows the on-off states of power semiconductors in each switching state. Energy flow paths in each switching state of the converter are shown in



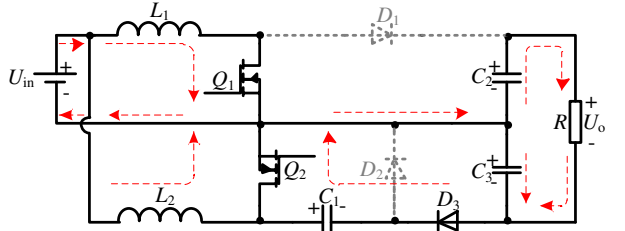
(a) $S_1S_2=10$



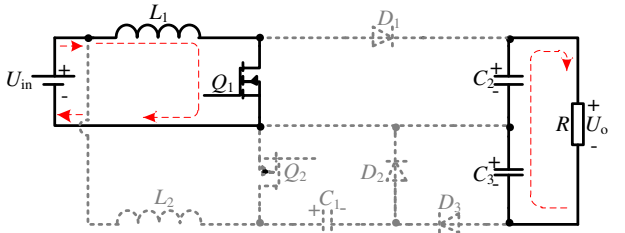
(b) $S_1S_2=00$



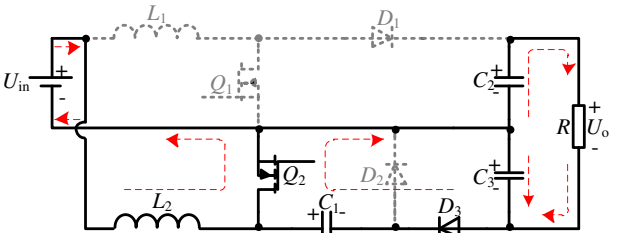
(c) $S_1S_2=01$



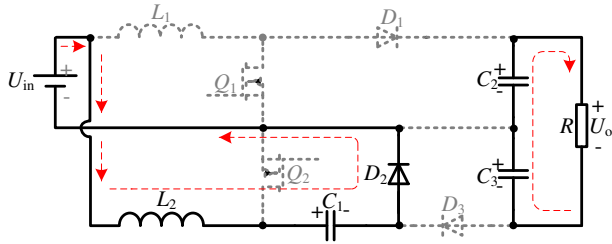
(d) $S_1S_2=11$



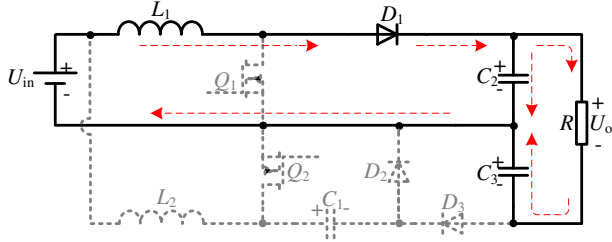
(e) $S_1S_2=10_D$ (DCM)



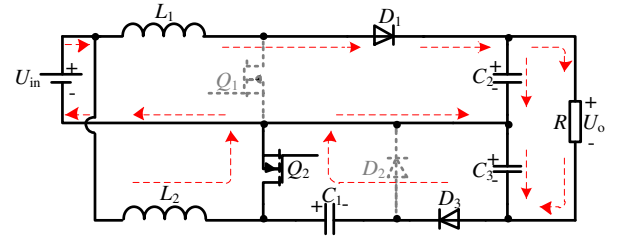
(f) $S_1S_2=01_D$ (DCM)



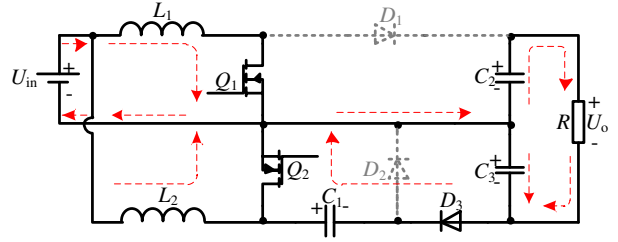
(g) $S_1S_2=00_{D1}$ (DCM)



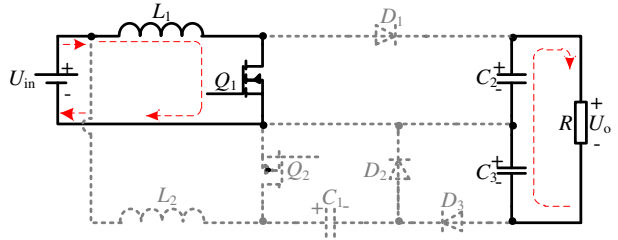
(h) $S_1S_2=00_{D2}$ (DCM)



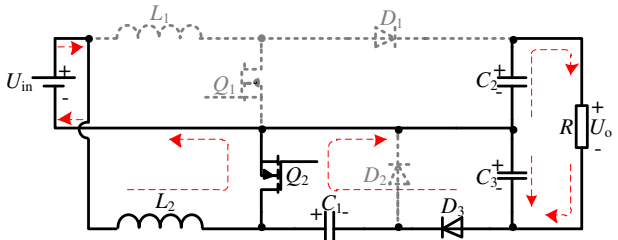
(c) $S_1S_2=01$



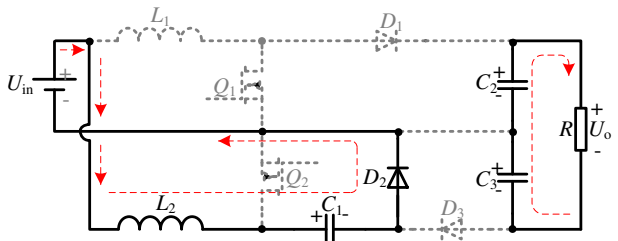
(d) $S_1S_2=11$



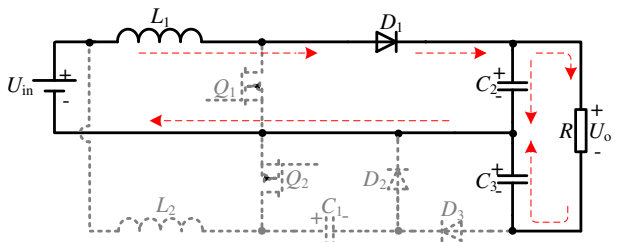
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



(g) $S_1S_2=00_{D1}$ (DCM)

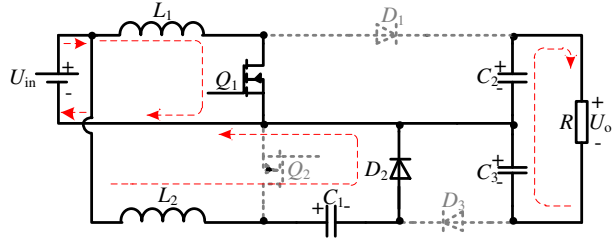


(h) $S_1S_2=00_{D2}$ (DCM)

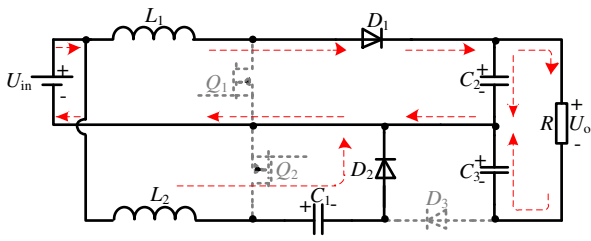
Fig. 2. The main waveforms for the proposed converter are given in Fig. 3.

Tab. 1 ON-OFF states of power semiconductors in each switching state

Switching state S_1S_2	Q_1	Q_2	D_1	D_2	D_3
10	ON	OFF	OFF	ON	OFF
00	OFF	OFF	ON	ON	OFF
01	OFF	ON	ON	OFF	ON
11	ON	ON	OFF	OFF	ON
10_D	ON	OFF	OFF	OFF	OFF
01_D	OFF	ON	OFF	OFF	ON
00_{D1}	OFF	OFF	OFF	ON	OFF
00_{D2}	OFF	OFF	ON	OFF	OFF

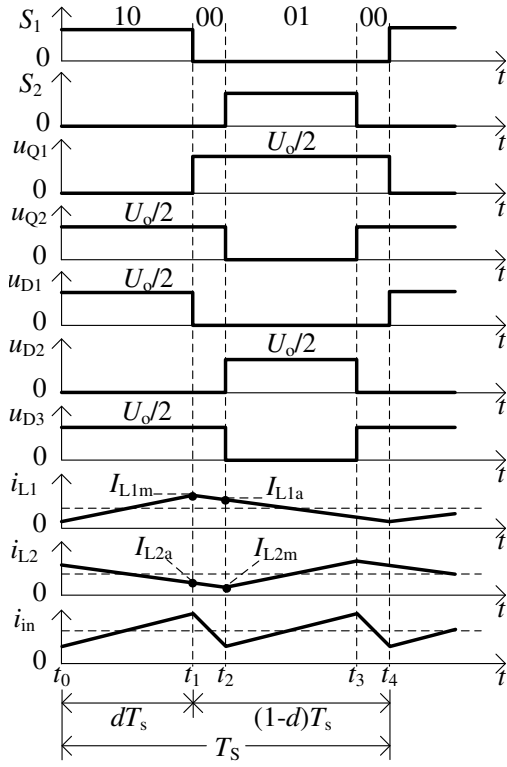


(a) $S_1S_2=10$

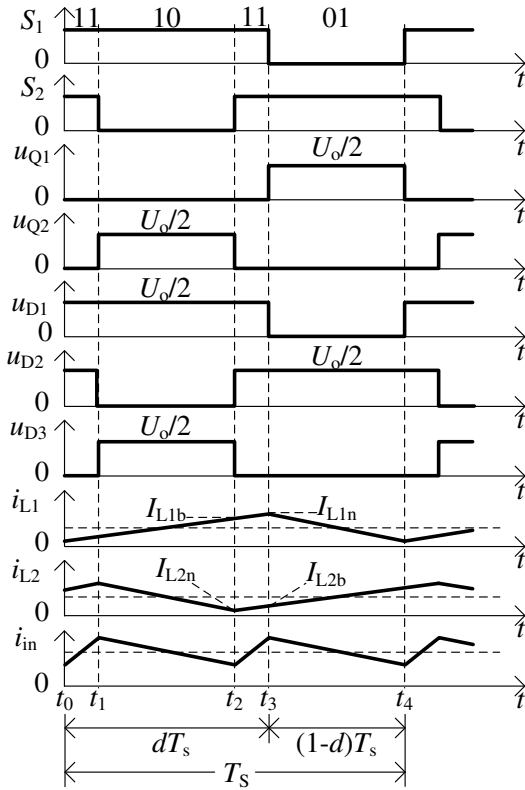


(b) $S_1S_2=00$

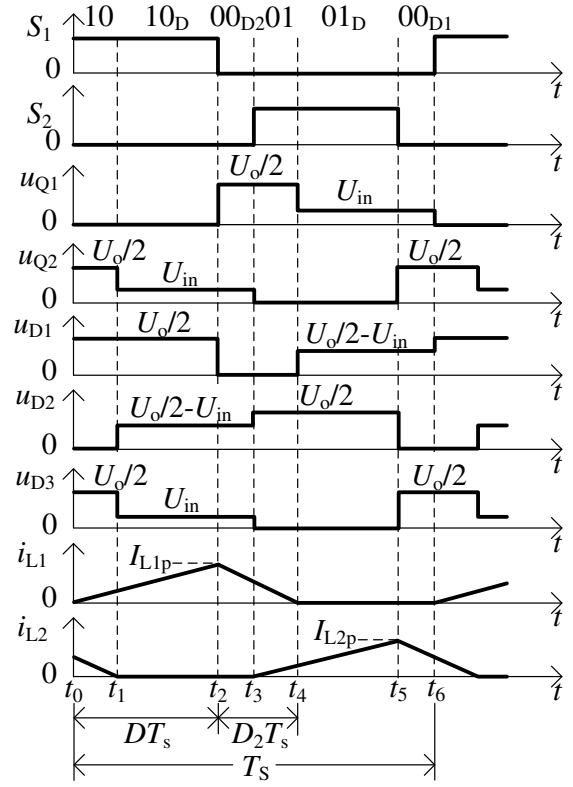
Fig. 2 Energy flow paths in each switching state.



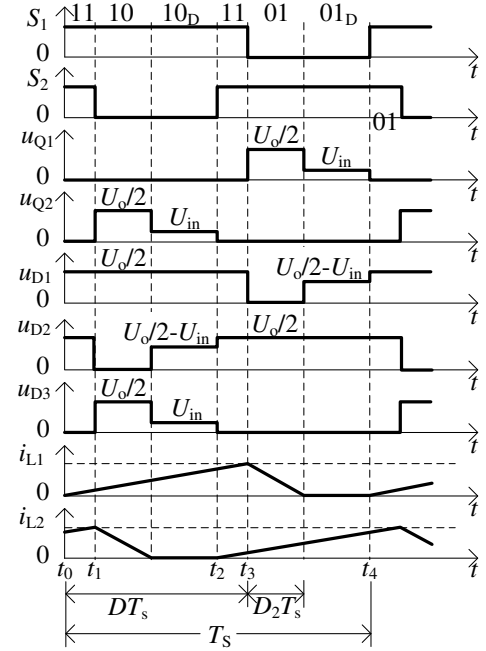
(a) The main waveforms in the range of $0 < d < 0.5$ (CCM)



(b) The main waveforms in the range of $0.5 < d < 1$ (CCM)



(c) The main waveforms in the range of $0 < d < 0.5$ (DCM)

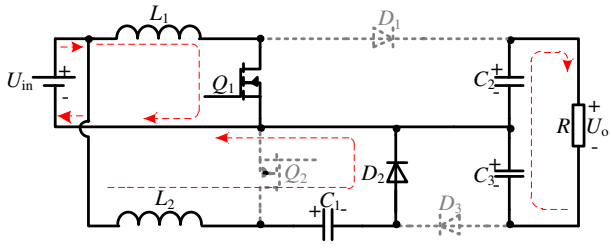


(d) The main waveforms in the range of $0.5 < d < 1$ (DCM)

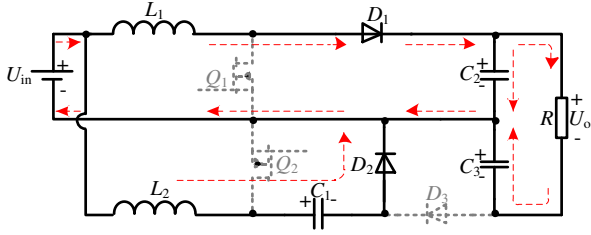
Fig. 3 The main waveforms for the proposed converter.

A. CCM operation

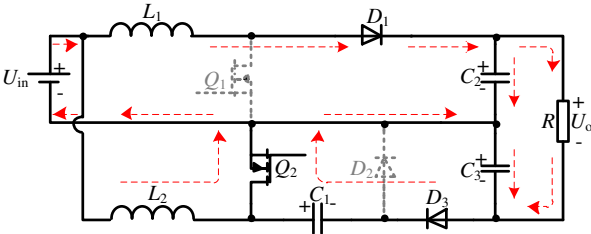
When $S_1S_2=10$: power switch Q_1 is turned on and Q_2 is turned off. Diodes D_1 and D_3 are turned off, while D_2 is turned on. The energy flow path in this switching state is shown in



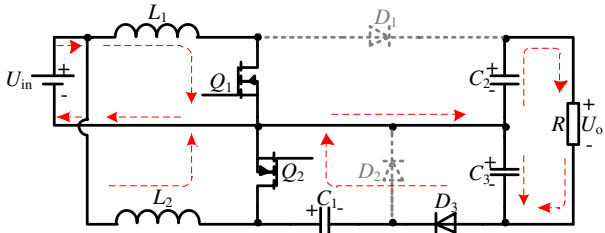
(a) $S_1S_2=10$



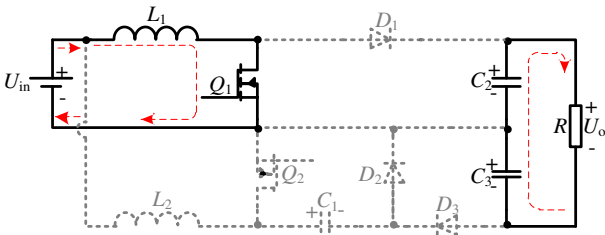
(b) $S_1S_2=00$



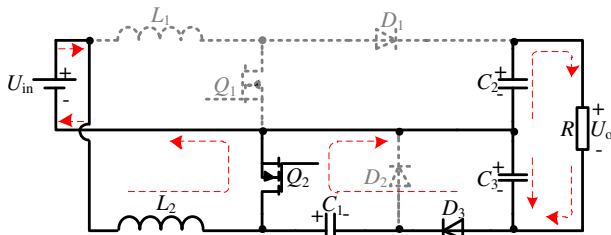
(c) $S_1S_2=01$



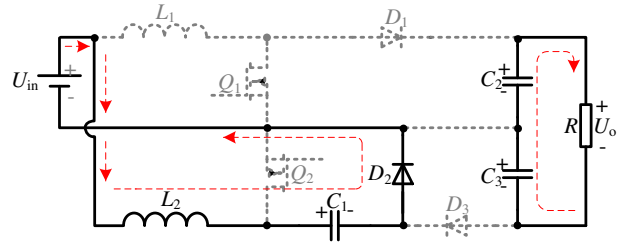
(d) $S_1S_2=11$



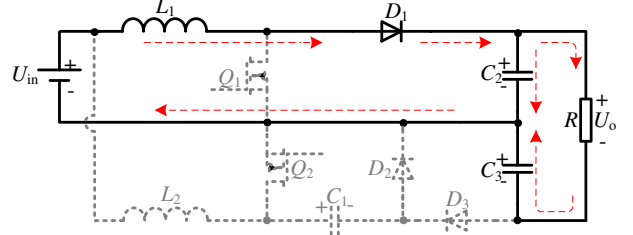
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



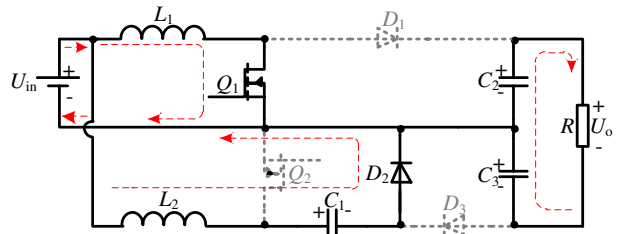
(g) $S_1S_2=00_{D1}$ (DCM)



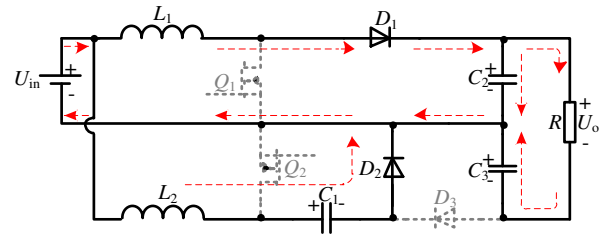
(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(a). Inductor L_1 is being charged by the DC source, while L_2 is discharging. At the same time, C_1 is being charged by inductor L_2 , while C_2 and C_3 are discharging. Capacitors C_2 and C_3 are connected in series to transfer energy to the load.

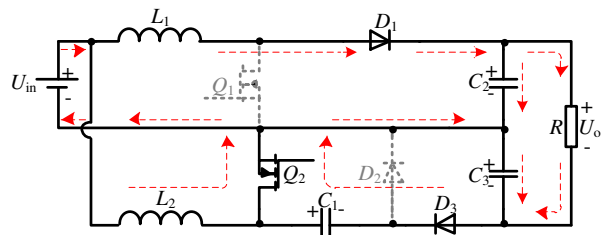
When $S_1S_2=00$: power switches Q_1 and Q_2 are turned off. Diodes D_1 and D_2 are turned on, while D_3 is turned off. The energy flow path in this switching state is shown in



(a) $S_1S_2=10$



(b) $S_1S_2=00$



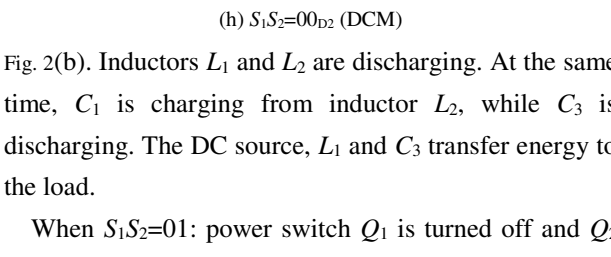
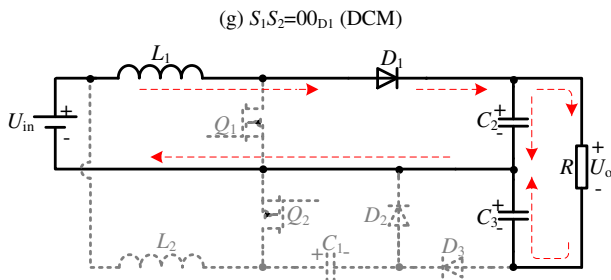
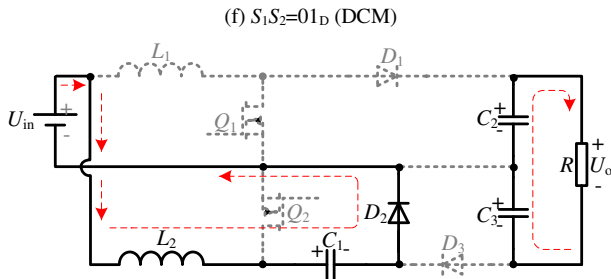
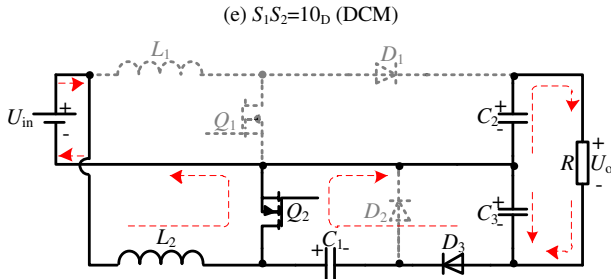
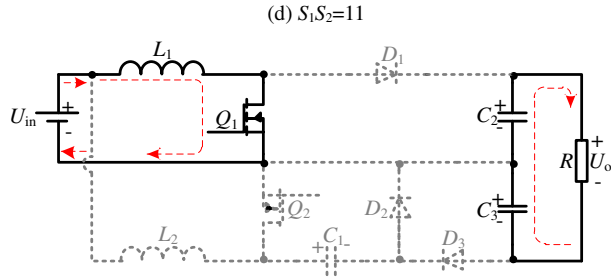
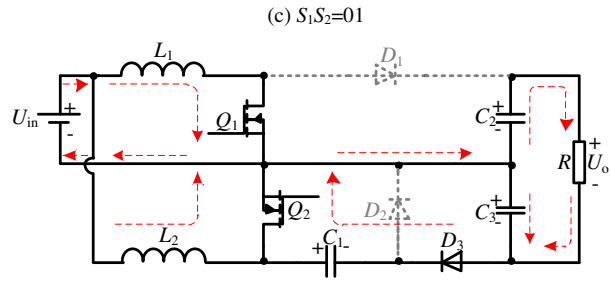
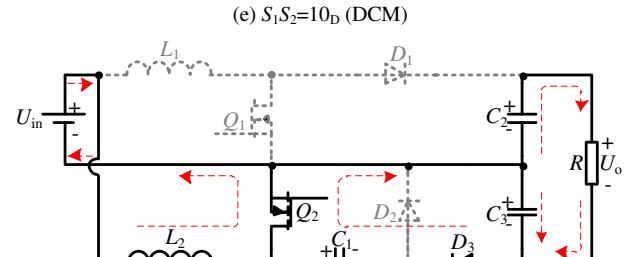
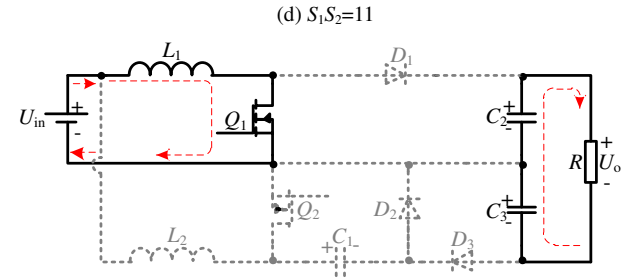
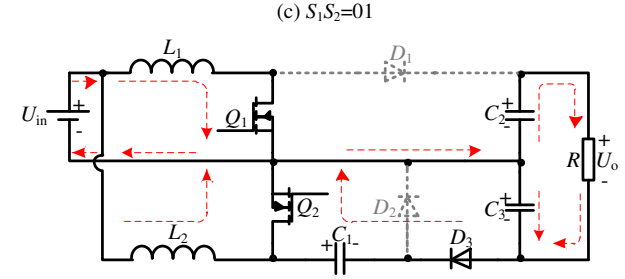
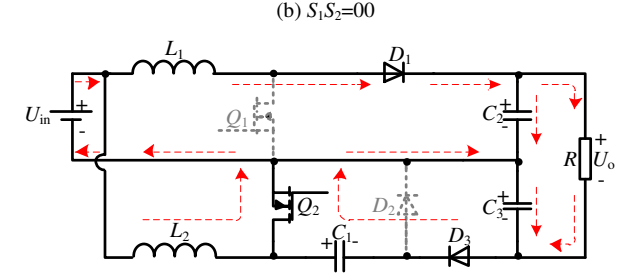
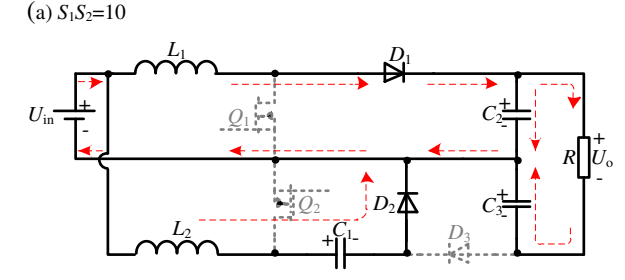
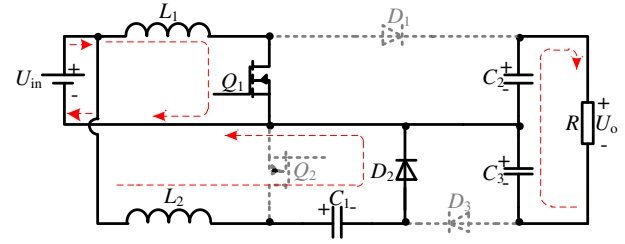


Fig. 2(b). Inductors L_1 and L_2 are discharging. At the same time, C_1 is charging from inductor L_2 , while C_3 is discharging. The DC source, L_1 and C_3 transfer energy to the load.

When $S_1S_2=01$: power switch Q_1 is turned off and Q_2 is turned on. Diodes D_1 and D_3 are turned on, while D_2 is turned off. The energy flow path in this switching state is

shown

in



(f) $S_1S_2=01_D$ (DCM)

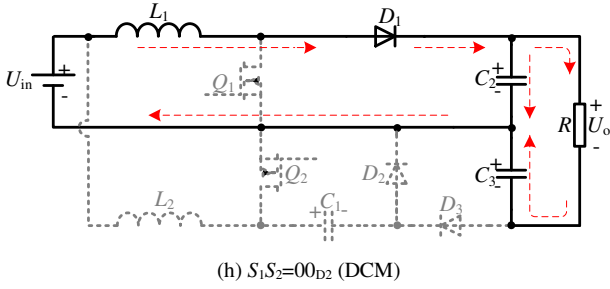
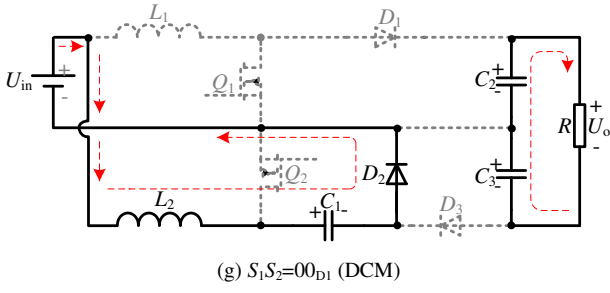


Fig. 2(c). Inductor L_1 is discharging, and L_2 is charging from the DC source. At the same time, C_2 is charging from inductor L_1 , while C_1 is discharging. In addition, C_3 is charging from C_1 . The DC source and L_1 transfer energies to the load.

When $S_1S_2=11$: power switches Q_1 and Q_2 are turned on. Diodes D_1 and D_2 are turned off, while D_3 is turned on. The energy flow path in this switching state is shown in

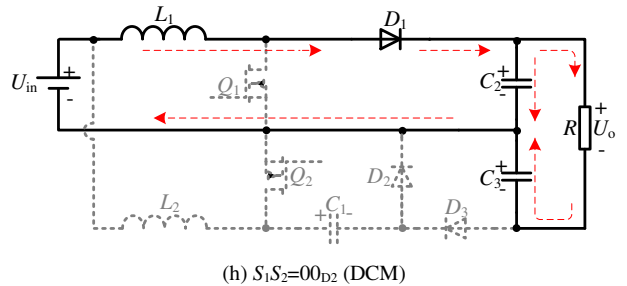
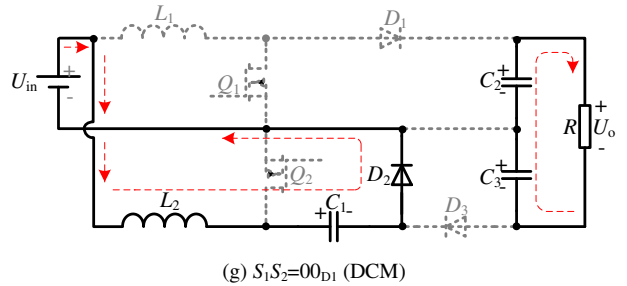
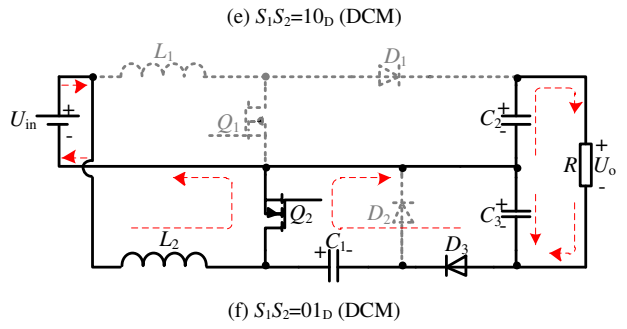
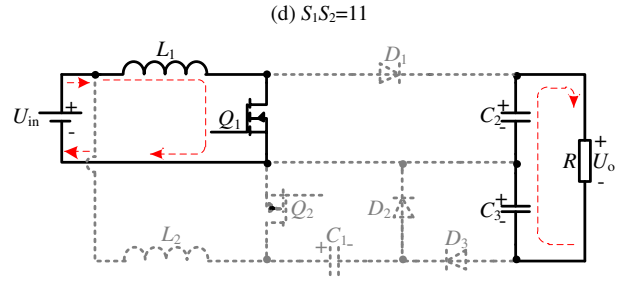
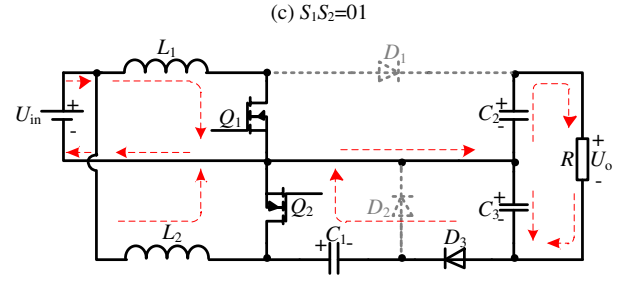
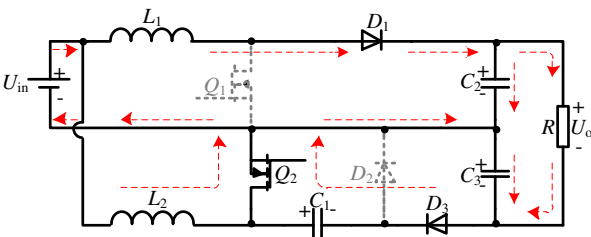
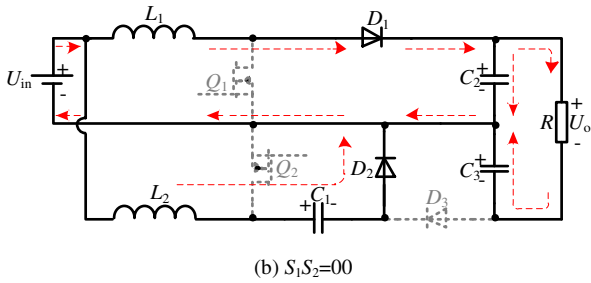
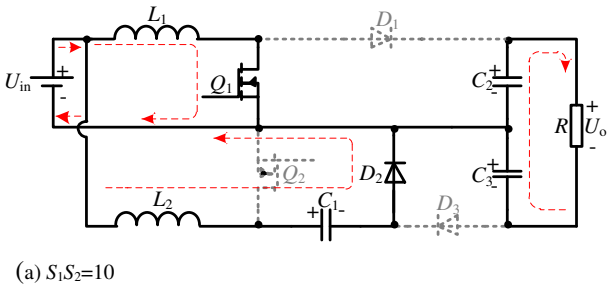
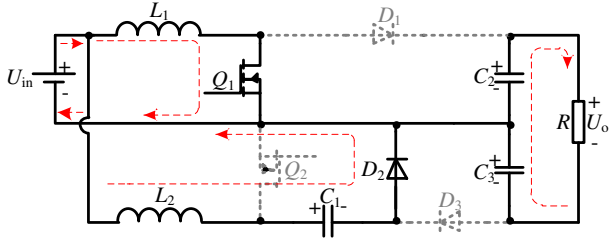


Fig. 2(d). Inductors L_1 and L_2 are charging from the DC source. At the same time, C_1 and C_2 are series connected to transfer energies to the load.

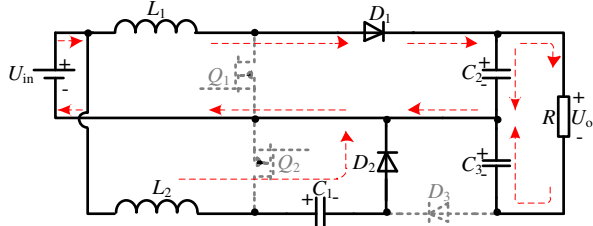
B. DCM operation

When $S_1S_2=10_D$, Q_1 is turned on and Q_2 is turned off. D_1 , D_2 and D_3 are turned off. The energy flow path in

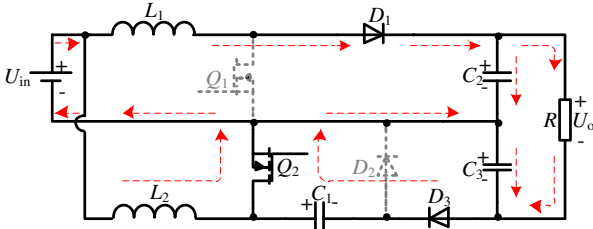
this switching state is shown in



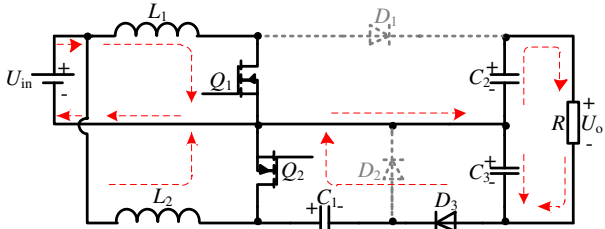
(a) $S_1S_2=10$



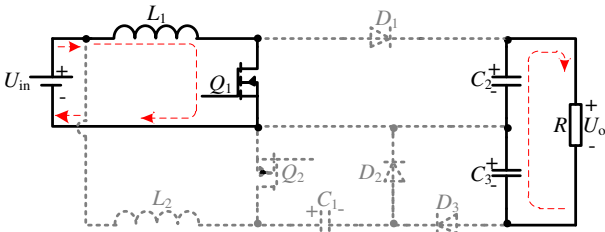
(b) $S_1S_2=00$



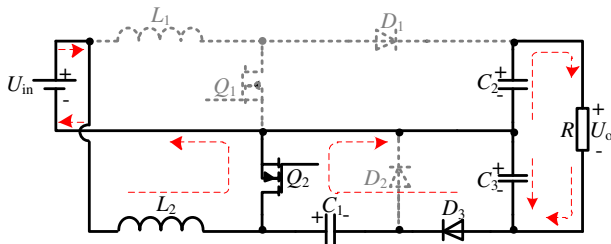
(c) $S_1S_2=01$



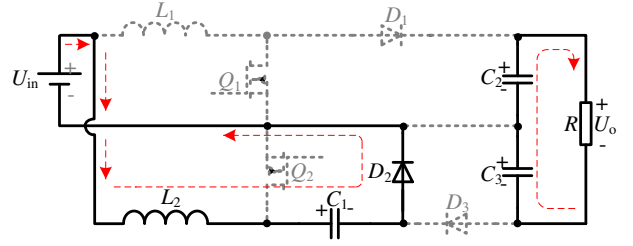
(d) $S_1S_2=11$



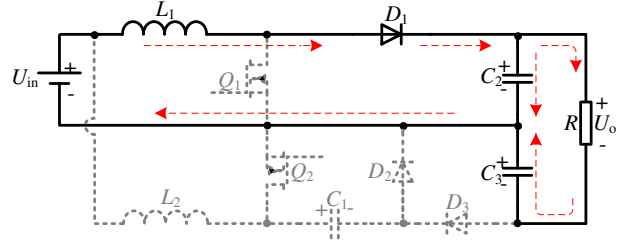
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



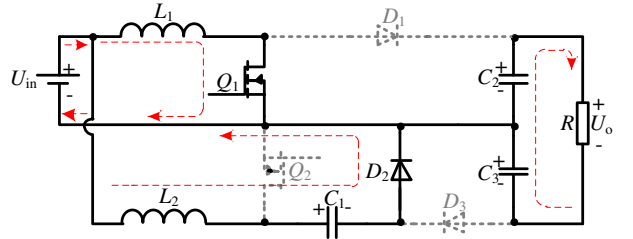
(g) $S_1S_2=00_{D1}$ (DCM)



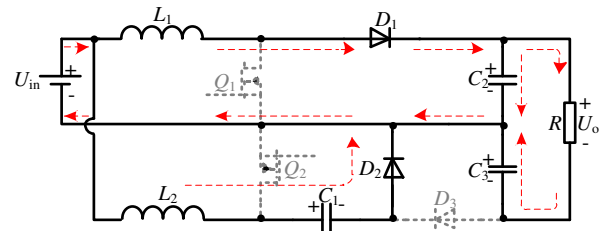
(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(e). Inductor L_1 is charging from the DC source, and inductor current i_{L2} is 0. At the same time, C_2 and C_3 are discharging in series to transfer energy to the load.

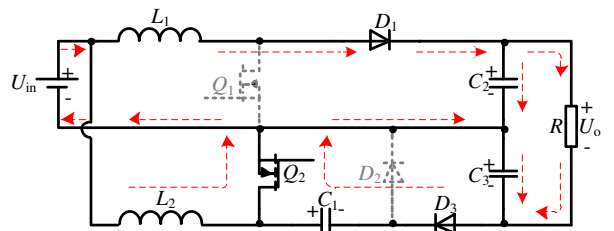
When $S_1S_2=01_D$, Q_1 is turned off and Q_2 is turned on. D_1 and D_2 are turned off, while D_3 is turned on. The energy flow path in this switching state is shown in



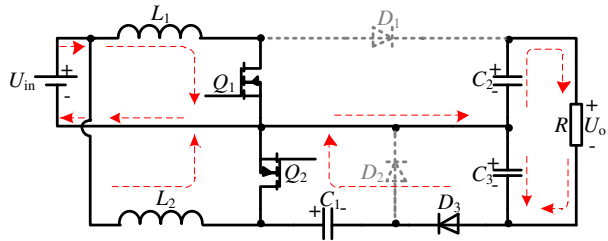
(a) $S_1S_2=10$



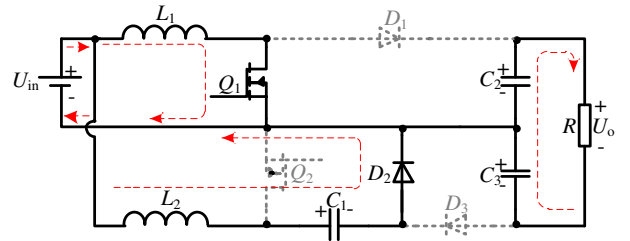
(b) $S_1S_2=00$



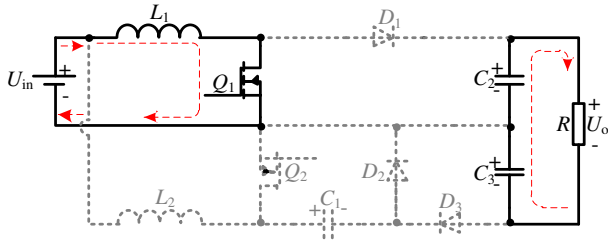
(c) $S_1S_2=01$



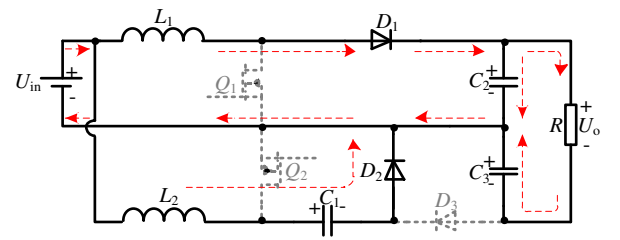
(d) $S_1S_2=11$



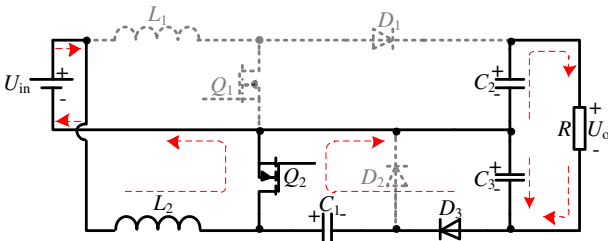
(a) $S_1S_2=10$



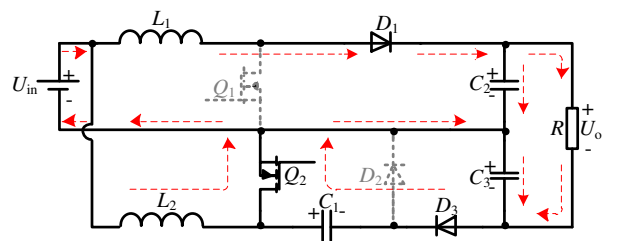
(e) $S_1S_2=10_D$ (DCM)



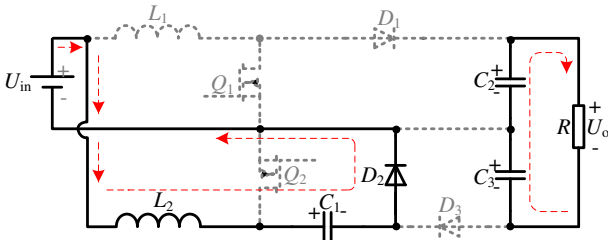
(b) $S_1S_2=00$



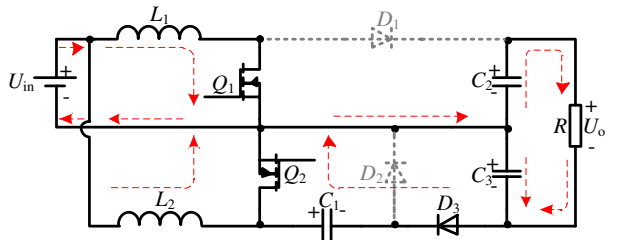
(f) $S_1S_2=01_D$ (DCM)



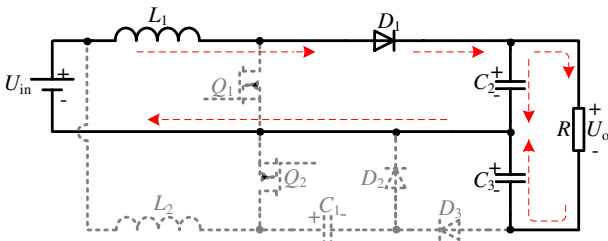
(c) $S_1S_2=01$



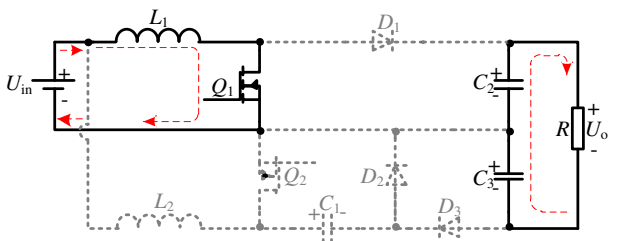
(g) $S_1S_2=00_{D1}$ (DCM)



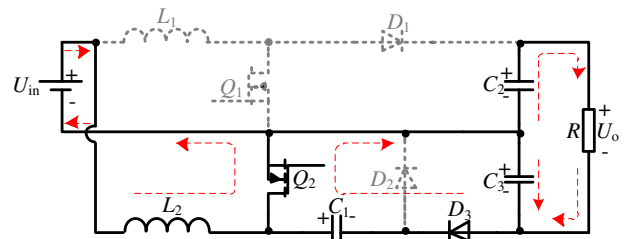
(d) $S_1S_2=11$



(h) $S_1S_2=00_{D2}$ (DCM)



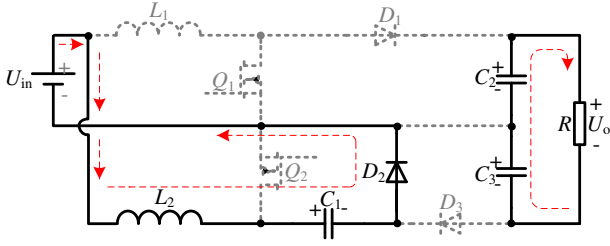
(e) $S_1S_2=10_D$ (DCM)



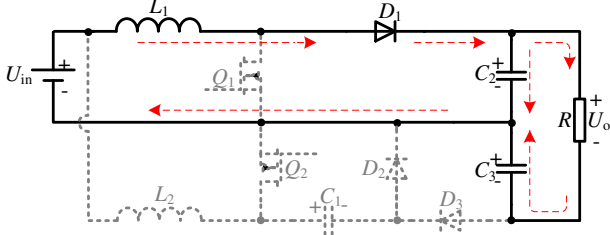
(f) $S_1S_2=01_D$ (DCM)

Fig. 2(f). Inductor current i_{L1} is 0 and inductor L_2 is charging from the DC source. At the same time, C_1 and C_2 are discharging in series to transfer energy to the load, while C_3 is charging from C_1 .

When $S_1S_2=00_{D1}$, Q_1 and Q_2 are turned off. D_1 and D_3 are turned off, while D_2 is turned on. The energy flow path in this switching state is shown in



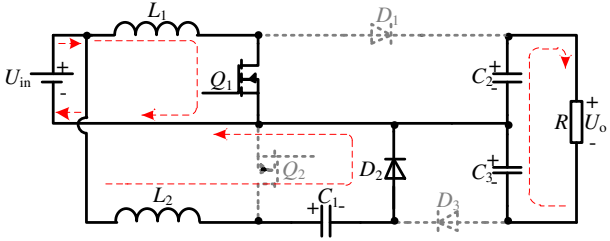
(g) $S_1S_2=00_{D1}$ (DCM)



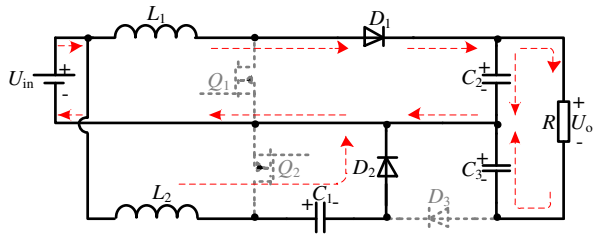
(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(g). Inductor current i_{L1} is 0, and inductor L_2 is discharging. At the same time, C_1 is charging from the DC source and L_2 , while C_2 and C_3 are discharging in series to transfer energy to the load.

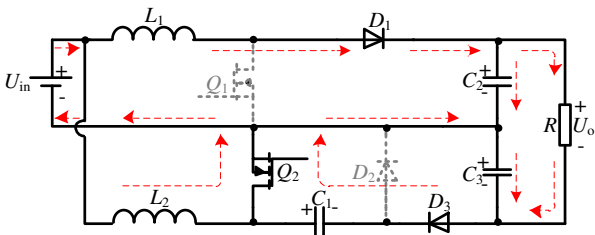
When $S_1S_2=00_{D2}$, Q_1 and Q_2 are turned off. D_1 is turned on, while D_2 and D_3 are turned off. The energy flow path in this switching state is shown in



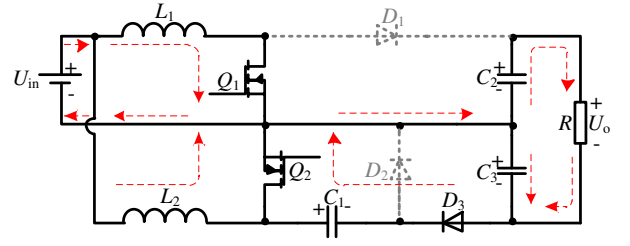
(a) $S_1S_2=10$



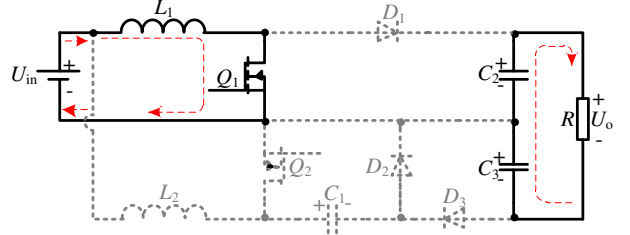
(b) $S_1S_2=00$



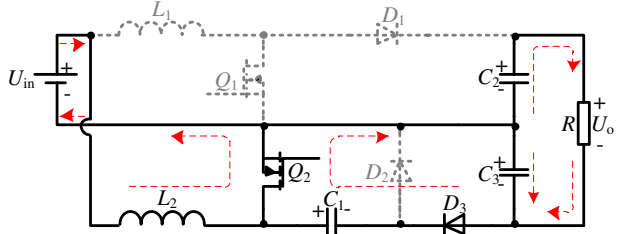
(c) $S_1S_2=01$



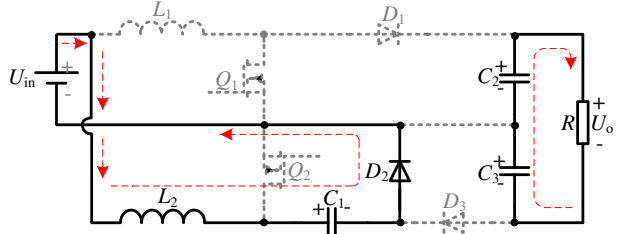
(d) $S_1S_2=11$



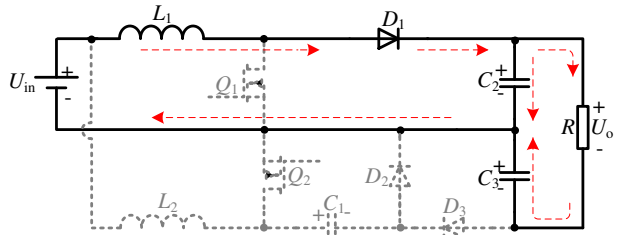
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



(g) $S_1S_2=00_{D1}$ (DCM)



(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(h). Inductor L_1 is discharging, and inductor current i_{L2} is 0. At the same time, C_2 is charging from the DC source and L_1 , while C_3 is discharging. The DC source, L_1 and C_3 transfer energy to the load.

When $S_1S_2=10$, 01 , and 11 , the operating principles of the proposed converter in DCM are the same as the ones in CCM.

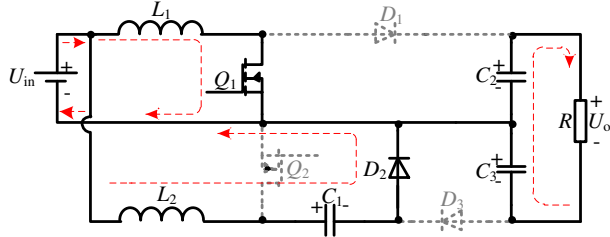
IV. ANALYSIS OF STEADY-STATE

CHARACTERISTICS

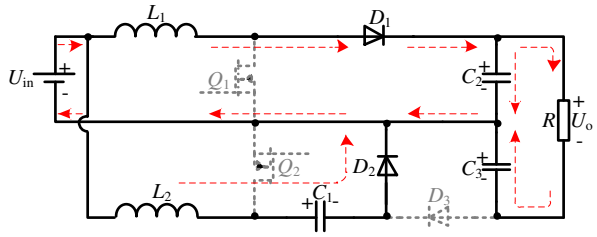
A. Voltage-gain in steady-state

1. Voltage-gain in CCM operation

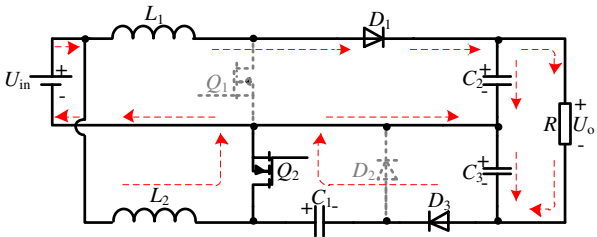
In the range of $0 < d < 0.5$, according to



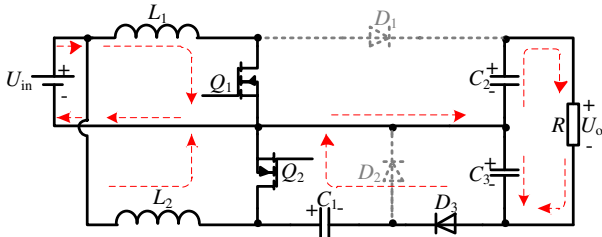
(a) $S_1 S_2 = 10$



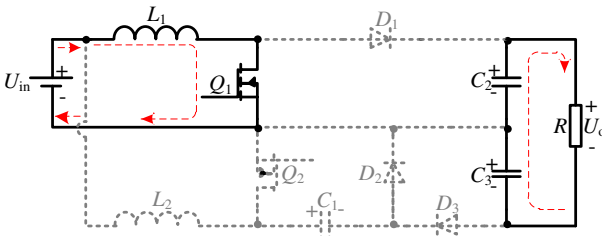
(b) $S_1 S_2 = 00$



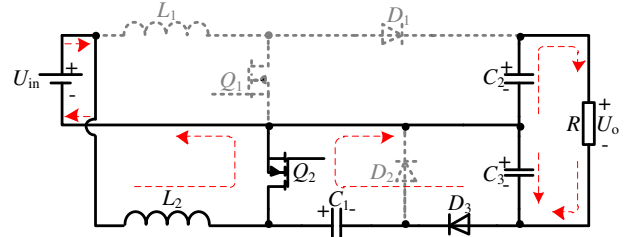
(c) $S_1 S_2 = 01$



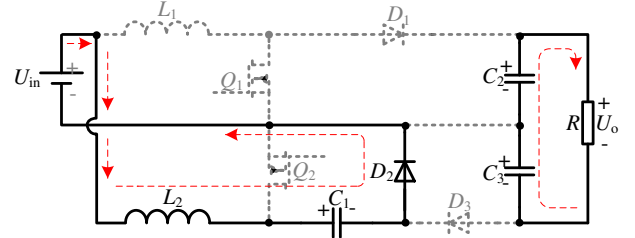
(d) $S_1 S_2 = 11$



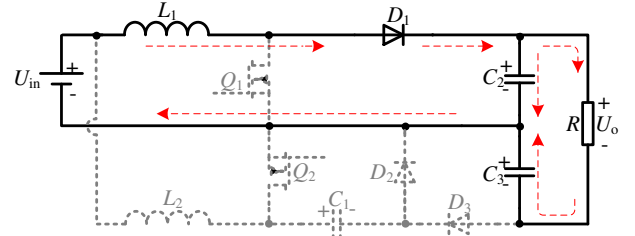
(e) $S_1 S_2 = 10_D$ (DCM)



(f) $S_1 S_2 = 01_D$ (DCM)



(g) $S_1 S_2 = 00_{D1}$ (DCM)



(h) $S_1 S_2 = 00_{D2}$ (DCM)

Fig. 2(c), power switch Q_2 and diode D_3 are turned on, so that C_1 and C_3 are connected in parallel. Therefore, the voltages of C_1 and C_3 are equal. By using the volt-second balance on L_1 and L_2 , the following equations can be obtained:

$$\begin{cases} d \times U_{in} = (1-d) \times (U_{C2} - U_{in}) \\ d \times U_{in} = (1-d) \times (U_{C1} - U_{in}) \\ U_{C1} = U_{C3} \end{cases} \quad (1)$$

Simplifying (1), the capacitor voltages and the output voltage are obtained as:

$$\begin{cases} U_{C1} = U_{C2} = U_{C3} = \frac{1}{1-d} U_{in} \\ U_o = \frac{2}{1-d} U_{in} \end{cases} \quad (2)$$

By using the amp-second balance on C_2 , the following equations can be obtained:

$$\begin{cases} d \times I_o = (1-d) \times (I_{L1} - I_o) \\ I_{in} \times U_{in} = U_o \times I_o \\ I_{in} = I_{L1} + I_{L2} \end{cases} \quad (3)$$

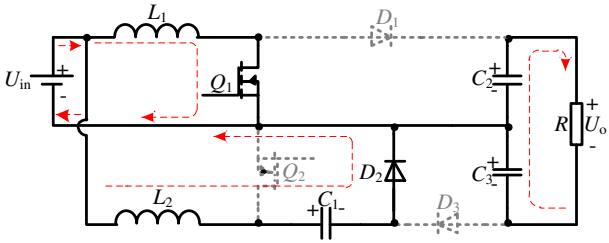
where I_{in} , I_{L1} and I_{L2} are the average currents of i_{in} , i_{L1} and i_{L2} respectively. Simplifying (3), I_{in} , I_{L1} and I_{L2} can be derived as:

$$\begin{cases} I_{in} = \frac{2}{1-d} I_o \\ I_{L1} = I_{L2} = \frac{1}{1-d} I_o \end{cases} \quad (4)$$

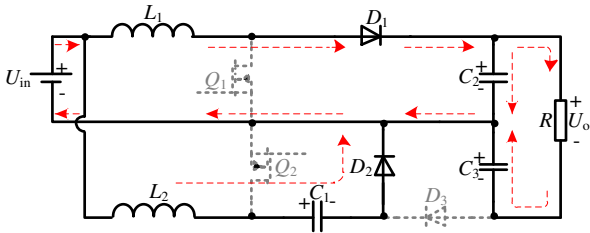
According to (2) and (4), the voltage-gain of the proposed converter is $2/(1-d)$, which is twice the voltage-gain of a conventional interleaved DC-DC Boost converter. In addition, the voltage stress of capacitors C_1 , C_2 and C_3 can be reduced to half of the output voltage. Inductor currents i_{L1} and i_{L2} are both half of the input current i_{in} . Similarly, the voltage-current relation of components within the range of $0.5 < d < 1$ can be obtained, which is the same as that within the range of $0 < d < 0.5$.

2. Voltage-gain in DCM operation

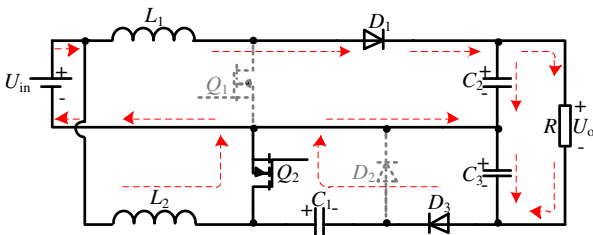
In the range of $0 < d < 0.5$, according to



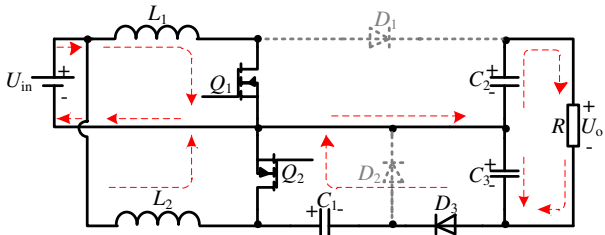
(a) $S_1S_2=10$



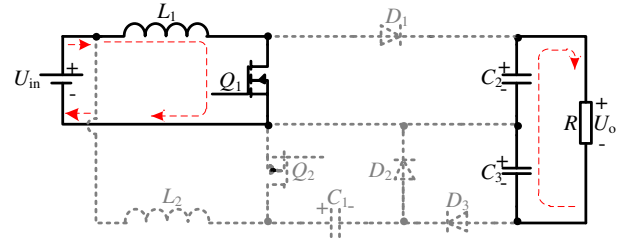
(b) $S_1S_2=00$



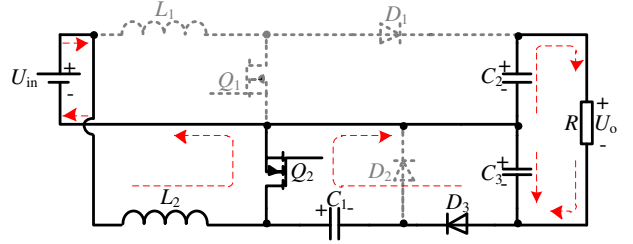
(c) $S_1S_2=01$



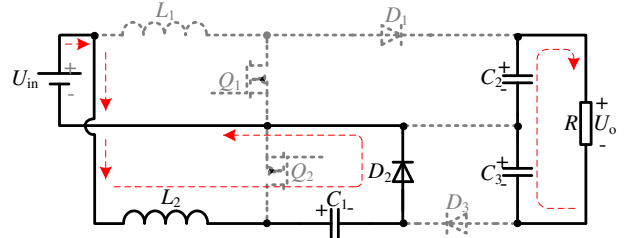
(d) $S_1S_2=11$



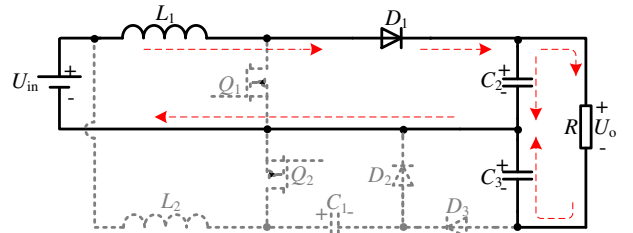
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



(g) $S_1S_2=00_{D1}$ (DCM)



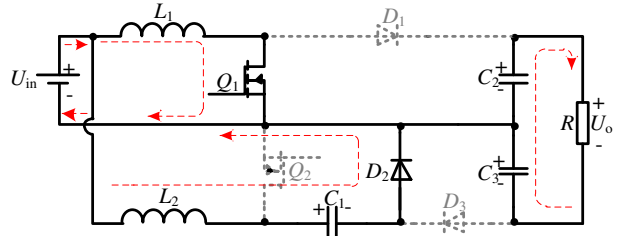
(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(a, e) and Fig. 3(c), when L_1 is charging from the DC source, the peak current I_{L1p} can be obtained as

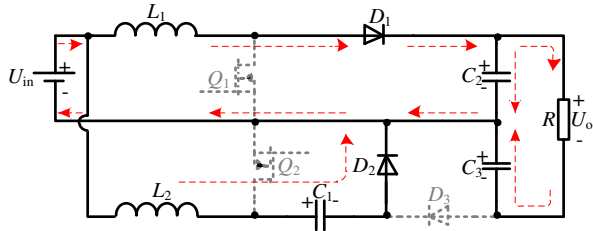
$$I_{L1p} = \frac{d \times T_s \times U_{in}}{L} \quad (5)$$

According

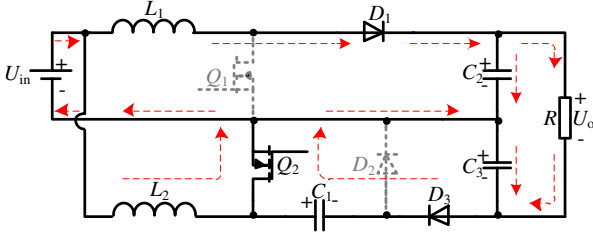
to



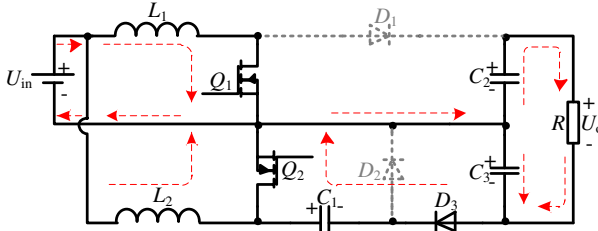
(a) $S_1S_2=10$



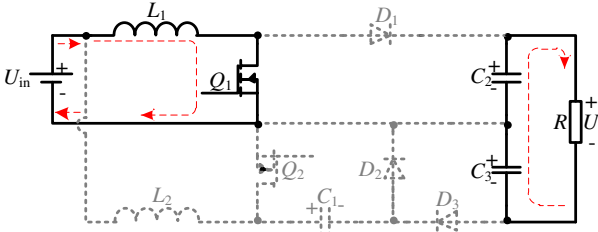
(b) $S_1S_2=00$



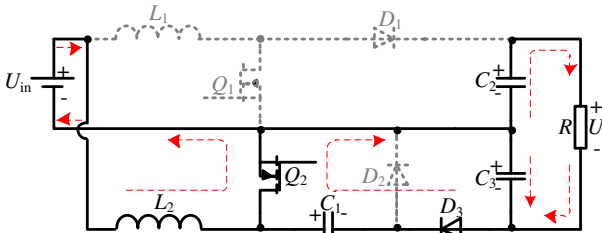
(c) $S_1S_2=01$



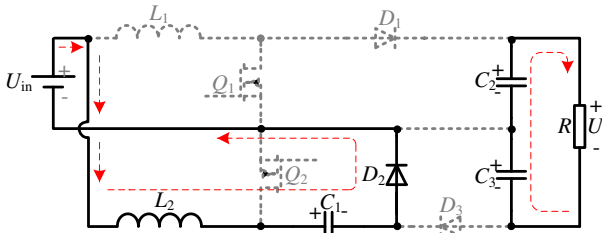
(d) $S_1S_2=11$



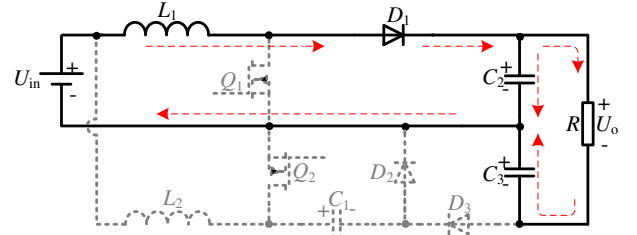
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



(g) $S_1S_2=00_{D1}$ (DCM)



(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(h, c) and Fig. 3(c), when L_1 is discharging, the peak current I_{L1p} can also be obtained as

$$I_{L1p} = \frac{d_2 \times T_s \times (U_{C2} - U_{in})}{L} \quad (6)$$

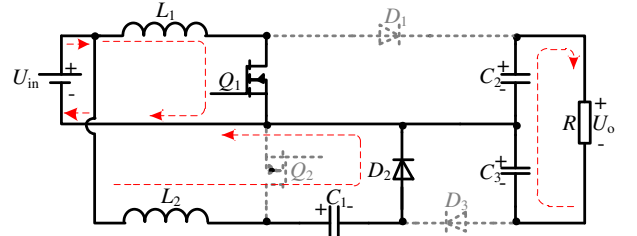
According to (5) and (6), d_2 can be derived as

$$d_2 = \frac{d \times U_{in}}{U_{C2} - U_{in}} \quad (7)$$

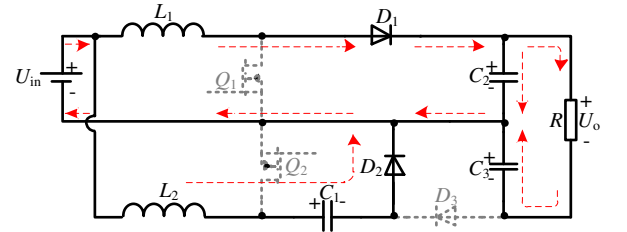
By

means

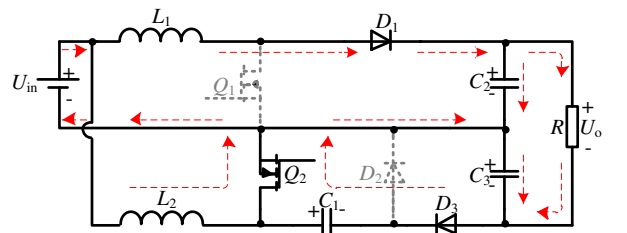
of



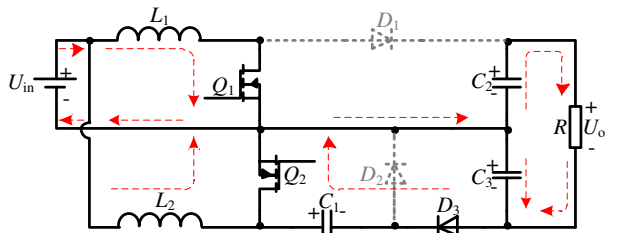
(a) $S_1S_2=10$



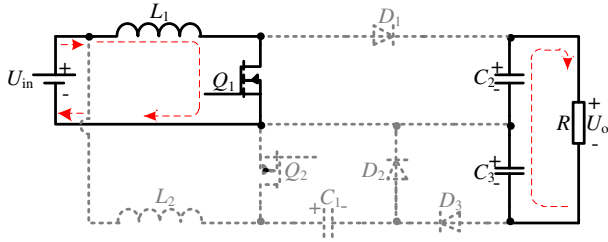
(b) $S_1S_2=00$



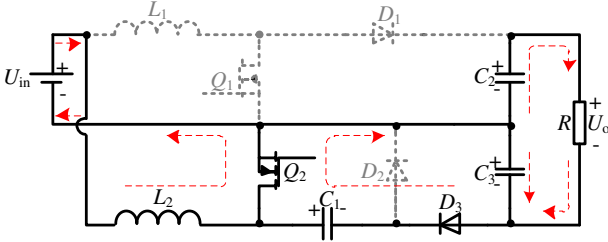
(c) $S_1S_2=01$



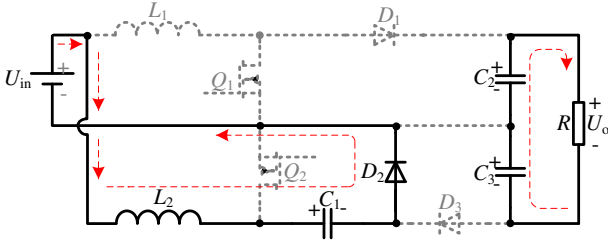
(d) $S_1S_2=11$



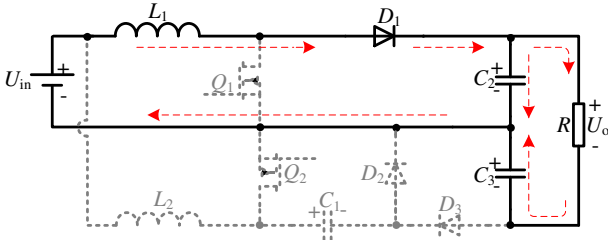
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



(g) $S_1S_2=00_{D1}$ (DCM)



(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(c), Q_1 is turned off and Q_2 is turned on, so that C_1 and C_3 are connected in parallel. Therefore, the voltages across C_1 and C_3 are equal. By using the voltage-second balance principle on L_1 and L_2 , the following equations can be obtained

$$\begin{cases} dU_{in} = d_2(U_{C2} - U_{in}) \\ dU_{in} = d_2(U_{C1} - U_{in}) \\ U_{C1} = U_{C3} \\ U_o = U_{C2} + U_{C3} \end{cases} \quad (8)$$

Simplifying (8), U_{C1} , U_{C2} and U_{C3} can be derived as

$$U_{C1} = U_{C2} = U_{C3} = \frac{U_o}{2} \quad (9)$$

By using the ampere-second balance principle on C_2 , the following equations can be obtained

$$(1-d_2) \times I_o = d_2 \times \left(\frac{I_{L1p}}{2} - I_o \right) \quad (10)$$

According to (5), (7), (9) and (10), the following equation can be obtained as

$$\frac{d^2 U_{in}^2 T_s}{2L \left(\frac{U_o}{2} - U_{in} \right)} = \frac{U_o}{R} \quad (11)$$

The normalized inductor time constant τ_L is defined as

$$\tau_L = \frac{L \times f_s}{R} \quad (12)$$

where f_s is the switching frequency ($f_s = 1/T_s$), and R is the load resistance.

Substituting (12) into (11), the voltage-gain of the proposed converter in DCM is given by

$$U_o = U_{in} \times \left(1 + \sqrt{1 + \frac{d^2}{\tau_L}} \right) \quad (13)$$

Similarly, the voltage-gain within the range of $0.5 < d < 1$ can be obtained, which is the same as the one within the range of $0 < d < 0.5$.

3. Boundary operating condition between CCM and DCM

When the proposed converter operates in the boundary conduction mode (BCM), the voltage-gain of the CCM operation is equal to the voltage-gain of the DCM operation. According to (2) and (13), the boundary normalized inductor time constant τ_{LB} can be derived as

$$\tau_{LB} = \frac{d \times (1-d)^2}{4} \quad (14)$$

The relationship between τ_{LB} and d is shown in Fig. 4. If $\tau_L > \tau_{LB}$, then the proposed converter is operating in CCM.

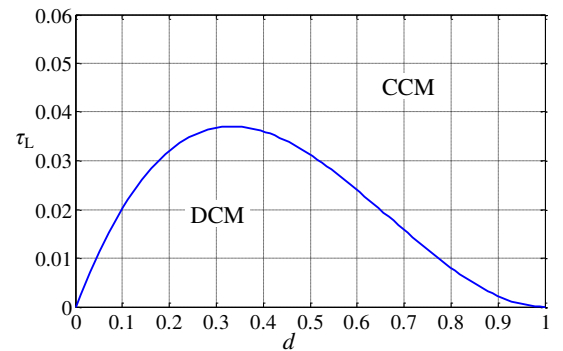
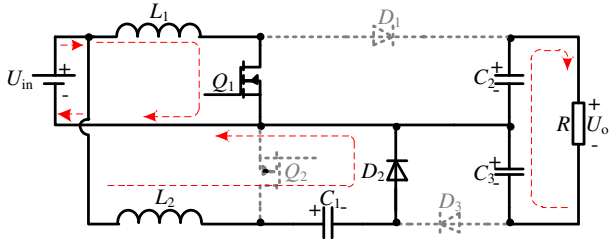


Fig. 4 Boundary condition of the proposed converter.

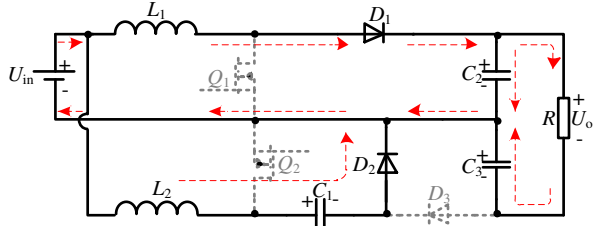
B. Voltage stress and current stress of the power

semiconductors

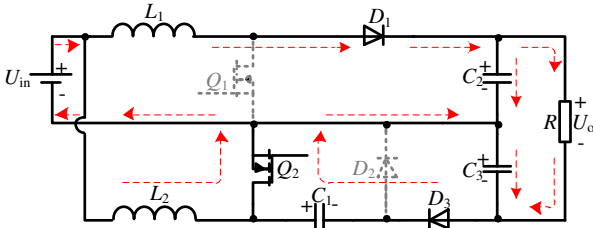
By means of



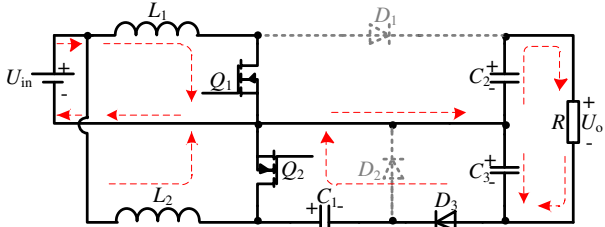
(a) $S_1S_2=10$



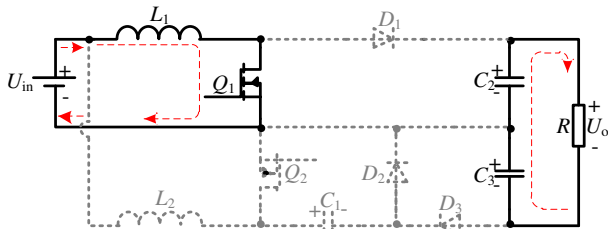
(b) $S_1S_2=00$



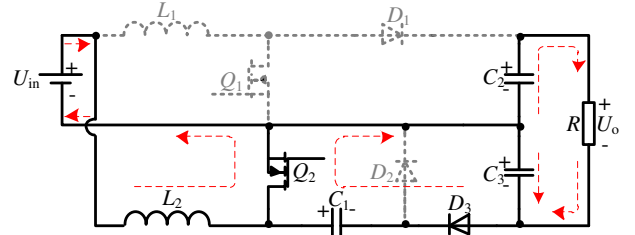
(c) $S_1S_2=01$



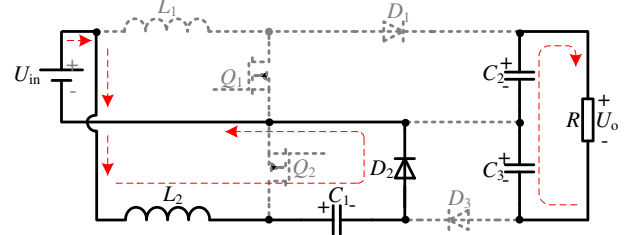
(d) $S_1S_2=11$



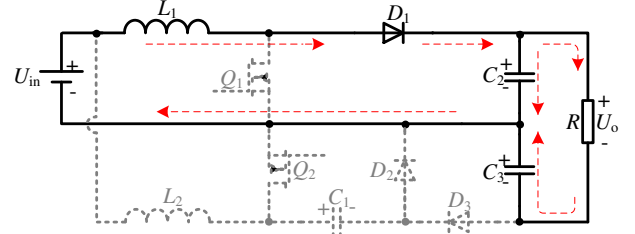
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



(g) $S_1S_2=00_{D1}$ (DCM)



(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(b, c), power switch Q_1 is turned off and diode D_1 is turned on, so that Q_1 and C_2 are connected in parallel. Therefore, the voltages of Q_1 and C_2 are equal. Symmetrically, the voltages of the other power semiconductors can be obtained. The voltage stress for the power semiconductors can be written as follows:

$$\begin{cases} U_{Q1} = U_{D1} = U_{C2} = \frac{U_o}{2} \\ U_{Q2} = U_{D2} = U_{C1} = \frac{U_o}{2} \\ U_{D3} = U_{C3} = \frac{U_o}{2} \end{cases} \quad (15)$$

Based on (15), the voltage stress for all of the power semiconductors is half of the output voltage.

The comparisons between the proposed topology and the four topologies which include the conventional interleaved DC-DC Boost converter, the three-level DC-DC Boost converter and the topology of the converter in [23] are shown in

Tab. 2.

Tab. 2 The comparisons between the proposed typology and the other four typologies

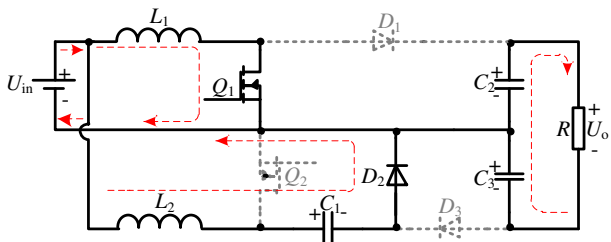
The conventional interleaved Boost DC-DC converter	The Boost three-level DC-DC converter	The typology of the converter in [23]	The proposed converter
--	---------------------------------------	---------------------------------------	------------------------

Voltage-gain	$1/(1-d)$	$1/(1-d)$	$2/(1-d)$	$2/(1-d)$
Voltage stress for power switches	U_o	$U_o/2$	$U_o/2$	$U_o/2$
Voltage stress for diodes	U_o	$U_o/2$	$U_o, U_o/2$	$U_o/2$
Input current ripple($d<0.5$)	$\frac{d(1-2d)U_oT_s}{L}$	$\frac{d(1-2d)U_oT_s}{2L}$	High	$\frac{d(1-2d)T_sU_o}{2L}$
Ripple rate of the input current($d<0.5$)	$\frac{d(1-d)(1-2d)RT_s}{L}$	$\frac{d(1-d)(1-2d)RT_s}{2L}$	High	$\frac{d(1-d)(1-2d)RT_s}{4L}$
Input current ripple($d>0.5$)	$\frac{(2d-1)(1-d)U_oT_s}{L}$	$\frac{(2d-1)(1-d)U_oT_s}{2L}$	High	$\frac{(2d-1)(1-d)T_sU_o}{2L}$
Ripple rate of the input current($d>0.5$)	$\frac{(2d-1)(1-d)^2RT_s}{L}$	$\frac{(2d-1)(1-d)^2RT_s}{2L}$	High	$\frac{(2d-1)(1-d)^2RT_s}{4L}$
The number of inductors	2	1	2	2
The number of power switches	2	2	2	2
The number of diodes	2	2	2	3

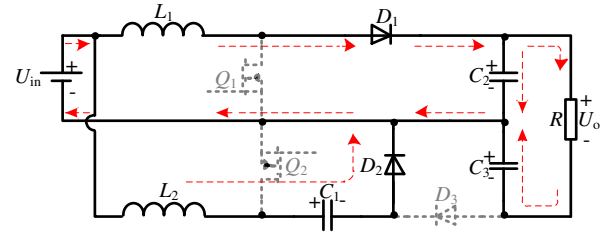
According to

Tab. 2, compared with the conventional interleaved DC-DC Boost converter, the proposed converter benefits from higher voltage-gain and lower voltage stress for the power semiconductors. The proposed topology can also achieve a higher voltage-gain than the voltage-gain of the three-level DC-DC Boost converter. In addition, compared with the topology in [23], the voltage stress for each power semiconductor of the proposed topology is half of the output voltage. Regarding the input current ripple, the converter in [23] suffers the highest input current ripple among these converters, because its input current is a pulse current which is discontinuous. According to **Error! Reference source not found.**, when these converters have the same parameters, such as the output voltage U_o , the duty cycle d , the switching period T_s , the inductance L and the load resistance R , the input current ripple of the proposed converter is lower than the one of the conventional interleaved Boost DC-DC converter. The ripple rate of the input current for the proposed converter is half of the one for the Boost three-level DC-DC converter, which means the proposed converter has the lowest ripple rate of the input current among these converters.

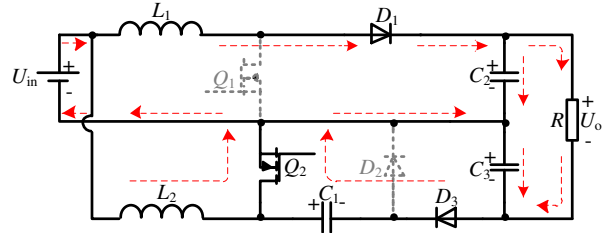
According



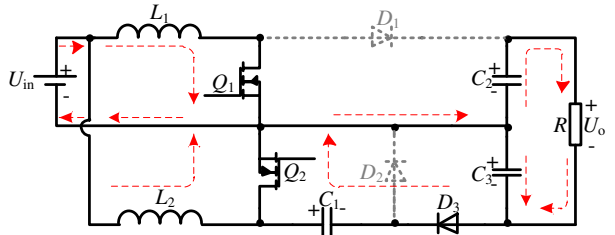
(a) $S_1S_2=10$



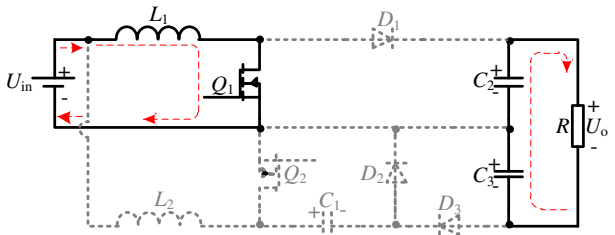
(b) $S_1S_2=00$



(c) $S_1S_2=01$



(d) $S_1S_2=11$



(e) $S_1S_2=10_b$ (DCM)

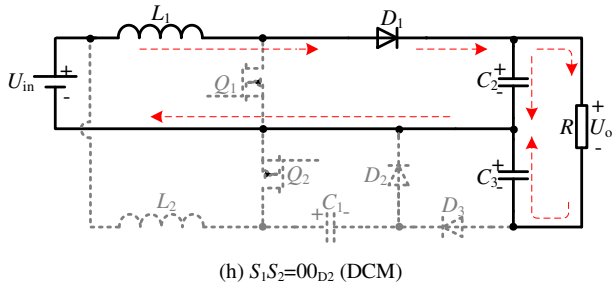
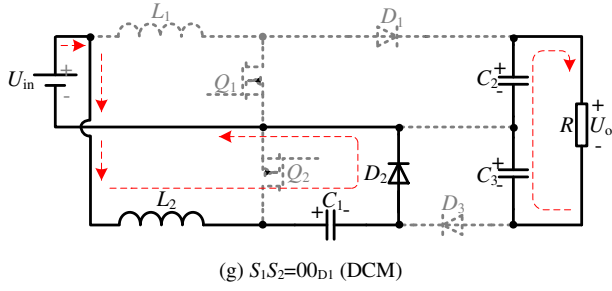
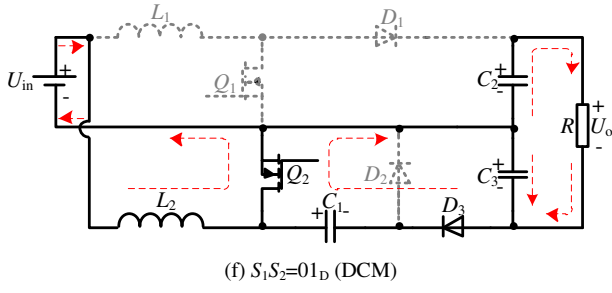


Fig. 2 and (4), the current stress of the power semiconductors can be obtained by using the voltage-balance on capacitors C_1 , C_2 and C_3 as given in (16).

$$\begin{cases} I_{Q1} = \frac{1}{1-d} I_o \\ I_{Q2} = (\frac{1}{1-d} + \frac{1}{d}) I_o \\ I_{D1} = I_{D2} = \frac{1}{1-d} I_o \\ I_{D3} = \frac{1}{d} I_o \end{cases} \quad (16)$$

Simplifying (16), the current stress of Q_2 is higher than that of Q_1 , but it is easier (and cheaper) to choose a MOSFET with a higher rated current than the one with a higher rated voltage. The proposed converter can also obtain a high voltage-gain while the duty cycle is in the range of $0.5 < d < 1$. In this case, the difference of the current stress between Q_1 and Q_2 is small. Therefore, the type of power switch Q_1 can be the same as the type of Q_2 , which means the difference of the current stress between Q_1 and Q_2 does not affect the selection of power switches.

The converters in [24] and [25] have the similar structures comparing with the proposed converter. The comparisons between the proposed converter and the other two similar converters are shown in **Error! Reference source not found..** The converters in [24] and [25] employ coupled inductors. To simplify the analysis, it is assumed that each coupled inductor has the same turn ratio N .

Tab. 3 The comparisons between the proposed converter and the other two similar converters

	The converter in [24]	The converter in [25]	The proposed converter
Voltage-gain	$2(N+1)/(1-d)$	$(2N+3+d)/(1-d)$	$2/(1-d)$
Voltage stress for power switches	$U_o/2(N+1)$	$U_o/(2N+3+d)$	$U_o/2$
The maximum voltage stress for diodes	$NU_o/(N+1)$	$(N+1)U_o/(2N+3+d)$	$U_o/2$
Input current ripple($d>0.5$)	$\frac{(1-k)(1-d)(2d-1)U_oT_s}{2L_k(N+1)}$	$\frac{(1-k)(1-d)(2d-1)U_oT_s}{(2N+3+d)L_k}$	$\frac{(2d-1)(1-d)T_sU_o}{2L}$
The number of inductors/coupled inductors	2	2	2
The number of power switches	2	2	2
The number of diodes	4	6	3
The number of capacitors	4	6	3

The input current ripple calculations of converters in **Error! Reference source not found.** and [25] are approximate ones, even though the practical input current ripple is still quite lower. According to **Error! Reference source not found.**, the converters in [24] and

[25] both obtain a higher voltage-gain and lower input current ripple. The voltage stress for power switches of the two converters is lower than that of the proposed converter. But the voltage stress for diodes of the proposed converter is lower than that of the converter in

[24] (when $N>1$). The converter in [25] benefits the lowest voltage stress for diodes among these converters. But, both the potential differences between the output and the input side grounds of the converters in [24] and [25] are high frequency PWM voltages (i.e. without a common ground), which may cause more EMI. In addition, the number of components for the proposed converter is the smallest one among these converters.

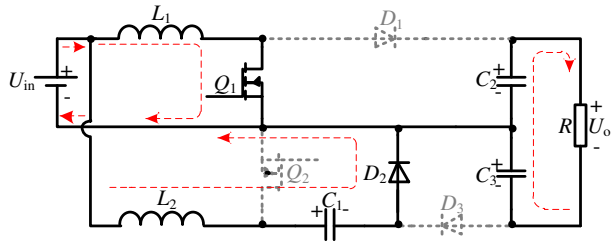
Regarding the voltage-gain of converters for fuel cell vehicles, a wide range of voltage-gain is really required because the output voltage of the fuel cell varies within a wide range when the load power varies widely. Therefore, sometimes the converters need to operate with a lower voltage-gain (i.e. the duty cycle is lower due to the higher output voltage of the fuel cell). According to Tab. 3, when these converters need to achieve the required lower voltage-gain, the duty cycle of the proposed converter is proper, i.e. a wider voltage-gain range can be realized.

C. Analysis of the input current ripple

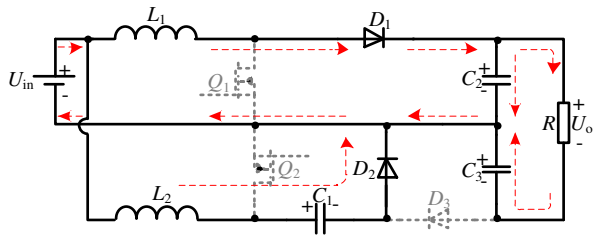
Within the range of $0<d<0.5$, the input current ripple Δi_{in} can be obtained as follows according to Fig. 3(a)

$$\begin{aligned}\Delta i_{in} &= (I_{L1m} + I_{L2a}) - (I_{L1a} + I_{L2m}) \\ &= (I_{L1m} - I_{L1a}) + (I_{L2a} - I_{L2m})\end{aligned}\quad (17)$$

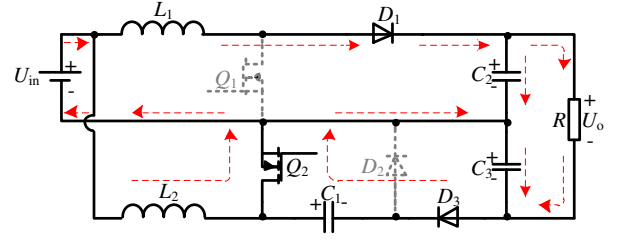
When $S_1S_2=00$ ($t_1\sim t_2$), the following equations can be obtained as follows according to



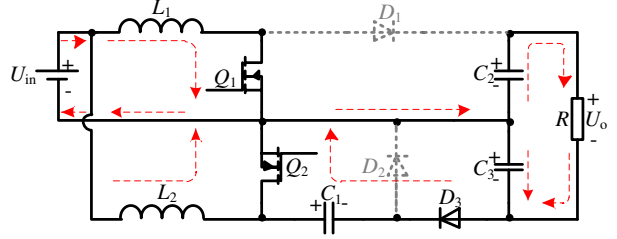
(a) $S_1S_2=10$



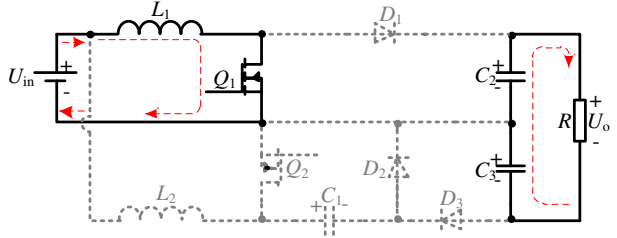
(b) $S_1S_2=00$



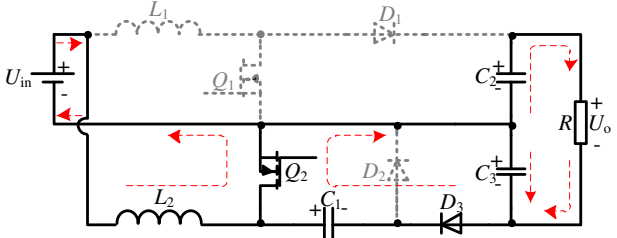
(c) $S_1S_2=01$



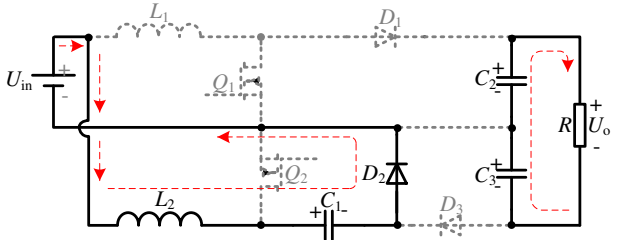
(d) $S_1S_2=11$



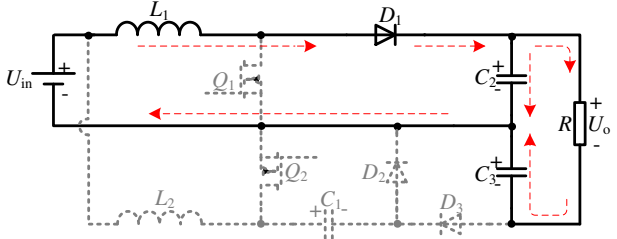
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



(g) $S_1S_2=00_{D1}$ (DCM)



(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(b) and Fig. 3(a),

$$\begin{cases} I_{L1m} - I_{L1a} = \frac{(U_{c2} - U_{in})(1-2d)T_s}{2L} \\ I_{L2a} - I_{L2m} = \frac{(U_{c1} - U_{in})(1-2d)T_s}{2L} \end{cases} \quad (18)$$

In terms of (2), (17) and (18), Δi_{in} can be derived as

$$\Delta i_{in} = \frac{d \times (1-2d) \times T_s \times U_{in}}{(1-d) \times L} = \frac{d \times (1-2d) \times T_s \times U_o}{2L} \quad (19)$$

Then, the ripple of i_{L1} , i_{L2} and i_{in} within the range of $0 < d < 0.5$ can be described as follows

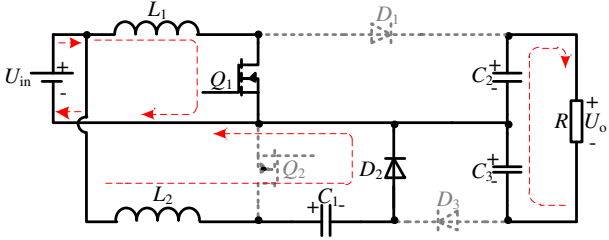
$$\begin{cases} \Delta i_{L1} = \Delta i_{L2} = \frac{d \times T_s \times U_{in}}{L} = \frac{d \times (1-d) \times T_s \times U_o}{2L} \\ \Delta i_{in} = \frac{d \times (1-2d) \times T_s \times U_{in}}{(1-d) \times L} = \frac{d \times (1-2d) \times T_s \times U_o}{2L} \end{cases} \quad (20)$$

where Δi_{L1} , Δi_{L2} and Δi_{in} are the ripple of i_{L1} , i_{L2} and i_{in} .

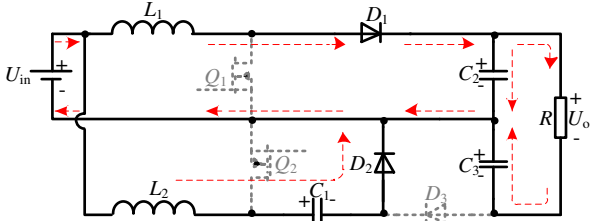
Within the range of $0.5 < d < 1$, according to Fig. 3(b), the input current ripple Δi_{in} can be obtained as

$$\begin{aligned} \Delta i_{in} &= (I_{L1n} + I_{L2b}) - (I_{L1b} + I_{L2n}) \\ &= (I_{L1n} - I_{L1b}) + (I_{L2b} - I_{L2n}) \end{aligned} \quad (21)$$

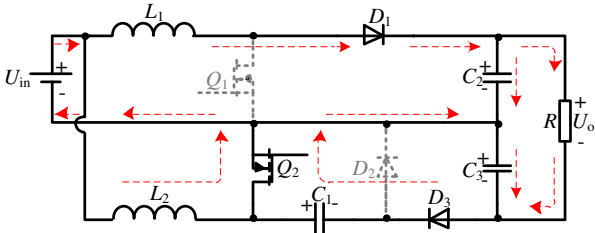
When $S_1 S_2 = 11$ ($t_2 \sim t_3$), the following equations can be obtained as follows according to



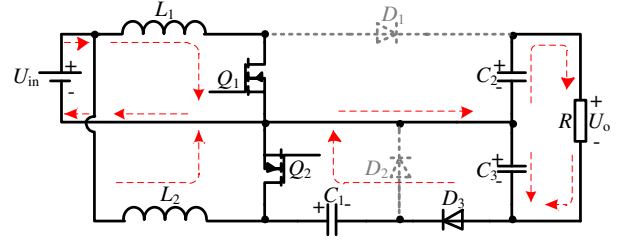
(a) $S_1 S_2 = 10$



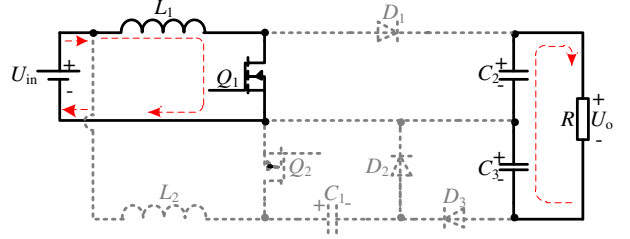
(b) $S_1 S_2 = 00$



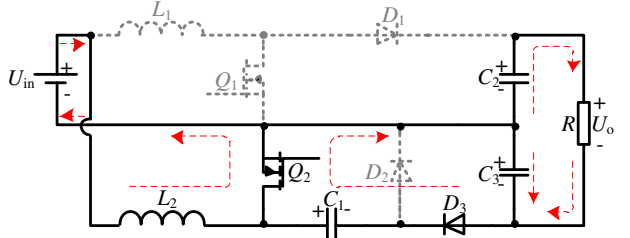
(c) $S_1 S_2 = 01$



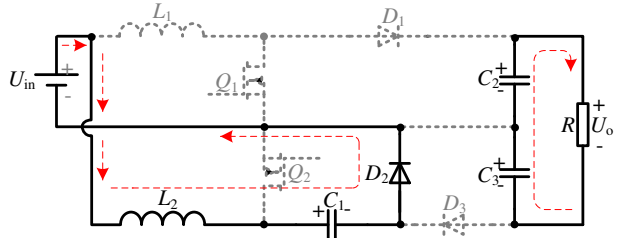
(d) $S_1 S_2 = 11$



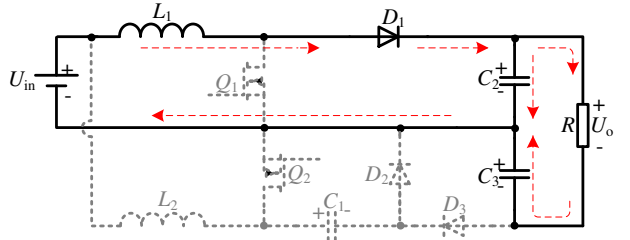
(e) $S_1 S_2 = 10_b$ (DCM)



(f) $S_1 S_2 = 01_b$ (DCM)



(g) $S_1 S_2 = 00_{b1}$ (DCM)



(h) $S_1 S_2 = 00_{b2}$ (DCM)

Fig. 2(d) and Fig. 3(b)

$$\begin{cases} I_{L1n} - I_{L1b} = \frac{(2d-1)U_{in}T_s}{2L} \\ I_{L2b} - I_{L2n} = \frac{(2d-1)U_{in}T_s}{2L} \end{cases} \quad (22)$$

By means of (2), (21) and (22), Δi_{in} can be derived as

$$\Delta i_{in} = \frac{(2d-1) \times T_s \times U_{in}}{L} = \frac{(2d-1) \times (1-d) \times T_s \times U_o}{2L} \quad (23)$$

Then, the ripple of i_{L1} , i_{L2} and i_{in} within the range of $0.5 < d < 1$ can be obtained as follows

$$\begin{cases} \Delta i_{L1} = \Delta i_{L2} = \frac{d \times T_s \times U_{in}}{L} = \frac{d \times (1-d) \times T_s \times U_o}{2L} \\ \Delta i_{in} = \frac{(2d-1) \times T_s \times U_{in}}{L} = \frac{(2d-1) \times (1-d) \times T_s \times U_o}{2L} \end{cases} \quad (24)$$

For the case when $U_o=400V$, $L=226\mu H$, $f_s=20kHz$ and $R=100\Omega$, using (20) and (24), the current ripple rate of i_{L1} , i_{L2} and i_{in} can be calculated and is shown in Fig. 5, where $\Delta i/I$ is the current ripple rate. According to Fig. 5, the ripple rate of the input current is lower than the ripple rate of i_{L1} and i_{L2} . When the DC source is in the range of $U_{in}=50V \sim 120V$, the duty cycle varies in the range of $0.4 < d < 0.75$. In this case, the minimum ripple rate of the input current is zero, while the duty cycle $d=0.5$. In the range of $0.4 \leq d < 0.5$, the maximum ripple rate of the input current is 27%, when the duty cycle is $d=0.4$. In addition, the maximum ripple rate of the input current is 20.5%, when the duty cycle is $d=0.67$ within the range of $0.5 < d < 0.75$.

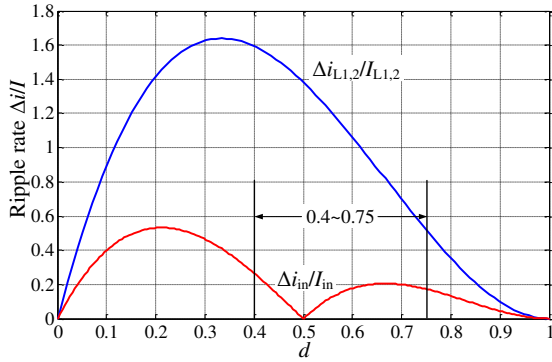


Fig. 5 The ripple rate of i_{L1} , i_{L2} and i_{in} .

D. Parameters design of the converter

1. Power switches and diodes

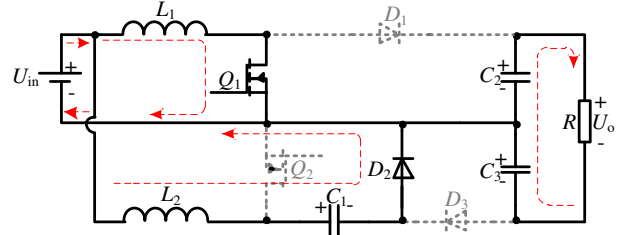
When the output voltage is $U_o=400V$, the voltage stress for each power semiconductor is 200V based on (15). When the voltage-gain is 8 ($d=0.75$) and the load resistance is $R=100\Omega$, the current stress (namely average currents in the *ON* state) for power semiconductors can be obtained as: $I_{Q1}=16A$, $I_{Q2}=21.3A$, $I_{D1}=I_{D2}=16A$, and $I_{D3}=5.3A$ according to **Error! Reference source not found..** The power switches and diodes can be selected by these referenced voltage and current stresses.

2. Inductors and capacitors

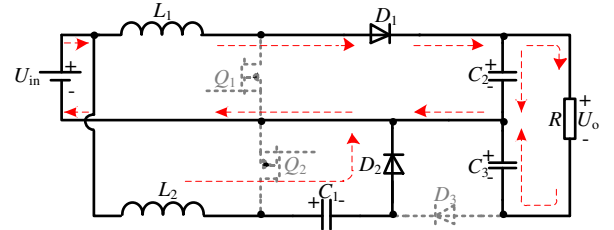
According to (24), the inductances of L_1 and L_2 can be obtained as

$$\begin{cases} L_1 = \frac{d \times U_{in} \times T_s}{\Delta i_{L1}} \\ L_2 = \frac{d \times U_{in} \times T_s}{\Delta i_{L2}} \end{cases} \quad (25)$$

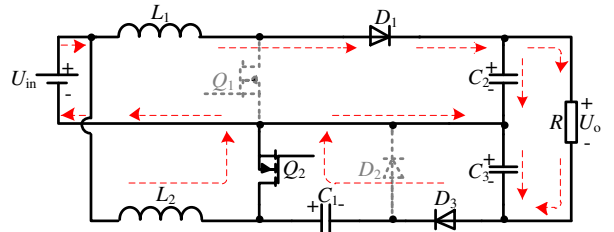
In terms of



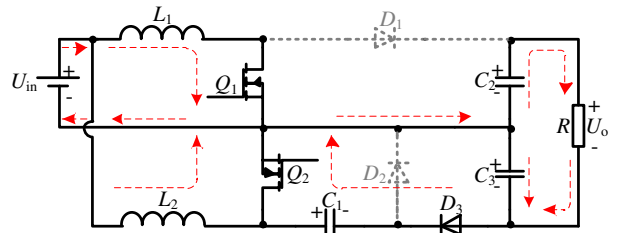
(a) $S_1S_2=10$



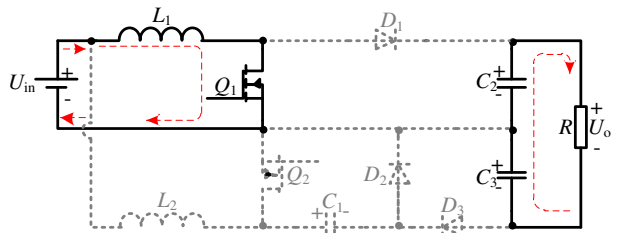
(b) $S_1S_2=00$



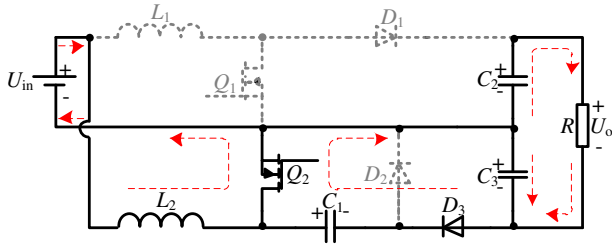
(c) $S_1S_2=01$



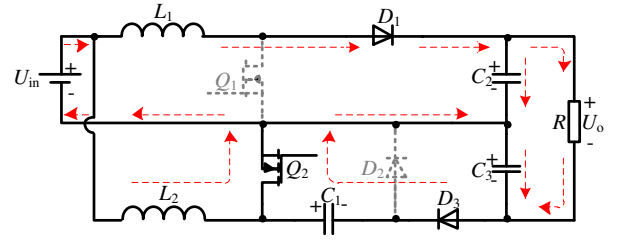
(d) $S_1S_2=11$



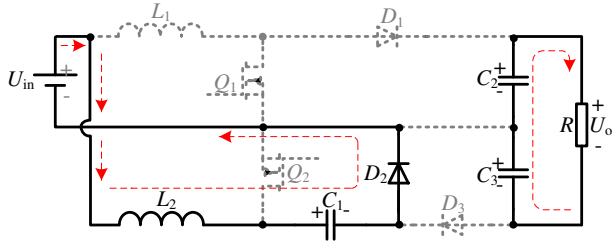
(e) $S_1S_2=10_D$ (DCM)



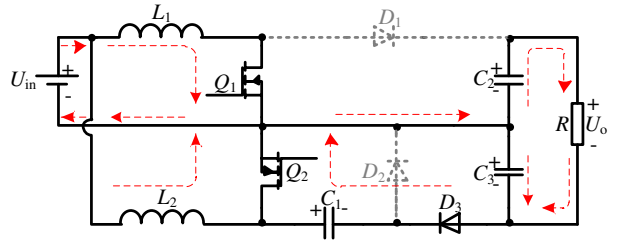
(f) $S_1S_2=01_D$ (DCM)



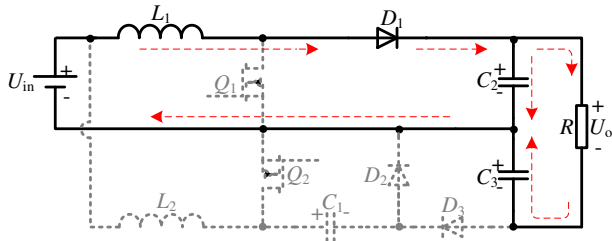
(c) $S_1S_2=01$



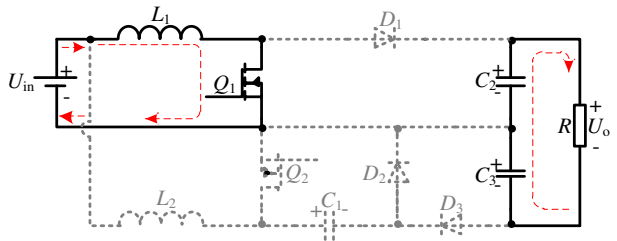
(g) $S_1S_2=00_{D1}$ (DCM)



(d) $S_1S_2=11$



(h) $S_1S_2=00_{D2}$ (DCM)



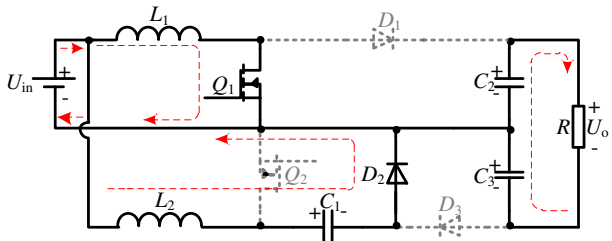
(e) $S_1S_2=10_D$ (DCM)

Fig. 2(a, b), when the power switch Q_2 is turned off, C_1 is charging from inductor L_2 and the DC source. Then, the capacitance of C_1 can be obtained as

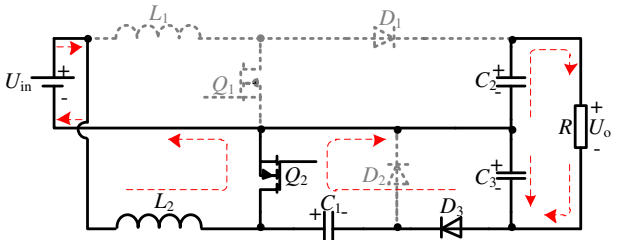
$$C_1 = \frac{(1-d)I_{L_2}T_s}{\Delta U_{C_1}} \quad (26)$$

where ΔU_{C_1} is the capacitor voltage fluctuation.

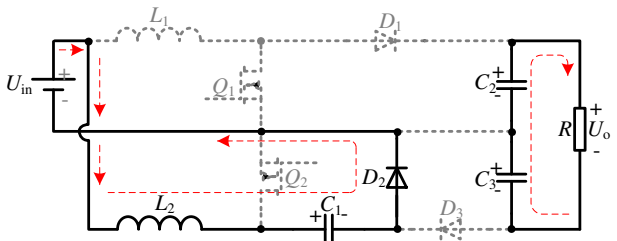
By means of



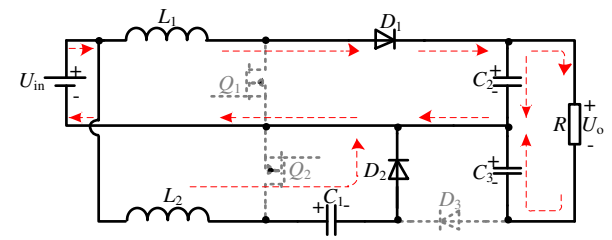
(a) $S_1S_2=10$



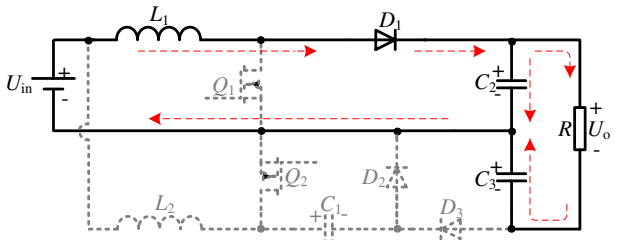
(f) $S_1S_2=01_D$ (DCM)



(g) $S_1S_2=00_{D1}$ (DCM)



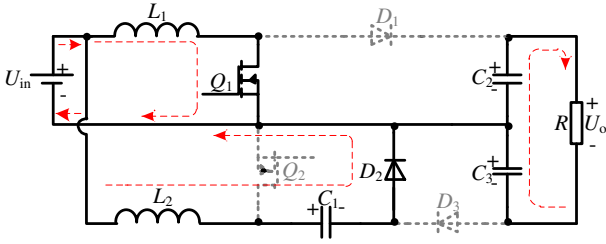
(b) $S_1S_2=00$



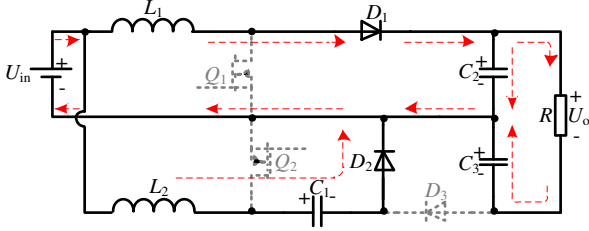
(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(a, d), when the Q_1 is turned on, C_2 is discharging.

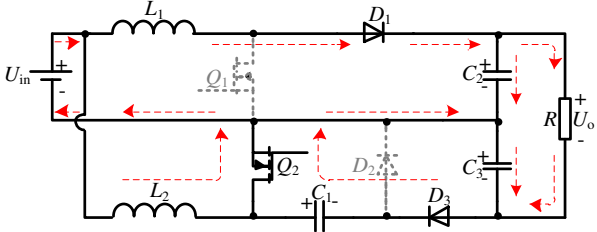
Similarly, according to



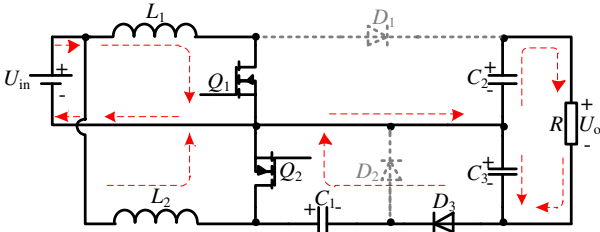
(a) $S_1S_2=10$



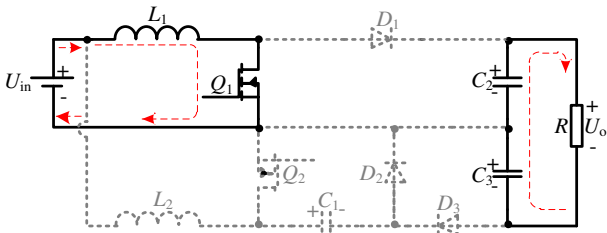
(b) $S_1S_2=00$



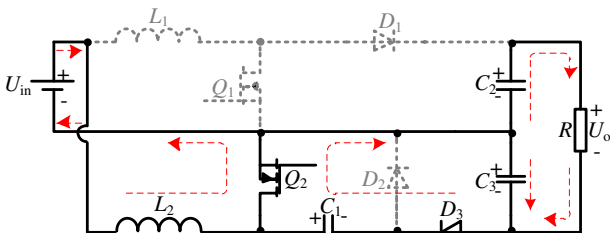
(c) $S_1S_2=01$



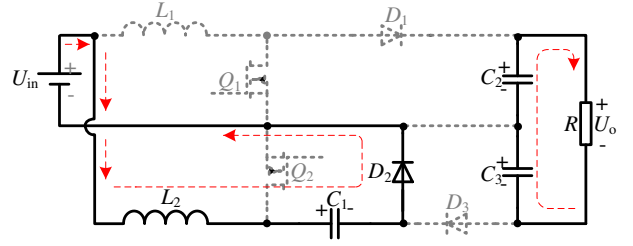
(d) $S_1S_2=11$



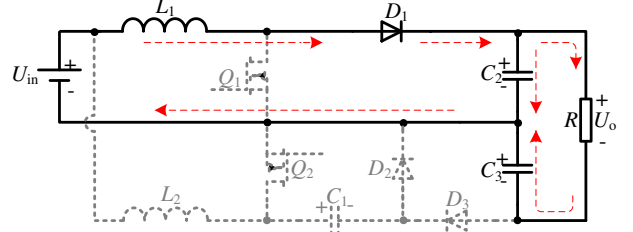
(e) $S_1S_2=10_D$ (DCM)



(f) $S_1S_2=01_D$ (DCM)



(g) $S_1S_2=00_{D1}$ (DCM)



(h) $S_1S_2=00_{D2}$ (DCM)

Fig. 2(a, b), when Q_2 is turned off, C_3 is discharging. Therefore, the capacitances of C_2 and C_3 can be obtained as

$$\begin{cases} C_2 = \frac{d \times I_o \times T_s}{\Delta U_{C2}} \\ C_3 = \frac{(1-d) \times I_o \times T_s}{\Delta U_{C3}} \end{cases} \quad (27)$$

where ΔU_{C2} and ΔU_{C3} are the capacitor voltage fluctuations of C_1 and C_2 .

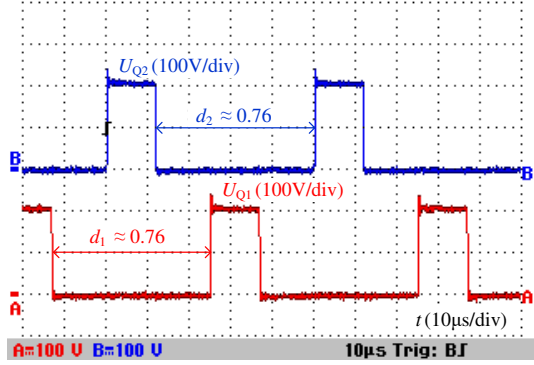
In terms of (25), (26) and (27), the inductances of inductors L_1 and L_2 , and the capacitances of capacitors C_1 , C_2 and C_3 can be designed in this paper.

V. EXPERIMENT RESULTS AND ANALYSIS

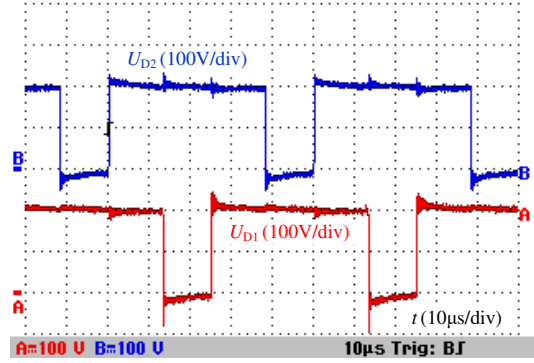
In order to validate the feasibility and effectiveness of the proposed converter, an input-parallel output-series Boost DC-DC converter was constructed which uses an adjustable DC source with a range of $U_{in}=50V \sim 120V$ to replace the fuel cell stack source. The converter voltage loop is controlled by a TMS320F28335 DSP. The power circuit uses IXTK102N30P MOSFETs (which has a rated voltage of 300V and a rated current of 102A, while the output voltage of the converter is 400V), and also uses DPG60C300HB Schottky Barrier Diodes. The switching frequency is 20kHz, The inductors are $L_1=227\mu H$ and $L_2=225\mu H$ respectively and the capacitances are $C_1=C_2=C_3=470\mu F$. The reference output voltage is 400V, and the load resistance is $R=100\Omega$.

When the input voltage is $U_{in}=50V$, the voltage of each power semiconductor is shown in Fig. 6. Fig. 6(a)

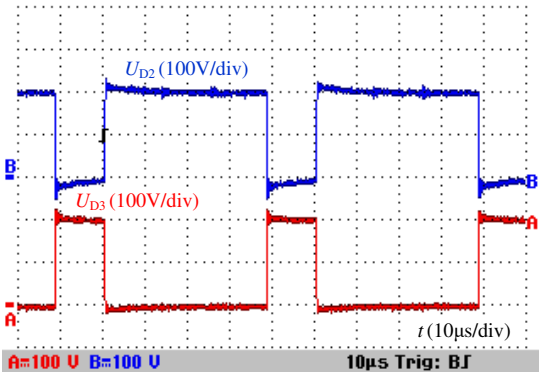
shows the voltages of power switches Q_1 and Q_2 , and Fig. 6(b) shows the voltages of diodes D_1 and D_2 . The voltages of D_2 and D_3 are shown in Fig. 6(c). The voltage of each power semiconductor is 200V, i.e. half of the output voltage, as shown in Fig. 6.



(a) The voltages of power switches Q_1 and Q_2



(b) The voltages of diodes D_1 and D_2



(c) The voltages of D_2 and D_3

Fig. 6 The voltage of each power semiconductor when the input voltage is $U_{in}=50V$.

When the input voltage is $U_{in}=50V$, the voltages of capacitors C_2 and C_3 are shown in Fig. 7. According to Fig. 7, the voltages of C_2 and C_3 are both 200V, i.e. half of the output voltage. The potential difference between the output and input sides of this converter is the voltage

across C_3 , whose ripple is quite low.

When the input voltage is $U_{in}=50V$, the input current i_{in} , and inductor currents i_{L1} and i_{L2} are shown in Fig. 8. Inductor currents i_{L1} and i_{L2} are shown in Fig. 8(a). Fig. 8(b) shows the input current i_{in} and inductor current i_{L1} . According to Fig. 7, the ripple rate of i_{L1} is 53.13%, and the ripple rate of i_{L2} is 56.25%. In addition, the ripple rate of the input current is 17.65%. The conclusion here is that the current ripple of i_{in} is much lower than the current ripple of i_{L1} and i_{L2} . According to (24), the ripple rate of i_{L1} and i_{L2} is 51.81%, and the ripple rate of i_{in} is 17.28% theoretically. These results are very similar to the theoretical results.

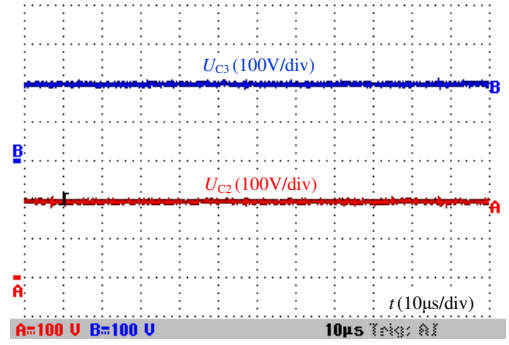
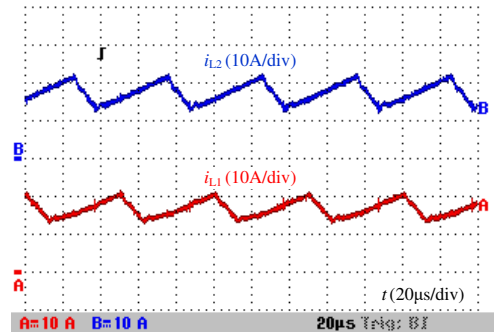
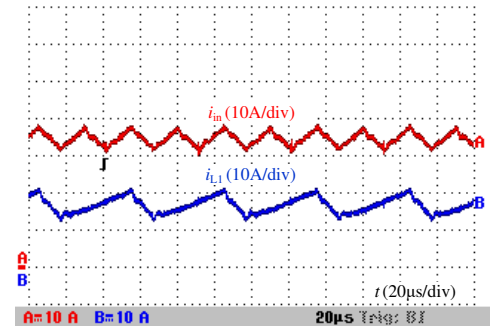


Fig. 7 The voltages of capacitors C_2 and C_3 when the input voltage is $U_{in}=50V$.



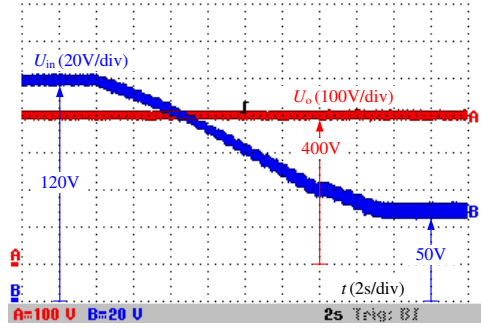
(a) Inductor currents i_{L1} and i_{L2}



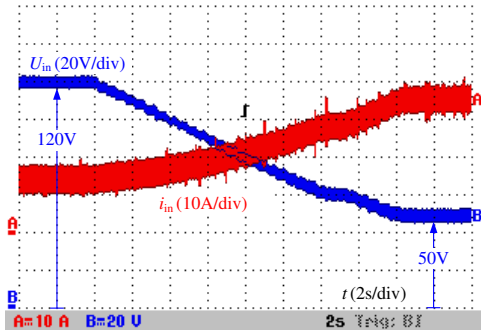
(b) The input current i_{in} and the inductor current i_{L1}

Fig. 8 The input current i_{in} , inductor currents i_{L1} and i_{L2} when the input voltage is $U_{in}=50V$.

The output voltage remains close to the reference voltage 400V under the action of the voltage control loop. Fig. 9 shows the dynamic response of the output voltage and the input current when the input voltage was changed from 120V to 50V. Fig. 9(a) shows the output and input voltages, while Fig. 9(b) shows the input current and voltage. According to Fig. 9(a), when the input voltage U_{in} is changed gradually from 120V to 50V, the output voltage stays around 400V, which means the proposed converter has a wide voltage gain range varying from 3.3 to 8. Correspondingly, the input current increases gradually (from 13A to 34A) with this large reduction of input voltage (from 120V to 50V), as shown in Fig. 9(b).



(a) The output and input voltages



(b) The input current and voltage

Fig. 9 The output voltage and the input current with the wide-range changed input voltage from 120V to 50V in dynamical state.

When the output voltage is $U_o=400V$ and the load resistance is $R=100\Omega$, the ripple rate of the input current within the wide input voltage range from 50V to 120V is shown in Fig. 10, where $\Delta i_{in1}/I_{in1}$ is the experimental ripple rate of the input current, and $\Delta i_{in2}/I_{in2}$ is the ripple rate of the input current which is calculated by (4), (19)

and (23). According to Fig. 10, the theoretical results are similar to the experiment results.

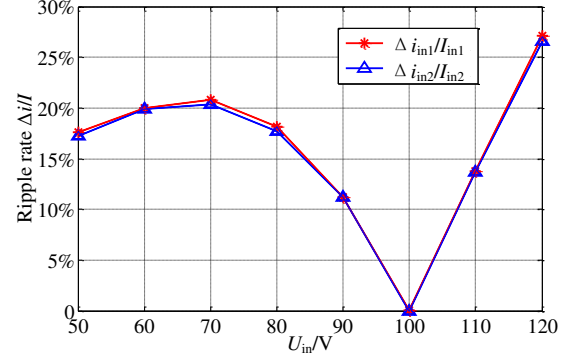


Fig. 10 The ripple rate of input current within the wide input voltage range from 50V to 120V.

When the output voltage is $U_o=400V$ and the load resistance is $R=100\Omega$, the efficiency η_e measured by a Power Analyzer (Yokogawa-WT3000) for different input voltages ranging from 120V to 50V is shown in Fig. 11. The maximum efficiency is 96.62%, when the voltage-gain is 3.3 ($U_{in}=120V$). The minimum efficiency is 94.14%, when the voltage-gain is 8 ($U_{in}=50V$). The input current increases when the voltage gain changes from 3.3 to 8, and this effect decreases the efficiency of the proposed converter.

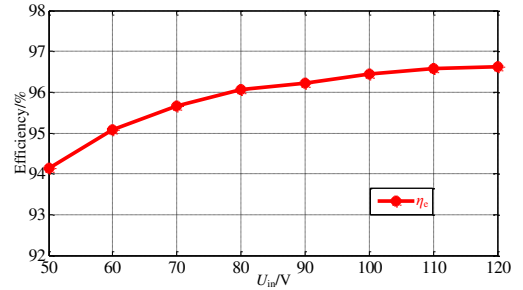


Fig. 11 The efficiency with the wide-range changed input voltage from 120V to 50V when the output voltage is $U_o=400V$ and the load resistance is $R=100\Omega$.

VI. CONCLUSION

In this paper, an input-parallel output-series DC-DC Boost converter with a wide input voltage range is presented. The converter can obtain a wide range of voltage-gain. The voltage stress of each power semiconductor is half of the output voltage. The input current ripple is low, which can prevent accelerated reductions of the life time of a fuel cell. In addition, the potential difference between output and input grounds of the proposed converter is a constant capacitor voltage

rather than a high frequency PWM voltage. Therefore, it is suitable for fuel cell vehicles.

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