INSULATED GATE BIPOLAR TRANSISTOR (IGBT) MODELING USING IG-SPICE

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Abstract - A physics-based model for the Insulated Gate Bipolar Transistor (IGBT) is implemented into the widely available circuit simulation package IG-SPICE. Based on analytical equations describing the semiconductor-physics, the model accurately describes the nonlinear junction capacitances, moving boundaries, recombination, and carrier scattering, and effectively predicts the device conductivity modulation. In this paper, the procedure used to incorporate the model into IG-SPICE and various methods necessary to ensure convergence are described. The effectiveness of the SPICE-based IGBT model is demonstrated by investigating the static and dynamic current sharing of paralleled IGBTs with different device model parameters. The simulation results are verified by comparison with experimental results.

I. Introduction

The Insulated Gate Bipolar Transistor (IGBT) was introduced into the family of power devices to overcome the high on-state loss of power MOSFETs while maintaining the simple gate drive requirements of MOSFETs. The IGBT combines both the bipolar and MOSFET structures and posseses the best features of both device types. Because the IGBT has a low power gate drive requirement, a high current density capability, and a high switching speed, it is preferred over other devices in many high-power applications.

A schematic representation of an single cell of a *n*-channel IGBT is shown in Fig. 1, where the arrows indicated by I_h and I_e show the direction of the hole current and the electron current, respectively. The IGBT structure is similar to that of a Vertical Double diffused MOSFET (VDMOSFET) with the exception that a *p*-type, heavily doped substrate replaces the *n*-type drain contact of the conventional VDMOSFET. The effect of this extra *p*-type layer is to act as an emitter to inject minority carriers (holes) into the main conducting region of the device, reducing its resistance and decreasing the on-state voltage drop of the device. These excess minority carriers drift and diffuse through the base and are collected by the p^+ body region (see Fig. 1). Thus the IGBT behaves as a bipolar transistor that is supplied base current by a MOSFET as indicated by the simplified equivalent circuit in Fig. 2.

A physics-based IGBT model suitable for general circuit simulation has been previously introduced [1-6] and verified for representative circuit operating conditions. This model is based on the analytical equations describing the semiconductor physics. The model accurately describes the nonlinear junction capacitances, moving boundaries, recombination, and carrier scattering, and effectively predicts the device conductivity modulation. Although many types of power devices exist, the semiconductor device models presently provided within most circuit simulation programs are based upon microelectronic devices and cannot readily be used to describe the internal MOSFETs and internal bipolar transistors of the power devices.

The Simulation Program with Integrated Circuit Emphasis (SPICE circuit simulator) is used worldwide. It is appropriate to implement Hefner's model in a SPICE-based simulator to make the model available to many circuit designers. However, the physics-based Hefner's model [3] consists of many nonlinear equations that must be implemented into the simulator due to the complex physical mechanisms that govern the behavior of IGBTs. Although SPICE provides a limited capability for implementing equations via the use of controlled dependent sources, this capability is not sufficient for implementing complicated equations. Although the PSPICE simulator (Personal computer SPICE) allows more flexibility by providing the user with the capability to

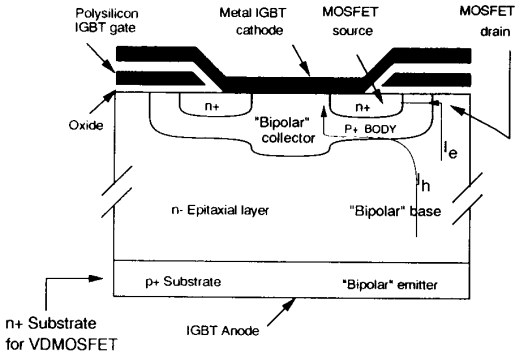

Fig. 1. A single *n*-channel IGBT cell.

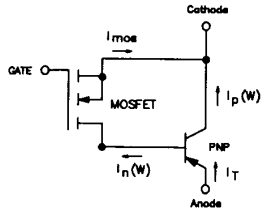

Fig. 2. Simplified IGBT equivalent circuit.

implement equations through the use of a supplemental program called Behavioral Modeling [7], it does not allow for conditional commands (ie., IF, THEN, ELSE). On the other hand, the IG-SPICE simulator (Interactive Graphics SPICE) overcomes these limitations by allowing the user to implement equations using controlled dependent sources and by providing the user with programming capability to describe these nonlinear controlled sources [8]. Therefore, the IG-SPICE circuit simulator is used in this work to implement Hefner's model.

The purpose of this paper is to describe the implementation of the physics-based IGBT model into the commercially available circuit simulator IG-SPICE. The techniques used to ensure convergence of the IG-SPICE model, and the applicability of these techniques to other power semiconductor devices are also reviewed. Furthermore, the techniques used to ensure convergence in IG-SPICE are also applicable to other SPICE-based simulators, because all SPICE-based programs use the same numerical algorithms. The effectiveness of the IG-SPICE IGBT model developed in this paper is demonstrated by examining the static and dynamic current sharing of paralleled IGBTs.

II. IGBT Physical Model

Figure 3 shows the detailed IGBT equivalent circuit superimposed on one cell of an n-channel IGBT. In Fig. 3, the components connected between the emitter (e), base (b), and collector (c) nodes are associated with the bipolar transistor, and the components connected between the drain (d), gate, and source (s) nodes are associated with the VDMOSFET. As mentioned earlier, the structure of the IGBT is similar to that of the power VDMOSFET, with the exception that the n^+ drain contact of the conventional MOSFET is replaced by

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the p^+ anode contact for the IGBT. Thus the MOSFET portion of the model behaves similarly to a VDMOSFET with the exception that the lightly doped epitaxial layer of the IGBT is considered as the conductivity-modulated base resistance, R_b, of the bipolar transistor. In addition, the drain-source and the gate-drain depletion capacitances overlap with the base-collector depletion capacitance of the bipolar transistor, and hence this capacitance is only included in the MOSFET. The details of the equivalent circuit are discussed below.

A. VDMOSFET

The MOSFET components of the equivalent circuit are defined as follows:

C_{gs} = gate-source capacitance,
C_{oxs} = gate oxide capacitance of the source overlap,
C_m = source metallization capacitance,
C_{gd} = gate-drain feedback capacitance (Miller Capacitance),
C_{oxd} = gate-drain overlap oxide capacitance,
C_{gdj} = gate-drain overlap depletion capacitance, and
C_{dsj} = drain-source depletion capacitance,

where the MOSFET symbol represents the MOSFET channel current, I_{mos}. The VDMOSFET gate-source capacitance C_{gs} consists of the parallel combination of the gate oxide capacitance of the source overlap C_{oxs}, and the source metallization capacitance C_m. The VDMOSFET gate-drain feedback capacitance (or Miller capacitance) consists of the series combination of the gate-drain overlap oxide capacitance C_{oxd}, and the gate-drain overlap depletion capacitance C_{gdj}. The VDMOSFET drain-source capacitance C_{dsj} consists of the depletion capacitance of the drain-source junction. To describe IGBTs made with other MOSFET structures, only the components of Fig. 2 associated with the MOSFET portion of the device, need to be changed.

B. Bipolar Transistor

The bipolar transistor components of the equivalent circuit are defined as follows:

C_{cer} = collector-emitter redistribution capacitance,
R_b = conductivity-modulated base resistance,
C_{ebd} = emitter-base diffusion capacitance, and
C_{ebj} = emitter-base depletion capacitance,

where the BJT symbol represents the charge-controlled components of collector and base current. The collector-emitter redistribution capacitance C_{cer} is a result of the non-quasi-static behavior of the bipolar transistor base charge for the changing base-collector depletion width. This capacitance is orders of magnitude larger than the depletion capacitances and dominates the effective output capacitance of the IGBT during turn-off [1]. The bipolar transistor also contributes a conductivity-modulated base resistance R_b, an emitter-base diffusion capacitance C_{ebd}, and an emitter-base depletion capacitance C_{ebj}.

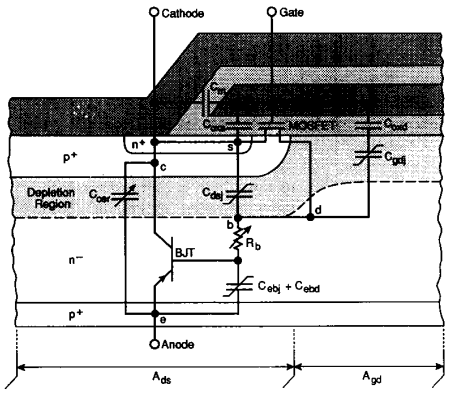


Fig. 3. Detailed IGBT equivalent circuit components superimposed on a schematic of one cell of an *n*-channel IGBT.

III. IG-SPICE IGBT Model Implementation

In this section, the requirements for implementing model equations into IG-SPICE, and the procedures used to implement the IGBT model into IG-SPICE are described. The expressions describing the components of the IGBT equivalent circuit are given in Appendices 1 and 2. For detailed discussions of these equations, refer to [6]. These equations are separated into two categories which describe the anode voltage and the anode current of the IGBT. These equations are then implemented as an interconnection of controlled-current and voltage sources that depend upon node voltages or branch currents. When the IGBT model is included in a circuit, the simulator iterates the node voltages and branch currents until KVL (Kirchoff's Voltage Law) and KCL (Kirchoff's Current Law) are satisfied for the entire circuit using the controlled current and voltage source functions of the IGBT. Thus each of the model equations necessary to describe the behavior of the IGBT [3] must be implemented as IG-SPICE controlled sources as described below [8].

A. Implementing General Device Models into IG-SPICE

SPICE users are constantly faced with the inability to analyze circuits that contain devices that are not well described by the SPICE semiconductor models. This can be overcome by the use of the programming capabilities of IG-SPICE. The IG-SPICE simulation program is an extended version of the SPICE-2 computer-aided design and analysis program. IG-SPICE is designed to be more graphics-oriented and provides the user with programming capability. This programming capability of IG-SPICE enables the user to implement general device models without having to add additional components such as diodes or transistors to emulate the device model equations. The ability to directly implement model equations as IG-SPICE controlled sources results in more computationally efficient simulations without the problems associated with convergence.

1) *IG-SPICE user defined device models:* When implementing model equations into the IG-SPICE user-defined model subroutine, the following formalities need to be considered in detail:

1. The model must be formulated as an interconnection of controlled current and voltage sources which depend upon controlling currents or voltages, but not both currents and voltages.
2. The variables must be normalized so that each variable that is solved for by the simulator has a comparable absolute error tolerance.
3. The independent variables must be converted into the current and voltage types.
4. In general, the partial derivatives of the expressions for the controlled sources with respect to the controlling variables must be evaluated.

The programming capability of IG-SPICE is made possible by the use of dependent controlled sources where the equations describing the controlled sources are implemented using the user-defined model subroutine. There are four types of controlled sources in the IG-SPICE simulation program:

Voltage-Controlled Current Source	(VCCS),
Voltage-Controlled Voltage Sources	(VCVS),
Current-Controlled Current Sources	(CCCS), and
Current-Controlled Voltage Sources	(CCVS).

In implementing these controlled sources into the user-defined model subroutine, the user must follow a particular format in order for the data to be passed properly between the IG-SPICE input file (which provides a list of voltages or currents and a list of constant model parameters) and the user-defined model subroutine (which computes the actual output voltage or current values based on the input lists). IG-SPICE requires that the inputs of the controlling variables be of only one source type: either all voltage or all current. Therefore, in the cases where the output is dependent upon both current and voltage type variables, the controlling variables of one of the types must be transformed into the other type.

2) *IG-SPICE controlled sources:* The IG-SPICE controlled sources are realized using the polynomial controlled sources of SPICE, which depend upon controlling variables. For example, the general input format for a voltage-controlled current source in all SPICE programs is as follows:

Gxxx <NS+> <NS-> Poly(<ND>) (<NC1+>, <NC1->)
(<NC2+>, <NC2->) . . . <P0, P1, . . .> ,

where <NS+> and <NS-> are the output connection nodes of the controlled source, Poly(<ND>) specifies the dimension of the polynomial as ND, and P0, P1 . . . are the polynomial coefficients. For the voltage-controlled sources, the nodes <NCi+> and <NCi-> specify the positive and negative connections of the controlling voltage. For the current-controlled sources, the controlling voltage pair is replaced by the name of the null voltage source <VSx> which is specified as a current probe. The current probe statements have the form: VSx <NS+>, <NS-> 0Probe, where the nodes <NS+>, and <NS-> are introduced in the controlling current branch and have zero voltage between them.

However, when the programming capability of IG-SPICE is utilized to implement a general model expression, the polynomial coefficient values are not used in the input field. Instead, the program function name followed by the sequence of data are specified. This data is passed to the user-defined model subroutine to determine the values of the polynomial coefficients. An example of the input field when utilizing the programming capability of IG-SPICE is:

GImos 7 60 POLY(2) (30,60) (2, 60) Imos(Vt = 5.0).

GImos is the name of the voltage-controlled current source (VCCS) in which the current enters through the positive node 7 and exits through the negative node 60. POLY(2) specifies that the dimension of the number of controlling voltages is 2, where the node pairs (30,60) and (2,60) specify the controlling voltages. Imos is the name of the output function within the user-defined model subroutine, and Vt is an example of a data value which is passed to the function Imos.

3) *Implementing partial derivatives of model functions:* In addition to evaluating the source function, the user-defined model subroutine must also evaluate the partial derivative of the source functions with respect to each of the controlling variables. These partial derivatives are required by the numerical algorithms of the SPICE-based simulators to facilitate convergence. To describe the procedure for implementing the partial derivatives into the model subroutines, let the variable Y be an output (dependent source function), and let X1, X2, . . . Xn be the input variables (controlling sources). The source functions then take the form:

$$Y = F(X1, X2, \ldots Xn) \tag{1}$$

where F is the model equation that must be implemented to describe the controlled source.

In general, IG-SPICE controlled source functions must be expressed in the form of a polynomial expression:

$$Y = Co + C1*X1 + C2*X2 + \ldots . \tag{2}$$

The advantage of the IG-SPICE user-defined controlled sources is that the coefficients need not be constants, so that general expressions for the source functions containing conditional commands can be implemented. In IG-SPICE user-defined controlled sources, the coefficients of the polynomial expression represent the partial derivatives of the output source function with respect to the input controlling variables:

$$C1 = \frac{\partial Y}{\partial X1}, \quad C2 = \frac{\partial Y}{\partial X2}, \ldots . Cn = \frac{\partial Y}{\partial Xn} \tag{3}$$

The variable Co is then calculated as follows:

$$Co = Y - C1*X1 - C2*X2 - \ldots Cn*Xn, \tag{4}$$

so that the sum of the terms of the polynomial eq. (2) will be equal to the source function Y. The values of the bias-dependent coefficients calculated in the user-defined controlled source function are returned to the IG-SPICE controlled source, which is then interpreted just as the generic SPICE polynomial controlled source function.

4) *Implementing time derivatives of controlling variables:* Another very important feature of the IG-SPICE program is the ability to save the state of the system variables between time steps during the transient analysis. The values of the previous state can be retrieved within the user-defined model subroutine to implement complicated state equations which require the time rate-of-change of the controlling variable. Basically, the time rate-of-change of a controlling current or voltage is calculated in a differential manner, using the variable at the previous time step:

$$\frac{dV}{dt} = \frac{V - V'}{\Delta t}, \tag{5}$$

where V' is the value of the variable V at the previous time step, and Δt is the time-step size. The detailed explanation of the procedure for accessing the value of variables at the previous time steps are discussed in the IG-SPICE users manual [8].

B. Implementing IGBT Model Equations

The analytical IGBT model given in Appendices 1 and 2 is suitable for incorporation into general purpose circuit simulator [3-5]. These equations are simplified expressions representing the functions of the equivalent circuit as shown in Fig. 3. The circuit in Fig. 4 is an IG-SPICE IGBT equivalent circuit representation of Hefner's analytical model which shows the interconnection of the various controlled sources required to implement the equations in Appendices 1 and 2. The model is implemented using various controlled sources that are dependent on node voltages or branch currents (but not both the currents and voltages) as required by IG-SPICE. In the remainder of this section the procedures used to convert the equations which describe the IGBT into equivalent IG-SPICE current, and voltage sources are discussed. The methods used to ensure convergence of the IG-SPICE model are also discussed.

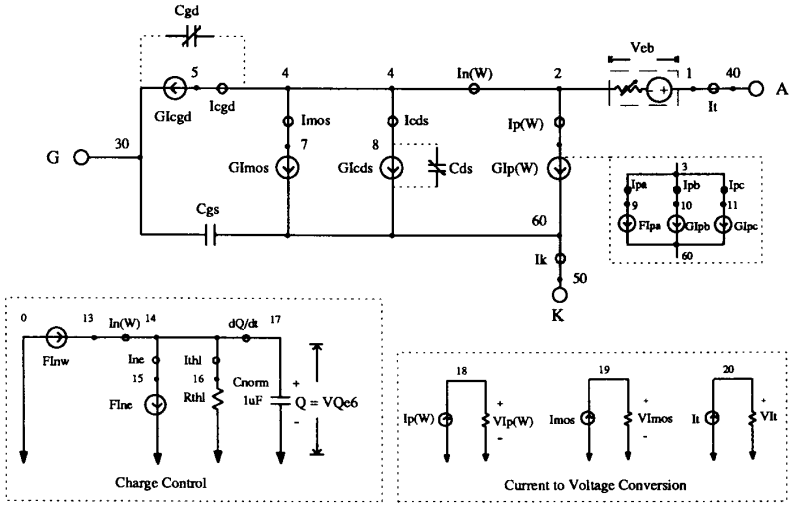


Fig. 4. IG-SPICE IGBT equivalent circuit.

1) *MOSFET:* As stated above, the MOSFET current supplies the electron current to the base of the bipolar transistor. This electron current, $I_n(W)$, consists of both static and dynamic currents that flows through the MOSFET. Thus the expression describing the electron current at the collector edge of neutral base is expressed as the sum of the MOSFET channel current and the displacement currents through the drain-source and gate-drain capacitances [3]:

$$I_n(W) = I_{mos} + (C_{dsj} + C_{gd})\frac{dV_{ds}}{dt} - C_{gd}\frac{dV_{gs}}{dt}, \tag{6}$$

where Imos is given in terms of the system variables of the IGBT as shown in Appendix 1.

In the IG-SPICE IGBT equivalent circuit model, this electron current is decomposed into three user-defined functions: Imos, Icds, and Icgd. The current sources corresponding to these functions are indicated in Fig. 4 as: GImos, GIcgd, and GIcds, respectively. The MOSFET channel current of the IG-SPICE IGBT model is described by the current source GImos, while the currents through the nonlinear capacitances (C_{gd} and C_{ds}) are represented by the controlled sources GIcgd and GIcds. These nonlinear voltage-dependent depletion capacitances (C_{gd} and C_{ds}) are indicated on Fig. 4 by the capacitor symbols with diagonal lines through them.

When implementing the capacitor currents, the value of the capacitor voltage at the previous time step needs to be used (see eq. 5) to calculate the derivative of the capacitor voltage Then the current through the capacitances can be expressed as:

$$ic = C \cdot \frac{dV}{dt}. \tag{7}$$

The gate-source capacitance C_{gs} of the IG-SPICE IGBT model is assigned a fixed value. The feedback capacitance C_{gd} is voltage dependent and has a two-phase of dependency: (one phase for $V_{ds} < V_{gs} - V_{Td}$ and another for $V_{ds} > V_{gs} - V_{Td}$ as described in Appendix 1), where the capacitor C_{oxd} is a fixed value. The drain-source depletion capacitance is also voltage dependent, but there is only one phase associated with this capacitance.

2) *Bipolar transistor collector current:* The hole current at the collector edge of the neutral base for the moving boundary condition is expressed as [3]:

$$I_p(W) = \left(\frac{1}{1+b}\right) I_T + \left(\frac{b}{1+b}\right)\frac{4D_p}{W^2}Q + \frac{C_{bcj}}{3}\cdot\frac{Q}{Q_B}\cdot\frac{dV_{bc}}{dt}. \tag{8}$$

The first term on the right-hand side of this equation results from the coupling between the transports of electrons and holes for ambipolar transport, the second term is the high-level injection charge control term, and the third term is a non-quasi-static term which describes the redistribution of carriers for the moving boundary condition [1]. This third term is represented as the collector-emitter redistribution capacitance C_{cer} in Fig. 3, which is proportional to the instantaneous change in the base, because this term depends on the time rate-of-change of the base-collector voltage.

Equation (8) depends upon current type, voltage type, and charge type controlling variables (ie., I_T, Q, V_{bc}). As previously mentioned, the controlling variables of the source functions need to be of one type: either current or voltage. To accomplish this, eq. (8) is separated into three different dependent sources: FIpa, GIpb, and GIpc, which are paralleled to obtain the total bipolar transistor hole current $I_p(W)$. This paralleling method, which reduces the number of controlling source type conversions, ensures better convergence. The collector hole current portion of Fig. 4 is shown in Fig. 5.

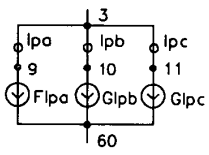


Fig. 5. Collector hole current circuit.

The first term in eq. (8) is represented as the current-controlled current source FIpa, where I_T is the total current of the device which is defined as a current source probe (see Fig. 4). The second and third terms are implemented as voltage-controlled current sources GIpb and GIpc, respectively, where the base charge Q is represented as a node voltage.

3) *Bipolar transistor base charge control:* The equation describing the conservation of excess majority carrier base charge is [6]:

$$\frac{dQ}{dt} = I_n(W) - \frac{Q}{\tau_{hl}} - \frac{Q^2}{Q_B^2}\cdot\frac{4N_B^2}{n_i^2}Isnc, \tag{9}$$

where the charge Q is supplied by the electron current at the collector edge of the base $I_n(W)$, and is depleted by the recombination in the base (the second term on the right-hand-side of the equation) and by the injection of electrons into the emitter (third term on the right-hand-side of the equation). The same problem encountered with the hole current is encountered in eq. (9). That is, the expression consists of several controlling sources, and it would be impractical to implement the whole equation within a single controlled source. Therefore, this equation is also separated into different parts. In addition, because Q is neither current nor voltage type, it must be expressed as a voltage or current type.

To do this, the expression describing the relationship between the charge, capacitance, and voltage: Q = CV, is substituted into eq. (9). By using C = 1 F, the voltage on the 1 F capacitance (VQ) represents the base charge Q, and the carrier lifetime τ_{hl} can now be identified as a resistance. As a result, the following equivalent expressions are derived:

$$\frac{dQ}{dt} \equiv \text{net current through capacitance C, and} \tag{10}$$

$$\tau_{hl} \equiv R \approx 1.0e\text{-}6\text{: where } Q/R \approx Ithl. \tag{11}$$

In addition, because the value of the resistance associated with τ_{hl} is on the order of magnitude of 10^{-6} ohms, the values of (VQ) that are solved for by the simulator are many orders of magnitude smaller than the other voltages in the circuit. This would require that the error tolerance be made very small for the SPICE-based algorithm, which would result in much longer convergence times. This problem can be alleviated by normalizing eq. (9) [4], in order to increase the resistance associated with τ_{hl} to a value on the order of 1.0. In doing this, a value of capacitance 1 uF is used to convert the charge-type variable Q to voltage (VQe6) type variable. The resulting normalized charge control expression is converted to an auxiliary circuit which is shown in the IG-SPICE IGBT equivalent circuit of Fig. 5 and is repeated in Fig. 6.

In the base charge control circuit of Fig. 6, the current-controlled current sources, FInw and FIne, describe the base current and the component of electron current injected into the emitter, respectively. The current through the resistance Rthl, which emulates the recombination in the base is represented by the current probe Ithl. The current through the normalizing capacitance Cnorm, represents the time rate-of-change of stored base charge (VQe6).

4) *Emitter-base voltage and conductivity modulated resistance:* The emitter-base voltage consists of three components as shown in Fig. 3: 1) the voltage drop across the conductivity-modulated base resistance, 2) the emitter-base diffusion capacitance potential, and 3) the emitter-base depletion capacitance potential. For forward conduction the emitter-base voltage was shown in [3] to be given by:

$$V_{eb} = V_{ebd}(V_{bc}, Q) + I_T \cdot R_b(V_{cb}, Q) + I_T \cdot R_s \tag{12}$$

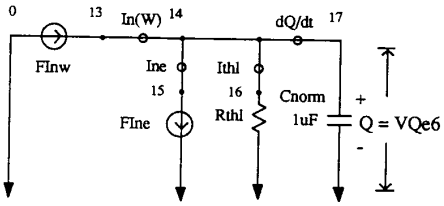


Fig. 6. Base charge control circuit.

where the conductivity-modulated resistance R_b, and the potential drop across the emitter-base diffusion capacitance V_{ebd} are obtained in terms of instantaneous values of both Q and V_{bc}. For dynamic operation, the total current I_T can flow through the base before sufficient charge, Q, is present to modulate the base resistance R_b; thus IGBTs can exhibit dynamic saturation [3, 9]. The emitter-base junction depletion capacitance C_{ebj} is important when the emitter-base junction is reverse biased or has a small forward biases, but for large forward bias, C_{ebd} is dominant.

Appendix 2 shows the equations that are needed to describe the behavior of the emitter-base voltage junction. To describe this emitter-base voltage and the conductivity-modulated base resistance R_b, a voltage-controlled voltage source (VCVS) is used. Therefore, all of the current-type controlling sources are transformed into voltage-type controlling sources by the use of the simple resistor networks shown in the lower right-hand corner of Fig. 4. Due to the complexity of the Veb function, the partial derivatives must be analyzed in detail in order to reduce the discontinuity between the partial derivatives associated with the junction depletion capacitance C_{ebj} and those associated with the diffusion capacitance C_{ebd}. In general, a discontinuity in the partial derivatives can cause convergence problems.

IV. Simulation Results

In order to examine the effectiveness of the IG-SPICE IGBT model, tests were performed for single and paralleled IGBTs with an inductive load circuit (see Figs. 5 and 6). The test conditions were such that the anode voltage was 300 V, and the gate voltage pulse amplitude was 20 V. The external load resistance RL was set so that the maximum steady-state current was 10 A. Appendix 3 shows the nominal values for the IGBT model parameters and the semiconductor device constants.

A. *Single IGBT*

The test circuit used to simulate the inductive load operation of a single IGBT is shown in Fig. 5. The simulated and measured anode voltage and anode current results are shown in Fig. 7. Extensive testing of the device was also performed for all of the circuit conditions presented in reference [3]. The simulated results of the IG-SPICE IGBT model are nearly identical to the results obtained in [3].

B. *Paralleled IGBT Operation*

Paralleled IGBTs are used extensively in power modules to obtain higher current ratings [10, 11]. However, the typical process variation of device model parameters within a given device type is significant enough to result in uneven static and dynamic current sharing if the paralleled devices were chosen randomly from a given lot of IGBTs of the same type. Simulations of paralleled IGBTs are given in Figs. 8 and 9 for variation in device parameters which are representative of a situation which would occur if the devices were not screened for similar parameters and were chosen randomly. The test circuit used to examine the paralleled operation of IGBTs is shown in Fig. 6.

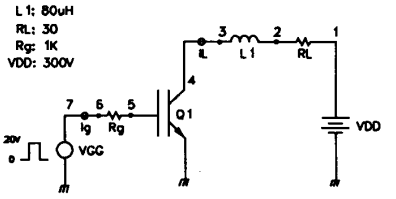


Fig. 5. Inductive load operation for a single IGBT.

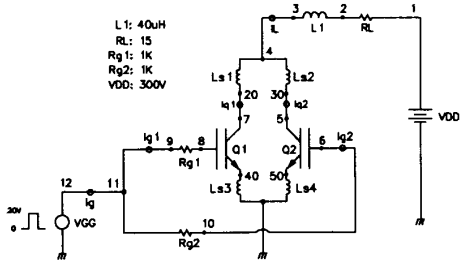


Fig. 6. Paralleled IGBTs used In inductive load.

For the paralleled operation, the gate resistances (Rg1 and Rg2), load resistance RL, and the load inductance L1, were chosen so that the devices operated similar to the single IGBT circuit of Fig. 5 when the nominal parameter values were used for both devices. In order to accomplish this task, the values of L1, and RL were reduced by a factor of 2, and the gate resistor values were fixed at 1kΩ for each device.

In order to observe how the dissimilar parameters affected current sharing of the paralleled IGBTs, the parameters lifetime τ_{bl}, threshold voltage Vt, and transconductances Kp were varied from the nominal values. These parameters were chosen because the normal process variation of these parameters has the most impact on current sharing for parallel operation. The test results for these parameter variations are shown in Figs. 8 and 9. Figure 8 compares the (a) simulated and (b) measured anode current and voltage waveforms for paralleled IGBTs where the base lifetime of one of the devices is varied from the nominal values in Appendix 3 (ie., τ_{bl} = 2.45 us for one of the devices). Figure 9 compares the (a) simulated and (b) measured anode current and voltage waveforms for parallel operation of IGBTs where one of the devices has a threshold voltage and transconductance that are varied from the nominal values (ie., Vt=3.8 V and Kp_{sat} = 0.64 A/V^2 for one of the devices).

The anode voltage and anode current waveforms of the paralleled IGBTs with different device base lifetimes (Fig. 8) are similar to those for the single device (Fig. 7), with the exception that the static current sharing of the paralleled devices are uneven, and the current tail is smaller for the lower lifetime device. For the devices with different MOSFET threshold voltages and transconductances (Fig. 9), a turn-on delay exists for the device with the lower transconductance, and a turn-off current spike exists for the device with the larger transconductance. The turn-on delay occurs for the lower transconductance device because it has a higher resistance than the other device until its gate voltage becomes large enough that the on-state resistances of both devices are primarily determined by the bipolar emitter-base voltages. The turn-off current spike in the higher transconductance device occurs because the resistance of the low transconductance device becomes larger sooner than for the high transconductnace device, and the inductor current is transferred to the lower resistance, high transconductance device.

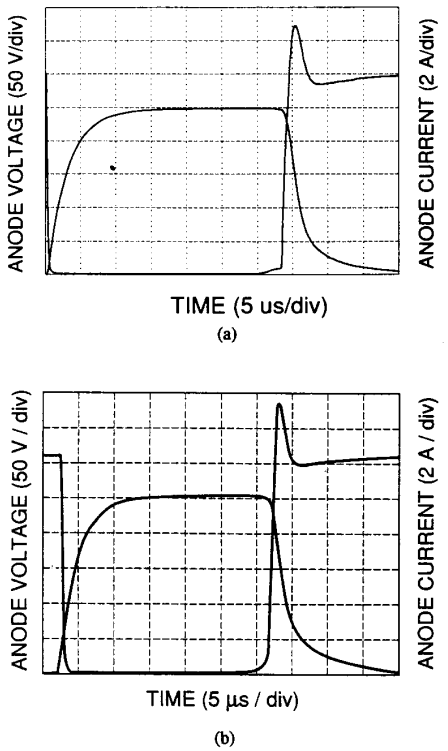
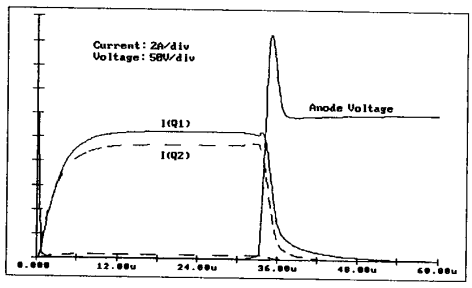
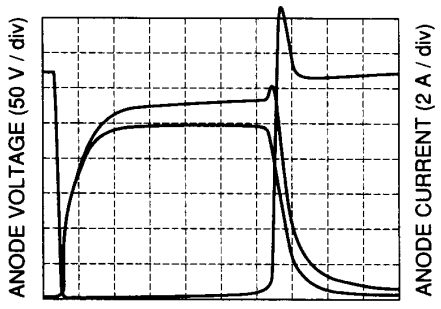


Fig.7. Anode current and voltage waveforms for a single IGBT switched with an inductive Load. (a) simulated (b) measured.

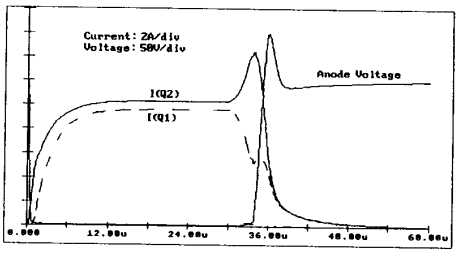


(a)

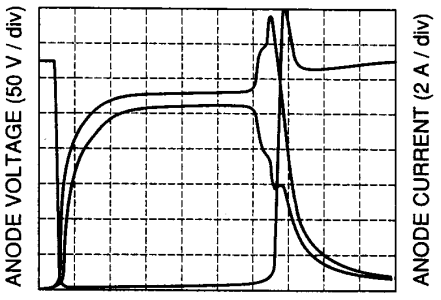


(b)

Fig. 8. Paralleled IGBTs with variation in lifetime: (a) simulated (b) measured.



(a)



(b)

Fig. 9. Paralleled IGBTs with threshold voltage and transconductance variation: (a) simulated (b) measured.

V. Conclusion

A previously developed physics-based IGBT model is implemented into the IG-SPICE circuit simulator. The IG-SPICE circuit simulator was chosen for this study because it provides the user with programming capability. This programming capability is essential for implementing the complex model equations that are necessary to describe the behavior of the IGBT. When implementing physics-based models into IG-SPICE: 1) the model must be formulated as an interconnection of controlled sources, 2) the variables used to formulate the model must be normalized so that each variable has a comparable absolute error tolerance, and 3) the partial derivatives of the controlled source functions with respect to each controlling variable must be evaluated.

The IG-SPICE IGBT model developed in this paper is verified by comparing the results of the model with experimental results for various circuit operating conditions. The model performs well and describes experimental results accurately for the range of static and dynamic conditions in which the device is intended to be operated. The effectiveness of the IG-SPICE IGBT model is demonstrated by examining the effects of the normal process variation of the model parameters upon the static and dynamic sharing of paralleled IGBTs. The results indicate that the threshold voltage and transconductance variations tend to result in dynamic current spikes, whereas lifetime variations tend to result in uneven current tails. Both lifetime and transconductance variations result in uneven static sharing.

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Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

APPENDIX 1
IGBT Current Sources [1]

$$N_{scl} = N_B + I_p(W)/(qAv_{psat}) - I_{mos}/(qAv_{nsat})$$

$$W_{gdj} = \sqrt{2\epsilon_{si}(V_{ds} - V_{gs} + V_{Td})/qN_{scl}}$$

$$W_{dsj} = \sqrt{2\epsilon_{si}(V_{ds} + 0.6)/qN_{scl}}$$

$$W_{bcj} = \sqrt{2\epsilon_{si}(V_{bc} + 0.6)/qN_{scl}}$$

$$W = W_B - W_{bcj}$$

$$BV_{cbo} = BV_f \cdot 5.34 \times 10^{13} \cdot N_{scl}^{-0.75}$$

$$M = 1/[1 - (V_{cb}/BV_{cbo})^{BV_n}]$$

$$Q_B = qAWN_{scl}$$

$$C_{bcj} \equiv A\epsilon_{si}/W_{bcj}$$

$$C_{dsj} = (A - A_{gd})\epsilon_{si}/W_{dsj}$$

$$C_{gdj} = A_{gd}\epsilon_{si}/W_{gdj}$$

$$C_{gd} = \begin{cases} C_{oxd} & \text{for} \quad V_{ds} \le V_{gs} - V_{Td} \\ C_{oxd}C_{gdj}/(C_{oxd} + C_{gdj}) & \text{for} \quad V_{ds} > V_{gs} - V_{Td} \end{cases}$$

$$I_{mos} = \begin{cases} 0 & \text{for } V_{gs} < V_T \\ \dfrac{K_{Plin}\left[(V_{gs} - V_T)V_{ds} - \dfrac{K_{Plin}V_{ds}^2}{2K_{Psat}}\right]}{[1 + \theta(V_{gs} - V_T)]} & \text{for } V_{ds} \le (V_{gs} - V_T)\dfrac{K_{Plin}}{K_{Psat}} \\ \dfrac{K_{Psat}(V_{gs} - V_T)^2}{2[1 + \theta(V_{gs} - V_T)]} & \text{for } V_{ds} > (V_{gs} - V_T)\dfrac{K_{Plin}}{K_{Psat}} \end{cases}$$

$$I_p(W) = \left(\frac{1}{1+b}\right) I_T + \left(\frac{b}{1+b}\right)\frac{4D_p}{W^2}Q + \frac{C_{bcj}}{3}\cdot\frac{Q}{Q_B}\cdot\frac{\mathrm{d}V_{bc}}{\mathrm{d}t}$$

$$I_{gen} = 2qn_iAW_{bcj}/\tau_{HL}$$

$$I_{mult} = M \cdot I_{gen} + (M-1)\cdot(I_p(W) + I_{mos})$$

$$I_g = (C_{gs}+C_{gd})\cdot\frac{\mathrm{d}V_{gs}}{\mathrm{d}t} + C_{gd}\cdot\frac{\mathrm{d}V_{bc}}{\mathrm{d}t}$$

$$I_n(W) = I_{mos} + I_{mult} + (C_{dsj}+C_{gd})\frac{\mathrm{d}V_{ds}}{\mathrm{d}t} - C_{gd}\frac{\mathrm{d}V_{gs}}{\mathrm{d}t}$$

$$I_T = I_n(W) + I_p(W)$$

APPENDIX 2
IGBT Anode Voltage

$$1/\mu_c = \left[\ \overline{\delta p}\ \ln(1 + \alpha_2\ (\overline{\delta p})^{-2/3})\right]/\alpha_1$$

$$\mu_{nc} = 1/(1/\mu_n + 1/\mu_c)$$

$$\mu_{pc} = 1/(1/\mu_p + 1/\mu_c)$$

$$\mu_{eff} = \mu_{nc} + \mu_{pc}Q/(Q + Q_B)$$

$$D_{ccs} = (kT/q)\mu_{nc}\mu_{pc}/(\mu_{nc} + \mu_{pc})$$

$$L = \sqrt{D_{ccs}\tau_{HL}}$$

$$P_0 = Q/(qAL\tanh\tfrac{W}{2L})$$

$$\overline{\delta p} \equiv P_0\sinh(W/2L)/\sinh(W/L)$$

$$Q_0 = A\sqrt{2\epsilon_{si}qN_B0.6}$$

$$n_{eff} \equiv \frac{\frac{W}{2L}\sqrt{N_B^2 + P_0^2\mathrm{csch}^2(\frac{W}{L})}}{\arctanh\left[\dfrac{\sqrt{N_B^2 + P_0^2\mathrm{csch}^2(\frac{W}{L})}\tanh(\frac{W}{2L})}{N_B + P_0\mathrm{csch}(\frac{W}{L})\tanh(\frac{W}{2L})}\right]}$$

$$R_b = \begin{cases} W/(q\mu_{nc}AN_B) & \text{for} \quad Q < 0 \\ W/(q\mu_{eff}An_{eff}) & \text{for} \quad Q \ge 0 \end{cases}$$

$$V_{ebj} = 0.6 - (Q - Q_0)^2/(2qN_B\epsilon_{si}A^2)$$

$$V_{ebd} = \frac{kT}{q}\ln\left[\left(\frac{P_0}{n_i^2} + \frac{1}{N_B}\right)\left(N_B + P_0\right)\right] - \frac{D_{ccs}}{\mu_{nc}}\ln\frac{P_0 + N_B}{N_B}$$

$$V_{ebq} = \begin{cases} V_{ebj} & \text{for} \quad Q < 0 \\ \min(V_{ebj}, V_{ebd}) & \text{for} \quad Q_0 > Q \ge 0 \\ V_{ebd} & \text{for} \quad Q \ge Q_0 \end{cases}$$

$$V_{eb} = V_{ebq} + I_T \cdot R_b$$

$$V_A = V_{eb} + V_{cb}$$

$$\frac{\mathrm{d}Q}{\mathrm{d}t} = I_n(W) - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2}\cdot\frac{4N_{scl}^2}{n_i^2}I_{snc}$$

APPENDIX 3
Nominal Device Parameters

τ_{HL}	$7.5\ \mu s$
N_B	$2 \times 10^{14}\ cm^{-3}$
A	$0.1\ cm^2$
W_B	$93\ \mu m$
I_{snc}	$6.0 \times 10^{-14}\ A$
K_{Psat}	$0.46\ A/V^2$
K_{Plin}	$0.95\ A/V^2$
V_T	$4.7\ V$
A_{gd}	$0.05\ cm^2$
C_{oxd}	$1.6\ nF$
C_{gs}	$0.6\ nF$
V_{Td}	$\sim 0\ V$
n_i	$1.45 \times 10^{10}\ cm^{-3}$
μ_n	$1500\ cm^2/V\text{-}s$
μ_p	$450\ cm^2/V\text{-}s$
ϵ_{si}	$1.05 \times 10^{-12}\ F/cm$
α_1	$1.428 \times 10^{20}(cmVs)^{-1}$
α_2	$4.54 \times 10^{11}cm^{-2}$
v_{nsat}	$1.1 \times 10^7 cm/s$
v_{psat}	$0.95 \times 10^7 cm/s$
BV_f	1.0
BV_n	4.0
θ	$0.01\ V^{-1}$

[1] The symbols used in Tables 1, 2, and 3 are defined in reference [3].