INTEGRATED ACTIVE FILTER AUXILIARY POWER MODULES IN ELECTRIFIED VEHICLE APPLICATIONS

INTEGRATED ACTIVE FILTER AUXILIARY POWER MODULES IN ELECTRIFIED VEHICLE APPLICATIONS

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To my Parents, Guoqiang and Bangyu,

and my Fiancee, Wen

ABSTRACT

In this thesis, integrated active filter auxiliary power modules (AFAPMs) is presented in electrified vehicle applications.

A topological evaluation is conducted particularly for the auxiliary power module (APM) applications in the electrified vehicles. Several primary and secondary base topologies are compared in terms of VA rating and performance. Multiple input/output topology configurations are compared with different connection configurations and control schemes. The MOSFET loss analysis is given. Based on the MOSFET loss analysis, the modular full bridge current doubler with input-series-output-parallel configuration presents better performance in terms of the switch efficiency and cost analysis.

Bulk capacitor banks occupy large volume and impact the reliability in the traction inverter and HV battery charger in the vehicle applications. A capacitor-less design is relatively urgent for the next generation electrified vehicle. Active filter (AF) is one potential solution to reduce the corresponding dc-link capacitance. However, additional components are required which increases the system complicity and decreases its reliability. Hence, it would be great to integrate the AF into the LV battery charger for the vehicle applications. Based on the power switch requirements, the AFAPM is evaluated for traction inverter and HV battery charger, respectively. The evaluation result shows that the AFAPM for the HV battery charger system is a feasible and attractive

solution. Furthermore, a simple and effective dual-mode dual-voltage charging system operating principle is proposed. The integrated AFAPM converter charges the LV battery when the vehicle is running and operates as an AF when the vehicle is connected to the grid and the HV battery is charging. Hence, the low-frequency second-order harmonic current is alleviated without a bulk capacitor bank or an extra AF circuit in the HV battery charger.

For magnetic design, there is a trend toward integration and planarization. Two planar transformers are built for two different AFAPM prototypes. A minimized leakage inductance method is presented and implemented on a 20:1 center-tapped planar transformer.

Three different integrated AFAPM converters are proposed. By applying these AFAPM converters, the required extra components to form the AF for the HV battery charger are reduced and thus the cost, size and weight for the dual-voltage charging system in the electrified vehicle applications can be reduced. Two prototypes are built. The experiments show promising results confirming the effectiveness of the proposed converters.

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LIST OF ABBREVIATIONS

AF	Active filter
AFAPM	Active filter auxiliary power module
AP	Area Product
APM	Auxiliary power module
CO_2	Carbon dioxide
DAB	Dual active bridge
DCM	Discontinuous conduction mode
DPCI	Dual-phase-coupled-inductor
DPDI	Dual-phase-dual-inductor
DPDT	Double pole double throw
DPS	Dual-phase-shift
DPSI	Dual-phase-single-inductor
EDSR	External-driven synchronous rectification
EMI	Electromagnetic interference
EPA	Environmental protection agency
EPS	Extended-phase-shift
ESE	Extension of Steinmetz equation
FBCD	Full bridge with current doubler
GHG	Greenhouse gas
HV	High-voltage
ICE	Internal combustion engine
IGBT	Insulated-gate bipolar transistor
IPOP	Input-parallel-output-parallel
IPOS	Input-parallel-output-series
ISOP	Input-series-output-parallel
ISOS	Input-series-output-series
KG	Core Geometry

LV	Low-voltage
MIMO	Multiple-input-multiple-output
MLT	Mean-length-turn
MMF	Magnetomotive force
MnZn	Manganese-zinc
NiZn	Nickel-zinc
OSE	Original Steinmetz equation
PFC	Power factor correction
PHEV	Plug-in electric vehicle
PWM	Pulse-width modulation
REEV	Range extended electric vehicle
SBD	Schottky barrier diode
SDSR	Self-driven synchronous rectification
SiC	Silicon-Carbide
SIMO	Single-input-multiple-output
SIOP	Single-input-output-parallel
SISO	Single-input-single-output
SOC	State-of-charge
SPS	Single-phase-shift
SPWM	Sinusoidal pulse-width modulation
SR	Synchronous rectification
SVPWM	Space vector pulse-width modulation
THD	Total harmonic distortion
WBG	Wide band-gap
WCSE	Waveform-Coefficient Steinmetz equation
ZVS	Zero voltage switching

Chapter 1

INTRODUCTION

1.1 INTRODUCTION TO ELECTRIFIED VEHICLES

1.1.1 Architectures of electrified vehicles

Nowadays more attention has been attracted to fuel economy, due to the concern for worldwide uncertainty in energy supplies, global climate change, and pollution control. There is growing public acceptance that carbon dioxide (CO_2) emissions are one of the primary contributors to global climate change. The CO_2 generated by burning fossil fuels is a major contributor to the greenhouse gas (GHG) emissions [1]. In the meanwhile, in 2012, the U.S. environmental protection agency (EPA) established new fuel economy standards. They mandate that the average fuel economy of passenger cars and light-duty trucks in the U.S. has to rise to 54.5 miles per gallon by 2025 [2]. This target can be hardly achieved by improving the internal combustion engine (ICE) technology. As one of the most promising and practical sustainable solutions for transportation, electrified vehicles enable cleaner, greener, and, in many regions, domestically produced electricity to replace petroleum [3-4]. Electrified transportation is a paradigm shift from conventional ICE-based vehicles to more efficient and cleaner electrified vehicles. Electrification can occur in both vehicular propulsion and nonpropulsion loads. Higher degrees of electrification represent a larger power electrical path leading to less use of

fossil fuels and hence, better fuel economy and lower GHG emissions [5]. The U.S. plug-in electric vehicle sales by model from 2011 to 2015 can be found in the Fig. 1.1 [6]. Note that the listed vehicles include plug-in hybrid electric vehicles (PHEV) and range extended electric vehicles (REEV). Only full-sized vehicles sold in the U.S. and capable of 60mph are listed. It is clear that in recent years, more car manufacturers start to enter the competitive market of PHEV and REEV. In addition, the sales for most of the vehicle models are rising.

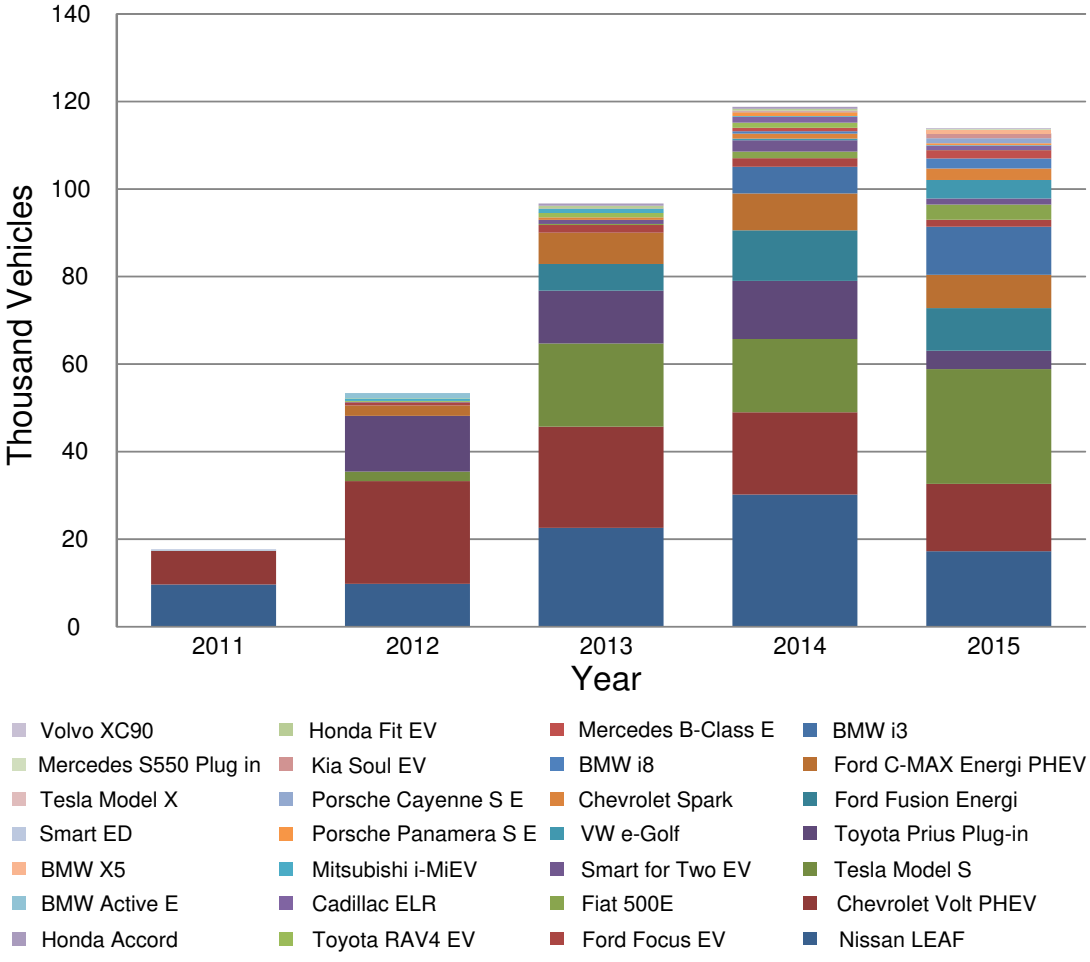


Fig. 1.1. 2011-2015 U.S. plug-in electric vehicle sales by model [6].

Power electronics plays an increasingly important role in the electrified vehicle applications [7]. The power electronic techniques provide compact and high-efficient solutions to power conversion [8-10]. Power electronic converters and traction motor drives have been responsible for a major part of the vehicle's energy usage. The Tesla model S is a typical example. Its electrified power-train architecture is shown in Fig. 1.2 [11]. A high-voltage (HV) battery is the main power source in the vehicle. It is charged by a HV battery charger thru the charge port when the vehicle is plugged in. A traction inverter is applied to control the traction motor. A low-voltage battery (LV) is needed to provide the power for the nonpropulsion loads. A LV battery charger auxiliary power module (APM) is placed between the HV and LV battery for the power conversion.

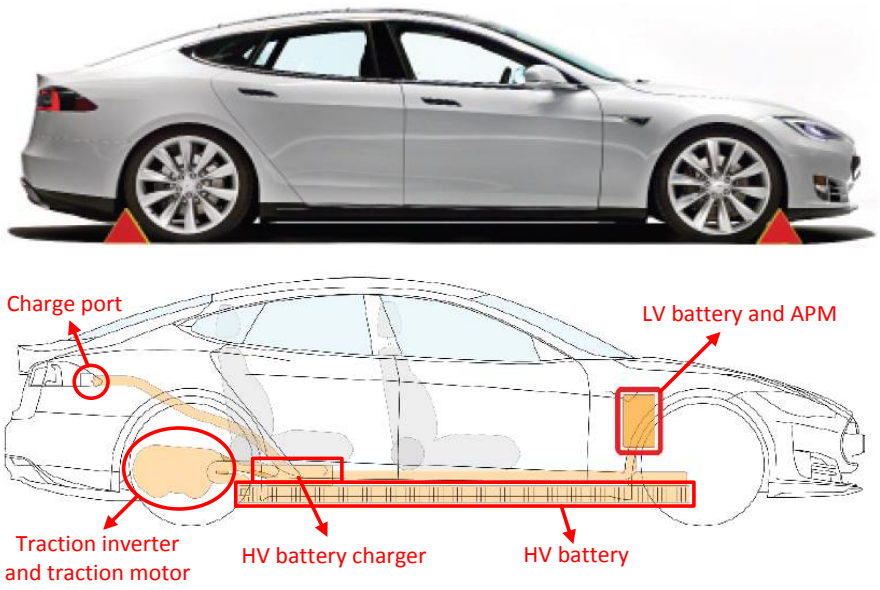


Fig. 1.2. The Tesla Model S electrified power-train architecture [11].

One of the biggest challenges for the next generation of power electronic system in vehicle application will be the cost reduction to provide more affordable solutions,

which has become one of the major barriers for electrified vehicle to mass commercialization. Size, weight and reliability are the other main constrains on power electronic system in vehicle applications.

1.1.2 Requirements of traction inverter in electrified vehicles

The requirements on the traction drive system depend on its specific power-train. According to the degree of hybridization, power-trains can be divided into three categories: micro, mild, and full hybrids [12-13]. In micro hybrid, the power rating of the traction electric machine is low as it is only applied to start the vehicle and capture partial energy from the regenerative braking without any electric propulsion. In mild hybrid, besides the stop/start feature and regenerative braking capability, it incorporates a limited use of electric power for propulsion assist. In the full hybrid systems, the traction drive system is capable of functioning together or independently to propel the vehicle based on the drive requirements. The electric-only drive mode is made possible with a traction motor that can be rated as high as 80 kW. To cater to such high-electric-power requirements, full hybrids are equipped with a larger battery pack compared to mild hybrids [13-15].

Three-phase inverters for traction drive are the vital power processing units between the dc-link and electric machines. A 55 kW traction inverter with Infineon power module is shown in Fig. 1.3 [16]. In addition, based on different traction drive requirements, a boost converter can be added before the traction inverter to improve the overall system efficiency by increasing dc-link voltage of the inverters. The detailed

traction drive specification for different types of powertrain can be summarized in Table 1.1.

Table 1.1. Traction drive system specifications for different powertrains.

	Micro hybrid	LV mild hybrid	HV mild hybrid	Full hybrid
Power (kW)	3-7	8-12	12-20	20-80
DC-link voltage (V)	<60	<60	110-200	170-450
Switching frequency (kHz)	15-30	15-30	5-15	5-15

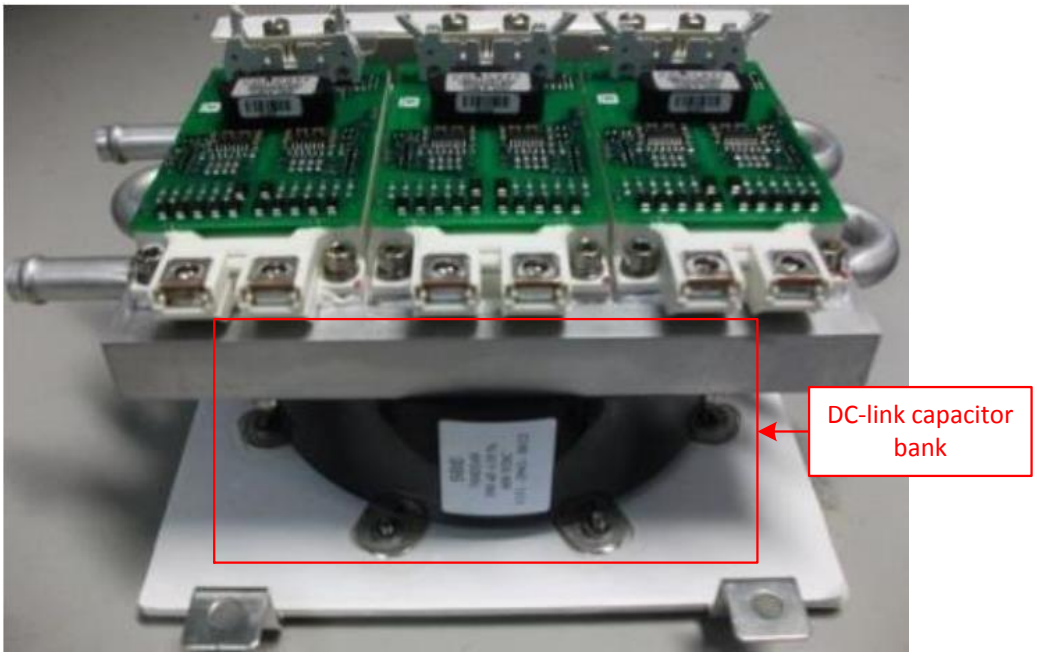


Fig. 1.3. A 55 kW traction inverter with Infineon power module [16].

1.1.3 Requirements of HV battery charger in electrified vehicles

The charging approaches for the electrified vehicle applications can be divided into two categories: conductive and inductive charging [17]. Conductive charging has hard-wired connection between the power supply and the charger. Inductive charging does not use wired connection. It is also known as wireless charging. Conductive charging can also be divided into two types: the ac charging system and dc charging system. The ac charging system is commonly an on-board charger mounted inside the vehicle and is connected to the grid. The dc charging system is commonly an off-board charger mounted at fixed locations, supplying required regulated dc power directly to the batteries inside the vehicle [18]. Usually, the ac three-phase battery storage system is used for bulk energy storage devices for industry and the ac single-phase battery storage system is for small home storage systems.

From the topology aspect, the ac conductive charging topologies can be categorized into two types: single-stage and two stage charger, as shown in the Fig. 1.4. The single-stage charger is compact and it combines both ac/dc and dc/dc into one stage. It can achieve smaller size, lower cost, and higher efficiency. The drawbacks are that it might not provide isolation, and usually it contains large low frequency current ripple in the converter [19-20]. For the two-stage charger, it is an ac/dc power factor correction (PFC) boost converter followed by either a non-isolated or an isolated dc/dc converter.

The role of the front-end ac/dc converter is to convert the supply ac voltage into dc voltage and also act as input current shaper for PFC and harmonic reduction. Power factor and total harmonic distortion (THD) are the major factors that influence the

selection of a particular PFC rectifier topology [17]. Boost type topologies and their variants are widely used for PFC rectification purposes [21]. The main function of this second stage dc/dc converter is to offer regulated voltage and current to better charge the HV battery. The advantages of the two-stage topology are that it provides high power factor, wide line regulation performance and clean charge current [18]. In the meanwhile, isolated charger is preferred for onboard use considering the safety aspect [15].

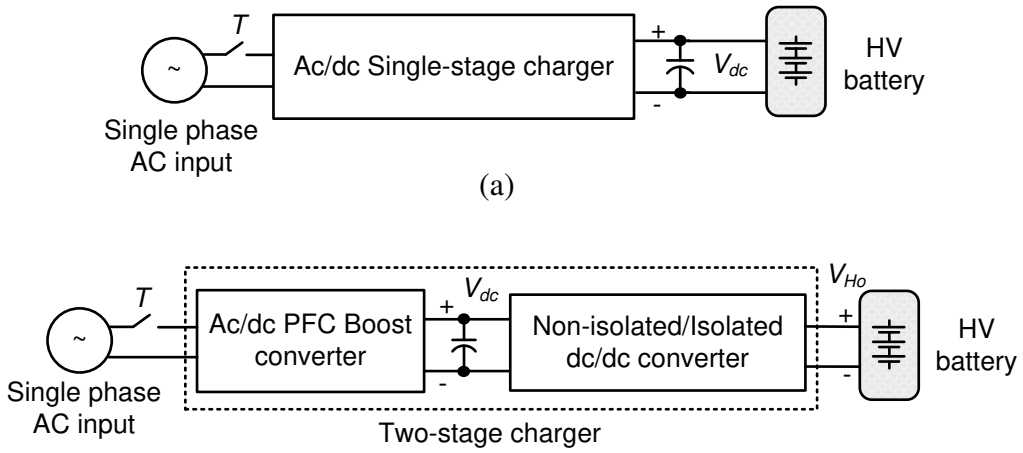


Fig. 1.4. Conductive charging topologies (a) Single-stage charger. (b) Non-isolated/isolated two-stage charger.

The ac single-phase battery charger can also be classified by the level of power they can provide to the battery pack, as shown in Table 1.2 [22]. Generally speaking, for the ac input voltage level, most of Europe, Asia, Africa and most of South America use a supply that is within 6% of 230 V. Japan and North America use a voltage between 100 and 127 V. The 230 V standard has become widespread so that 230 V equipment can be

used in most parts of the world. Hence, the dc-link voltage after the PFC is usually around 400 V [16, 22]. A 3.3 kW bridgeless interleaved PFC prototype for single-phase EV charger from Delta-Q is shown in Fig. 1.5 [24].

Table 1.2. HV battery charger specifications for different EV powertrains.

	AC level 1	AC level 2	AC level 3
Power (kW)	1.08-1.44	3.3-6.6	≥14.4
AC input voltage (V_{AC})	120	208-240	208-240
AC line frequency (Hz)	50-60	50-60	50-60
HV battery DC bus voltage V_{dc} (V)	200-400	200-400	200-400

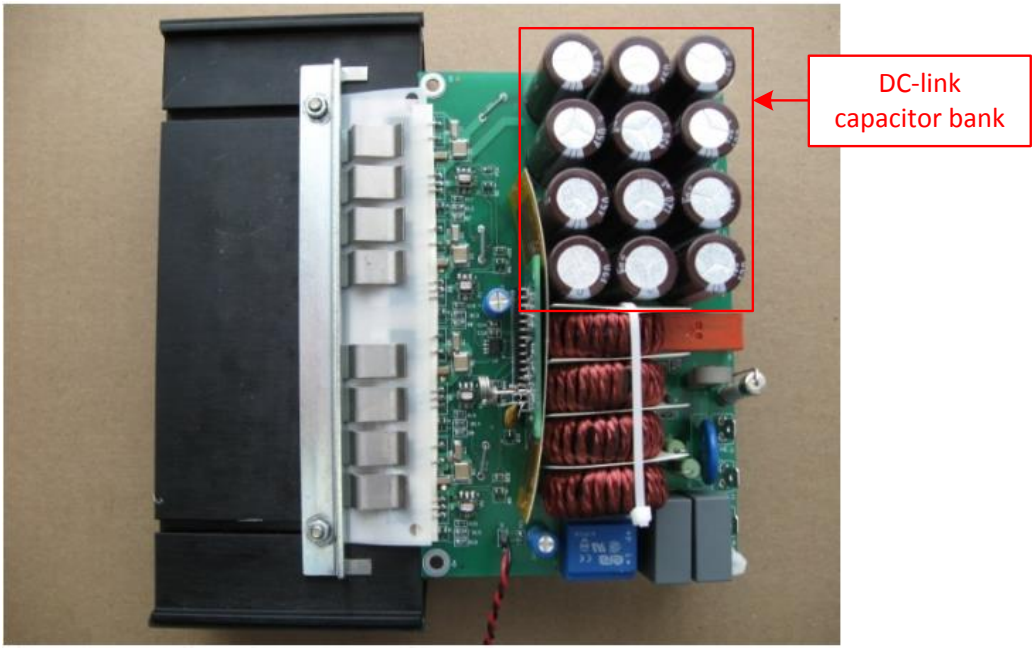


Fig. 1.5. A 3.3 kW PFC prototype for single-phase EV charger from Delta-Q [24].

1.2 INTRODUCTION TO AUXILIARY POWER MODULES

In conventional vehicles, the traction power is supplied by the ICE. In order to provide power to the vehicle electrical loads, a LV system is utilized, which includes a belt-driven alternator, LV battery and various electrical loads. When the engine is running, it provides torque to the alternator, which then provides electrical energy to the 12 V battery. In conventional vehicles, synchronous generators are utilized, due to their low cost structure and reliable operation [25]. Depending on the charging current of the LV battery and the load requirements in the vehicle electrical system, the field current of the alternator is controlled by a regulator to keep the system voltage constant. In light-duty vehicles, battery voltage is usually 12 V and, when the vehicle is running, system voltage is approximately 13.5 V in summer time and 14.5 V in winter time [25]. With the engine stopped, only LV battery supplies power to the electrical loads. The battery also behaves like a buffer in the electrical systems and stores energy.

With the improvements in vehicle technology, safety requirements and increasing customer demands, many electric and electronic loads have been added to the vehicle electrical system. In conventional vehicles, the electrical system has to supply enough power to the entire vehicle network, provided that the quality of the voltage is high enough to ensure the functional safety of electronic loads, especially control units.

In electrified vehicles, similar LV electric and electronic loads still exist. However, traction system voltage is usually much higher than the vehicular electrical system voltage. The vehicular system voltage is 12 V. In all-electric vehicles, the voltage

levels are also similar. In belt-driven starter generator applications, the traction power is usually supplied by lead-acid batteries and the voltage is set around 48 V. This is mainly because the precautions required for HV systems do not need to be applied in a 48 V system, since HV standards are applied over 60 VDC [13]. The traction motors, generator or starter alternators in electrified powertrain applications are designed for the above mentioned voltage levels and they cannot be utilized to supply power directly to the vehicular loads. For this reason, power converters are required, which convert HV from the traction battery to a lower voltage in order supply power to the vehicular electrical and electronic loads, and also to charge the LV battery. This power converter is usually called as APM.

Depending on the road and weather conditions, many electric loads are on and off when the vehicle is being driven or stopped. Therefore APM can draw power from the HV battery anytime throughout the drive cycle and it might affect the state-of-charge (SOC) of the HV battery. In hybrid electric vehicles, if the SOC of the HV battery is low, the engine turns on and charges the battery through the generator. This increases vehicle's emissions and fuel consumption. In all-electric vehicles, lower SOC reduces the range of the vehicle. Therefore, efficiency of the APM is very important to maintain a higher vehicle performance.

1.2.1 LV nonpropulsion loads in electrified vehicle applications

The LV battery in the vehicle applications is usually lead-acid battery. Its capacity is typically around 60-70 Ah [26-27]. The LV system in a vehicle constitutes many different loads. These can be categorized as lighting, wiper and window systems, air

conditioning and heater, electronic, battery and power electronics cooling system, and other loads. As shown in Fig. 1.6, air conditioning loads draw most of the power from the electrical system. These include radiator fan, blowers and seat heaters.

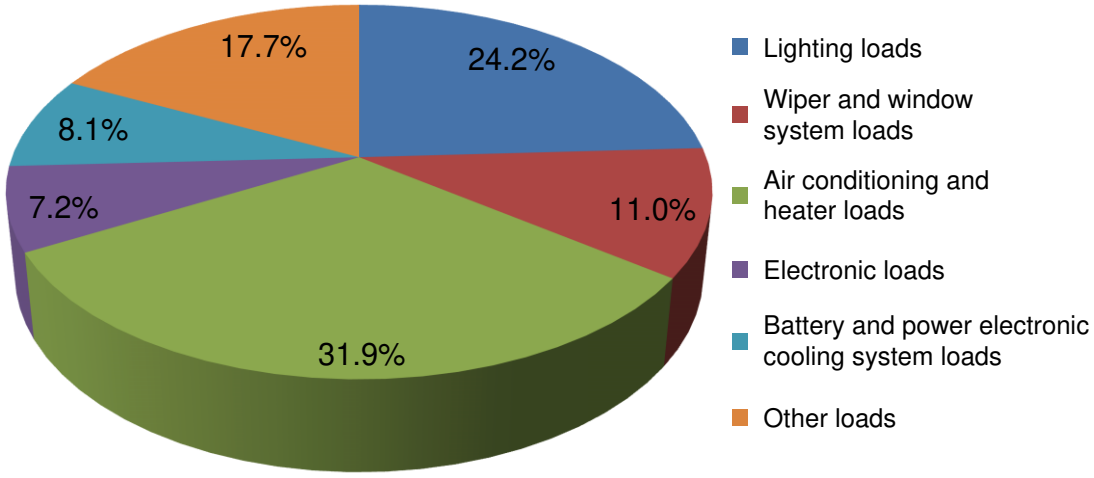


Fig. 1.6. Load power distribution in a 2.4 kW LV system of vehicle application.

Lighting loads consume around 24.2% of the total power in a vehicular electrical system [25]. They are composed of many different loads including headlights, park lamps, flashers, turn signals, fog lamps, etc. Among these back lights, headlamps, and fog lamps draw most of the power. In a typical vehicle, wiper and window system related loads draw around 11% of the total power [25]. Electronic loads include the control units, displays, CD player, Bluetooth, and power outlets. They occupy around 7.2% of the total power. The coolant pumps for the battery and power electronic system draw the most power in the cooling system loads. It takes around 8.1% of the total power. Last but not

least, the electric power steering and motor engaging park brake are some other loads in the LV electric power system.

Most of the loads in the LV electrical system are resistive loads. The resistance that is seen from the supply side changes with the current drawn by the load. The fans, pumps, wipers and power windows all have electric motors, which are usually controlled by their corresponding control system. The power drawn by the fans is dependent on the fan speed. Ambient temperature and the cabin temperature set by the driver determines the coolant flow rate and, hence, the electrical power drawn by the coolant pump. In some circumstances many of these loads can operate together. However, the status of the vehicle and the driving conditions usually determine the activation of the loads.

Table 1.3 shows several APM ratings from electrified vehicles on the market [28-31]. There is a chance that the load current level of the LV system might be rated higher in vehicles where additional luxury loads are requested, such as sunroof, active suspension system or other entertainment systems.

Table 1.3. LV battery charger APM specifications for several EVs on the market.

Models	Toyota Prius II and III	Chevrolet Volt 2011	Tesla Roadster 2008
Power (kW)	1.4	2.2	2.4
Nominal input voltage (V)	202	360	366
Output current (A)	100	165	200

1.2.2 Requirements of auxiliary power module

APM draws power from the HV battery and powers the loads in the LV system. In an electrified powertrain, the size of the HV battery determines the range and the emissions of the vehicle. The more current the APM draws, the higher the drop in the SOC of the HV battery. This might have a significant effect on the vehicle performance. Therefore, the most important requirement for APM is its efficiency. With a higher efficiency, APM draws less power from the HV battery and the battery charge can be utilized more to power the drivetrain. In practice, the peak efficiency of APM is expected to be higher than 95% in the medium and heavy load conditions. The reliability of APM is also very important since it powers all microprocessors in the vehicle and, thus, keeps the vehicle awake [25].

As the APM creates an electrical conversion between the HV system and the LV system of the vehicle, a galvanic isolation must be used for safety reasons. This ensures that a failure within the HV system won't affect the LV system and shut down the vehicle. The opposite is also true, galvanic isolation would protect the HV system from a failure happening on the LV system, which is directly accessible to the driver and passengers within the vehicle.

The other important requirement for APM is the quality of the output voltage. Especially the electronic loads, such as the control units, radio, and the CD player are very sensitive to the ripple content of the voltage supplied by the APM [25]. For this reason, the output voltage ripple of APM should be quite low, which might require

designing output filters. As such a filter is generally bulky in comparison to the converter; it brings challenges in defining the switching frequency which strongly affects the filtering requirements, but also losses, and as well as the output capacitance and inductance of the converter.

The SOC of the HV battery varies depending on the traction power requested from the HV battery. The terminal voltage and, hence, the input of the APM changes in this case. Therefore, APM is required to operate in a certain input voltage range and provide the output voltage specifications for the entire input voltage range.

Finally, APM should be designed to operate in various temperature conditions. In automotive system, the operating temperature usually varies between -40 °C to 85 °C, so that the vehicle could operate in different climatic regions around the world. For a power converter with high efficiency requirements, the ambient temperature is very important when defining the size of the cooling system. As an example, the resistance of the transformer and inductor windings and the conduction losses of the power semiconductor switches are dependent on temperature. Therefore, the designer should design the thermal management system for the given specifications, which ensures that the required efficiency can be maintained in various ambient conditions.

1.3 INTRODUCTION TO CAPACITOR-LESS DESIGN

Although electrified vehicles present superior fuel economy compared to the conventional ICE vehicles, the integration of power electronic converters and inverters

into the system of vehicles has side effects on the reliability of the whole system [32]. In addition, the ambient temperature of power electronic converters in electrified vehicles is relatively high and, therefore, the thermal stress of components is relatively high, which reduces the reliability. Furthermore, automotive industry is a safety critical application field. Any malfunctions of components will lead to shutdown of the system directly. These unscheduled interruptions not only cast significant safety concerns, but also increases system operation cost and partially offsets the benefits of introducing power electronic systems [33]. Therefore, the reliability of power electronic converters in electrified vehicles is important and it attracts more and more attentions [16].

It has been proven that the power switch devices and capacitors are the most vulnerable components in the power electronic systems [33]. Therefore, the reliability of the system can be improved with the minimum increased number of power switch devices and capacitors.

In general, for electrified vehicle applications with a single-phase charging approach, there are mainly two bulk capacitor banks exist inside the vehicle as shown in Fig. 1.7. The first is on the dc-link of the traction inverter and the other is in the on-board HV battery charger, where it is normally on the dc-link after the PFC boost converter. From Fig. 1.3 and 1.5, it is clear that those two bulk capacitor banks occupy considerable spaces, which impact the power density of the inverter and converter significantly.

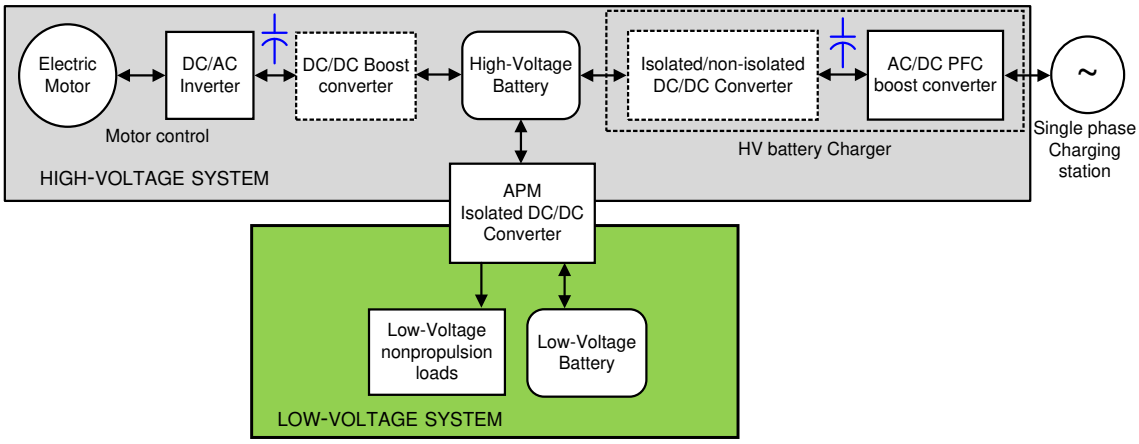


Fig. 1.7. Typical electrified vehicle powertrain block diagram.

In power electronics converters, the dc-link capacitor can be electrolytic, film or ceramic capacitors. A comparative overview of these three capacitor types has been done in [34]. Ceramic capacitor can operate at relatively high temperature. However, it is brittle and is not preferred by car manufacturers due to its destructive failure mechanism [35]. One typical failure mechanism of the ceramic capacitor is cracking, when the PCB is bent. This will damage the capacitor body as shown in Fig. 1.8 [36].

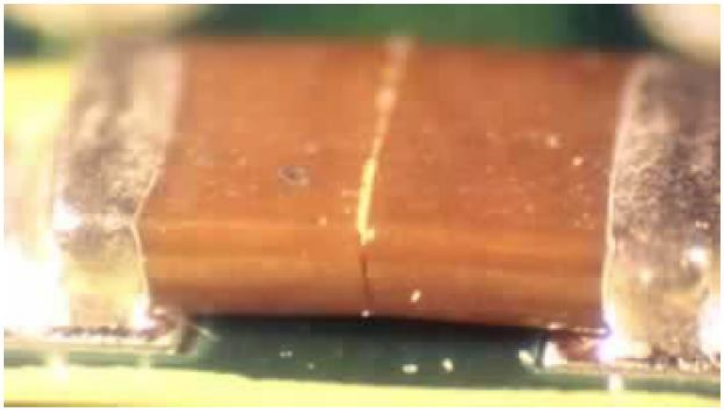


Fig. 1.8. A cracked ceramic capacitor [36]

In the meanwhile, the HV electrolytic capacitor is not promising in electrical systems of automotive applications considering its short lifetime and safety issues [34]. One issue is the electrolyte leakage, as shown in Fig. 1.9 [37]. Electrolyte leakage poses several potential safety hazards: human contact with electrolyte and electrolyte residue, and short-circuiting of adjacent electronic systems, which could become a disaster for both the automakers and users.

Fig. 1.9. Electrolyte leakage issue of electrolytic capacitor [37].

The merits of film capacitor are low ESR and ESL, no liquid electrolyte, and strong overvoltage capability [38]. In addition, film capacitor also has self-healing capability [34]. Therefore, film capacitors are preferred to be installed on the HV dc-link in electrified vehicles rather than electrolytic capacitors [39]. However, compared to electrolytic capacitors, the capacitance to volume ratio of film capacitors is much lower. A size comparison between a 500 μF/450 V film capacitor and a 330 μF/450 V electrolytic capacitor can be seen in Fig. 1.10, regardless of the ripple current rating. By

adding the bulk film capacitor, it results in larger converter volume and lower power density. This issue becomes more stringent for the on-board power electronics system, which is preferred to be light weight, small size, and low cost [5, 17].

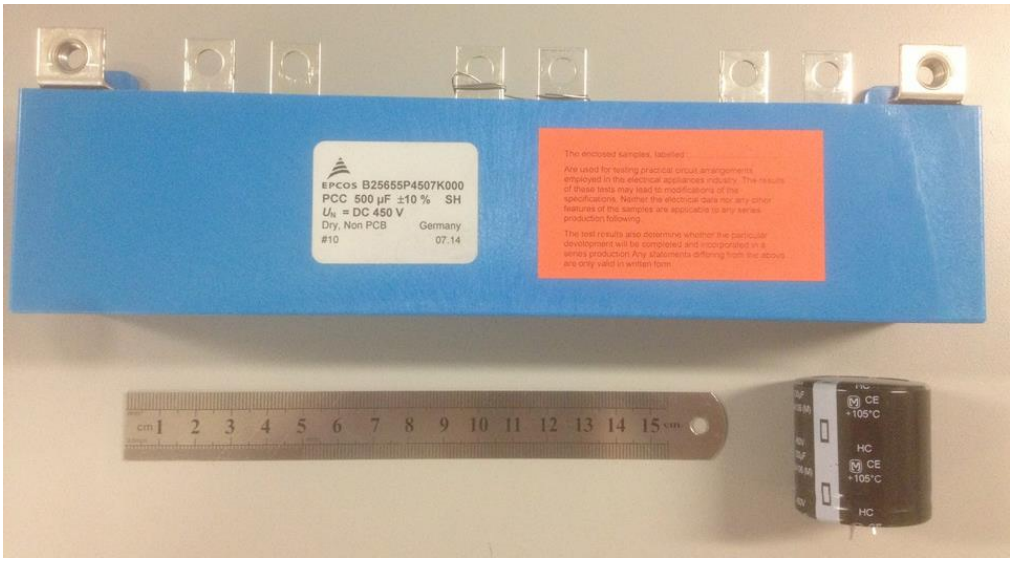


Fig. 1.10. A comparison between 500 µF/450 V film capacitor and a 330 µF/450 V electrolytic capacitor.

In order to improve the power density and reliability of power electronic system, researchers have made large efforts to reduce the dc-link capacitance in the power electronics field [35, 39-56].

1.3.1 Overview of capacitor-less methods in traction inverters

For the traction inverters, several methods have been proposed as shown in Fig. 1.11. In [39], an interleaving control scheme is applied to the dual traction inverters so that the required dc-link capacitance can be reduced. The analytical results show that if

both of the electric machines operate in the same modes, the interleaving angle should be set to 90°; if both electric machines operate in different modes, the interleaving angle is set to 0°.

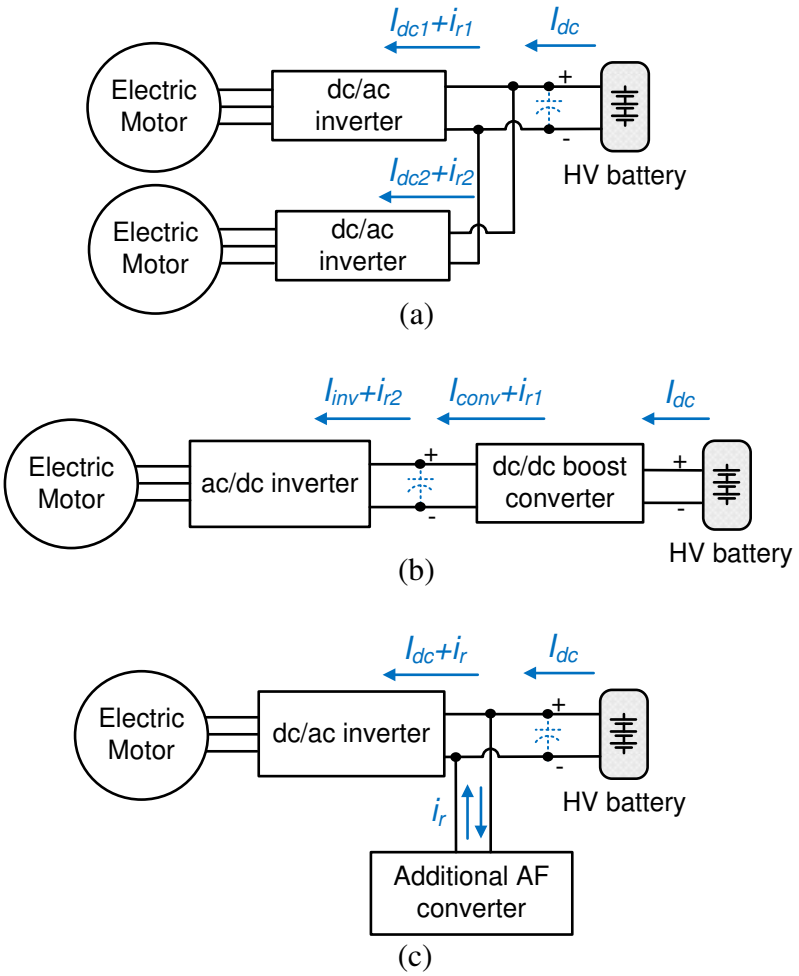


Fig. 1.11. Conventional capacitor-less methods for traction inverter in vehicle applications. (a) Interleaving dual inverter method. (b) Synchronization between inverter and boost converter. (c). Additional AF method.

In [43], the authors propose a new carrier modulation method so that the dc-link ripple reduction is achieved by synchronizing between the traction inverter and its boost converter. However, under some scenarios, the vehicle driving condition could be so complicated that it is not easy to synchronize both traction inverters all the time. Any mismatch could leads to an unexpected high current ripple, which could damage the dc-link capacitor bank. In [35, 51], an additional active filter (AF) is applied in parallel to the traction inverter's dc-link to reduce its capacitance. However, additional power switches and inductor are required, which increase the system complexity.

1.3.2 Overview of capacitor-less methods in HV battery chargers

For the single-phase HV battery chargers, several methods have been proposed and they are summarized in Fig. 1.12.

One way to eliminate the capacitor bank is to add an AF as shown in Fig. 1.12 (a) [40, 44, 45, 48, 52, 56]. With this method, the dc-link capacitor bank can be reduced significantly. However, more components need to be added into the system. In [41, 42, 46], authors propose sinusoidal charging methods for the HV battery as shown in Fig. 1.12 (b). The HV battery charging current contains the dc component I_{dc} and also the low-frequency second-order harmonic current i_r, so that the bulk film capacitor bank can be reduced. However, it might be better to have a constant dc charging current to the Lithium-ion battery. A deep study needs to be conducted further on the impact of the low-frequency sinusoidal current to the Lithium-ion battery, as electrolytes are inside the Lithium-ion battery, which tend to be flammable exacerbating the fire hazard [57].

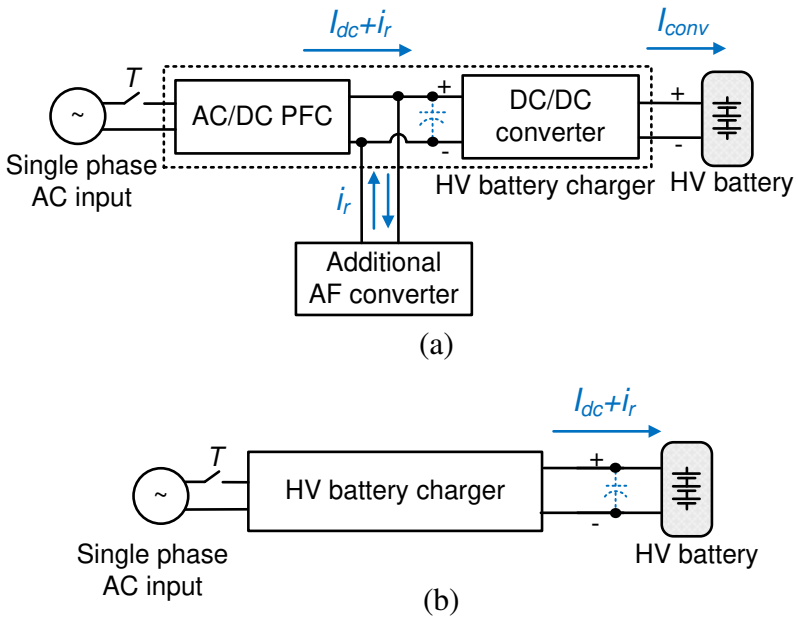


Fig. 1.12. Conventional capacitor-less methods for single-phase HV battery charger in vehicle applications. (a) Additional AF method. (b) Sinusoidal charging method.

1.4 MOTIVATION

AFs, based on topology and control scheme, can compensate current harmonics, voltage harmonics, reactive power, load imbalance, neutral current, voltage imbalance, voltage regulation and voltage flicker [50]. The AF can be applied on both dc-links of traction inverter and HV battery charger. The fundamental idea is to divert the ripple power to another specific energy storage component with relatively small size and long lifetime by an extra active switching circuit [55]. For example, a bidirectional buck AF is applied to the single-phase rectifier for the aerospace application in [40]. The main idea is to apply an active energy storage capacitor with much greater swing and thus reduce the

required capacitance on the main HV dc-link. With these additional AF circuits, the dc-link capacitor volume can be reduced significantly.

However, extra power switches, active energy storage components, corresponding heat sinks and gate drivers are required to form the AF circuit. With more components adding into the system, the system complexity is increased and its reliability is decreased. In addition, the cost is not reduced as much as the capacitance is. For instance, by applying an AF on a 6.6 kW HV battery charger's dc-link, a cost comparison from the ripple energy storage aspect can be made as shown in Fig. 1.13. With the extra active filter converter method, the required HV dc-link capacitance can reduce to 9% of the capacitance of traditional capacitor method. However, the cost of the conventional active filter can only decrease to 70.7% of the cost of traditional capacitor method.

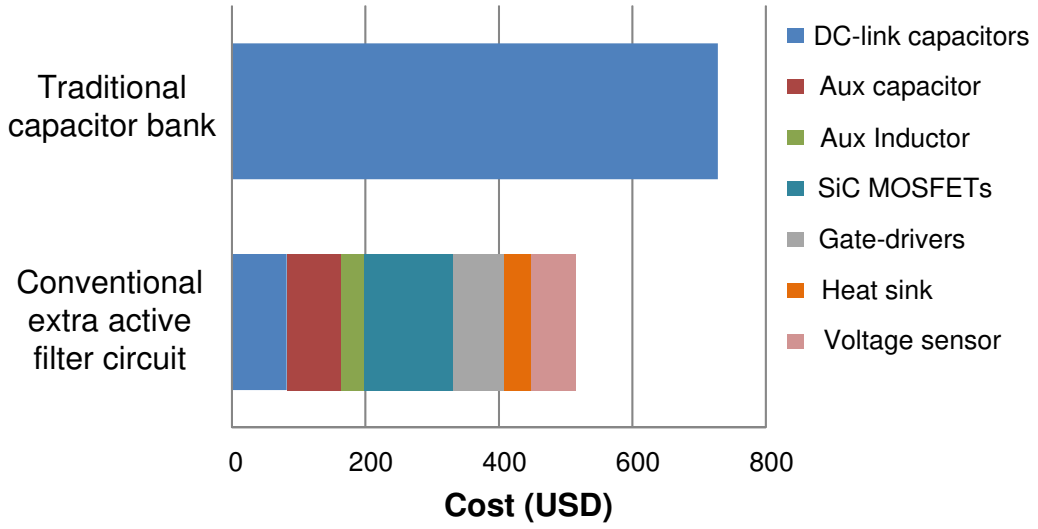


Fig. 1.13. A main components cost comparison of ripple energy storage for 6.6 kW HV battery charger.

Therefore, the challenge and motivation of the power electronic system in the vehicle applications is to increase the power density and reliability, and reduce the cost with the minimized dc-link capacitors and power switch devices. Hence, the objective of this thesis is to integrate the AF into the APM to form an integrated active filter auxiliary power module (AFAPM) converter and, thus, reduce the capacitance on the dc-links of other power electronic converters without extra power switches. By doing so, the required number of power switch devices and capacitors is reduced, which reduce the cost and improve the power density and reliability of the power electronic system. This yields a smaller, lighter, more reliable and more affordable solution for the electrified vehicles.

1.5 CONTRIBUTIONS

The author has contributed to a number of original developments in modular APM converter topologies and integrated AFAPM converter topologies. These contributions are briefly described below.

(1) The introduction of APM and its requirements; published in [25].

(2) A topological evaluation of isolated dc/dc converters for APM in electrified vehicle applications; published in [58].

(3) An evaluation of integrated AFAPM in electrified vehicle applications; published in [59].

(4) The different AFAPM-based dual-voltage charging systems and an integrated AFAPM for electrified vehicles with single-phase onboard chargers; published in [60-61].

(5) A dual active bridge-based full-integrated AFAPM for electrified vehicles with single-phase onboard chargers; published in [62].

(6) A primary full-integrated AFAPM for electrified vehicles with single-phase onboard chargers; accepted in [63].

1.6 OUTLINE OF THIS THESIS

This thesis mainly focuses on the invention of the integrated AFAPMs in electrified vehicle applications. The thesis consists of six chapters. They are organized as following.

Chapter 1 introduces the background information and literature reviews of architectures of electrified vehicles and the requirements of their power electronic converters. The LV nonpropulsion loads and APMs are introduced. The overview of capacitor-less methods in the vehicle applications are introduced briefly. Then the challenge and motivation of the thesis is presented.

Chapter 2 presents a topological evaluation of isolated dc/dc converter for APMs in the electrified vehicle applications. Different basic topologies for the APM are reviewed. By applying the full bridge current doubler as the base topology, different multiple topology configurations and their control schemes are reviewed and discussed. A multiple topology selection is presented in terms of switch efficiency and cost. If the desired APM is scalable and efficiency-oriented, the full bridge current doubler with input-series-output-parallel configuration presents better performance based on the switch

efficiency and cost analysis.

Chapter 3 starts with an evaluation of integrated AFAPMs in electrified vehicle applications. The AF requirements in traction inverters and HV battery chargers are reviewed and analyzed. Chapter 3 then proposes the operating principle of the dual-voltage charging system and possible system structures. With the proposed method, the required capacitance in the HV battery charger can be reduced significantly.

Chapter 4 then focus on the planar transformer design for APM applications. The selections of turn ratio and number of turn for different dc/dc converter topologies are illustrated. Different methodologies to calculate the core loss are presented. The calculated core losses are then compared with the simulation results from ANSYS/Maxwell. Under different layer arrangements, the current sharing and copper loss are simulated and compared. The leakage inductance calculation is presented. Finally, the implementation and experimental results of the planar transformer are presented.

Chapter 5 presents three different integrated AFAPM converters. The first proposed converter integrates the AF on the primary stage. A relay is needed to achieve the multi-functions. The converter topology, control and design considerations are presented. Simulation results are presented. A 1.2 kW converter prototype is built. Implementation results are provided to verify the effectiveness of the proposed converter. The second proposed converter is fully integrated. There is no hardware change on the proposed dual-active-bridge converter. The second-order harmonic energy is stored on

the secondary-stage output capacitor bank of the dual active bridge converter. The converter control and design considerations are presented. Simulation results are provided. The third proposed converter still integrates the AF on the primary stage. In addition, the relay is avoided. Only an active energy storage capacitor is needed to form the AF. The converter control and design considerations are provided. A 720 W converter prototype is built. Simulation results and implementation results are presented to confirm the effectiveness of the proposed converter.

Conclusions and future work are made in Chapter 6.

Chapter 2

TOPOLOGICAL EVALUATION OF AUXILIARY POWER MODULES IN ELECTRIFIED VEHICLE APPLICATIONS

2.1 INTRODUCTION

Topology selection is essential to the power efficiency, power density, and cost. For the APM application, the dc/dc converter must incorporate galvanic isolation to protect the LV electronic system from the potentially hazardous HV. This requirement restricts the available topologies to those containing a transformer. In the meanwhile, the traditional flyback, forward and push-pull converters are not suitable for this application due to their relatively large transformer size and high switch voltage stress [25]. Other than these three converters, many other dc/dc converter topologies with transformer are available and some of them are well suited for the APM application. This chapter presents a comparative evaluation of the suitable isolated dc-dc converters for the APM in electrified vehicle applications. The basic single-input-single-output (SISO) dc-dc converter topologies are reviewed. The full bridge current doubler is selected as the base topology and its operating principle is presented. Different multiple configurations and their control strategies are presented.

A 3 kW rated APM is targeted with 200-250 V input voltage and 12 V output voltage in this chapter. The MOSFET loss analysis is introduced. By applying full bridge current doubler as the base topology, the different multiple topology configurations are compared from a MOSFET switch efficiency drop and cost aspect. Results of the study show that the input-series-output-output-parallel (ISOP) topology configuration presents better performance for the APM application in terms of switch efficiency and cost.

2.2 APM base topology selection

2.2.1 Primary part topology selection

For high power conversion, full bridge (shown in Fig. 2.1 (a)) is usually applied as it is relatively simple and robust, and it meets the high power density and efficiency demands [64]. The switch voltage stress is equal to the input voltage, which leads to a flexible switch selection for the APM. In addition, at high frequency, the zero voltage switching (ZVS) technique can be implemented on the full bridge topology by employing the phase-shift control in order to reduce the switching losses [64-66].

Compared to the full bridge, the conventional half bridge (shown in Fig. 2.1 (b)) only needs two switches instead of four. However, these two switches are required to carry two times as much current as compared to the full bridge converter. In the meanwhile, the voltage stress for these two switches is still equal to the dc input voltage. Thus, it's clear that the switch requirements for the conventional half bridge are higher than full bridge. Therefore, conventional half bridge is usually not suitable for high power

applications due to the limitations in switch selection. On the other hands, in order to achieve ZVS operation for half bridge, asymmetric control (also called complementary control), needs to be applied [67]. This control strategy leads to uneven voltage and current stresses on the components.

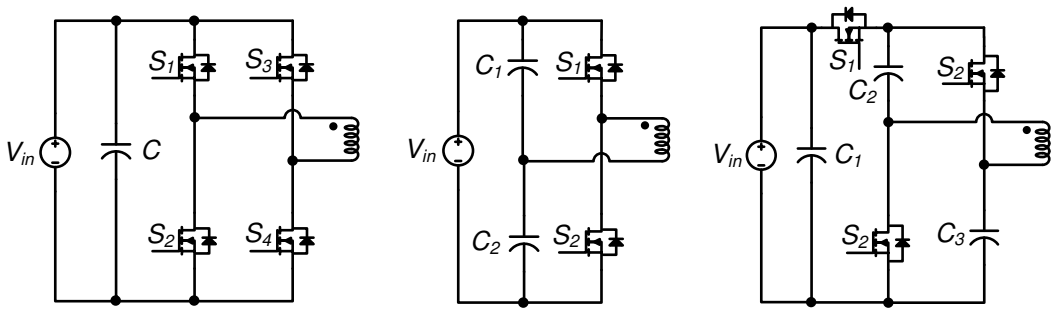


Fig. 2.1. Primary side topologies. (a) Full bridge. (b) Half bridge. (c) Quasi-switched-capacitor bridge.

Recently, Zhang *et al.* [68] developed an isolated quasi-switched-capacitor dc/dc converter, which obtains reduced number of switches and voltage stresses (Fig. 2.1 (c)). The primary side of the converter needs three switches instead of four in the full bridge. In the meanwhile, the voltage stress on HV-side switching devices is 2/3 V_{in} and that across the transformer is 1/3 V_{in}, which results in reduced transformer turns ratio as well [68]. However, this converter requires two capacitors to be charged and discharged by the primary current. By doing so, the reliability of this converter is decreased in comparison to full- and half- bridge. In order to make up for this deficiency, very high switching frequency is required to get lower ripple of those two capacitors.

2.2.2 Secondary part topology selection

For the isolated low output voltage topologies, the secondary side power losses are dominant because of the high current circulating through it. For the given specifications, an output voltage of 12 V associated to a full load power of 3 kW yields an output current of 250 A. This has a major effect on the conversion efficiency. Hence, it is critical to select the most suitable secondary side topology to maximize the conversion efficiency.

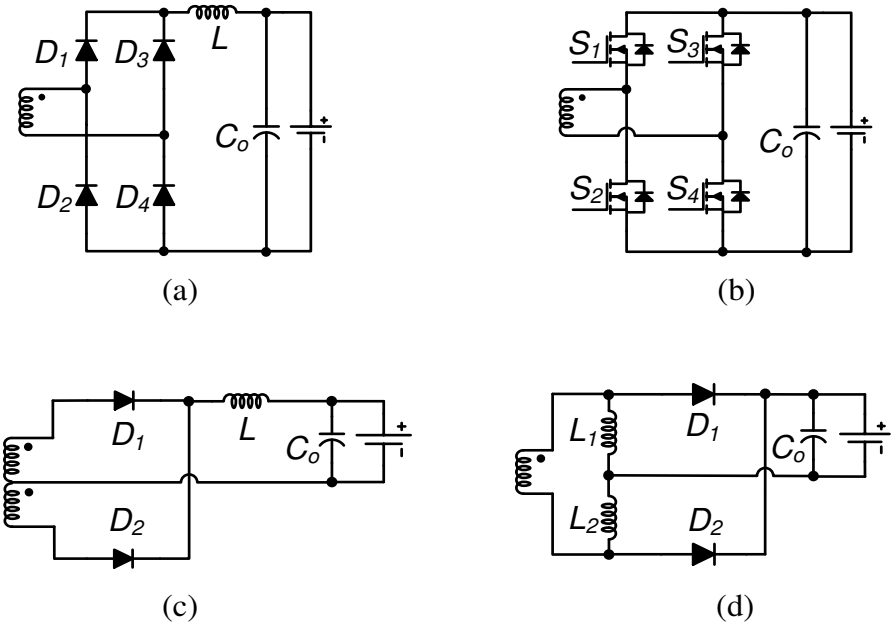


Fig. 2.2. Secondary side topologies. (a) Bridge rectifier. (b) DAB. (c) Center-tapped rectifier. (d) Current doubler rectifier.

The bridge rectifier requires four semiconductors, as shown in Fig. 2.2 (a). If the APM is required to operate in bidirectional mode, the most prominent bidirectional

converter topology is the dual active bridge (DAB) converter [69-78]. The DAB consists of a full bridge on the primary stage and another full bridge with MOSFETs on the secondary stage, as shown in Fig. 2.2 (b).

There are mainly two popular converter topologies for the secondary side of a unidirectional APM. These are center-tapped rectifier (shown in Fig. 2.2 (c)) and current doubler rectifier (shown in Fig. 2.2 (d)). Both of them are widely used in industrial products as well as in academia. Many studies have already been conducted to compare those two circuits in the literature and diverse conclusions have been made considering different aspects [79-80].

Current doubler has two switches and two inductors, and each inductor operates at the same switching frequency as the switches. On the other hand, center-tapped rectifier requires two switches with one inductor, which, inherently operates at two times the switching frequency. From the inductor aspect, the characteristics of current doubler is similar to dual-phase-dual-inductor topology (DPDI), whereas center tapped rectifier resembles to dual-phase-single-inductor (DPSI) topology. Both topologies have been investigated in [81] and it was concluded that the losses in the DPSI's inductor are lower than in DPDI.

However, the current doubler's dual inductors can be integrated on a single magnetic core [79, 82]. This dual-phase-coupled-inductor (DPCI) structure can reduce the inductor losses significantly, as well as the volume. In other words, with a proper design, the inductors of DPCI might be able to present a comparable performance as DPSI.

From the transformer aspect, the current doubler is more attractive than the center tapped rectifier. The biggest drawback of the center-tapped rectifier is that its transformer winding needs to be doubled compared to current doubler or bridge rectifier. This means that the center-tapped rectifier has poorer transformer utilization factor. Current doubler has a simpler transformer with only one secondary winding. Thus, it is possible to parallel more windings on the secondary to reduce the conduction losses for high current applications. Another advantage of current doubler is that it minimizes high current connections since the secondary winding and the inductors are connected in series [80]. Finally, it is interesting to see that the two inductors can be integrated in the transformer in order to simplify the converter packaging and may reduce the overall size of the magnetics as well [83-86].

Since APM is required to produce high current and low voltage at the output, the characteristics of the current doubler are more attractive and suitable for this application. Therefore, in this chapter, the full bridge with current doubler (FBCD) is applied as the base topology for the further analysis in APM design. The small signal analysis for the phase shifted full bridge can be found in [65]. In fact, to simplify the model, the FBCD can be represented by a two-phase buck converter with a transformer turn ratio [87].

2.2.3 Synchronous rectification

High current requirement on the secondary side usually results in high conduction losses. The conduction loss of diode rectifiers contributes significantly to the overall power loss due to the high voltage drop. A typical PN-junction power diode voltage drop

is 1.2 V and even Schottky Barrier Diode (SBD) still has 0.6 V voltage drop [88]. For a 12 V output APM application, this becomes a significant portion of the voltage drop (10%) and penalizes the efficiency. MOSFET presents lower conduction loss than diode. As a result, the concept of synchronous rectification (SR) came to reduce the conduction loss and maximize the conversion efficiency on the secondary side. In SR, rectifying diodes are replaced by synchronous MOSFETs. Corresponding topology for the current doubler circuit with a full bridge on the primary is shown in Fig. 2.3.

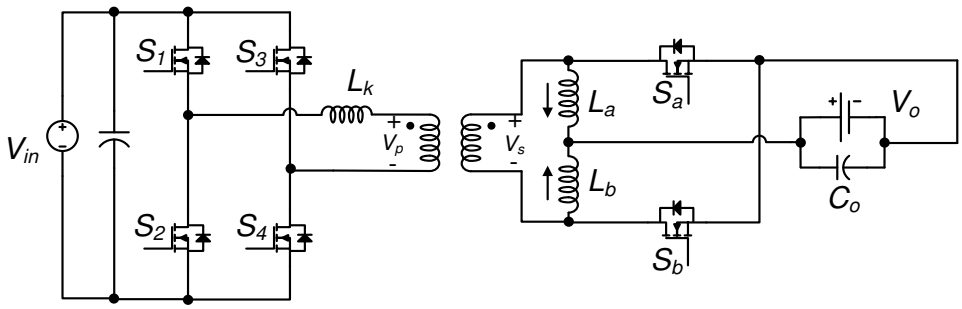


Fig. 2.3. Full bridge current doubler with SR.

The synchronous MOSFETs operate in the third quadrant. The body diode of the MOSFET conducts prior to the turn on of the switch. In other words, conduction loss of the body diode is generated just before the synchronous MOSFET turns on. However, it can be turned on in ZVS, which results in negligible switching loss at turn-on. At the turn-off, the MOSFET stops conducting prior to the body diode, which means that the synchronous rectifier still has the reverse recovery losses from its body diode [89].

If the voltage stress across the semiconductor is relatively high, MOSFETs with higher voltage rating need to be used. MOSFETs with higher voltage rating have larger on-state resistance, which might reduce the system efficiency. In this case, a Schottky Diode based configuration might provide a comparable efficiency in the secondary side with a lower cost as compared to SR MOSFET based configuration.

Typically, there are two different techniques to control the SR: External-driven SR (EDSR) and self-driven SR (SDSR) [90-91]. As shown in Figure 2.4 (a), in the EDSR technique, the control signals are generated by an external controller which guarantees the appropriate timing. By doing so, the switches can be turned-on during the whole rectification period, and the efficiency can be maximized [92]. However, circuit to generate the gate pulses and drivers to charge the gate capacitance of the MOSFETs are required.

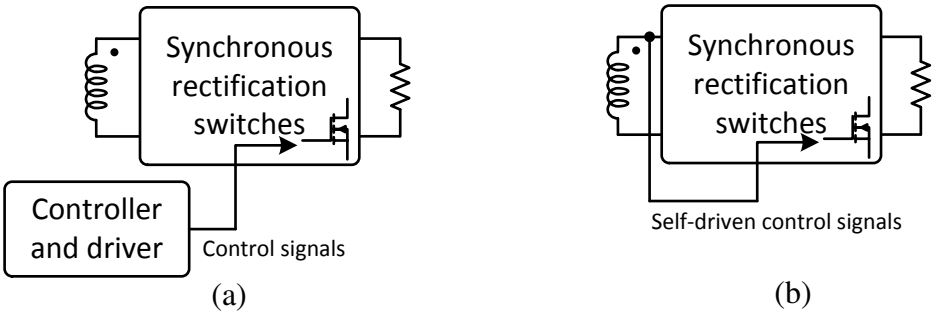


Fig. 2.4. SR control techniques. (a) EDSR. (b) SDSR.

Unlike the EDSR, the control signals as well as the energy to drive the SDSR switches are obtained from the secondary side of the transformer and no driver is needed

[90], as shown in Figure 2.4 (b). As a result, a simple, low-cost rectification control can be implemented. However, there are mainly two drawbacks for SDSR. The first one is the voltage with which the MOSFETs are driven is variable, and it depends on the input voltage. Secondly, not too many topologies are suitable for SDSR. The most suitable topologies for using SDSR are the ones that drive the transformer asymmetrically with no dead time.

In this thesis, the EDSR is applied. The drive signals of current doubler S_a and S_b are derived from drive signals of the primary full bridge S_1 to S_4. The drive logic diagram is shown in Fig. 2.5.

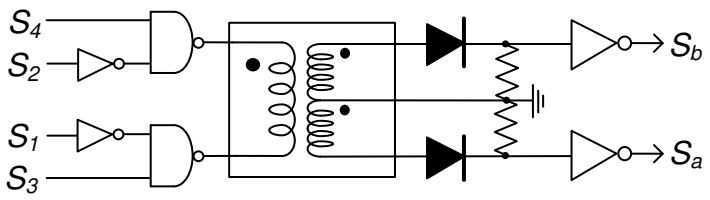


Fig. 2.5. Current doubler drive logic diagram.

2.3 MULTIPLE INPUT/OUTPUT TOPOLOGY CONFIGURATIONS

From the converter modularity aspect, the selected base topology can be categorized as SISO. The general SISO configuration is shown in Fig. 2.6. In order to further reduce the thermal and electrical stresses and, thus, to improve the efficiency, a high power converter can be constructed by connecting multiple converter modules in series or parallel at the output and input sides. Another advantage of multiple converter

modules is that it enables the expansion of power system capability and also offers scalability [93]. There are mainly two multiple input/output topology configurations suited for the APM: single-input-multiple-output (SIMO) and multiple-input-multiple-output (MIMO).

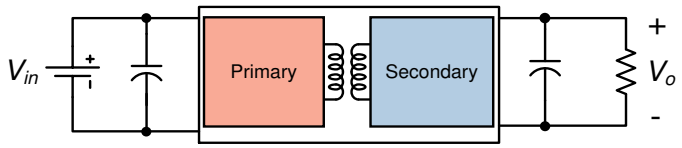


Fig. 2.6. SISO configuration.

2.3.1 SIMO configuration

SIMO configuration is appropriate for high output current application. This configuration has single converter on the primary side while two or more converters are connected in parallel or in series on the secondary side. For the APM, the parallel connection of multiple outputs would be preferred to share the high output current. The general single-input-output-parallel (SIOP) configuration is shown in Fig. 2.7.

The FBCD with SIOP configuration is shown in Fig. 2.8. It should be noted that if SR is applied, two different control schemes can be produced. One is to operate all the modules simultaneously and the other is to apply individual interleaving control [89, 94].

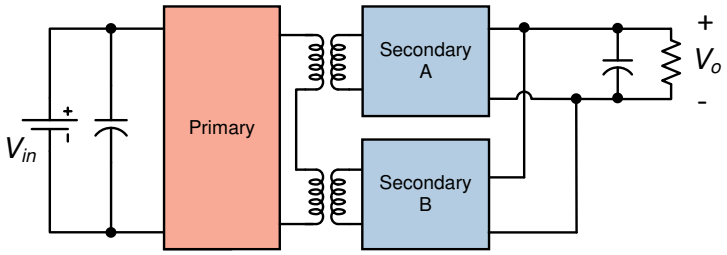


Fig. 2.7. SIOP configuration.

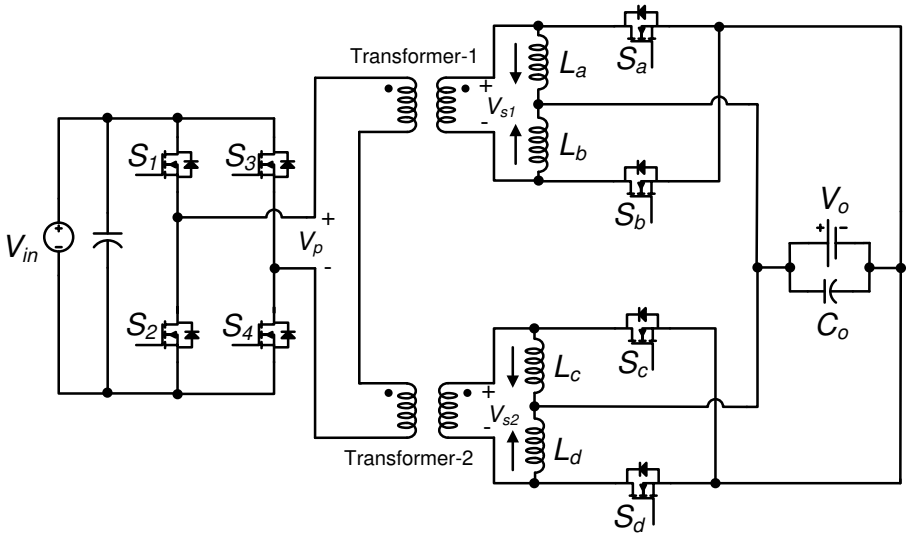


Fig. 2.8. FBCD with SIOP modular connection.

2.3.2 MIMO configuration

Typically, MIMO topology can be classified into four possible architectures in terms of the connection forms. These are input-parallel-output-parallel (IPOP), input-parallel-output-series (IPOS), input-series-output-parallel (ISOP), and input-series-output-series (ISOS), as shown in Fig. 2.9. Each configuration has its own specific application areas [93, 95].

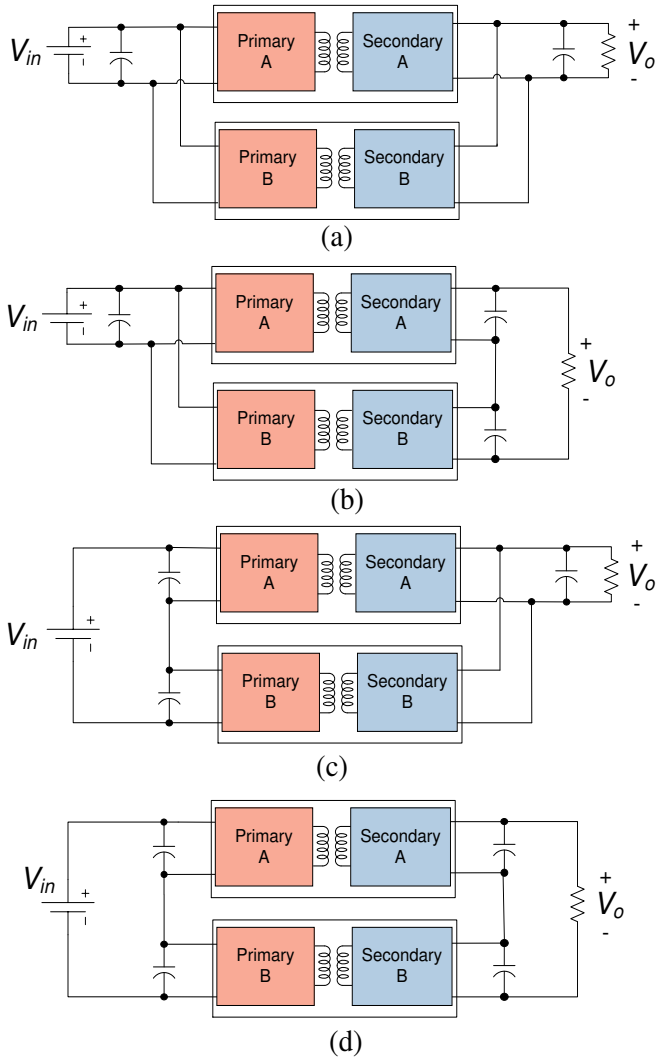


Fig. 2.9. Four possible connection architectures of MIMO configuration. (a) IPOP. (b) IPOS. (c) ISOP. (d) ISOS.

IPOP, as shown in Fig. 2.9 (a), is the most widely adopted MIMO configuration in the computer and telecommunication industries, where distributed power systems with paralleled modular converters delivering low output voltage and high output current are

utilized [93]. Since it shares the current on both input and output, the current ratings for both primary and secondary side are reduced to 1/*N*, where *N* is the number of modules.

IPOS configuration, as shown in Fig. 2.9 (b), is capable of sharing the input current and output voltage. For applications requiring high output voltages, such as X-ray equipment, photovoltaic systems, and electrostatic precipitators, IPOS becomes the desired choice [93].

ISOP configuration, as shown in Fig. 2.9 (c), can share the input voltage and output current. It can be used in applications where the input voltage is relatively high and the output voltage is relatively low, such as in high-speed train power systems, industrial drives, and undersea observatories [93, 96].

ISOS configuration, as shown in Fig. 2.9 (d), makes the input and output both in series, which results in the shared voltages on both input and output. Thus, it is well suited for applications where both the input voltage and output voltage are high [93, 97].

A noticeable characteristic of parallel-output configuration is interleaving technique. With proper phase-shifting among modules, interleaving is easy to implement on ISOP and IPOP configurations. By doing so, the output voltage ripple, and therefore the bulky capacitor size, can be significantly reduced.

For the APM application, since it obtains relatively high input voltage and high output current, it is more desirable to make the primary in series while the secondary in parallel. Hence, the ISOP configuration is more attractive and becomes one promising

solution as the final topology for the APM. The ISOP FBCD is shown as following Fig. 2.10.

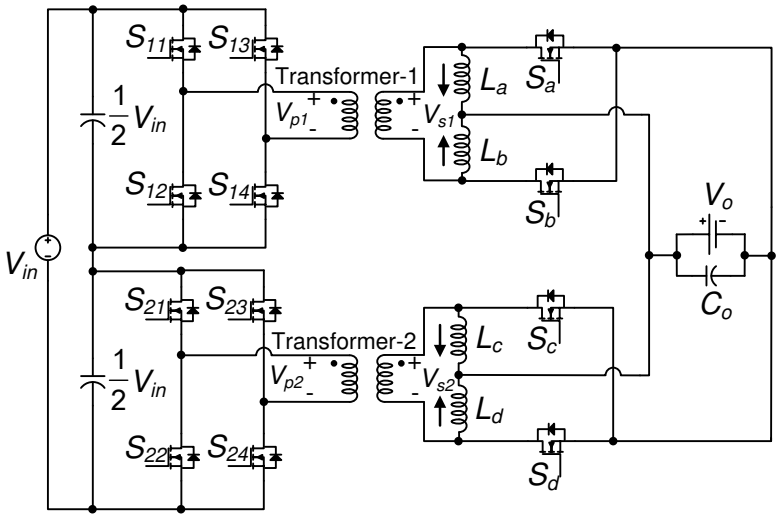


Fig. 2.10. FBCD with ISOP modular connection.

2.4 CONTROL SCHEMES FOR MULTIPLE INPUT/OUTPUT TOPOLOGIES

2.4.1 Basic SISO full bridge current doubler configuration

Fig. 2.11 and Fig. 2.12 show the equivalent circuit of each mode and key waveforms. Switch S_1 and S_2 are complimentary with 50% duty cycle minus a short dead time. Switch S_3 and S_4 are also switches complimentary with 50% duty cycle minus a dead time. A phase shift angle between the two bridges is used for output voltage regulation.

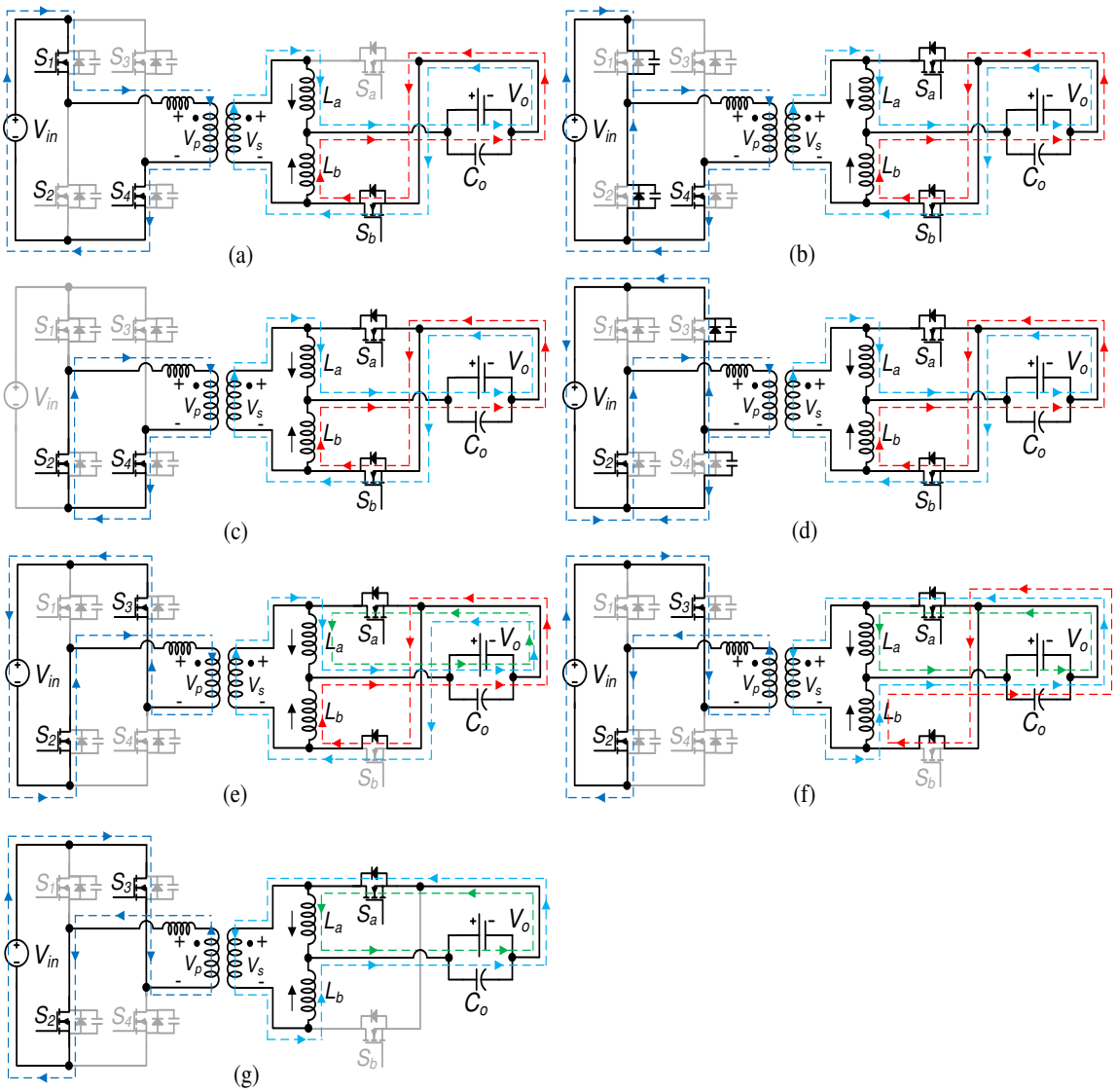


Fig. 2.11. Half cycle equivalent circuit diagrams of the SISO FBCD converter. (a) Mode 1: t_0 - t_1. (b) Mode 2: t_1 - t_2. (c) Mode 3: t_2 - t_3. (d) Mode 4: t_3 - t_4. (e) Mode 5: t_4 - t_5. (f) Mode 6: t_5 - t_6. (g) Mode 7: t_6 - t_7.

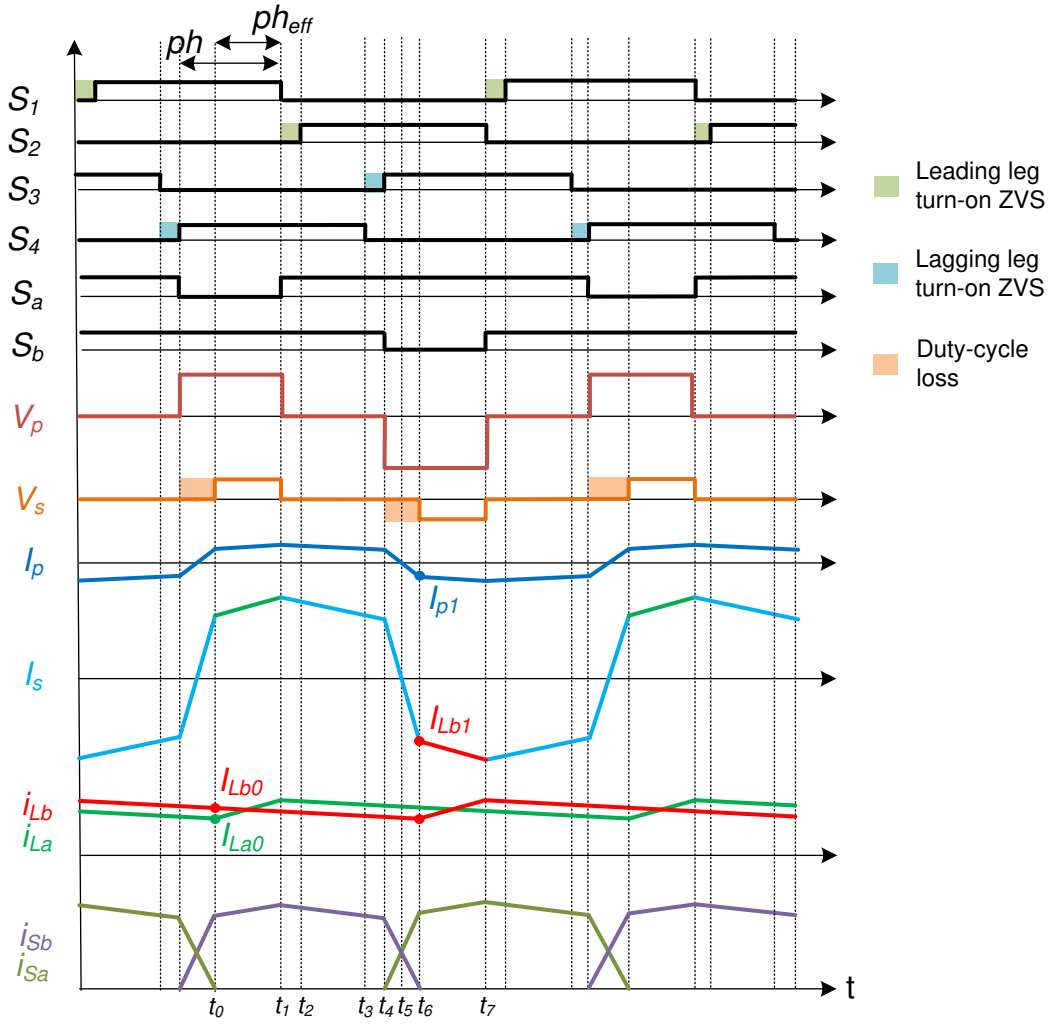


Fig. 2.12. SISO FBCD phase shift control scheme.

A. *Mode 1: (t_0 - t_1)*

In this mode, the switch S_1 and S_4 are turned on. The transformer primary voltage is V_p and secondary voltage is V_s,

$$V_s = \frac{N_s}{N_p} V_{in} \tag{2.1}$$

During that period, power is delivered from primary to the secondary. Hence, this time period is also the effective phase shift ph_{eff}. The inductor L_a is charging. The inductor L_b is discharging. The charging and discharging rates are,

$$I_{La} = I_{La0} + \frac{\frac{N_s}{N_p} V_{in} - V_o}{L_a} t \tag{2.2}$$

$$I_{Lb} = I_{Lb0} - \frac{V_o}{L_b} t \tag{2.3}$$

S_b carries both inductors current. At the end of t_1, the switch S_1 is turned off.

B. Mode 2: (t_1 - t_2)

Mode 2 is the dead time between the S_1 and S_2. As the S_1 is turned off, the primary current I_p starts to charge the output capacitance of S_1 and discharge the output capacitance of S_2. If C_2 can be fully discharged down to zero, its body diode D_2 will be conducted. As the body diode is conducted, there will be zero voltage across the switch S_2. Then S_2 can be turned on in ZVS. Therefore, there are certain requirements on the primary current and the leakage inductance, in order to provide sufficient inductive energy to fully charge and discharge these two capacitors (capacitive energy).

Due to the characteristics of phase shift modulation, the inductive energy for leading leg and lagging leg are different. The leading inductive energy includes the leakage inductor and secondary inductor,

$$E_{L\_leading} = \frac{1}{2} L_a \cdot I_{L1}^2 + \frac{1}{2} L_k \cdot I_{pri}^2 \tag{2.4}$$

where I_{pri} is the primary current at the starting time of ZVS. Due to the duty cycle loss, the lagging leg's two capacitors are charging and discharging by leakage inductor's energy only,

$$E_{L\_lagging} = \frac{1}{2} L_k \cdot I_{pri}^2 \tag{2.5}$$

The capacitive energy can be obtained as,

$$E_C = C_{oss} \cdot V_{in}^2 + \frac{1}{2} C_{TR} \cdot V_{in}^2 \tag{2.6}$$

Where C_{oss} is the MOSFET's equivalent energy related output capacitance and C_{TR} is the transformer parasitic capacitance.

Another requirement to ZVS is the deadtime. The required deadtime should be at least one fourth of the resonant period T_r. The resonant period T_r can be obtained as,

$$T_r = 2\pi\sqrt{L_k(2C_{oss} + C_{TR})} \tag{2.7}$$

Deadtime below $T_r/4$ will cause switching at partial ZVS. In the meanwhile, too long deadtime will cause extra body diode conduction losses and might cause losing ZVS

if the resonant circuit is highly damped. A ZVS circuit and its corresponding simulation results are shown in Fig. 2.13 and 2.14, respectively. G_{s1} is the gate drive signal.

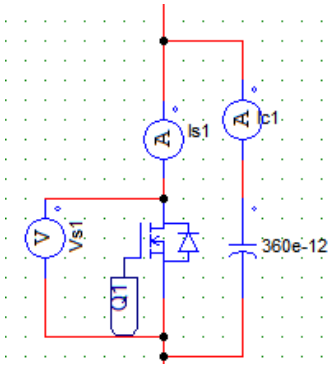


Fig. 2.13. ZVS electrical circuit.

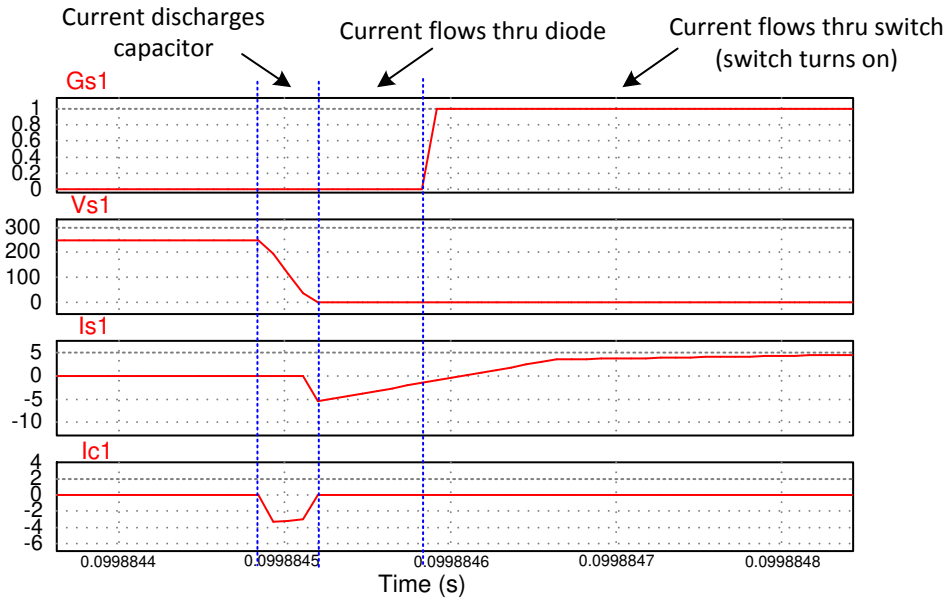


Fig. 2.14. ZVS simulation result.

C. Mode 3: (t_2 - t_3)

The ZVS is achieved during the deadtime. At the beginning of t_2, the switch S_2 is turned on in ZVS. Current I_p freewheels through S_2 and S_4. The transformer primary and secondary voltage are both zero. Secondary two inductors keep discharging. At the end of t_3, S_4 is turned off.

D. Mode 4: (t_3 - t_4)

As S_4 is turned off, the primary current charges the capacitor of S_4 and discharges the capacitor of S_3. Again, if the capacitor of S_3 can be fully discharged, the body diode D_3 will be conducted. The primary current will flow thru that body diode D_3 and this yields zero voltage across S_3.

E. Mode 5: (t_4 - t_5)

At the beginning of t_4, the switch S_3 is turned on in ZVS. At that time, as S_2 and S_3 are conducted, the transformer primary voltage is $-V_{in}$. However, due to the effect of the leakage inductor, the transformer current is lagging to its voltage. There is still a primary current with an unchanged flowing direction. Hence, the secondary stage remains freewheeling and the transformer secondary voltage will remain zero. The transformer secondary current keep decreasing until it reverses its direction.

F. Mode 6: (t_5 - t_6)

The transformer current reverses its direction and rise in the negative direction. Transformer secondary voltage will remain zero until the primary transformer current reaches the reflected output inductor current $I_{p1}*N_s/N_p$ at $t=t_6$.

G. Mode 7: (t_6 - t_7)

As the transformer primary current catches up the reflected output inductor current I_{Lb1}, the transformer secondary voltage rises, and thus the power is delivered to the output again. During this period, the secondary transformer current i_s is equal to the inductor current i_{Lb}. Then, the negative half cycle starts which is similar to the positive half cycle.

2.4.2 SIOP configuration

The general SIOP control scheme is the same as SISO's. If multiple outputs are connected in parallel, all the secondary parts just share the load current. The semiconductors in the secondary parts can be either diodes or switches. If the design is focused on the power density, Schottky diodes with small reverse recovery time can be applied. If the efficiency of the design is more of a concern, synchronous rectification should be applied using switches. The SIOP full bridge current doubler control scheme is shown in Fig. 2.15. Note that the duty cycle loss is neglected.

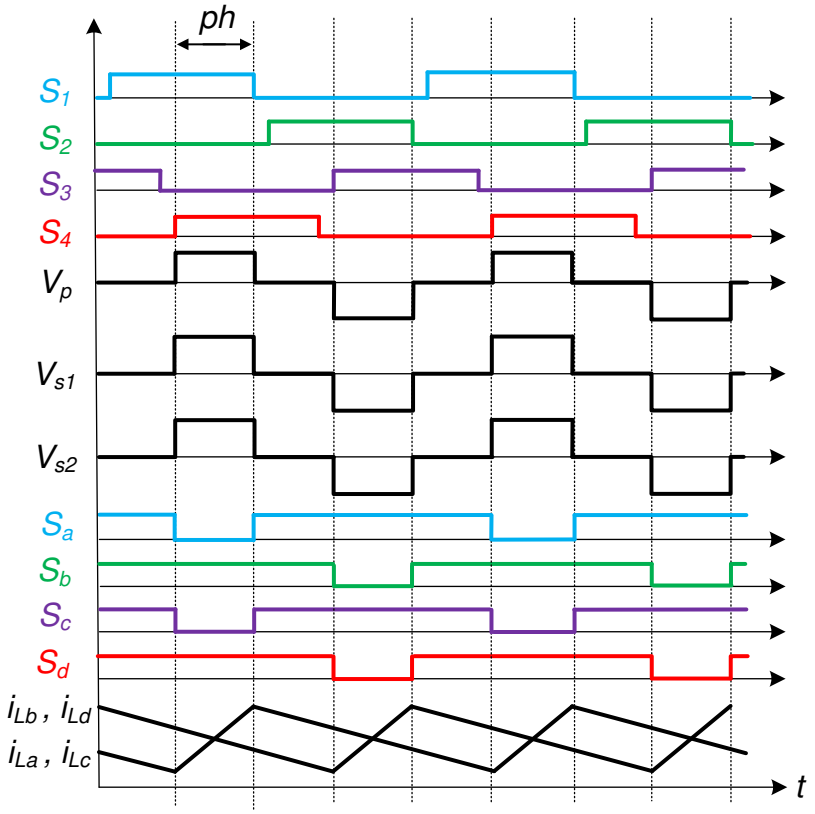


Fig. 2.15. SIOP FBCD general control scheme.

Interleaving control for SIOP has been proposed and developed in [89]. This interleaving control method is achieved by reducing the switching frequency of the phase-shifted paralleled secondary switches while only one primary side topology is applied, as shown in Fig. 2.16. Note that the duty cycle loss is neglected. In this thesis, this method is called as "quasi-interleaving". Because of the reduced switching frequency for the synchronous MOSFET, the body diode conduction losses and the reverse recovery related losses are lower. In addition, the interleaving effect results in the reduced filter size and improved transient response [94].

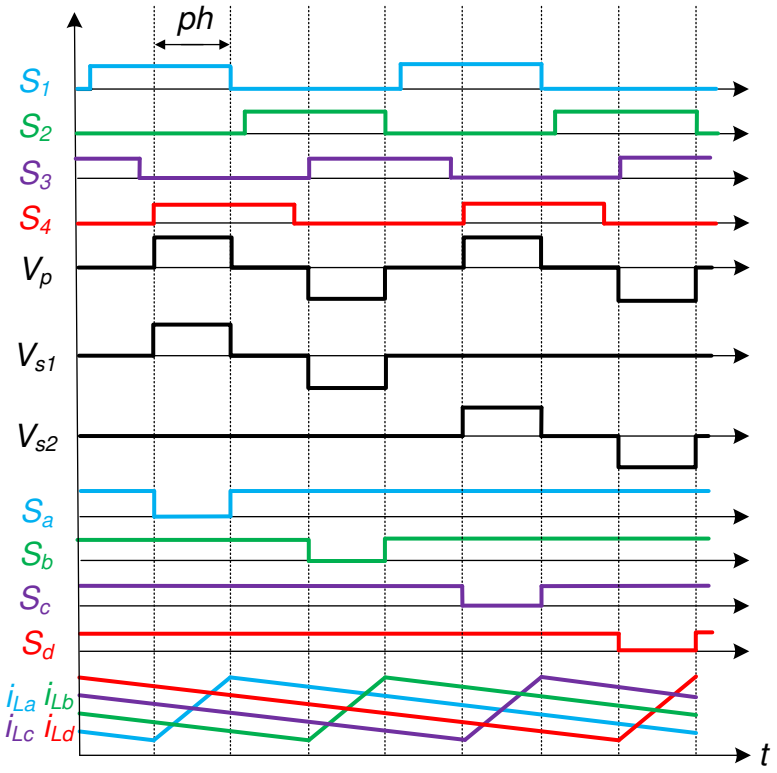


Fig. 2.16. SIOP FBCD quasi-interleaving control scheme.

However, there is one noticeable drawback for this control method. When transformer-1 is working, transformer-2 is short circuited. As a result, all the energy has to be transferred by transformer-1 only. Hence, all the voltage has to be applied to that single secondary module. In other words, all the voltage stress is on the transformer-1. Since the synchronous MOSFETs' voltage stress is equal to the secondary transformer winding voltage, this quasi-interleaving control method doubles the voltage stress on the transformer-1 in comparison of non-interleaved scheme where the two outputs are working in parallel. Similar phenomenon happens on the transformer-2 when it is operating. Therefore, the quasi-interleaving control requires the use of secondary switches

S_a, S_b, S_c, and S_d with higher voltage rating, which leads to a higher on-state resistance value. As a result, the converter efficiency decreases when using this control method.

2.4.3 ISOP configuration

The ISOP control scheme is shown in Fig. 2.17. Note that the duty cycle loss is neglected. The switching signals of two or more modules can be phase shifted with a suitable angle to achieve interleaving.

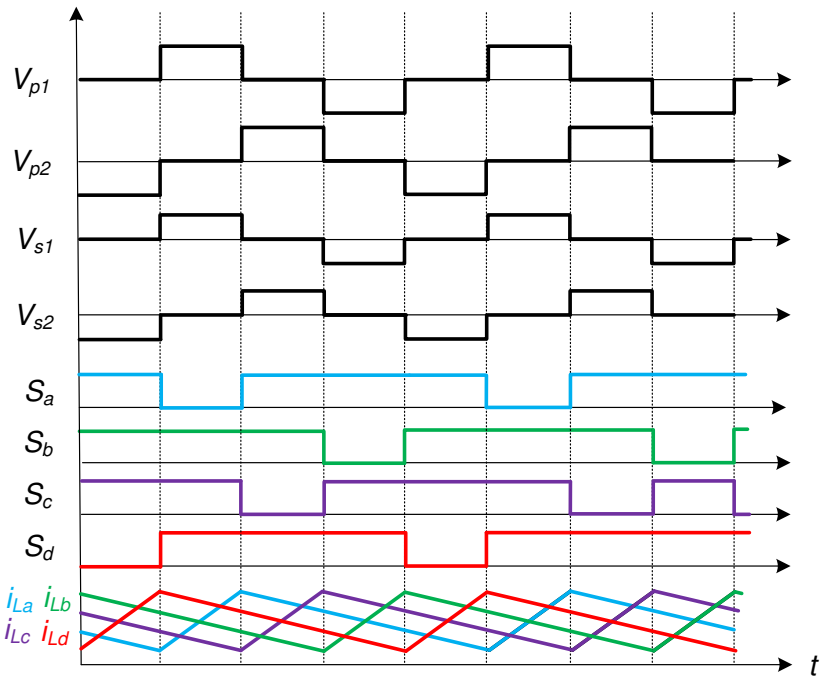


Fig. 2.17. ISOP FBCD interleaving control scheme.

The basic design objective of the ISOP converter is to make sure that the DC/DC converter modules share the input voltage and output current evenly. The common duty ratio control strategy relies on the inherent self-correcting characteristic of the ISOP

configuration when the duty ratio of all the modules is the same [98]. There are two loops in the common duty ratio control: the common output-voltage loop for all the modules and one inner current loop for the "master" converter. All the other "slave" converters have the same duty ratio as the "master" one. It is relatively simple for the ISOP system with well-matched modules. In [95], a dedicated input-voltage control loop is added to form a three-loop control method. In [99], an independent input-voltage sharing loop is developed. Operating along with the common output-voltage loop, the ISOP converters can be well regulated. The Table 2.1 lists the number of sensor required by applying each control strategy above to the ISOP FBCD.

Table 2.1. Sensor requirements for different control strategies of ISOP FBCD.

Control strategy	Voltage sensor quantity	Current sensor quantity
Three-loops control	2 at input 1 at output	2
Common-duty-ratio control	1 at output	1
Input-Voltage-Sharing control	2 at input 1 at output	0

2.5 MOSFET LOSS ANALYSIS AND SELECTION

In APM design, switches are the most expensive components. In the meanwhile, they are also the main cause of the efficiency drop [83]. As a result, the switches are relatively critical when selecting and designing the APM. The operating requirements of APM are shown in Table 2.2. Due to the different powertrain requirements, the APM requirements can be varied. In this chapter, the input voltage is set to 250V. Note that the input voltage can be rated higher which is according to the specific HV battery voltage range.

Table 2.2. APM operational requirements.

Specifications	Values	Specifications	Values
Input voltage (V)	250	Output current (A)	250
Output voltage (V)	12	Phase shift angle	0.25
Junction temperature (°C)	85	Inductor current ripple (peak-to-peak)	20%

The specific operating conditions for each configuration are shown in Table 2.3. In order to have an equitable comparison, the turns ratio is set based on assuming that all the modules operating at the same phase shift angle. In this section, the 0.25 phase shift angle is set for all the converter configurations.

In order to select the topologies among SISO, SIOP and ISOP in terms of the available switch cost and efficiency, efficiency drop and cost analysis based on the FBCD for each configuration are conducted. Here, the efficiency drop calculation for the SISO FBCD has been performed. The calculation of SIOP and ISOP are similar to SISO's so that they are not repeated. Note that all the MOSFET candidates in this chapter are all Si-based MOSFET.

Table 2.3. Specific operating condition for SISO, ISOP and SIOP.

	Transformer turn ratio	Switching frequency
SISO	125:24	200 kHz
SIOP (two phase simultaneous)	125:48	200 kHz
SIOP (quasi-interleaving)	125:48	200 kHz (primary)
		100 kHz (secondary)
ISOP	125:48	100 kHz

2.5.1 MOSFET Loss analysis

The circuit for the MOSFET with drive signal is shown in Fig. 2.18. The input capacitance C_{iss} are useful for the gate driving circuit. The input capacitance C_{iss} includes

C_{GD} and C_{GS}. The capacitance C_{GD} is also the reverse transfer capacitance C_{rss}. The output capacitance C_{oss} limits the *dv*/*dt* at switching transitions for the hard switching. For soft switching applications, this capacitor is important as it is part of the resonant tank. The output capacitance C_{oss} includes C_{GD} and C_{DS}. The driver circuit voltage changes from 0V to U_{Dr}. U_{GS} is the voltage across the capacitor C_{GS}.

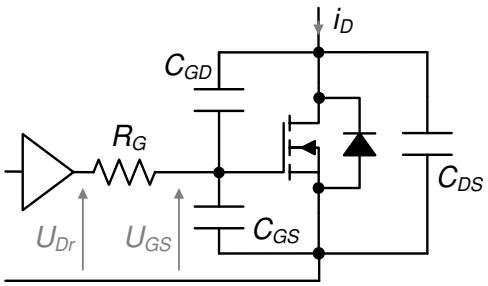


Fig. 2.18. Model of MOSFET with drive signal.

The power loss in the MOSFET can be mainly divided into three parts. They are the conduction loss P_c, switching loss P_{sw}, and gate drive loss P_{gd},

$$P = P_c + P_{sw} + P_{gd} \tag{2.8}$$

The switching loss includes three parts. They are the switch turn-on loss P_{onM}, switch turn-off loss P_{offM}, and the diode turn-on reverse-recovery loss P_{onD}. Hence, the overall switching loss can be expressed as the summation of all the above mentioned losses,

$$P_{sw} = P_{onM} + P_{offM} + P_{onD} \tag{2.9}$$

The conduction loss for the MOSFET can be obtained as,

$$P_c = R_{DSon} \cdot I_{Drms}^2 \tag{2.10}$$

Where I_{Drms} is the RMS value of the MOSFET on-state current.

Fig. 2.19 shows the switching transients of a MOSFET. For the turn-on transient, the driver voltage changes to U_{Dr}. Then the gate voltage rises to the threshold voltage $U_{GS(th)}$, with the time-constant defined by the gate resistor R_G and the input capacitance C_{iss}. The output of the MOSFET will not change until the gate voltage reaches the $U_{GS(th)}$. The gate current I_{G1} can be obtained by,

$$I_{G1} = \frac{U_{Dr} - 0}{R_G} \tag{2.11}$$

After the $U_{GS(th)}$ has been reached, the drain current I_D starts to rise. The time period from 0 to I_{Don} for I_D is the current rising-time t_{ri}. During this period, the diode is still conducting and V_{DS} is still U_{DD}. Once the MOSFET drain current reach I_{Don}, the diode is going to be turned off. In order to switch off the diode, the reverse-recovery current has to be absorbed by the MOSFET. The duration is t_{rr} and the peak current is I_{rr}, which can be calculated as,

$$I_{rr} = \frac{2 \cdot Q_{rr}}{t_{rr}} \tag{2.12}$$

where Q_{rr} is the reverse-recovery charge.

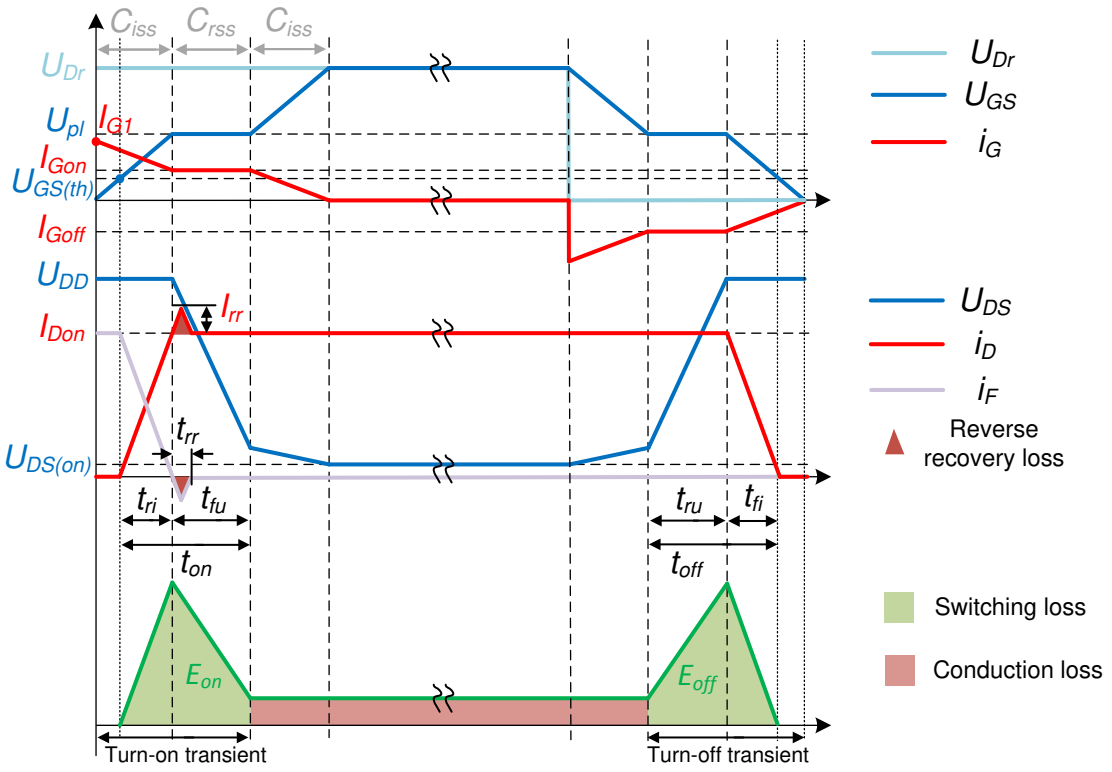


Fig. 2.19. Switching transients of MOSFET.

After the diode has been turned off, the V_{DS} is falling from U_{DD} to its on-state value $U_{DS(on)}$, which can be obtained as,

$$U_{DS(on)} = R_{DS(on)} \cdot I_{on} \tag{2.13}$$

The Miller effect takes place and U_{GS} is clamped at the plateau voltage U_{pl}. The gate current I_{Gon} during that period can be calculated as,

$$I_{Gon} = \frac{U_{Dr} - U_{pl}}{R_G} \tag{2.14}$$

The voltage fall-time t_{fu} is determined by the gate current I_{Gon} flowing through the C_{GD} or C_{rss}. C_{rss} is highly dependent on the voltage V_{DS}. The methods to better calculate the C_{rss} based on the datasheet can be found in [100-101]. The voltage fall-time t_{fu} can be obtained as,

$$t_{fu} = (U_{DD} - R_{DSon} \cdot I_{Don}) \cdot R_G \cdot \frac{C_{rss}}{(U_{Dr} - U_{pl})} \tag{2.15}$$

The switching-off process is similar to the switching-on in a reverse order. In addition, the reverse recovery will not happen during the switching-off period. Hence, the turn-on and turn-off switching loss P_{onM} and P_{offM} can be obtained as,

$$P_{onM} = f_s \cdot \int_0^{tri+tfu} u_{ds}(t) \cdot i_D(t)\, dt = f_{sw} \cdot \left(U_{DD} \cdot I_{Don} \cdot \frac{t_{ri} + t_{fu}}{2} + Q_{rr} \cdot U_{DD} \right) \tag{2.16}$$

$$P_{offM} = f_s \cdot \int_0^{tru+tfi} u_{ds}(t) \cdot i_D(t)\, dt = f_{sw} \cdot \left(U_{DD} \cdot I_{Don} \cdot \frac{t_{ru} + t_{fi}}{2} \right) \tag{2.17}$$

2.5.2 Input stage MOSFET selection

For the input stage, by assuming that ZVS is achieved in the converters, turn-on loss P_{onM} and output capacitance C_{oss} switching loss can all be neglected and considered equal to zero. Hence, the input stage switch loss consists of conduction loss P_c, turn off switching loss P_{offM} and gate drive loss P_{gd}. The voltage gain of the full bridge current doubler can be expressed as,

$$\frac{V_o}{V_{in}} = \frac{N_s}{N_p} \cdot ph - I_o \cdot (\frac{N_S}{N_P})^2 \cdot \frac{L_k}{V_{in}} \cdot f_s \tag{2.18}$$

The first term is the ideal phase shift angle and second term is the duty cycle loss. For the convenience of efficiency comparison performed here, the duty cycle loss effect is ignored. As a result, the voltage gain of FBCD can be expressed by,

$$\frac{V_o}{V_{in}} = \frac{N_s}{N_p} ph \tag{2.19}$$

where N_s/N_p is the turn ratio of the transformer, and ph is the phase shift angle as represented in Fig. 2.15. The transformer primary RMS current can be obtained by,

$$I_{rms\_pri} = \frac{I_o}{2} \cdot \frac{N_s}{N_p} \tag{2.20}$$

Since each switch operates at 50% duty cycle, the RMS current circulating through the MOSFETs of the primary side can be calculated by,

$$I_{S,rms\_pri} = \frac{I_o}{2} \cdot \frac{N_s}{N_p} \cdot \sqrt{\frac{1}{2}} \tag{2.21}$$

where I_o is the output current. The primary MOSFET conduction loss can be obtained as,

$$P_{c\_pri} = {I_{S,rms\_pri}}^2 \cdot R_{DSon\_pri(85℃)} \tag{2.22}$$

In order to calculate the turn-off loss, the inductor peak current value needs to be obtained. It can be calculated as,

$$\Delta I_{La} = \Delta I_{Lb} = \%Ripple \cdot \frac{I_o}{2} \tag{2.23}$$

where I_o is the output current. Since the inductor current peak-to-peak ripple requirement is 20%, the ΔI_L is 20 A for the considered operating point. Then, the inductor peak current can be obtained,

$$I_{L,pk} = \frac{I_o}{2} + \frac{\Delta I_{L1}}{2} \tag{2.24}$$

Another method to estimate the MOSFET switching off time can be obtained as [102],

$$t_{off} = Q_{gd} \cdot \frac{R_g}{V_{pl}} + Q_{gs} \cdot \frac{V_{pl} - V_{GS(th)}}{V_{pl}} \cdot \frac{2R_g}{V_{pl} + V_{GS(th)}} \tag{2.25}$$

where Q_{gd} is MOSFET gate-drain charge, Q_{gs} is MOSFET gate-source charge, R_g is MOSFET gate resistance, V_{pl} is MOSFET gate plateau voltage, $V_{GS(th)}$ is MOSFET gate threshold voltage.

Then, considering (2.24) and (2.25), the MOSFET turn-off loss can be expressed as,

$$P_{offM\_pri} = 0.5 \cdot I_{L,pk} \cdot \frac{N_s}{N_p} \cdot V_{in} \cdot t_{off} \cdot f_s \tag{2.26}$$

The gate drive loss can be obtained as [102],

$$P_{gd\_pri} = V_g \cdot Q_g \cdot f_s \tag{2.27}$$

where V_g is the gate driver voltage and Q_g is the MOSFET total gate charge.

Considering available MOSFETs on the market, possible candidates are identified and their losses are evaluated for each topology. Fig. 2.20 shows the loss distribution for Single-Input and Input-Series two configurations, respectively.

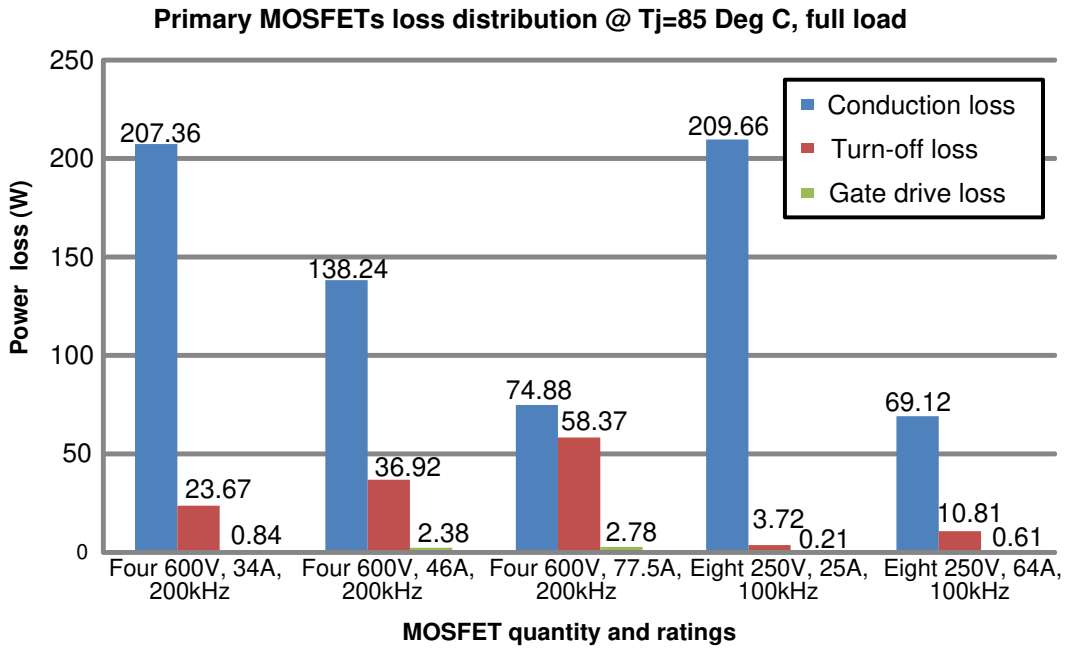


Fig. 2.20. Primary MOSFETs losses distribution.

The primary MOSFETs' efficiency drop and cost curves can be drawn in Fig. 2.21. By connecting two inputs in series, the voltage rating of corresponding switch can be reduced to half, as well as the switching frequency. These yields lower switching loss from the switches. This is observed in Fig. 2.21 where the switching loss is reduced significantly. However, the conduction loss of single input and two inputs in series have only slight difference by using the selected available switches.

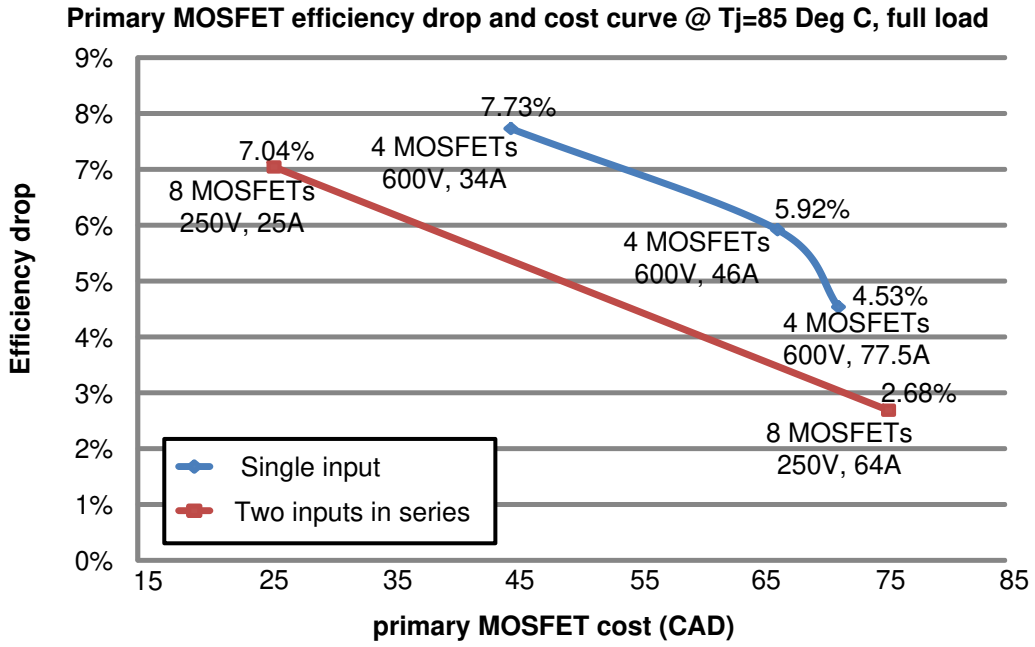


Fig. 2.21. Primary MOSFET efficiency drop and cost curve.

2.5.3 Output stage MOSFET selection

For the secondary part, the high current output makes conduction losses dominant. Due to the very short on-time of the body diode of about 50 ns to 100 ns, the reverse recovery charge loss can be neglected. Therefore, for the secondary switching loss, it only consists of gate drive loss and output capacitance switching loss. The voltage stress of SR MOSFET in a current doubler circuit is equal to the output voltage of the transformer is expressed as,

$$V_{stress\_SR} = V_{in} \cdot \frac{N_s}{N_p} \tag{2.28}$$

The RMS current circulating through the SR MOSFETs can be obtained by,

$$I_{rms\_SR} = I_o \cdot \sqrt{\frac{ph}{2} + \frac{1}{4}} \tag{2.29}$$

Then, the conduction loss in SR can be obtained by,

$$P_{C\_SR} = {I_{rms\_SR}}^2 \cdot R_{DSon\_SR(85℃)} \tag{2.30}$$

The output capacitance C_{oss} switching loss is [102],

$$P_{oss\_SR} = \frac{1}{2} \cdot Q_{oss} \cdot \frac{V_o}{ph} \cdot f_s \tag{2.31}$$

where Q_{oss} is MOSFET output capacitance charge. The SR gate drive loss is [102],

$$P_{gd\_SR} = V_g \cdot Q_g \cdot f_s \tag{2.32}$$

The secondary MOSFET/Schottky diode efficiency drop and cost curve can be drawn in Fig. 2.22. It can be observed that the SIOP four phase quasi-interleaving method presents lower efficiency. This is due to the higher voltage rating requirements for the secondary switches caused by that control scheme. Since the SIOP two phase simultaneously method and SISO obtains the same control scheme and switching frequency, all the loss distributions are identical. By paralleling more switches conduction loss can be further reduced with the penalty of higher cost. Since four phase interleaving method can reduce the switching frequency to 100 kHz, the turn-off loss of switches can be reduced. Thus, the overall loss is a little bit less than SISO. Moreover, it can be seen

that for high current application, SR obtains lower efficiency drop compared to Schottky diodes.

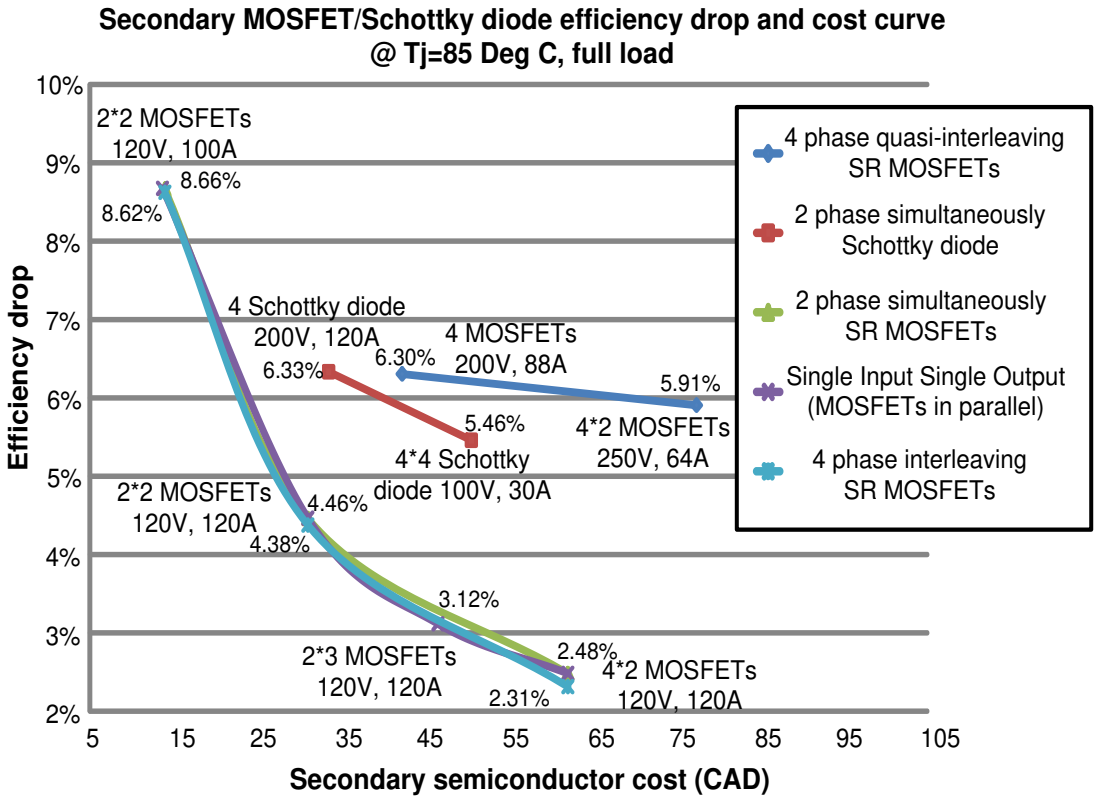


Fig. 2.22. Secondary MOSFETs/diodes efficiency drop and cost curve.

2.6 CONCLUSIONS

In this chapter, the basic topologies for the APM are reviewed. By applying the full bridge current doubler as the basic topology, different types of multiple topology configurations and their control schemes are reviewed and discussed. Among them, the SISO, SIOP and ISOP are more suited for the APM application. A multiple topology

selection is presented in terms of switch efficiency and cost. If the desired APM is scalable and efficiency-oriented, the ISOP full bridge current doubler presents better performance based on the switch efficiency and cost analysis.

Chapter 3

INTEGRATED ACTIVE FILTER AUXILIARY POWER MODULE-BASED SYSTEM STRUCTURES IN ELECTRIFIED VEHICLE APPLICATIONS

3.1 INTRODUCTION

With the development of electrified vehicles, there is now a strong demand for the development of advanced integrated power electronics system architectures for the next-generation automotive applications in order to achieve light weight, high power density, and high performance [103-109]. Multifunctional converters have been proposed to achieve LV battery charging when vehicle is in operation; and HV battery charging when the vehicle is connected to the grid [104-105]. By using these converters, several switches are shared during LV and HV battery charging periods, respectively. However, it might be a challenge for the circuit configuration proposed in [104] to reach high power rating of the 12 V LV battery charger, as the integrated front-end full bridge needs to carry both high-voltage from the grid and high-current to the 12 V battery. Insulated-gate bipolar transistors (IGBTs) have to be used in this case, which may become a major obstacle to

reach higher switching frequency. By adding a transformer in [105], the integrated switch power rating is no longer an issue. However, the proposed multifunctional converter is limited to the dual-voltage charging systems with a non-isolated two-stage HV battery charger. In addition, the charging current from the HV battery to the LV battery always flows thru an IGBT body diode, which may impact the efficiency.

In [108-109], a multiport converter has been proposed in an attempt to downsize complex power conversion systems in vehicle applications. The phase shift angle is used to control one converter and the duty cycle is applied to control another converter. Thus the switch quantity is reduced by four. However, those integrated switches need to carry the overall power for both power conversions, which leads to a higher current rating on the power switches. This might become an obstacle on the power switches and cooling system to reach higher power in the vehicle applications. In addition, there is a trade-off between the duty cycle and phase shift angle which might limit the performance for both conversions.

As mentioned in the chapter 1, two bulk capacitor banks exist in a typical electrified vehicle: on the dc-link of the traction inverter and in the on-board HV battery charger. In order to increase the power density and reliability of the power electronic system in the vehicle applications, a capacitor-less design is relatively crucial. AF can be a potential solution to reduce the required capacitance. Four typical conventional single-phase AF converters are shown in Fig. 3.1 [40, 44, 47, 48, 110]. They are voltage source inverter, current source inverter, bidirectional buck converter and bidirectional boost

converter. With these additional AF circuits, the required capacitance can be reduced significantly. However, by adding an extra AF circuit, additional power electronic components are needed and thus the system complexity is also increased.

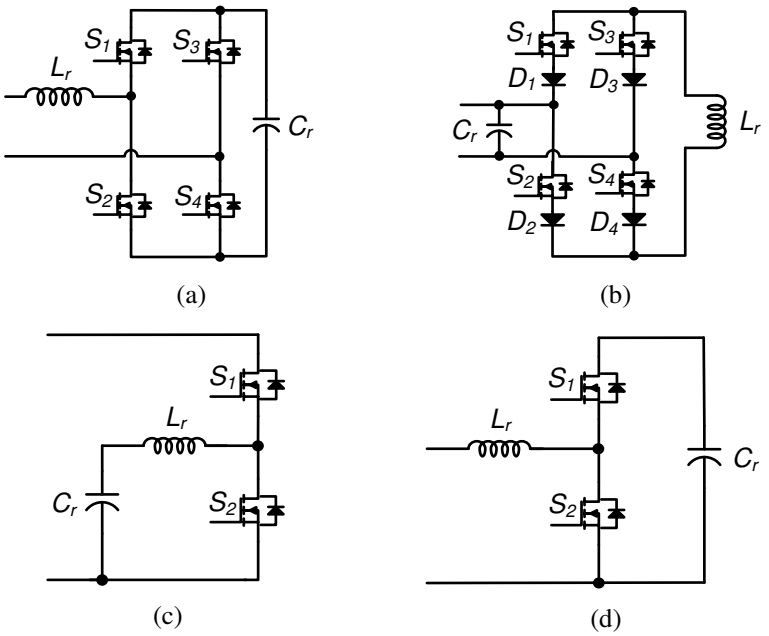


Fig. 3.1. Four typical conventional AFs. (a) Voltage source inverter. (b) Current source inverter. (c) Bidirectional buck converter. (d) Bidirectional boost converter.

In this chapter, the AF requirements for the traction inverter and the single-phase HV battery charger are discussed. The integrated AFAPM concept and different converter topologies are proposed. The operating principle of the proposed dual-voltage charging system and possible system structures are proposed.

3.2 ACTIVE FILTERS IN TRACTION INVERTERS

The traction drive requirements have been presented in Chapter 1. In traction inverters, the most common used modulation methods are sinusoidal pulse-width modulation (SPWM) and space vector pulse-width modulation (SVPWM) techniques. By applying these modulation methods, the output current of the inverter can be modulated in a desired sinusoidal shape for the traction motor. However, the dc-link ripple currents drawn from the battery are significant. As for the three-phase motor, the low-frequency three-phase harmonic current produced from the motor is not significant. The dominant harmonic currents on the dc-link are introduced by the switching behavior of the inverter, whose typical switching frequency is 5 to 15 kHz. A bulk film capacitor is needed on that dc-link to mitigate mainly these high-frequency high-current harmonics and to reduce the corresponding voltage ripple.

3.2.1 Harmonic current analysis

The switching function of each phase leg in the traction inverter can be expressed as,

$$S(t) = \begin{cases} 1, (\text{high side on}, \text{low side off}) \\ 0, (\text{high side off}, \text{low side on}) \end{cases} \tag{3.1}$$

In time domain, the overall instantaneous dc-link current of the inverter is the superposition of the switched current contributions from each phase leg, which can be obtained as,

$$i_{dc}(t) = i_a(t)S_a(t) + i_b(t)S_b(t) + i_c(t)S_c(t) \tag{3.2}$$

where a, b, and c represent each phase leg of the inverter and i_a, i_b, and i_c represent each phase current.

The double-integral Fourier series method [39, 111, 112] can be applied to represent the switching function, which is expressed as,

$$S(t) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty}[A_{0n}\cos(ny) + B_{0n}\sin(ny)] + \sum_{m=1}^{\infty}[A_{m0}\cos(mx) + B_{m0}\sin(mx)] + \sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}[A_{mn}\cos(mx+ny) + B_{mn}\sin(mx+ny)] \tag{3.3}$$

$$(x = \omega_c t + \theta_c, y = \omega_o t + \theta_o)$$

where ω_c and θ_c are angular frequency and initial phase angle of the carrier waveform, respectively; ω_o and θ_o are angular frequency and initial phase angle of the reference waveform, respectively. The switching function is represented as the summation of the dc component, fundamental harmonics related to the reference waveform, carrier harmonics related to the carrier waveform, and sideband harmonics related to both the reference and carrier waveforms. The coefficients of the switching function double-integral Fourier series are shown as [112],

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{x_{low}}^{x_{up}} S(t)\cdot e^{j(mx+ny)}dxdy \tag{3.4}$$

After the double-integral Fourier series analysis, the general expression of the inverter dc-link current can be derived in (3.5) and the coefficients of dc-link current harmonics $\bar{A}_{00}$, $\bar{A}_{mn}$, and $\bar{B}_{mn}$ are derived in (3.6) by using equation (3.4), where φ is the displacement angle and I_0 is the peak value of the phase current [111].

$$i_{dc}(t) = \frac{\bar{A}_{00}}{2} + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}[\bar{A}_{mn}\cos(mx+ny) + \bar{B}_{mn}\sin(mx+ny)] \quad (x = \omega_c t + \theta_c, y = \omega_o t + \theta_o) \tag{3.5}$$

$$\begin{cases} \bar{A}_{00} = \dfrac{3I_o}{2}(A_{01}\cos\varphi + B_{01}\sin\varphi) \\ \bar{A}_{mn} = \dfrac{I_o}{2}\left[\left(A_{m,n-1} + A_{m,n+1}\right)\cos\varphi + \left(B_{m,n-1} - B_{m,n+1}\right)\sin\varphi\right] \times \left(1 + 2\cos\dfrac{2\pi n}{3}\right) \\ \bar{B}_{mn} = \dfrac{I_o}{2}\left[\left(B_{m,n-1} + B_{m,n+1}\right)\cos\varphi - \left(A_{m,n-1} - A_{m,n+1}\right)\sin\varphi\right] \times \left(1 + 2\cos\dfrac{2\pi n}{3}\right) \end{cases} \tag{3.6}$$

The detailed integrated limits x_{up} and x_{low} are determined by the specific modulation schemes. If SVPWM is applied to the inverter, the following integral limits can be applied as shown in Table 3.1, where M is the modulation index, which is defined as the ratio of peak-to-peak phase voltage to the dc-link voltage [39].

A harmonic current spectrum on the dc-link with SVPWM method is shown in Fig. 3.2. The carrier frequency is 10 kHz. It is clear that the odd orders of carrier harmonics are equal to zero and the amplitudes of even orders of carrier harmonics decrease as the number of order increases. The dominant harmonics are the second-order and fourth-order harmonics, whose frequency are 20 kHz and 40 kHz, respectively.

Besides the SVPWM, the dc-link current harmonics analysis with other different modulation methods can be found in [39].

Table 3.1. Integral limits for coefficients of double-integral Fourier series with SVPWM.

y	x_{low}	x_{up}
$-\pi \le y \le -\frac{2}{3}\pi$	$-\frac{\pi}{2}(1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6}))$	$\frac{\pi}{2}(1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6}))$
$-\frac{2}{3}\pi \le y \le -\frac{1}{3}\pi$	$-\frac{\pi}{2}(1+\frac{3}{2}M\cos y)$	$\frac{\pi}{2}(1+\frac{3}{2}M\cos y)$
$-\frac{1}{3}\pi \le y \le 0$	$-\frac{\pi}{2}(1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6}))$	$\frac{\pi}{2}(1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6}))$
$0 \le y \le -\frac{1}{3}\pi$	$-\frac{\pi}{2}(1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6}))$	$\frac{\pi}{2}(1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6}))$
$\frac{1}{3}\pi \le y \le \frac{2}{3}\pi$	$-\frac{\pi}{2}(1+\frac{3}{2}M\cos y)$	$\frac{\pi}{2}(1+\frac{3}{2}M\cos y)$
$\frac{2}{3}\pi \le y \le \pi$	$-\frac{\pi}{2}(1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6}))$	$\frac{\pi}{2}(1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6}))$

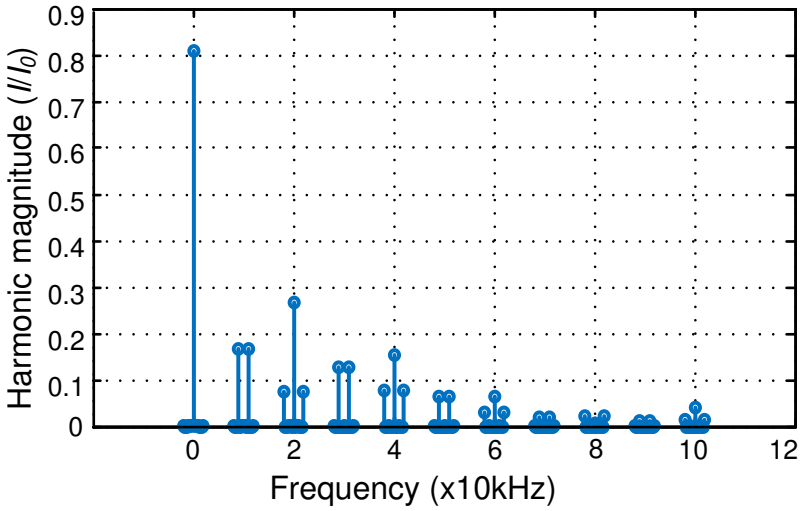


Fig. 3.2. Harmonic spectrum of dc-link current.

3.2.2 Active filter requirements

The conventional current source AF (shown in Fig. 3.1 (b)) can be applied in the traction drive system to reduce the dc-link capacitance. The hysteresis control is occupied on this AF converter [35, 51]. The switching operating diagram of the current source AF is shown in Fig. 3.3.

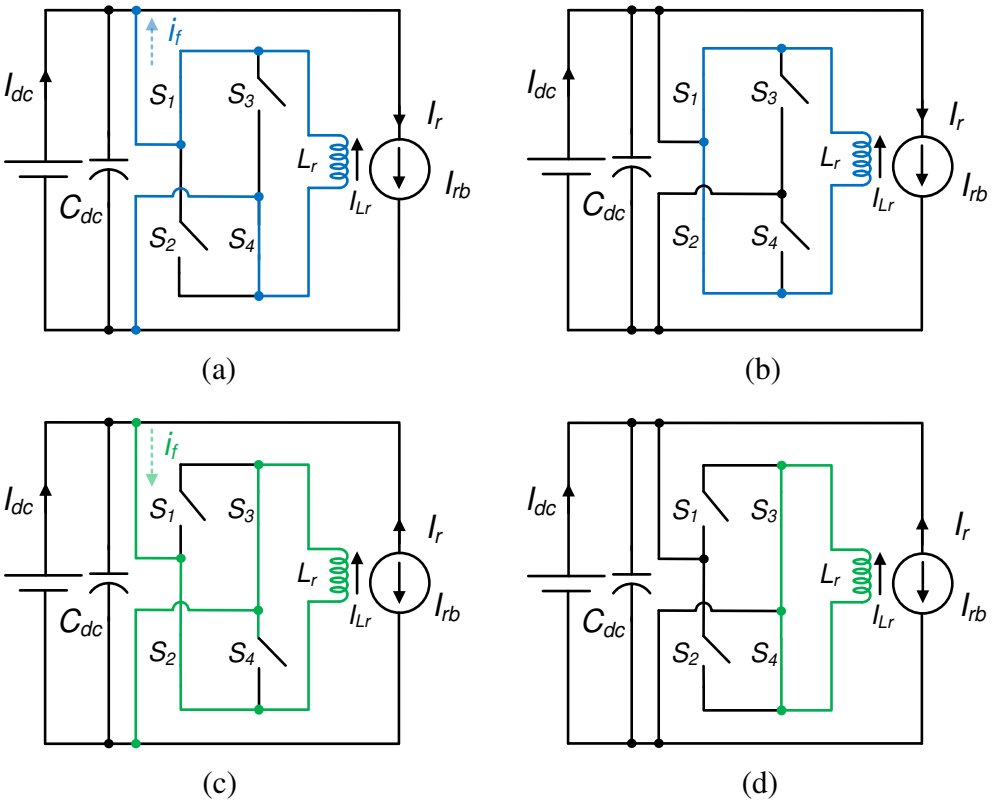


Fig. 3.3. Switching operating diagram of the current source AF inverter. (a) Current sourcing mode, capacitor voltage rising. (b) Freewheeling mode, capacitor voltage falling. (c) Current sinking mode, capacitor voltage falling. (d) Freewheeling mode, capacitor voltage rising.

Fig. 3.3 (a) shows that once the ripple current I_r flows into the load, switch S_1 and S_4 are turned on. The AF sources current. As the filter current i_f is larger than i_r, the capacitor is charged and hence its voltage V_{dc} increases. The capacitor voltage rising rate can be obtained as,

$$C_{dc}\frac{dv}{dt} = i_f - i_r \tag{3.7}$$

Once V_{dc} reaches its upper boundary, S_1 and S_2 are turned on. I_{Lr} is freewheeling as shown in Fig. 3.3 (b). The ripple current discharges the capacitor, which yields the capacitor voltage falling. The falling rate is,

$$C_{dc}\frac{dv}{dt} = -i_r \tag{3.8}$$

Once V_{dc} reaches its lower boundary, the freewheeling mode will be ended.

Once the ripple current i_r changes its direction, switch S_2 and S_3 are turned on. The AF sinks current, as shown in Fig. 3.3 (c). As the filter current i_f is larger than i_r, the capacitor is discharged and hence its voltage V_{dc} decreases. The capacitor voltage falling rate is,

$$C_{dc}\frac{dv}{dt} = -i_f + i_r \tag{3.9}$$

Once V_{dc} reaches its lower boundary, S_3 and S_4 are turned on. I_{Lr} is freewheeling as shown in Fig. 3.3 (d). The ripple current charges the capacitor, which yields the capacitor voltage rising. The rising rate is,

$$C_{dc}\frac{dv}{dt} = i_r \tag{3.10}$$

Once V_{dc} reaches its upper boundary, the freewheeling mode will be ended.

The detailed hysteresis control circuit is shown in Fig. 3.4. In the control circuit, the current i_{rb} needs to be measured so that the direction of ripple current i_r can be determined. V_{dc} needs to be measured so that the hysteresis bandwidth can be determined. In addition, in order to compensate the loss in the inductor and keep the inductor current to the desired value I_{Lr_ref}, I_{Lr} also needs to be controlled using a PI controller.

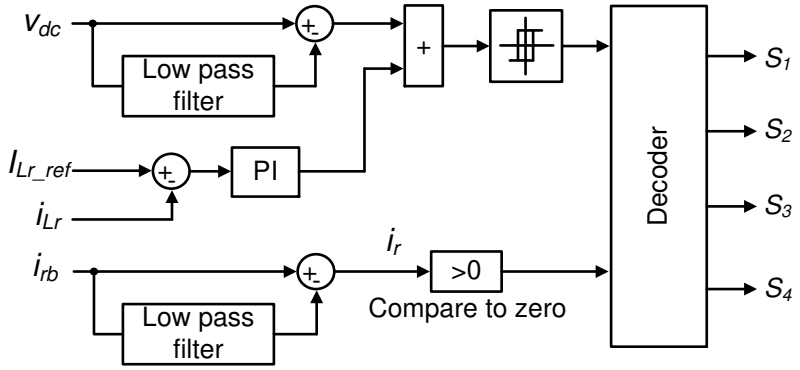


Fig. 3.4. Detailed hysteresis control circuit.

A 43 kW traction inverter is also simulated in this chapter as shown in Fig. 3.5. The traction drive system parameters are shown in Table 3.2.

Table 3.2. Parameters of the simulated traction drive system.

Parameter	Value	Parameter	Value
Output power P_o (kW)	43	Induction machine phase resistance R (Ω)	0.5
DC bus voltage V_{dc} (V)	330	Induction machine phase inductance L (mH)	0.77
Average DC current I_{dc} (A)	128	Three-phase inverter switching frequency f_s (kHz)	10
Modulation index M	0.8	Three-phase inverter modulation frequency f_m (Hz)	50

Before 0.006 s, the AF is turned off and all the harmonics are on the dc-link. After 0.006 s, the AF is turned on. The peak-to-peak voltage ripple of V_{dc} on the inverter's dc-link is limited to 1 V.

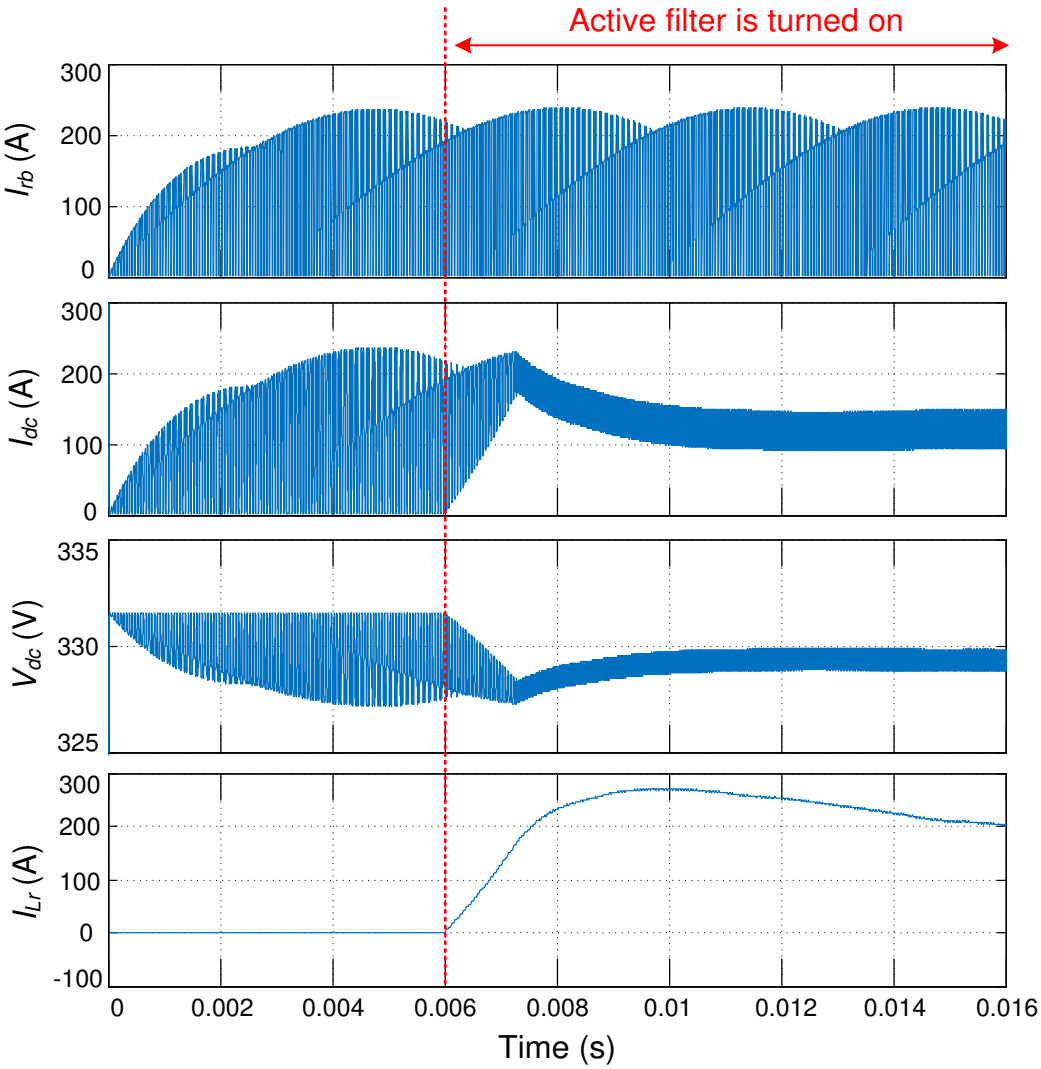


Fig. 3.5. Current source AF for traction inverter's harmonics simulation results.

In order to reduce the traction inverter's dc-link current harmonics and limit the peak-to-peak voltage ripple to 1 V, the first challenging component is the high-current high-inductance inductor. For proper operation of the current source inverter, it is necessary to maintain an inductor current I_{Lr}, whose magnitude is higher than the peak of the ripple current I_{ripple} [51, 110]. In this case, a 1 mH/200 A inductor L_r is needed to form

the AF. A 100 μF/600 V capacitor C_r is still needed on the dc bus to filter higher order harmonics. Since the hysteresis control is applied, the switching frequency is dependent on the bandwidth of the dc-link voltage ripple. With 1 V peak-to-peak voltage ripple requirement, the switching frequency would be around 300 kHz. At last, the Silicon Carbide (SiC) MOSFETs requirements are shown in the Fig. 3.6. They need to handle 400 V voltage stress with 100 A continuous current and operate at 300 kHz frequency. Furthermore, four 400 V/100 A SiC diodes are needed, as the current source AF requires reverse blocking. In addition, due to the relatively high switching frequency and high compensating current, a high-performance heat sink is required. At last, a current sensor with relatively high speed sampling frequency is required to track the instantaneous dc-link current. Therefore, the AF requirements to reduce the traction inverter's dc-link capacitance are relatively stringent.

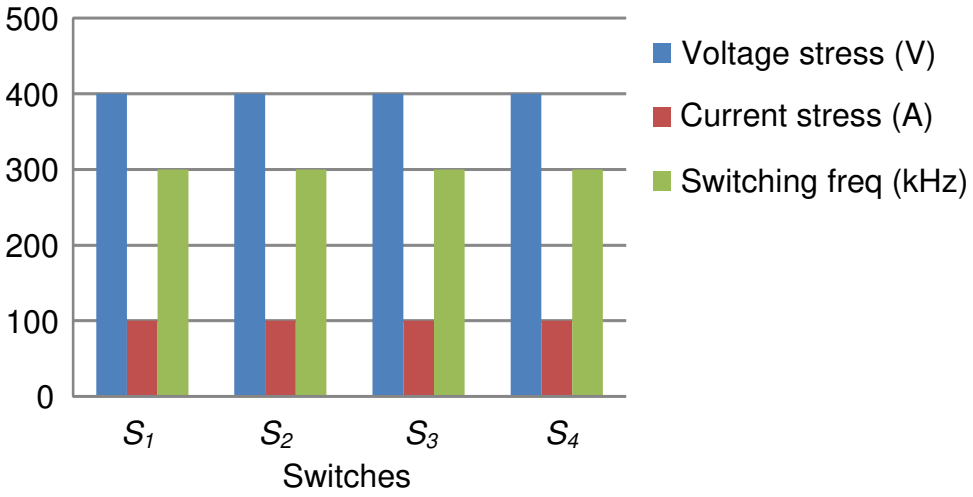


Fig. 3.6. Switch requirements of current source AF for 43kW traction inverter's dc-link.

3.3 ACTIVE FILTERS IN SINGLE-PHASE HV BATTERY CHARGERS

In a typical 50/60 Hz single-phase ac HV battery charger for the vehicle applications, as the input current is enforced to be varying sinusoidally in phase with the input voltage, the pulsating power at two times of the line frequency will be seen on the dc-link after the single-phase ac-dc PFC converter. Traditionally, large capacitance is required to balance out the instantaneous current difference between the pulsating input and the constant output current. In other words, the bulk capacitor is used to filter the low-frequency second-order harmonic current, whose frequency is 100/120 Hz.

By applying wide band-gap power (WBG) device, such as SiC, higher switching frequency and higher efficiency can be achieved [113-114]. Therefore, the size of the most passive components in the power electronic system can be shrinked. However, in this case, the corresponding required capacitance is dependent on the harmonic ripple power rather than the switching ripple. Hence, this becomes a major barrier in terms of power density.

3.3.1 Harmonic power analysis

For the single-phase HV battery charger input power, the input single-phase ac voltage and current are,

$$u_s(t) = U_s sin\omega t \tag{3.11}$$

$$i_s(t) = I_s \sin\omega t \tag{3.12}$$

where ω is the supply angular frequency. Accordingly, the supply power from the ac source can be obtained as,

$$P_{in} = u_s(t) i_s(t) = \frac{U_s I_s}{2} - \frac{U_s I_s}{2} \cos 2\omega t \tag{3.13}$$

It is obvious that P_{in} includes two parts. The first part is the average output power P_{Ho} which feeds the dc loads,

$$P_{Ho} = \frac{U_s I_s}{2} \tag{3.14}$$

The second part is the ripple power P_{Hr}, which is introduced by the second-order harmonic current i_r.

$$P_{Hr} = \frac{U_s I_s}{2} \cos 2\omega t \tag{3.15}$$

It is clear that the amplitude of the ripple current i_r is equal to the dc component I_{dc}, and its equation can be obtained as,

$$i_r = I_{dc} \cos 2\omega t \tag{3.16}$$

The output capacitor is sized mainly to meet the low frequency voltage ripple requirements. The output capacitor equation is below,

$$C_{dc} = \frac{P_o}{2 \cdot \pi \cdot f \cdot \Delta V_{dc} \cdot V_{dc}} \tag{3.17}$$

If the average output voltage V_{dc} is fixed at 400 V, the relation among the power level, capacitance, and its voltage ripple can be shown in Fig. 3.7,

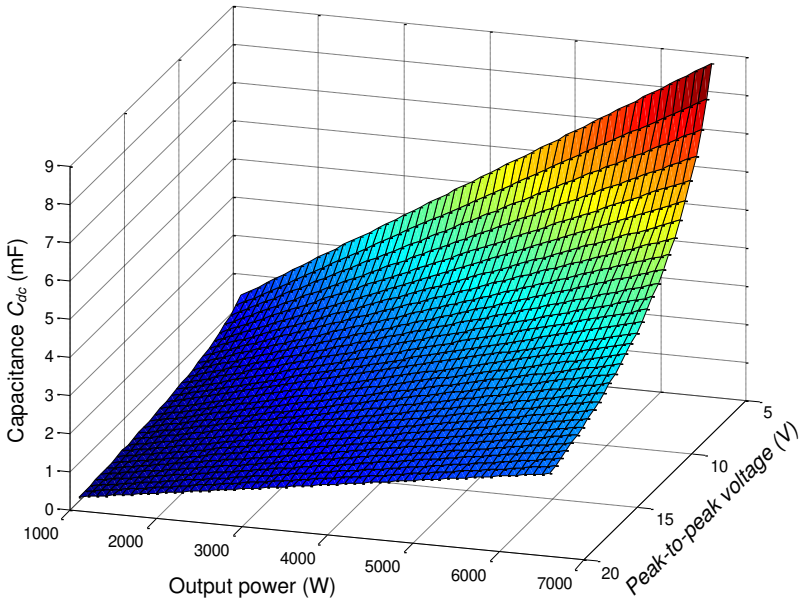


Fig. 3.7. Relation among the power level, capacitance, and its voltage ripple.

3.3.2 Active filter requirements

The conventional bidirectional buck converter (shown in Fig. 3.1(c)) can be applied in the HV battery charger. The feed-forward digital control method is occupied on this application. The duty cycle is calculated directly according to the corresponding system variables [40]. The switching operating diagram of the bidirectional buck converter is shown in Fig. 3.8.

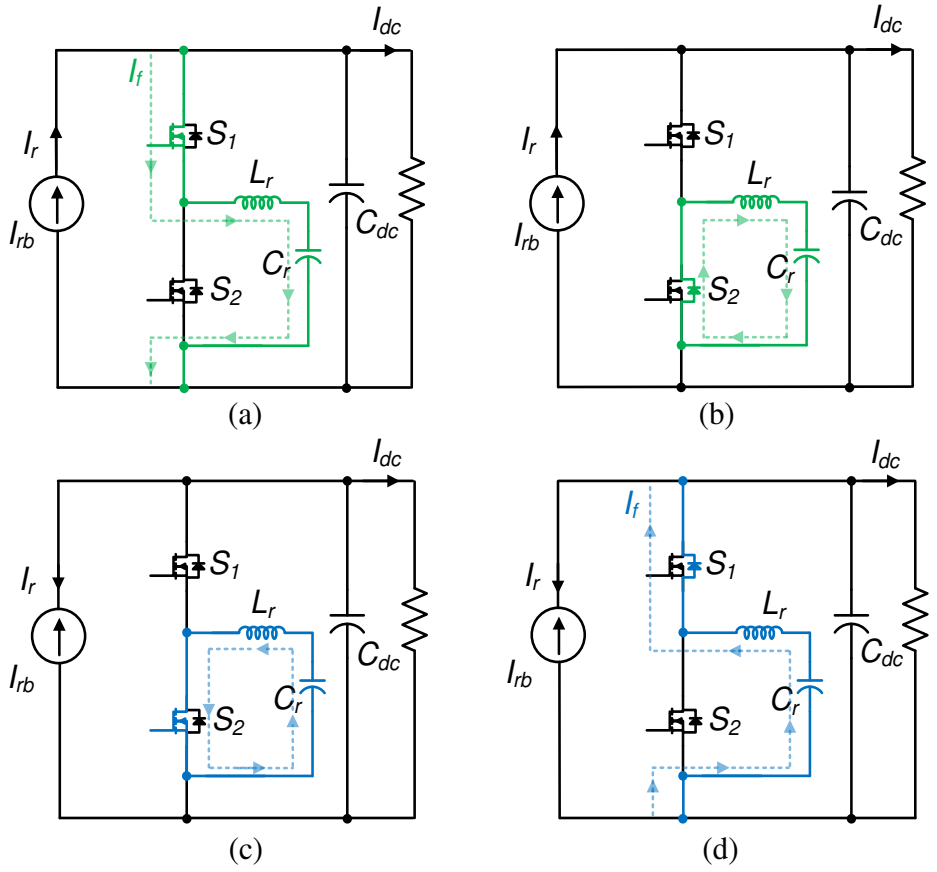


Fig. 3.8. Switching operating diagram of the bidirectional buck AF converter. (a) Buck mode, inductor current rising. (b) Buck mode, inductor current falling. (c) Boost mode, inductor current rising. (d) Boost mode, inductor current falling.

Fig. 3.8 (a) shows once the second-order harmonic current i_r is higher than zero, the converter needs to assimilate the harmonic current. At that time, the switch S_1 turn on. The harmonic current will charge both L_r and C_r. When S_1 is turned off, inductor L_r transfers its energy to C_r thru the diode of S_2, as shown in Fig. 3.8 (b).

The inductor current rising rate is,

$$\alpha_1 = \frac{V_{dc} - V_{Cr}}{L_r} \tag{3.18}$$

The inductor current falling rate can be expressed by,

$$\alpha_2 = -\frac{V_{Cr}}{L_r} \tag{3.19}$$

The average compensation current in a switching cycle can be calculated by the shaded triangular area in Fig. 3.9 (a). The average compensation current should be equal to the ripple current i_r. Hence, the relation between compensation current and duty cycle can be expressed by,

$$i_r \cdot T_s = \frac{1}{2} \cdot I_{peak} \cdot T_1 = \frac{V_{dc} - V_{Cr}}{2L_r} D_\alpha{}^2 T_s{}^2 \tag{3.20}$$

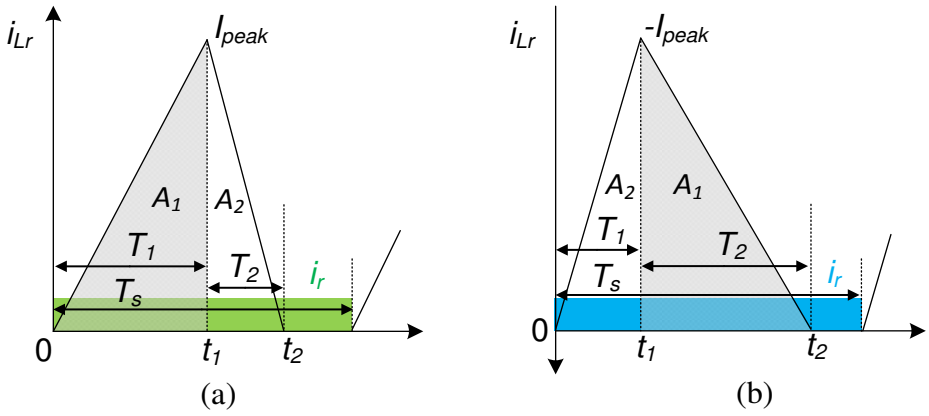


Fig. 3.9. Inductor currents. (a) Buck mode. (b) Boost mode.

Therefore, the duty cycle D_α for the S_1 can be obtained as,

$$D_\alpha = \sqrt{\frac{2 \cdot i_r \cdot f_s \cdot L_r}{V_{dc} - V_{Cr}}} \tag{3.21}$$

When the harmonic current i_r is lower than zero, the converter needs to release the stored energy back to the HV dc-link. At this time, S_2 is used to control the circuit in boost mode. During the turn-on interval of S_2, L_r is charged by the capacitor C_r, as shown in Fig. 3.8 (c). When S2 is turned off, both L_r and C_r are discharged and release the energy back to the HV dc-link thru the diodes of S_1, as shown in Fig. 3.8 (d).

The inductor current rising rate is,

$$\beta_1 = \frac{V_{Cr}}{L_r} \tag{3.22}$$

The inductor current falling rate can be expressed by,

$$\beta_2 = \frac{V_{Cr} - V_{dc}}{L_r} \tag{3.23}$$

The inductor current can be drawn as shown in Fig. 3.9 (b). Same as the buck mode, the average compensation current i_r in a switching cycle can be calculated by the shaded triangular area, since the inductor peak current I_{peak} satisfies,

$$I_{peak} = \beta_1 T_1 = \beta_2 T_2 \tag{3.24}$$

Therefore,

$$i_r \cdot T_s = \frac{1}{2}\frac{{\beta_1}^2}{\beta_2}{T_1}^2 = \frac{{V_{Cr}}^2}{2(V_{dc} - V_{Cr})L_r}{D_\beta}^2{T_s}^2 \tag{3.25}$$

Hence, the duty cycle D_β for the S_2 can be obtained as,

$$D_\beta = \sqrt{\frac{2 \cdot i_r \cdot (V_{dc} - V_{Cr}) \cdot f_s \cdot L_r}{{V_{Cr}}^2}} \tag{3.26}$$

The control circuit is shown in Fig. 3.10. To prevent the overcharging of the output capacitor, another voltage loop is used to control the average value of the capacitor voltage, where a low pass filter is applied.

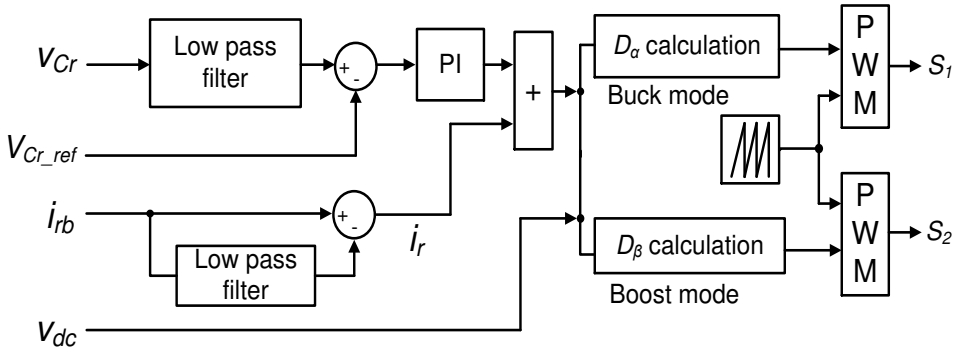


Fig. 3.10. Detailed feedforward control circuit.

A 6.6 kW HV battery charger for the electrified vehicles is also simulated in this chapter as shown in Fig. 3.11. The HV battery charger system parameters are shown in Table 3.3.

Table 3.3. Parameters of the HV battery charger system.

Parameters	Value
AC supply frequency	60 Hz
AC Input voltage	230 V
HV battery DC bus voltage V_{dc}	400 V
HV battery charger output power	6.6 kW

Before 0.037 s, the AF is turned off so that the 120 Hz second-order harmonic occurs on the dc-link V_{dc}. After 0.037 s, the AF is turned on. The voltage V_{dc} on the HV battery's dc-link is 400 V with relatively small ripple. The ripple energy is stored in the AF's capacitor C_r and the voltage ripple of that capacitor V_{cr} fluctuates between 100 V to 320 V.

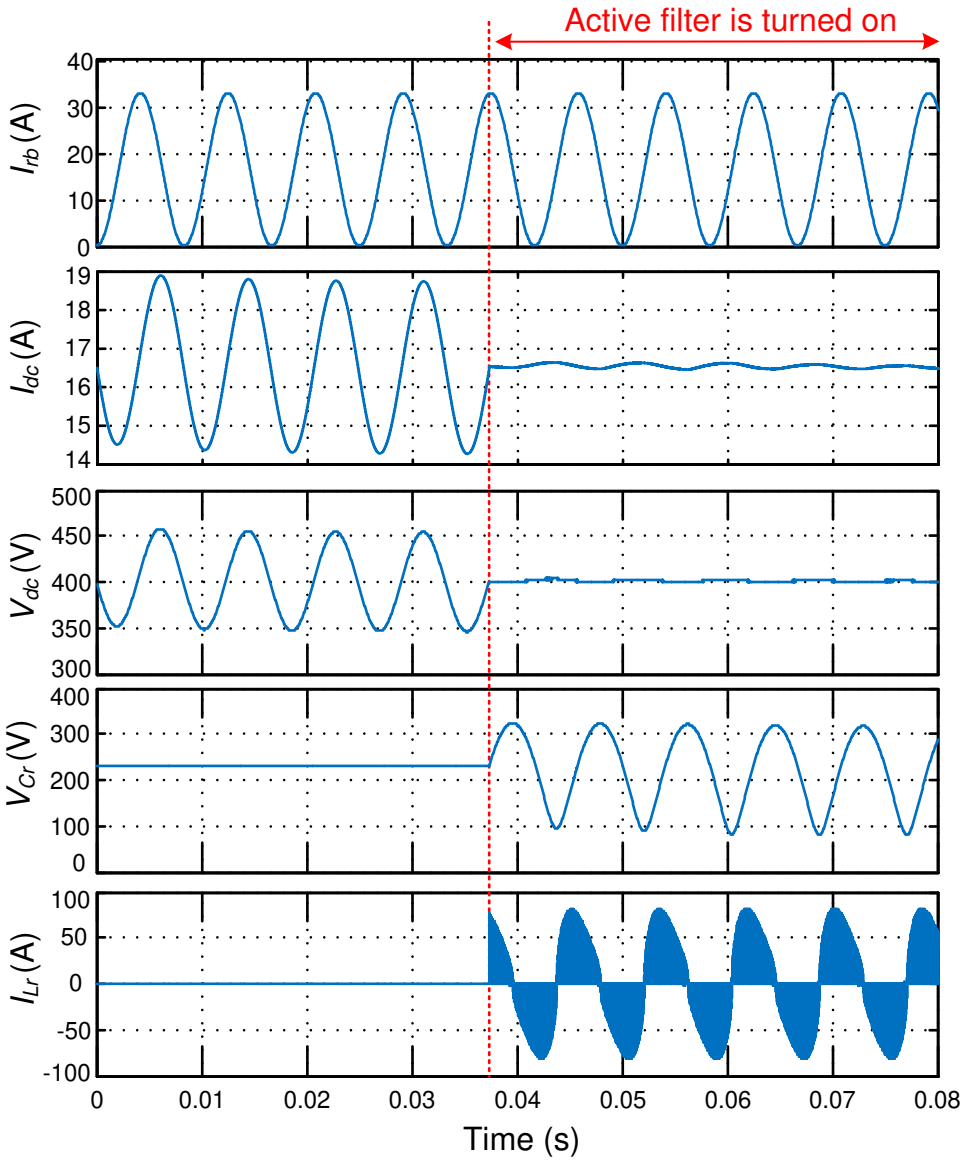


Fig. 3.11. Bidirectional buck-boost converter for single-phase HV battery charger second-order harmonic simulation results.

In order to mitigate the second-order harmonic current in the 6.6 kW single-phase HV battery charger, a 10 µH/80 A auxiliary inductor L_r and a 380 µF/400 V auxiliary capacitor C_r are needed to transfer and store the ripple energy respectively. Regarding the

power switches, due to the relatively low harmonic frequency, 100 kHz is sufficient for the active filtering. In addition, as the dc charging current is around 16.5 A, the magnitude of the second-order harmonic component is relatively low. This yields a relatively low current stress for the switches. The MOSFETs requirements are shown in Fig. 3.12. Clearly, only two 400 V/40 A switches are needed.

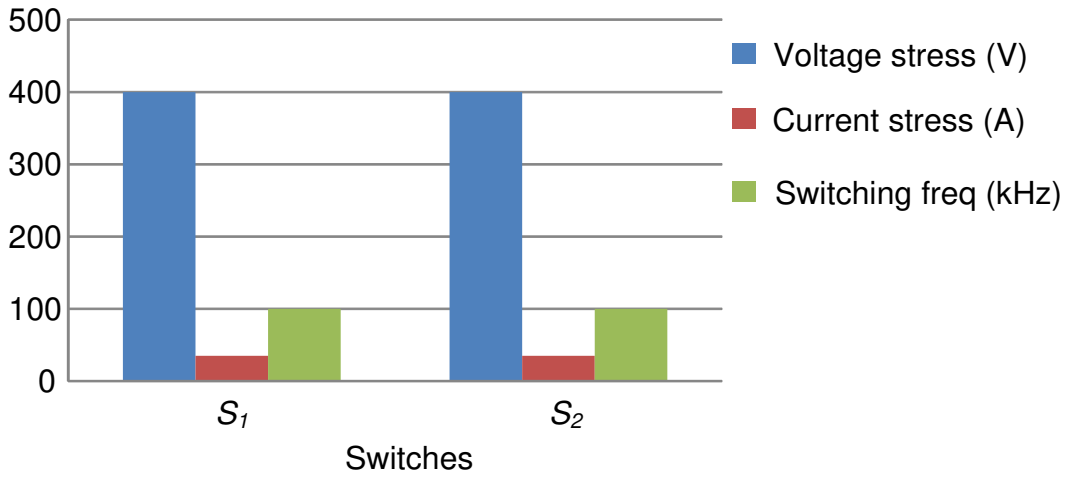


Fig. 3.12. Switch requirements of bidirectional buck AF for 6.6 kW HV battery charger's dc-link.

3.4 PROPOSED INTEGRATED AFAPM CONCEPT

3.4.1 System integration methods

The integrated AFAPM is an integration of the conventional AF and the conventional APM. It is not only a LV battery charger, but also acts as an AF to mitigate harmonics in the other power electronics sub-systems of the electrified vehicle powertrains. As a result, the required capacitance on the corresponding dc bus can be

reduced, while no extra power switches, heat sinks, and gate drivers are needed. Based on the different powertrain requirements, the boost converter shown in Fig. 1.6 for the traction inverter might not be required. In the meanwhile, the HV battery charger could be a single-stage charger or a two-stage charger containing the second-order harmonic current. Therefore, theoretically, two types of integrated AFAPMs can be applied in electrified vehicles as shown in Fig. 3.13.

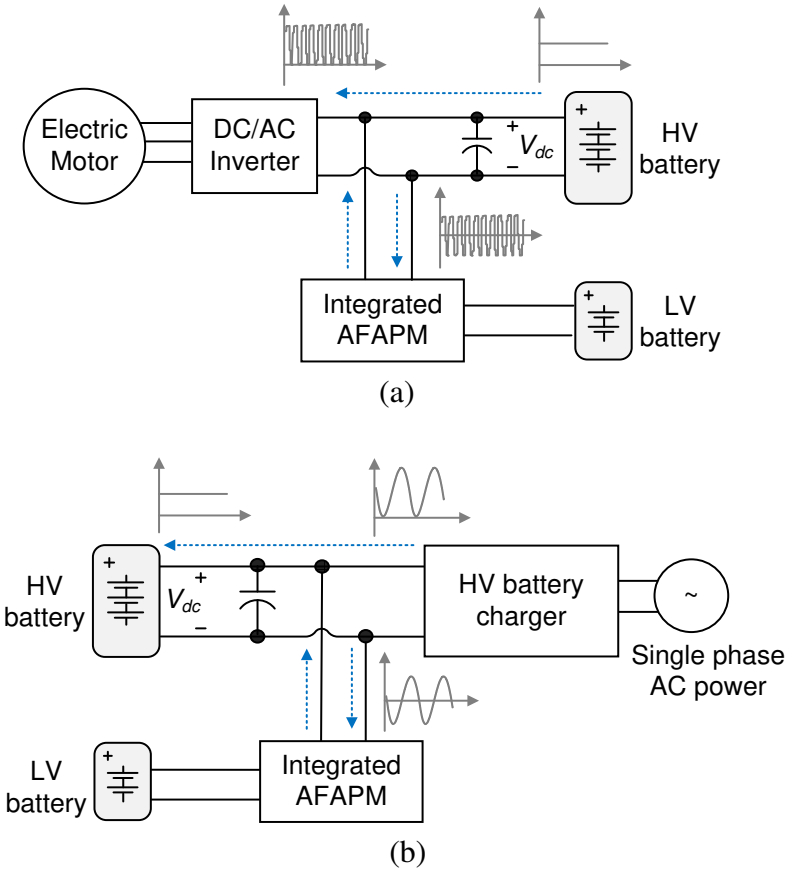


Fig. 3.13. Two types of system integration. (a) Type A. (b) Type B.

The Type A integrated AFAPM is used to fulfill the LV battery charging and active filtering for the traction inverter's dc-link harmonics; the Type B integrated AFAPM is applied to achieve the LV battery charging and active filtering for the single-phase HV battery charger's dc-link harmonics. However, the demanding requirements to the power switches make the Type A practically challenging. Because of the relatively low frequency of the second-order harmonic current, active filtering and, thus, the Type B integrated AFAPM is a promising method to replace or reduce the bulk film capacitor or the extra active filter circuit in the single-phase HV battery charger.

3.4.2 Topology integration methods

The topological evaluation of different isolated dc/dc converters for the APMs has been done in the Chapter 2. Typically, for a 2.4kW APM converter, the primary stage need to handle around 400 V high-voltage and the secondary stage are required to yield around 200 A high-current. A conventional full bridge with current doubler is used as a conventional APM converter. The switch ratings of a 2.4 kW APM design are shown in Fig. 3.14.

Besides the transformer, the main components in a conventional APM can be summarized and classified into two parts. They are power switches and LV battery filters. Same as the AF, it consists of switches and ripple filters. Hence, three different integration methods can be proposed. They are primary-integration, secondary-integration, and full-integration as shown in Fig. 3.15 respectively.

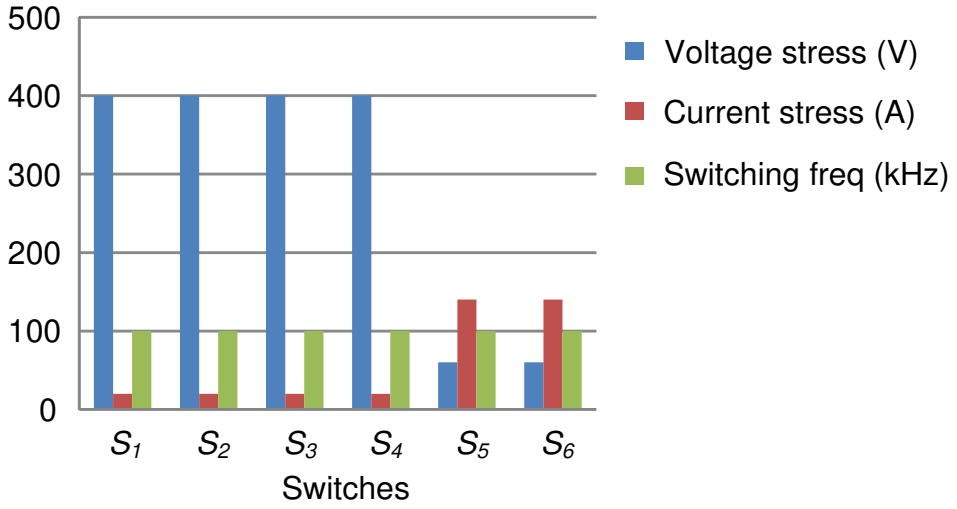


Fig. 3.14. Switch requirements of conventional 2.4 kW APM.

For the primary-integration method, the primary switches are shared by both APM and AF. Additional active ripple filters need to be installed on the primary stage of the AFAPM. For the secondary-integration method, the secondary switches and filter are shared by both APM and AF. All the components are shared by the AF and APM in the full-integration method.

Based on the APM switch requirements listed in Fig. 3.14, it is clear that the primary-integration and full-integration are suited for high-voltage low-current harmonics compensation as the harmonic currents are injected into the primary stage; the secondary-integration fits for low-voltage high-current harmonics compensation as the harmonic currents are injected into the secondary stage. For the full-integration, the high-voltage low-current harmonics have to be transformed to the secondary stage of the APM and converted to low-voltage high-current components. High current on the secondary side

will also introduce more conductive losses of the switches. Additional losses produced by the secondary-side switches as well as transformer have to be taken into account.

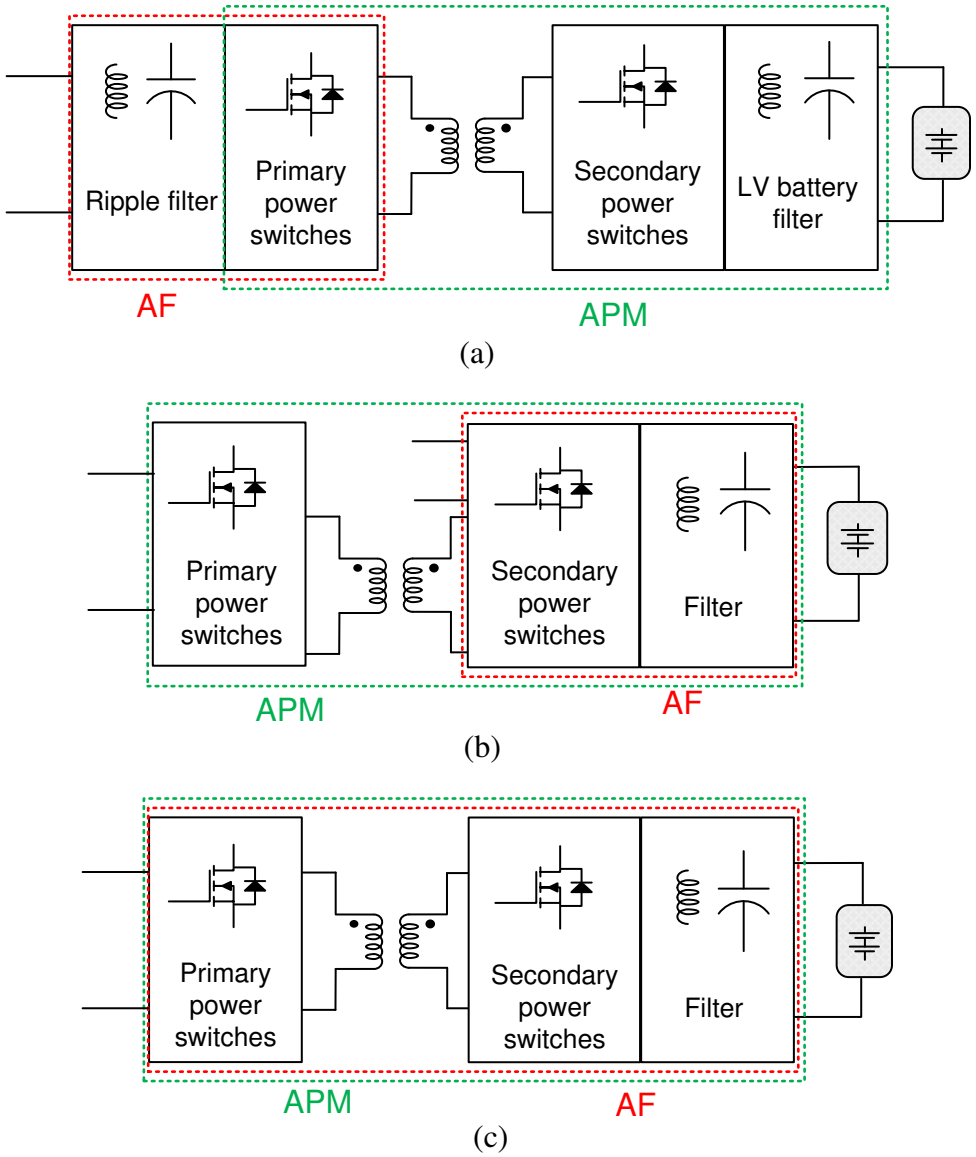


Fig. 3.15. Three AFAPM topology integration methods. (a) Primary-integration. (b) Secondary-integration. (c) Full-integration.

3.5 THE PROPOSED DUAL-VOLTAGE CHARGING SYSTEM

3.5.1 Proposed dual-voltage charging system operating principle

The proposed dual-voltage charging system operating principle includes two modes. The first mode is when the vehicle at charging station and the HV battery pack is charging thru the charge port, as shown in Fig. 3.16 (a). During this period, the single-phase ac power charges the HV battery thru the HV battery charger. In the meanwhile, the AFAPM converter works as an AF to compensate the second-order harmonic caused by the single-phase line. By doing so, the bulk capacitor which is applied to filter the second-order harmonic in the HV battery charger can be eliminated. Instead, only a small capacitor is needed on the dc-link to filter the high frequency harmonic currents.

The second mode is when the HV battery stops charging and the vehicle is running, as shown in Fig. 3.16 (b). During this mode, the single-phase ac power source is disconnected from the vehicle. The AFAPM converter now operates as a LV battery charger. The HV battery transfers power to the LV battery thru the AFAPM converter. Based on the different LV auxiliary load variations, the AFAPM converter can control and change its duty cycle independently according to the driving demands.

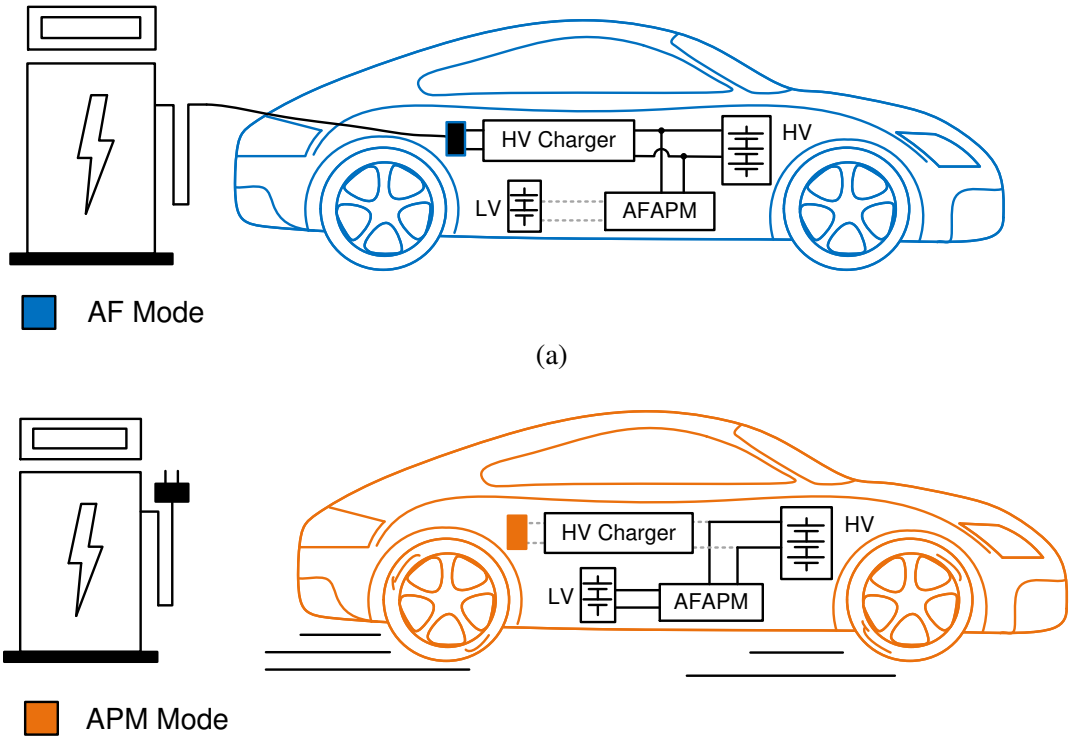


Fig. 3.16. Proposed dual-voltage system operating principle. (a) AF Mode, vehicle at charging station. (b) APM Mode, vehicle is running on the road.

3.5.2 Possible dual-voltage charging system topologies

For different conventional conductive on-board dual-voltage systems discussed in the chapter 1 shown in Fig. 1.3, several diverse new dual-voltage system topologies can be developed based on their distinguishing characteristics as shown in Fig. 3.17.

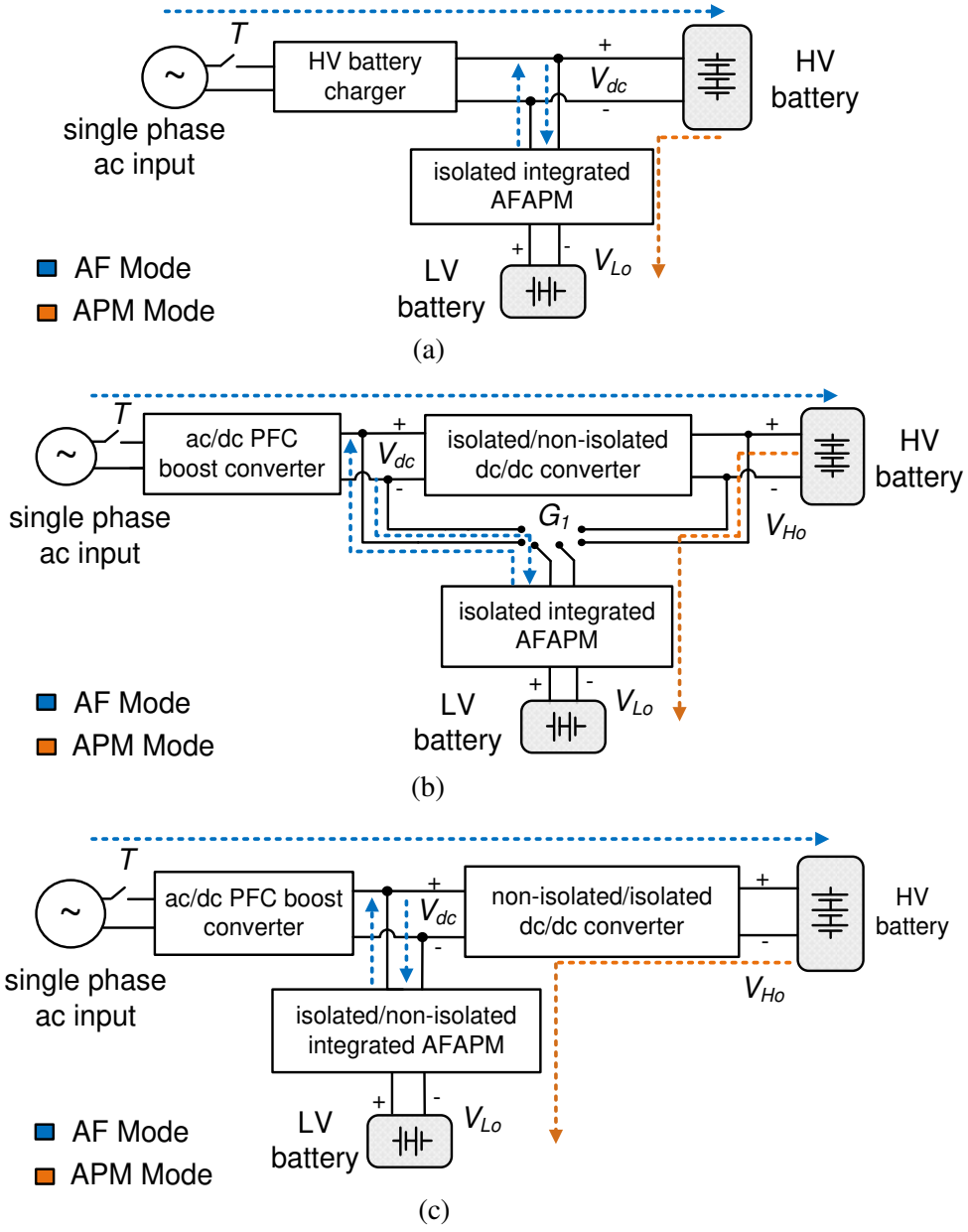


Fig. 3.17. The proposed dual-voltage charging systems and their operating principles. (a) With integrated AFAPM. (b) With switching integrated AFAPM. (c) With intermediate integrated AFAPM.

The simplest one should be the dual-voltage system with the single-stage or two-stage HV battery charger that containing the second-order harmonic current. As the second-order harmonic current occurs on the same dc-link connected to the integrated AFAPM, there will be no hardware change but the bulk capacitor can be removed as shown in Fig. 3.17 (a). The integrated AFAPM acts as AF during the Mode I and uses as a LV battery charger during the Mode II.

If the two-stage topology is applied to the HV battery charger, in which the second-stage dc/dc converter does not contain the second-order harmonic current, two possible dual-voltage charging system topologies are shown in Fig. 3.17 (b) and 3.17 (c), respectively. In Fig. 3.17 (b), a mechanical double pole double throw (DPDT) switch G_1 can be applied to switch the AFAPM between HV active filtering mode and LV charging mode. No matter the dc/dc converter in the HV charger is isolated or not, the integrated AFAPM has to be isolated. In Fig. 3.17 (c), this topology shifts the integrated AFAPM to the intermediate position between the PFC boost converter and the dc/dc converter of HV battery charger. As a result, during the HV battery charging period, the integrated AFAPM can compensate the second-order harmonic on the dc-link without any hardware change. And during the LV battery charging period, the charging current will flow thru the dc/dc converter in the HV battery charger and then thru the AFAPM. Please note here, if the dc/dc converter in the HV charger is non-isolated, an isolated AFAPM has to be applied; if the dc/dc converter in the HV charger is isolated, it already provides isolation between HV and LV battery and, hence, a non-isolated AFAPM topology is feasible.

3.6 CONCLUSIONS

This chapter explores and evaluates the proposed integrated AFAPM concept in electrified vehicle applications. The results show that the size of the dc-link capacitor in the traction inverter is determined by the switching ripple. In addition, the power rating of the traction inverter is much higher than the LV battery charger in a typical electrified vehicle. Hence, the AFAPM in the traction drive system is practically challenging. In the meanwhile, the size of the dc-link capacitor in the HV battery charger is determined by the second-order harmonic power rather than switching ripple. Moreover, the power rating of the HV battery charger is similar to the LV battery charger. Therefore, the AFAPM in the HV battery charger system is a feasible and attractive solution.

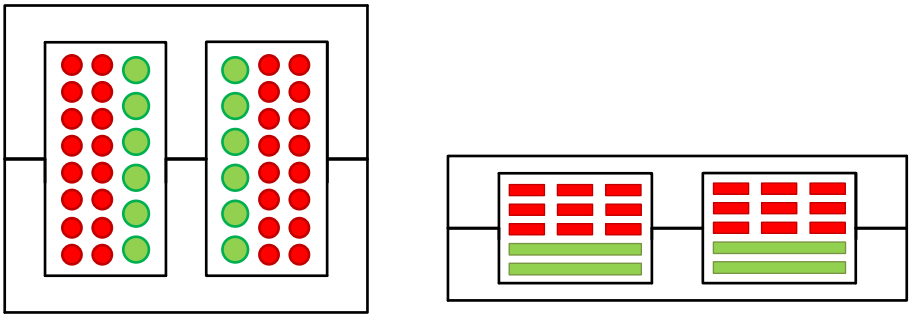
Furthermore, a simple and effective dual-mode dual-voltage charging system operating principle is proposed. The integrated AFAPM converter charges the LV battery when the vehicle is running and operates as an AF when the vehicle is connected to the grid and the HV battery is charging. Hence, the low-frequency second-order harmonic current can be alleviated without a bulk capacitor bank or an extra active filter circuit in the HV battery charger.

Chapter 4

PLANAR TRANSFORMERS FOR AUXILIARY POWER MODULE APPLICATIONS

4.1 INTRODUCTION

The momentum toward high efficiency, high operating frequency, high power density, and low profile in power converters has exposed a number of limitations in the use of conventional wire-wound magnetic component structures [115]. For example, high-frequency operation can lead to a reduction in magnetics size and an increase in power density. However, winding loss will be significantly increased due to the eddy current effect in conventional round conductors. In the meanwhile, for magnetic design, there is also a trend toward integration and planarization. Planar magnetic components intrinsically provide lower profiles than conventional wire-wound components, aiding the miniaturization of power converters [116-118]. The low profile planar cores lead to a better surface-to-volume ratio, as shown in Fig. 4.1. This provides a better thermal characteristic under the heat exchange surface, and thus yields a better thermal characteristic as shown in Fig. 4.2 [116].



(a) (b)

Fig. 4.1. Magnetics structures. (a) Conventional wire-wound structure. (b) Planar structure.

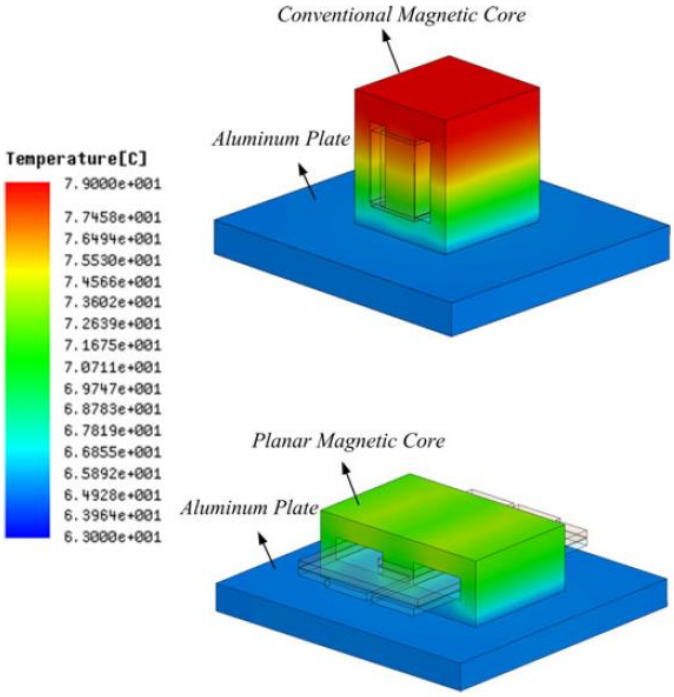


Fig. 4.2. Comparison of thermal behavior between conventional core and planar core [116].

Another advantage of planar transformer is its ease of implementation on winding interleaving. When the primary and secondary layers are sandwiched, the proximity effect can be strongly decreased. The reason behind is that the primary and secondary currents flow in opposite directions so that their magnetic fields will be cancelled out. Their currents will be distributed more uniformly after interleaving and the high frequency ac winding copper loss can be greatly reduced [116]. Another advantage of the interleaved planar transformer is its low leakage inductance, due to the magnetomotive force (MMF) reduction. Moreover, planar transformer also provides unrivalled repeatability. The PCB techniques are easily adapted for mass production.

In this chapter, the planar transformer design is presented which is particularly for the APM application. The turn ratio and number of turn selection are presented for two different converters: full bridge current doubler and DAB converter. The different core loss equation and calculation are discussed. The current sharing issue and copper loss calculation is included. Then a method to minimize the leakage inductance is also presented.

4.2 CORE MATERIAL SELECTION

In the transformer design, trade-offs always exist. The detailed planar transformer design iteration can be summarized in the Fig. 4.3. Once the converter topology is selected, the switching frequency should be determined as well. Based on the converter operating parameters, the core material can be determined.

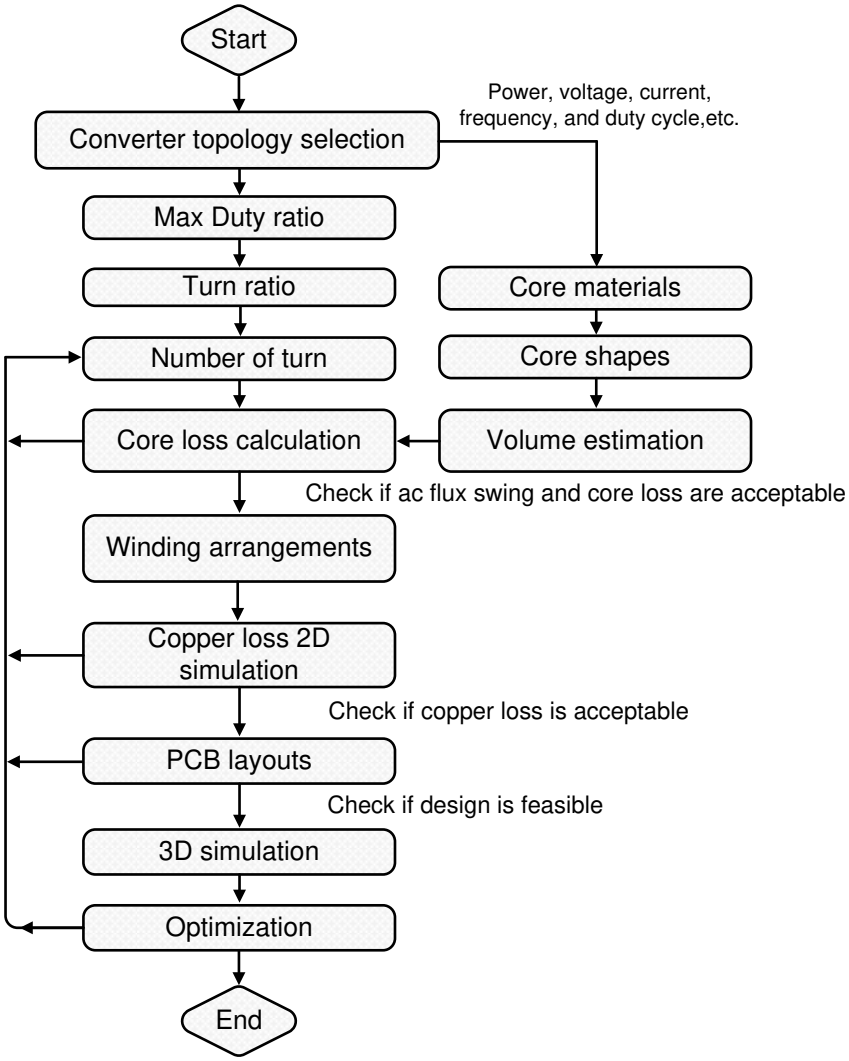


Fig. 4.3. Detailed planar transformer design iteration.

Ferrites that are used in transformer are soft ferrites, which have a low coercivity. Manganese-zinc (MnZn) and Nickel-zinc (NiZn) ferrites are the most common soft ferrites. MnZn have higher permeability and NiZn is more suitable for frequencies above 1 MHz. Transformers generally operate under saturation limited conditions. This requires power ferrites with high saturation levels. For the transformer core material selection, a

performance map for different soft ferrite MnZn materials from Ferroxcube is shown in Fig. 4.4 [119].

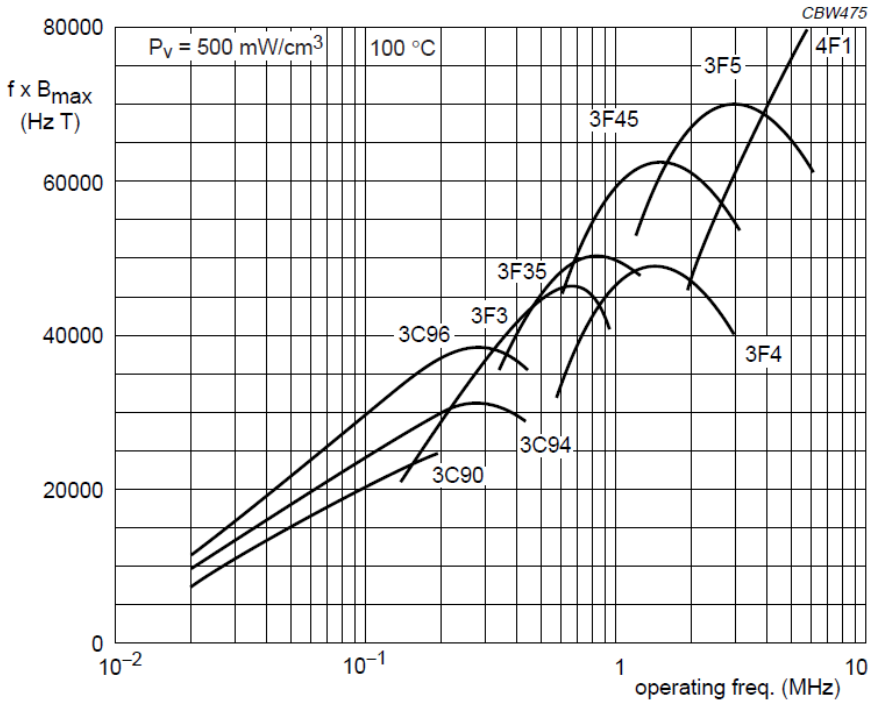


Fig. 4.4. Soft ferrite material performance map from Ferroxcube [119].

The above figure shows that at a certain loss level, the 3C96 can achieve highest maximum flux density at 100 kHz, which is the desired switching frequency of the converter. In this thesis, the 3C95 is selected as the core material, as it fits for the application at frequencies up to 500 kHz and has a similar performance as the 3C96. In addition, 3C95 is especially suited for broad temperature range applications like automotive [119]. The B-H curve of 3C95 material is shown in Fig. 4.5. It is clear that the maximum ac flux swing can be set at 250 mT. Beyond that point, the transformer might be saturated.

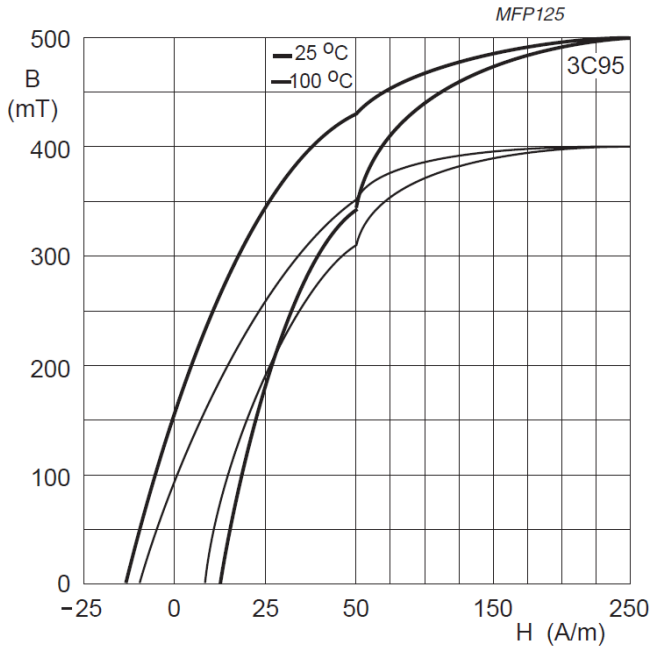


Fig. 4.5. B-H curve of 3C95 material [119].

4.3 TURN RATIO AND NUMBER OF TURN SELECTION

4.3.1 Transformer for full bridge current doubler

The voltage gain equation of the full bridge current doubler can be obtained as,

$$\frac{V_{Lo}}{V_{Ho}} = \frac{ph}{n} - \frac{I_{Lo}L_k f_s}{n^2 V_{Ho}} \tag{4.1}$$

where V_{Lo} is the output voltage, V_{Ho} is the input voltage, ph is the phase shift angle between the primary two bridges, n is the transformer turn ratio, I_{Lo} is the load current, L_k is the leakage inductance of the transformer referred to the primary stage, and f_s is the switching frequency. In the equation (4.1), the first term is the ideal voltage gain and the second term is the duty-cycle loss introduced by the transformer's leakage inductance. As

the initial step of the design, the leakage inductance of the transformer can be assumed to be ranged between 1 µH and 5 µH. By fixing the output voltage V_{Lo} to 12 V, a relation among the transformer turn ratio n, leakage inductance L_k, phase shift angle ph, and the range of the input voltage V_{Ho} can be drawn in Fig. 4.6.

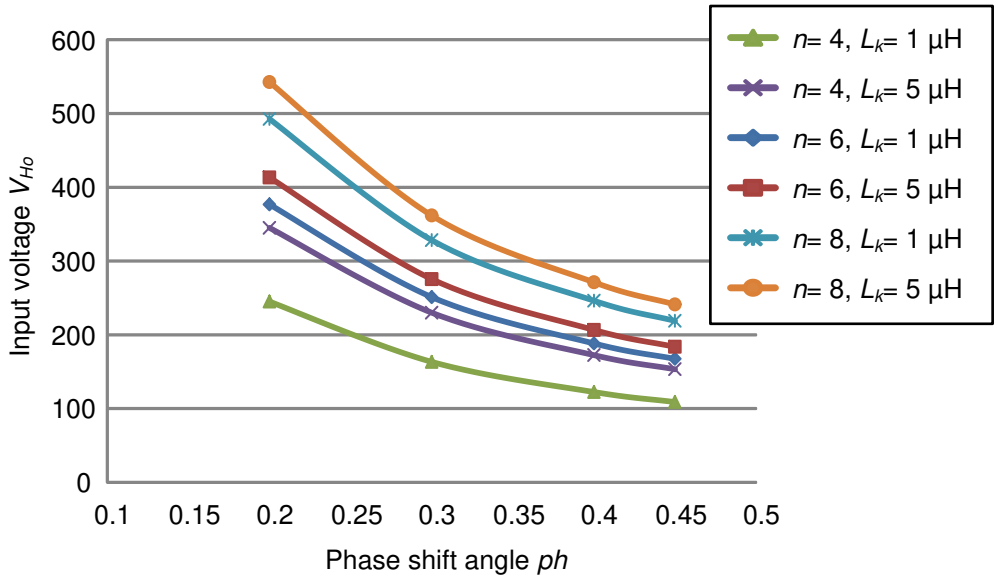


Fig. 4.6. Relation among transformer turn ratio, input voltage, leakage inductance and phase shift angle for full bridge current doubler.

A typical input voltage range is varied from 200 V to 400 V. Hence the transformer's turn ratio needs to meet this wide high conversion demand and produce 12 V output voltage for the LV battery. Therefore, from Fig. 4.6, the turn ratio n=6 is selected for the full bridge current doubler.

The number of primary turns N_p can be calculated as,

$$N_P = \frac{V_{Ho} \cdot ph}{2 \cdot B_{max} \cdot A_e \cdot f_s} \tag{4.2}$$

where B_{max} is the transformer's flux swing, A_e is the effective area of the core. A relation among ac flux density, the number of turns and the core structure can be obtained as shown in Fig. 4.7. Typically, higher number of turns yields a smaller maximum flux swing and thus, limits the core loss. As a tradeoff, with higher number of turns, the copper loss will be increased accordingly. For the core size, the volume estimation can be either Area Product (AP) method or Core Geometry (KG) method. However, these estimation methods fit more to the conventional wire-wound magnetic design. They might not be suitable for the planar magnetic design, due to their relatively low copper filling factor [117, 120]. Several planar E cores from the Ferroxcube are considered in this thesis. They are all in EE combination with the E38, E43, E58 and E64. The detailed core dimensions can be found in [121].

In addition, the number of layers is preferred to be an even number. This is because the windings will always start from the outer portion of the transformer and wind towards to the center of the core. Then it must go down one layer and wind back towards to the outer portion of the transformer and connect to the converter circuit. Considering from the ac flux density aspect, the E58 with 12 primary number of turn is a reasonable choice. Therefore, 12:2 is selected as the transformer turn ratio for the full bridge current doubler converter.

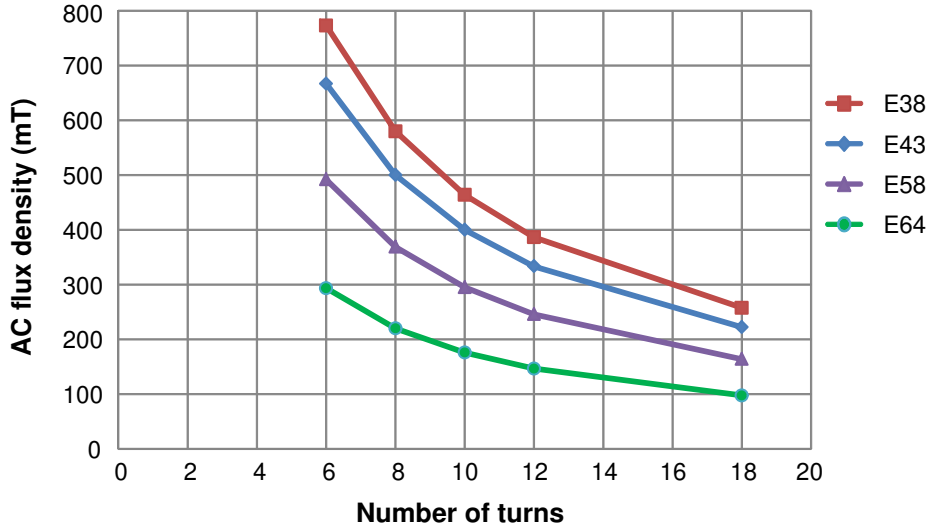


Fig. 4.7. Relation among core area, number of turns and ac flux density.

4.3.2 Transformer for dual active bridge converter

For the DAB converter, the selection of turn ratio n can be determined by the DAB soft switching constrains. The limits for the phase shift angle ϕ to maintain ZVS can be obtained as [71],

$$\begin{cases} \phi > 0.5 - \dfrac{V_{Ho}}{2nV_{Lo}}, if\ V_{Lo} \geq nV_{Ho} \\ \phi > 0.5 - \dfrac{nV_{Lo}}{2V_{Ho}}, if\ V_{Lo} \leq nV_{Ho} \end{cases} \tag{4.3}$$

Then a ZVS range can be plotted by varying nV_{Lo}/V_{Ho} and phase shift angle ϕ as shown in Fig. 4.8. It is clear that with the nV_{Lo}/V_{Ho} closer to 1, the phase shift range to achieve ZVS is wider. As the input voltage V_{Ho} from the HV battery might be varied between 300 V to 400 V and output voltage V_{Lo} might be varied between 12 V to 16 V, a

reasonable turn ratio n is ranged from 20 to 30. In this thesis, we choose the turn ratio n is 20. This is because a minimized leakage inductance from the transformer is desired, which will be explained in the next chapter.

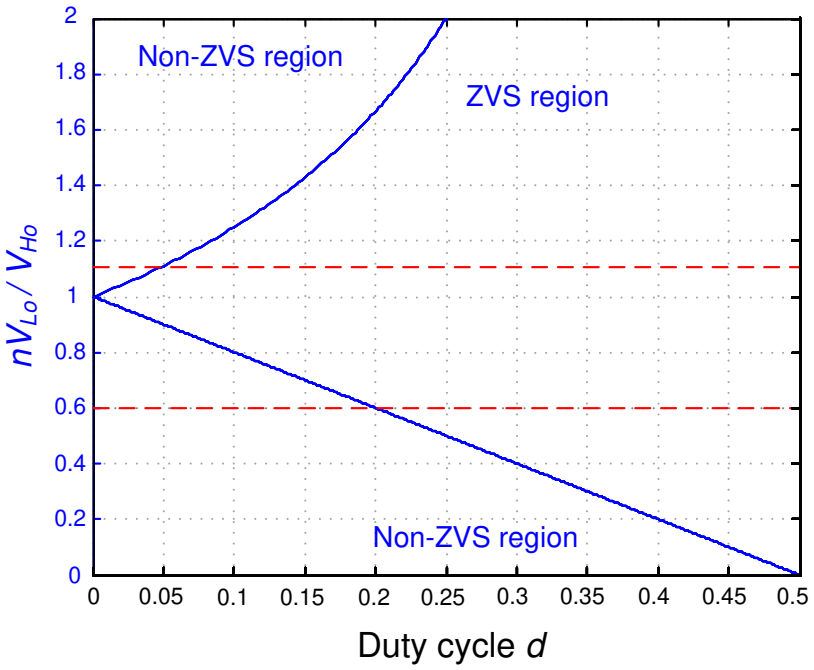


Fig. 4.8. DAB turn ratio design map.

4.4 CORE LOSS CALCULATION

The core loss calculation is based on several different core loss equations. Many studies have already been conducted to estimate the core loss and diverse equations have been developed [115, 122]. The Original Steinmetz equation (OSE) can be written as following,

$$P_v = K \cdot f_s^{\alpha} \cdot B_{max}^{\beta} \tag{4.4}$$

where α, β, K are the material parameter provided by the manufacturer [119, 123]. However, this equation fits for sinusoidal waveform voltage excitation. In [122], a Waveform-Coefficient Steinmetz equation (WCSE) is proposed. This one is suitable for square voltage waveform excitation. The equation is,

$$P_v = \frac{\pi}{4} \cdot K \cdot f_s^{\alpha} \cdot B_{max}^{\beta} \tag{4.5}$$

The third one is the Extension of Steinmetz equation (ESE) which is exactly for the full-bridge dc-dc converter operating with the symmetrical square waveform [115],

$$P_v = 2^{2\alpha-1} \cdot K \cdot f^{\alpha} \cdot B_{sqm}^{\beta} \cdot D^{\beta-\alpha+1} \tag{4.6}$$

where D is the duty cycle. B_{sqm} is the peak flux density when the square waveform is with 50% duty cycle, which can be obtained by,

$$B_{sqm} = \frac{V_{Ho}}{4N_p \cdot A_e \cdot f_s} \tag{4.7}$$

The relation among core loss, duty cycle and number of turns for each equation can be drawn in the following Fig. 4.9. Obviously, with higher number of turns, the core loss will decrease. In addition, with duty cycle increasing, the core loss will increase as the effective voltage increase.

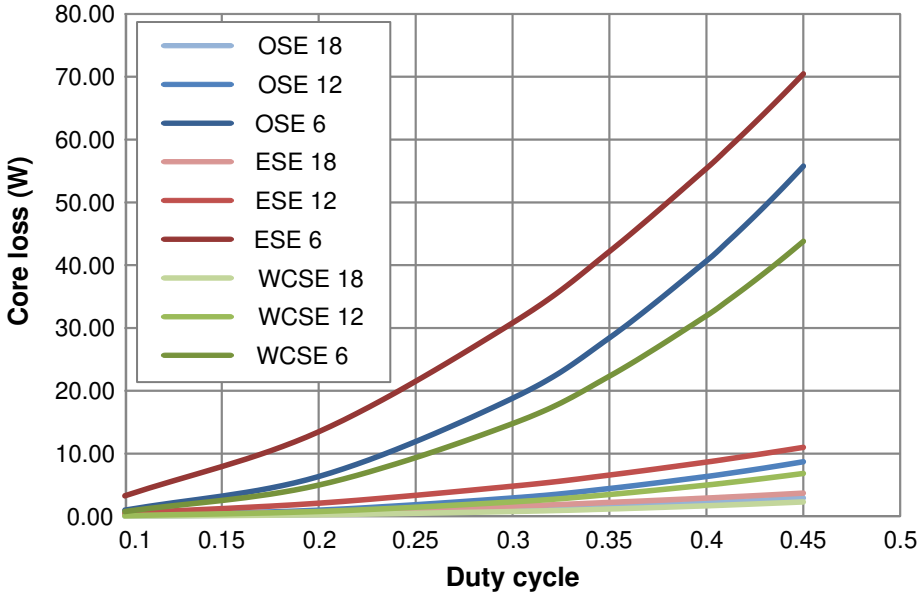


Fig. 4.9. Core loss variations under different number of turns and duty cycle with different core loss calculation methods.

4.5 COPPER LOSS AND CURRENT SHARING

The copper loss in the transformer can be classified as dc copper loss and ac copper loss. The dc copper loss is easy to obtain, which is,

$$P = I_{rms}^2 R_{dc} \tag{4.8}$$

where R_{dc} can be obtained by,

$$R_{dc} = \frac{l}{\sigma \cdot A} \tag{4.9}$$

where l is the copper length, σ is the conductor's conductivity and A is the cross section area. For the transformer RMS current in the full bridge current doubler converter, the primary RMS current can be obtained as,

$$I_{rms\_pri} = \frac{I_{Lo}}{2n} \tag{4.10}$$

Its secondary RMS current can be obtained as,

$$I_{rms\_sec} = \frac{I_{Lo}}{2}\sqrt{2ph} \tag{4.11}$$

Hence, for a 1.2 kW prototype, the transformer secondary RMS current would be around 50 A, and the primary RMS current would be around 8.5 A.

Due to the eddy current effects, the ac copper loss in the transformer can be dramatically increased with high operating frequency. This ac copper loss includes skin effect and proximity effect losses. For the skin effect loss, the skin depth equation is given as,

$$\delta = \sqrt{\frac{2}{2\pi f_s \mu_o \mu_r \sigma}} \tag{4.12}$$

where μ_o is the permeability of free space and μ_r is the conductor's relative permeability. For the copper coil which operates at 100 kHz, the skin depth can be calculated as 0.208 mm. Usually, for high switching frequency operation, in order to limit the skin effect, the

skin depth needs to be higher than the copper thickness. Therefore, in this design, 0.915 kg/m^2 (3 oz/ft^2) copper is applied.

For the proximity effect, as mentioned before, when the primary and secondary layers are sandwiched, the proximity effect can be strongly decreased. This will yield a more uniform current distribution. For a 12:2 planar transformer, three different layer arrangements and their MMF diagrams along a vertical direction are presented in the Fig. 4.10.

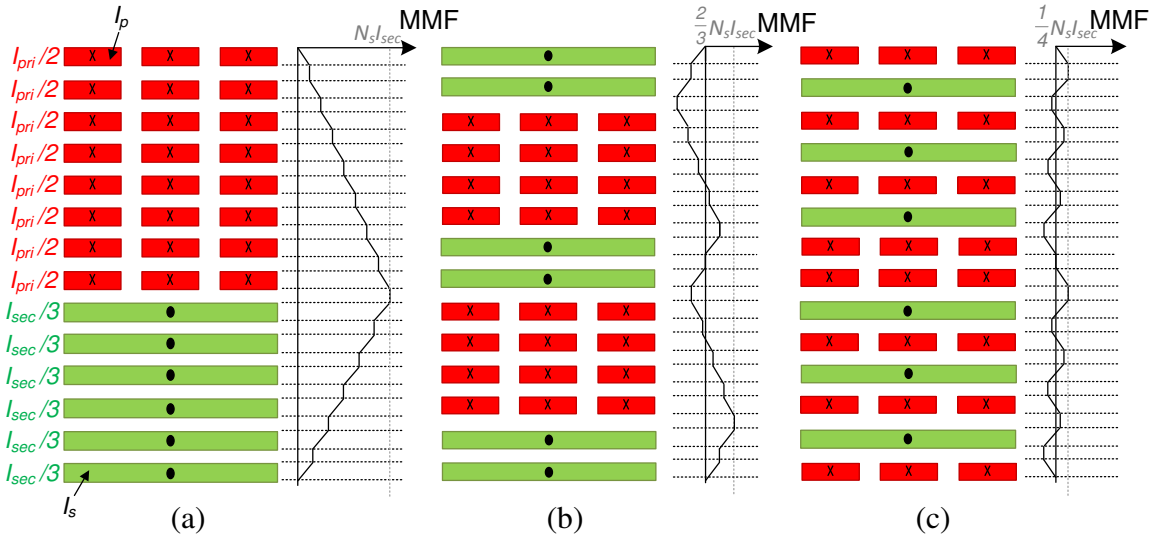


Fig. 4.10. The 12:2 transformer with different layer arrangements and their MMF diagrams. (a) Non-interleaving. (b) Half-interleaving. (c) Full-interleaving.

The MMF in each layer of the primary and secondary windings is given as,

$$MMF\_p = K_p \cdot I_p \tag{4.13}$$

$$MMF\_s = K_s \cdot I_s \tag{4.14}$$

where K_p and K_s is the number of turns in each layer of the primary and secondary sides, respectively, and I_p and I_s are the corresponding currents.

In the meanwhile, as the output current I_{Lo} is relatively high, paralleling windings on the secondary stage is necessary [124]. The biggest drawback of paralleling winding is that the current may not be equally shared among them. This behavior will produce circulating currents which yields extra copper loss. While, as the transformer applied in the thesis has no air gap, the fringing effect can be neglected. Therefore, a symmetrical fully interleaved structure might be still the best choice [116]. Note that for a planar inductor design with air gap, due to the fringing effect, the fully interleaved paralleling winding structure will no longer be the best option at high switching frequency [125-126].

A 2D transformer model is built in the ANSYS Maxwell [127]. In the simulation, the parallel current is assigned to each paralleled winding for excitation. The parallel current assigned to the primary and secondary windings are 8.5 A and 50 A, respectively. The current distribution comparison under the same current density scale is shown in Fig. 4.11.

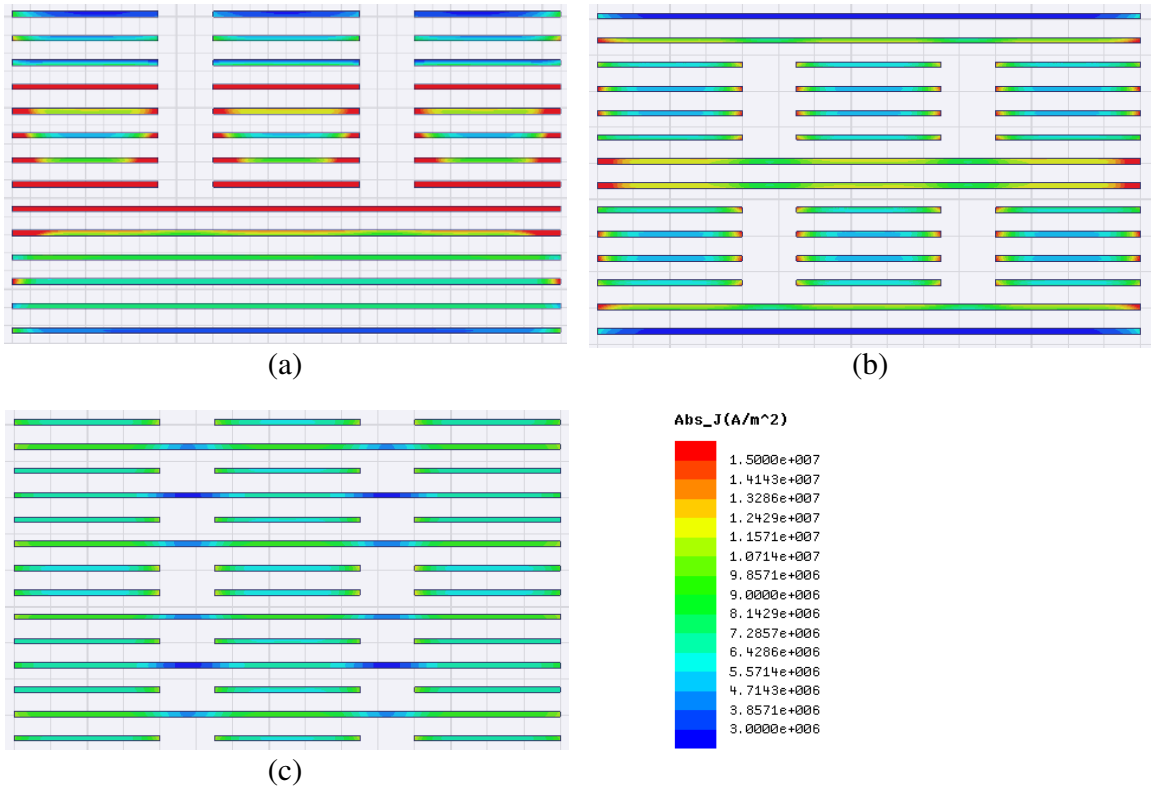


Fig. 4.11. The 12:2 transformer's winding current distribution. (a) Non-interleaving. (b) Half-interleaving. (c) Full-interleaving.

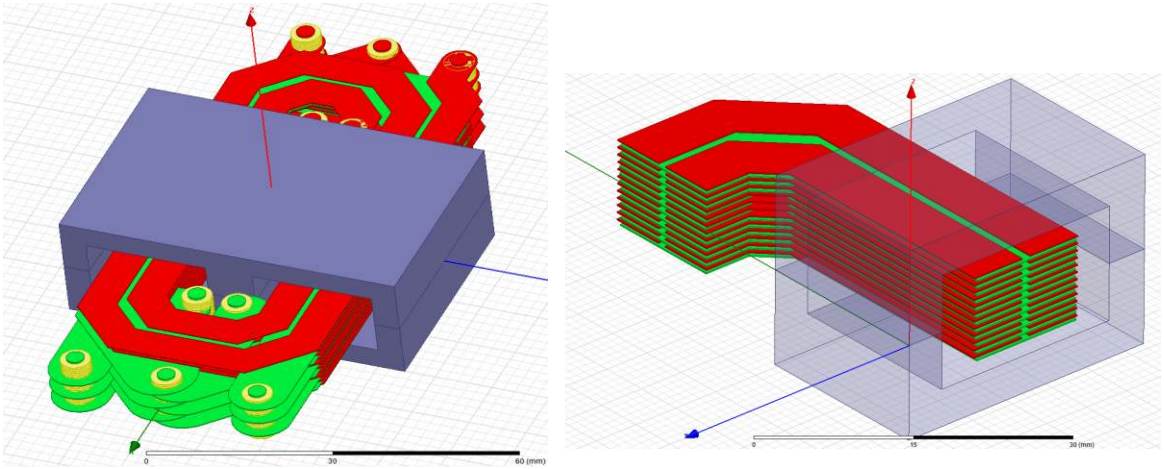
In addition, for the coil temperature prediction, the following empirical equation can be used to estimate the temperature rise on the external track of the PCB [124],

$$I = 0.048 \cdot T^{\,0.44} \cdot (b_w \cdot h)^{\,0.725} \tag{4.15}$$

where T is the temperature on the coil. b_w is the trace width and h is the copper thickness. For the internal track, it has to be de-rated at least by 50% for the same degree of heating [124]. In addition, a reasonable accuracy that up to 1 MHz each increase of 100 kHz in

frequency gives 2°C extra in temperature rise of the PCB compared to the values determined for the RMS current [128].

The copper loss of these three winding arrangement is also simulated in the ANSYS Maxwell 2D and 3D [129]. The main difference between the 2D model from the 3D model is the end winding. One 3D model is built as shown in Fig. 4.12 (a). In order to simplify the 3D simulation, the simulation can also be restricted to one quarter of the whole transformer, as shown in Fig. 4.12 (b).



(a) (b)

Fig. 4.12. The 8:4 planar transformer. (a) 3D model. (b) 3D quarter model.

The error of copper loss between the 2D and 3D model can be eliminated mostly by using mean-length-turn (MLT) as the depth in the 2D simulation. The MLT is particularly used to calculate the dc winding resistance. The MLT for the planar magnetic

design can be estimated by the core structure and the PCB layout, as shown in Fig. 4.13. For the rectangular design case, the estimated MLT equation can be obtained as,

$$MLT = 2F + 2C + 2.82 \cdot \frac{E - F}{2} \tag{4.16}$$

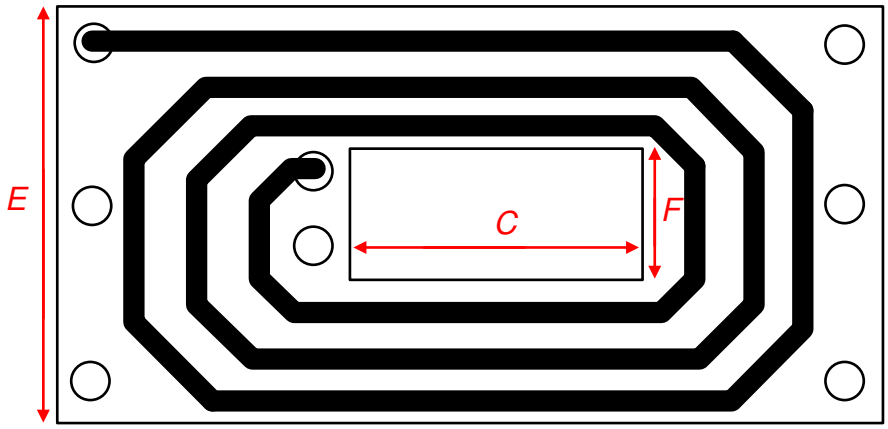


Fig. 4.13. The core structure and PCB layout relating to MLT.

A simulation result comparison has been made between the 2D and 3D model. The result shows that by using MLT in the 2D simulation, the error between 2D and 3D simulation is almost zero. Hence, 2D model is sufficient for the copper loss simulation. The paralleled winding current distribution and copper losses for the 12:2 planar transformer with different layer arrangements are shown in Fig. 4.14. Note that the excitation currents in the simulation are all pure sinusoidal. The copper loss will become larger if the excitation current is not pure sinusoidal, due to the higher-order harmonic currents.

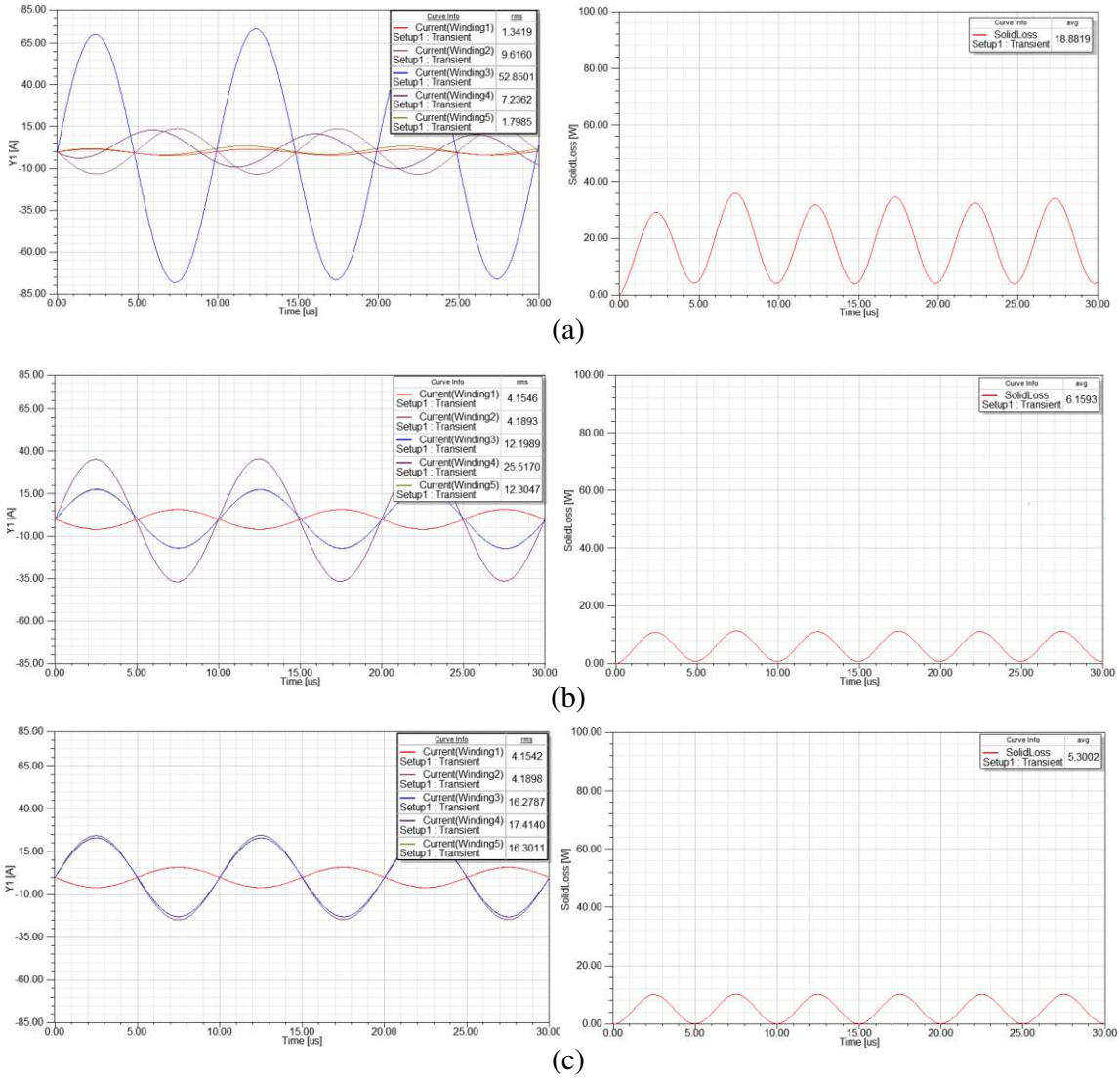


Fig. 4.14. The 12:2 transformer winding current distribution and copper loss. (a) Non-interleaving. (b) Half-interleaving. (c) Full-interleaving.

Based on the copper loss simulation and core loss calculation, the efficiency drop for the desired planar transformer is shown in Fig. 4.15. Therefore, the 1.2 kW planar transformer will yield around 16 W power loss in total. In other words, the efficiency drop from the transformer would be around 1.33%.

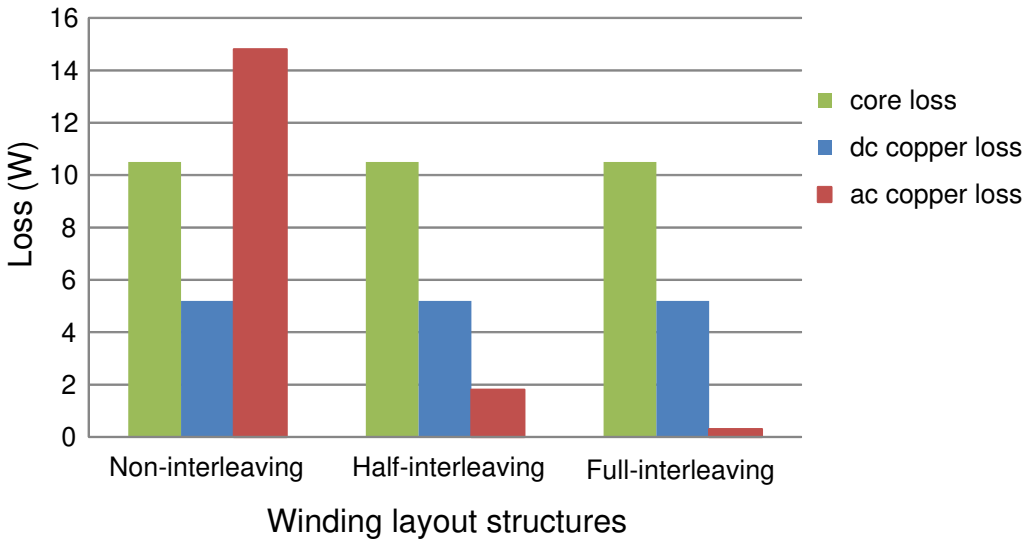


Fig. 4.15. The 1.2 kW 12:2 planar transformer loss distributions.

4.6 LEAKAGE INDUCTANCE

Not all the magnetic flux generated by ac current excitation on the primary windings follows the magnetic circuit and links with the secondary windings. The flux linkage between the two windings or parts of the same winding is never complete. Some flux will leak from the core and return to the air, winding layers, and insulator layers. These flux yields imperfect coupling and this partial coupling of the flux results in leakage inductance. As a parasitic element exists in transformers, the leakage inductance causes the main switch current at the device input to vary at a low slope between zero the rated value. In addition, the stored energy in the leakage inductance leads to a generation of voltage spikes on the main switch, which brings the electromagnetic interference (EMI) problems, increases the switching losses and

lowers the efficiency [115]. Depends on the application, some converters prefer a transformer with a minimized leakage inductance, while some prefer a transformer with a high leakage inductance, such as the soft-switching dc/dc converter. Sufficient inductive energy supplied from the leakage inductor is needed to fully charge and discharge the capacitor from the switches and transformer in order to turn on the switch in ZVS. One way to increase the leakage inductance is to add a small auxiliary inductor in series; another way is inserting a magnetic shunt with low permeability between the primary and the secondary inside the transformer [130-131].

The planar magnetic has not intrinsically a low leakage inductance, but planar magnetic is easier to obtain low leakage inductance than conventional wire-wound one. This is because the winding of the planar magnetic is easier to be arranged in interleaving structure. The interleaved windings reduce the MMF and thus lower the leakage inductance. Hence, for some converter applications with low leakage inductance requirement, the interleaving winding arrangement is a must.

If the objective is to minimize the leakage inductance further, one way is to reduce the number of turns. However, as discussed in the DAB turn ratio selection section, the voltage ratio between the input voltage and output voltage for this application is relatively high. Hence, the transformer turn ratio has to be made large. Another method is to decrease the MLT and/or increase the width of conductors. However, these parameters are mostly dependent on the core structure, while the core structure is selected mainly by the power, flux density and switching frequency.

Besides those, the other parameters can minimize the leakage inductance is the reduction of the thicknesses of conductors and insulators.

The leakage inductance calculation for the planar transformers can be found in [131]. As a fully interleaved layout is applied to the planar transformer, the transformer leakage inductance L_s can be estimated as [115, 120]:

$$L_s = \mu_o \cdot \frac{l_w}{b_w} \cdot 4\left(\frac{2h}{3} + h_\Delta\right) \tag{4.17}$$

where l_w is the length of each turn, b_w is the width of each turn, h is the copper thickness, and h_Δ is the height of the insulation between the layers. Hence, after the determination of the core shape, number of turns, length of each turn and width of conductors, a relation among the transformer leakage inductance, insulation layer and copper thickness can be drawn as shown in Fig. 4.16.

The restraints on the insulation layer are the dielectric strength and the manufacture capability. Safety standards like IEC 950 require a distance of 400 µm for main insulation between primary and secondary windings [128]. However, according to the standard IPC2221, the dielectric strength of the FR4 material is 39.4 kV/mm [116, 132]. Therefore, 300 µm insulation layer thickness is selected in this paper and it is sufficient to withstand 11 kV isolation. For the copper thickness, instead to have a thick copper layout design, we can apply paralleling winding for the transformer structure. This yields thinner copper thickness, which the leakage inductance can be minimized. Therefore, instead of a 1.83 kg/m^2 (3 oz/ft^2) copper design, we can parallel two windings for the primary and seven windings for the

secondary with 0.915 kg/m^2 (3 oz/ft^2) copper thickness for the DAB converter's transformer.

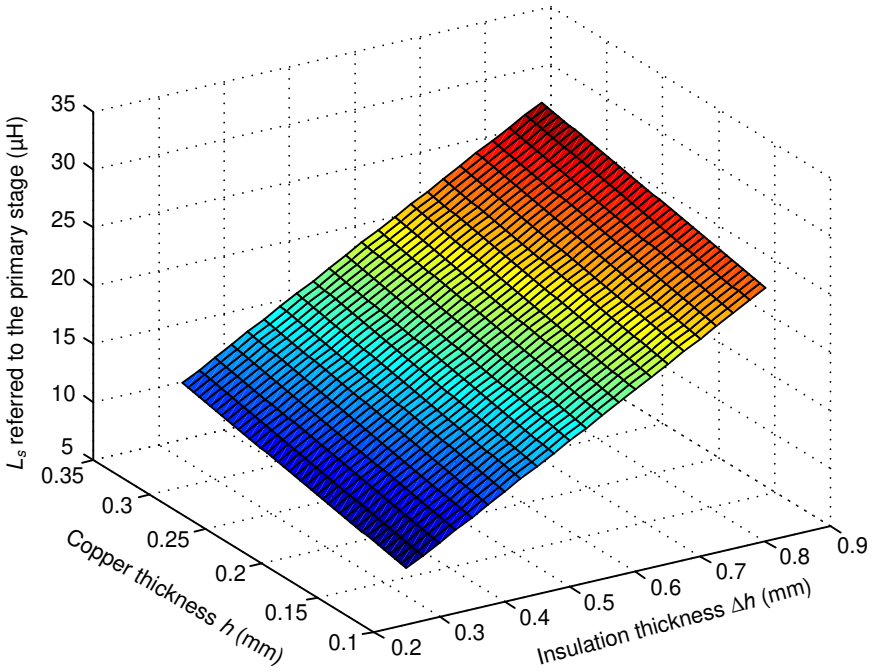


Fig. 4.16. The relation among the inductance L_s referred to the primary stage, copper thickness and insulation thickness.

The planar transformer layer arrangement and its MMF diagram along a vertical direction are shown in Fig. 4.17. Note that the required DAB transformer is a center-tapped one. The red and orange blocks indicate the two primary windings. The green blocks indicate the secondary winding. This structure will not only meet the current density requirement, but also minimize the leakage inductance of the transformer. By equation (4.17), the calculated leakage inductance is 31.5 nH referred to the secondary stage and 12.6 μH referred to the primary stage.

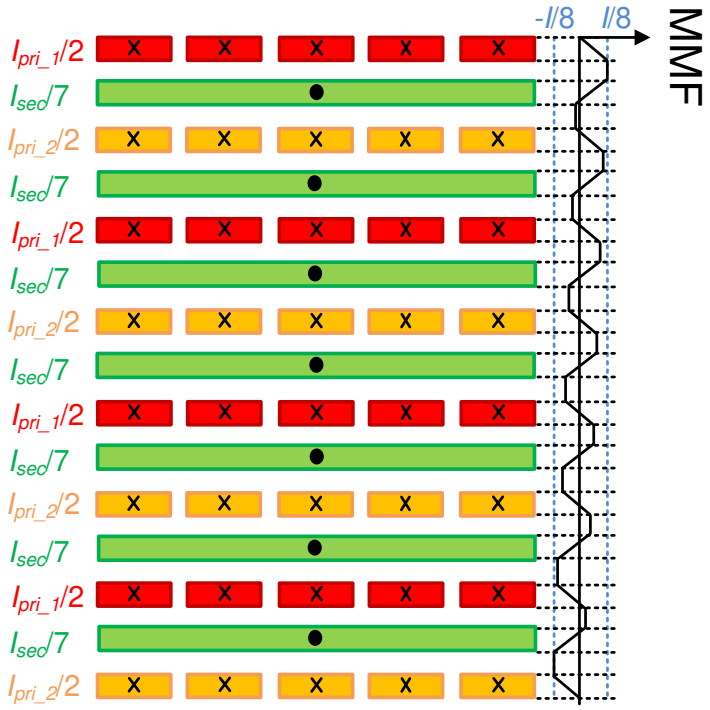


Fig. 4.17. The 20:1 center-tapped planar transformer full interleaved parallel layer arrangement and its MMF diagram.

A 2D model for this transformer is also built in the ANSYS Maxwell. The insulation is 0.3 mm and the copper thickness is 0.107 mm. In the simulation, the parallel current is assigned to each paralleled winding for excitation. The parallel current assigned to the primary and secondary windings are 3 A and 60 A, respectively. The current distribution is shown in Fig. 4.18.

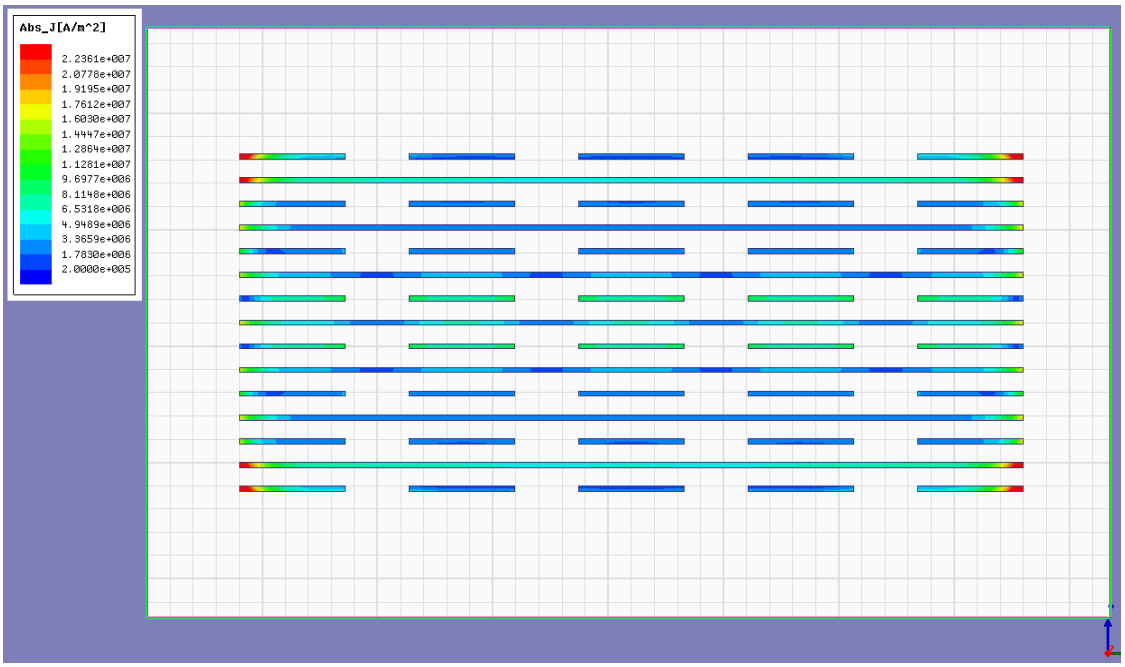


Fig. 4.18. Current density in the 20:1 center-tapped full-interleaved transformer.

4.7 IMPLEMENTATIONS

In this thesis, two planar transformers are built. One is 12:2 transformer for the full bridge current doubler converter. The other is 20:1 center-tapped transformer for the DAB converter. The PCB layout of the 12:2 planar transformer is shown in Fig. 4.19. The PCB is cut out and stacked up together. The finished 1.2 kW 12:2 planar transformer is shown in Fig. 4.20.

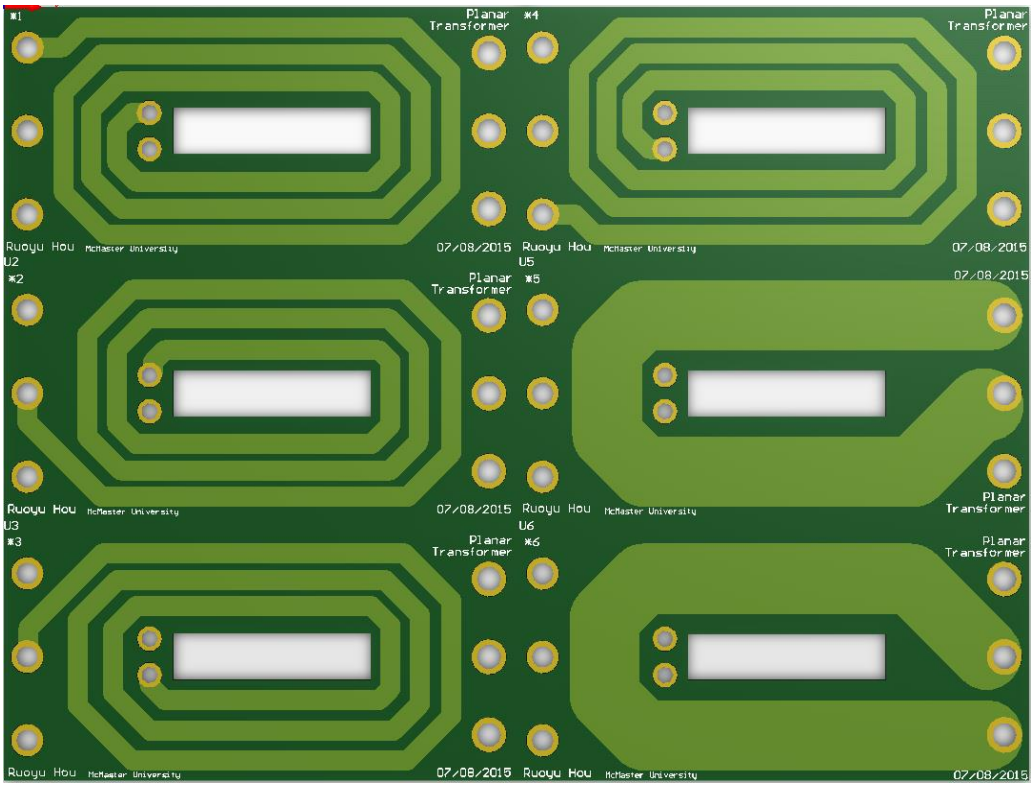


Fig. 4.19. PCB layout of the 12:2 planar transformer.

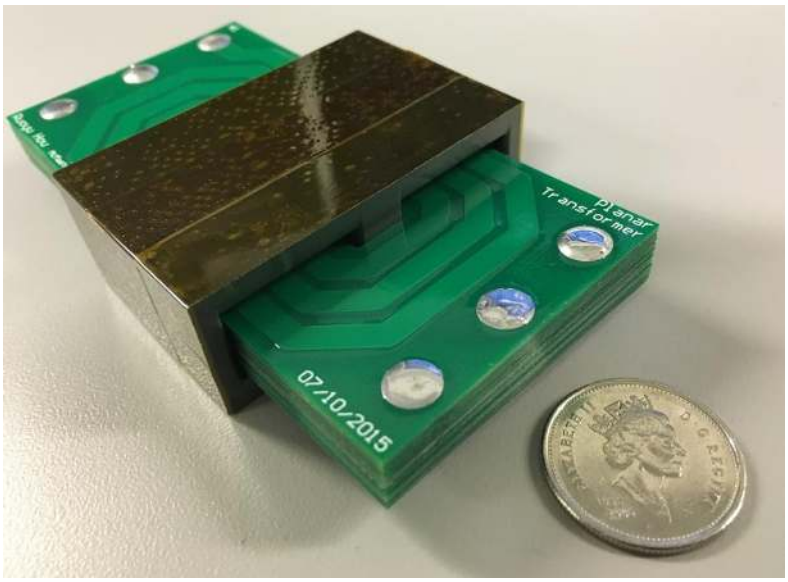


Fig. 4.20. The 1.2 kW 12:2 planar transformer prototype.

The 20:1 center-tapped planar transformer is also built as shown in Fig. 4.21. The measured L_m is 4 mH and measured L_s is 41.5 nH referred to the secondary stage and 16.6 μH referred to the primary stage.

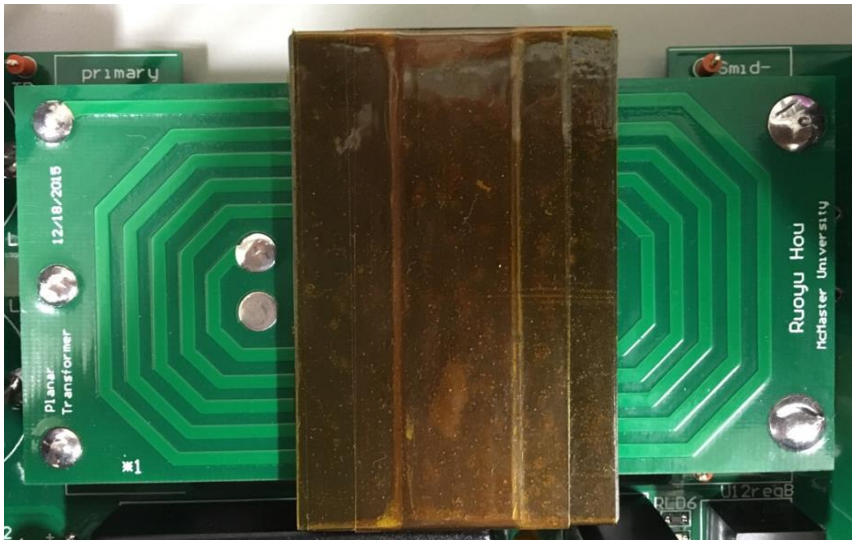


Fig. 4.21. The 20:1 center-tapped planar transformer prototype.

4.8 CONCLUSIONS

In this chapter, two planar transformers designed for two converter topologies. A 1.2 kW 12:2 planar transformer is designed for the full bridge current doubler. The detailed losses are analyzed. 2D and 3D simulation are built in ANSYS/Maxwell. Analysis and simulation results show that the efficiency drop from the transformer is around 1.33% for the 1.2 kW converter. The effects of interleaving winding structure on the current distribution and copper loss are observed from the simulation. A 20:1 center-tapped transformer is also built. Another target of this transformer is to minimize its

leakage inductance for the DAB converter. The built transformer leakage inductance is 41.5 nH referred to the secondary stage. These two transformers will be applied to the AFAPM converter prototypes, which will be presented in the next chapter.

Chapter 5

INTEGRATED ACTIVE FILTER AUXILIARY POWER MODULE CONVERTERS

5.1 Introduction

Chapter 3 explores and evaluates the proposed integrated AFAPM concept in electrified vehicle applications. The AFAPM converter is a HV AF for HV battery charger when the vehicle at charging station and is connected to the grid; it is a LV battery charger when the vehicle is running. By applying this method, the significant second-order harmonic current on the dc-link of single-phase HV battery charger can be assimilated by the AFAPM converter.

In this chapter, three different integrated AFAPM converters are proposed. The first is an integrated AFAPM converter that stores the HV second-order harmonic energy in the primary stage of the proposed converter. It needs a relay to switch between the two modes. The second one is a DAB-based full-integrated AFAPM converter that stores the HV harmonic energy into the secondary stage of the proposed converter. The last one is the primary full-integrated AFAPM converter that still stores the HV harmonic energy on the primary stage. The converter topology, control and design considerations for each converter are presented in this chapter.

5.2 Integrated AFAPM converter

5.2.1 Integrated AFAPM converter topology

The topological evaluation of different APM converters can be found in the Chapter 1. The full bridge with current doubler, the dual active bridge, and the full bridge with center tapped rectifier can be applied as part of the integrated AFAPM topology to achieve the LV battery charging function. In the meanwhile, Many different types of AFs have already been developed and a lot of studies have been conducted to compare them from different aspects [40, 44, 47, 48, 110]. The voltage source shunt AF, the bidirectional buck or boost converter can be part of the integrated AFAPM topology to fulfill the active filtering function for the mitigation of the second-order harmonic current in the HV battery charger. Relays can be applied to ensure the integrated AFAPM working properly in either filtering mode or charging mode.

An integrated AFAPM topology is proposed in this section as shown in Fig. 5.1. It is a dual-mode converter: AF mode and APM mode. As the objective is to propose an integrated AFAPM converter, the HV battery charging system is simplified to a single-phase PFC converter. In fact, this method is applicable to other single-stage chargers or other two-stage HV battery chargers containing the low frequency sinusoidal harmonic current, like the topologies proposed in [41, 42, 46], etc.

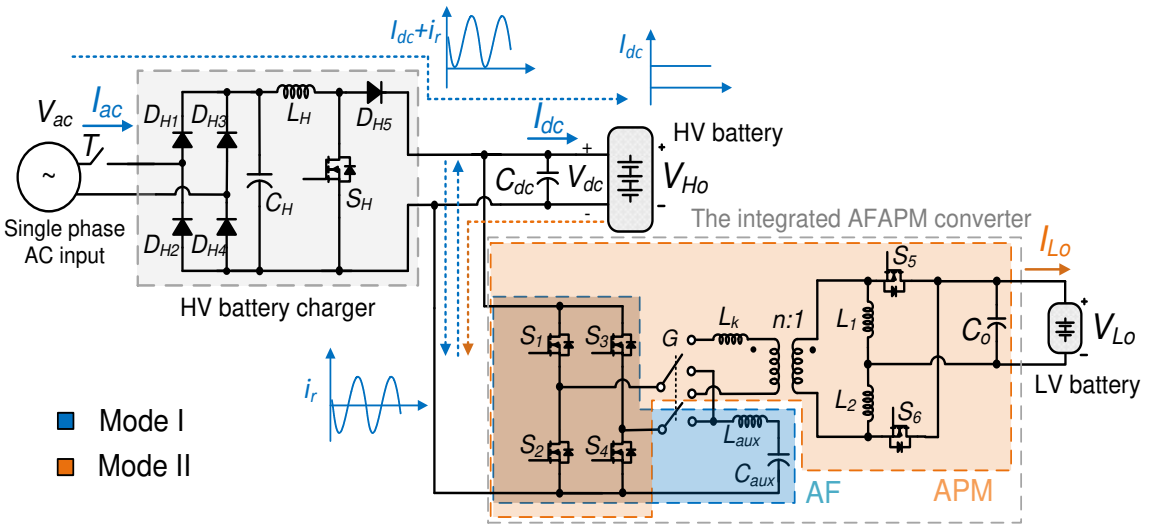


Fig. 5.1. Proposed integrated AFAPM-based dual voltage charging system.

The APM part is formed by a phase-shift full bridge with current doubler, due to its robustness, simplicity, easy to achieve ZVS, and better performance for the low-voltage high-current applications. By adding with an inductor L_{aux} and a capacitor C_{aux}, the primary stage composes a bidirectional buck converter with two bridges in parallel to store the second-order harmonic energy. Since it has been proved that capacitor has better energy storage capability than inductor, L_{aux} is used only to transfer the harmonic energy and C_{aux} is used to store the harmonic energy [40]. In other words, the bidirectional buck-boost converter will always work in the discontinuous conduction mode (DCM). By connecting the two bridges in parallel, the compensation current are shared. With the corresponding relatively small RMS current rating for the primary switches, WBG device such as SiC can be applied. Relatively high switching frequency can be applied to the converter with SiC MSOFETs and thus, the size of the AF's inductor can be reduced as well. The relay G is applied so that when the HV battery is charging, G is turned to the

AF mode and once the LV battery is charging, *G* is turned to the APM mode. Hence, compared to the conventional individual AF circuit, no extra power switches, gate drivers, and heat sinks are required to achieve the active filtering function. Note that in the system, there is still a need to apply a small film capacitor C_{dc} on the dc-link of the HV battery charger to filter high-frequency harmonics during the AF mode and also to work as the input capacitor for the LV battery charger during the APM mode.

5.2.2 Control strategy of the integrated AFAPM

The integrated AFAPM control strategy can be mainly divided into two modes. Mode I is the HV active filtering mode. Mode II is the LV battery charging mode.

A. Mode I, HV active filtering mode

When the vehicle at the charging station and the HV battery is charging, the converter is operating as an AF. From equation (3.16), it is clear that the amplitude of the ripple current i_r is equal to the dc component I_{dc}. The feed-forward digital control method is applied on this converter. The switch S_1 and S_3 operate with the same duty cycle and share the current in the buck mode. Same as to the switch S_2 and S_4, they operate with the same duty cycle in the boost mode. The switching operating diagram of the integrated AFAPM in AF mode is shown in Fig. 5.2.

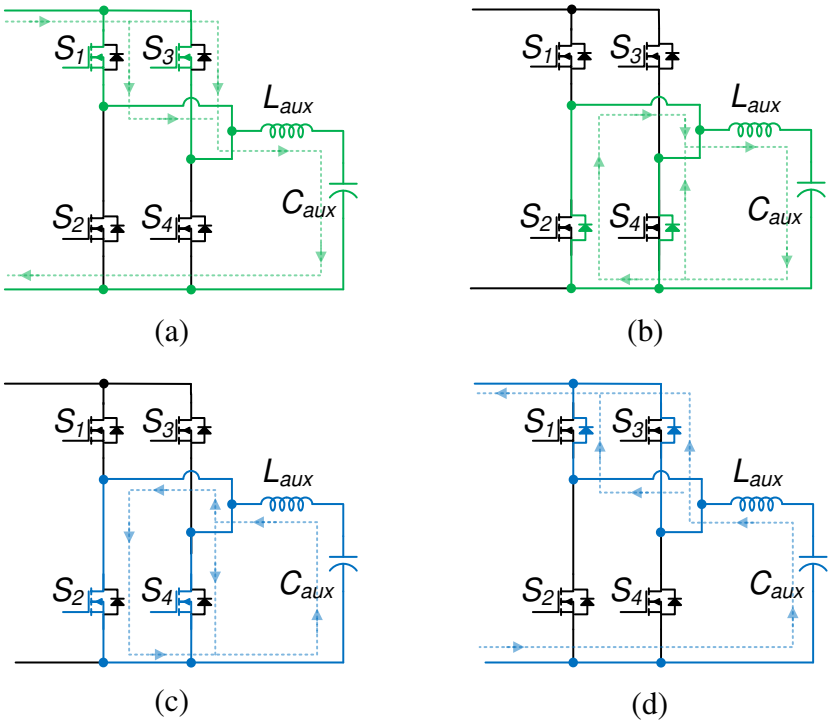


Fig. 5.2. Switching operating diagram of the integrated AFAPM in AF mode. (a) Buck mode, inductor current rising. (b) Buck mode, inductor current falling. (c) Boost mode, inductor current rising. (d) Boost mode, inductor current falling.

The duty cycle is calculated directly according to the corresponding system variables. In the chapter 3, the duty cycles for buck mode and boost mode have been derived as,

$$D_\alpha = \sqrt{\frac{2 \cdot i_r \cdot f_s \cdot L_{aux}}{V_{dc} - V_{c\_aux}}} \tag{5.1}$$

$$D_\beta = \sqrt{\frac{2 \cdot i_r \cdot (V_{dc} - V_{aux}) \cdot f_s \cdot L_{aux}}{V_{c\_aux}^2}} \tag{5.2}$$

In order to investigate the integration feasibility, it is critical to calculate the switch RMS current rating for both modes. For the proposed integrated AFAPM converter in this section, as both bridges are applied in parallel to form the AF during active filtering period, the RMS current can be divided by two. From the inductor current waveforms shown in the Fig. 3.9, the switch RMS current during the buck mode can be calculated based on the shaded triangular area *A1*,

$$I_{s\_AF,rms} = \frac{\sqrt{\frac{1}{T_s}\int_0^{t_1}\left(\frac{v_{dc} - v_{c\_aux}}{L_{aux}}\right)^2 t^2 dt}}{2} = \left(\frac{v_{dc} - v_{c\_aux}}{2L_{aux}f_s}\right)\sqrt{\frac{D_\alpha^3}{3}} \tag{5.3}$$

Accordingly, the RMS current in the diode during the buck mode can be calculated based on the triangular area *A2*,

$$I_{d\_AF,rms} = \frac{\sqrt{\frac{1}{T_s}\int_{t_1}^{t_2}\left(\frac{v_{c\_aux}}{L_{aux}}\right)^2 t^2 dt}}{2} = \left(\frac{v_{dc} - v_{c\_aux}}{2L_{aux}f_s}\right)\sqrt{\frac{\left(\frac{v_{dc} - v_{c\_aux}}{v_{c\_aux}}\right)D_\alpha^3}{3}} \tag{5.4}$$

With the same calculation procedure, the RMS current for the switches and diode can be calculated in the boost mode, whose corresponding areas are the same as in the buck mode.

B. Mode II, LV battery charging mode

When the HV battery stops charging and the vehicle is running, the HV battery pack starts to charge the LV battery thru AFAPM, which now works as a general full bridge current doubler. The control-driven SR control is applied on the S_5 and S_6. The desired gate drive signals are derived from the primary-stage pulse-width modulation (PWM) controller.

The overall dual-mode control diagram for the proposed AFAPM is shown in Fig. 5.3. In the AF mode, to prevent the overcharging of the output capacitor, another voltage loop is used to control the average value of the capacitor voltage, where a low pass filter is applied.

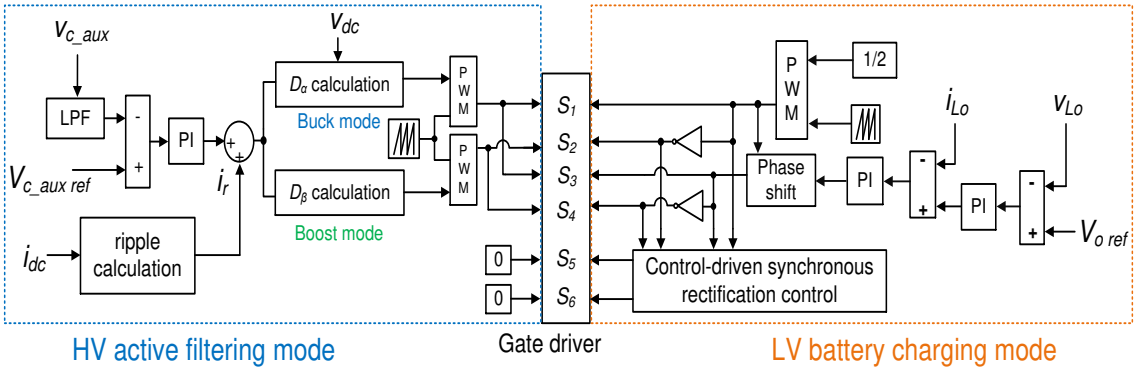


Fig. 5.3. Overall dual-mode control diagram of the proposed integrated AFAPM converter.

5.2.3 Design considerations of the integrated AFAPM

The switch voltage and current stress for the full bridge current doubler converter in the LV battery charging mode has been presented in the chapter 2. The design

considerations of the passive components for the full bridge current doubler are also discussed in the chapter 4. The HV active filtering components requirements will be discussed as follows.

A. HV active filtering components requirements

In order to make sure the circuit always work at DCM as well as limit the peak current under the saturation current rating for the inductor L_{aux}, the inductance L_{aux} needs to be calculated and selected based on two constrains, which are the DCM limit and peak current limit.

For the DCM limit, the inductance range can be calculated by,

$$\begin{cases} \dfrac{1}{2}(T_1+T_2)\dfrac{(V_{dc}-V_{c\_aux})}{L_{aux}}T_1 = I_{aux}\cdot T_s \\ T_2 = \dfrac{T_1(V_{dc}-V_{c\_aux})}{V_{aux}} \\ T_1+T_2 \le T_s \end{cases} \tag{5.5}$$

where I_{aux} is the average current in the capacitor C_{aux} within one switching cycle. Therefore,

$$L_{aux} \le \frac{T_s}{2\times I_{aux}}\cdot\frac{(V_{dc}-V_{c\_aux})V_{c\_aux}}{V_{dc}} \tag{5.6}$$

For the peak current limit,

$$\begin{cases} \frac{1}{2}(T_1 + T_2)\frac{(V_{dc} - V_{c\_aux})}{L_{aux}}T_1 = I_{aux} \cdot T_s \\ T_2 = \frac{T_1(V_{dc} - V_{c\_aux})}{V_{c\_aux}} \\ \frac{(V_{dc} - V_{c\_aux})}{L_{aux}}T_1 \leq I_{peak} \end{cases} \tag{5.7}$$

Therefore,

$$L_{aux} \geq \frac{2 \cdot I_{aux} \cdot T_s}{{I_{peak}}^2} \cdot \frac{(V_{dc} - V_{c\_aux})V_{c\_aux}}{V_{dc}} \tag{5.8}$$

Based on equations (5.6) and (5.8), if HV dc-link voltage V_{dc} is set to 400 V, the peak capacitor's voltage is set as 350 V, and the peak inductor current requirement I_{peak} is set to 60 A, a relation between inductance and switching frequency can be drawn in Fig. 5.4.

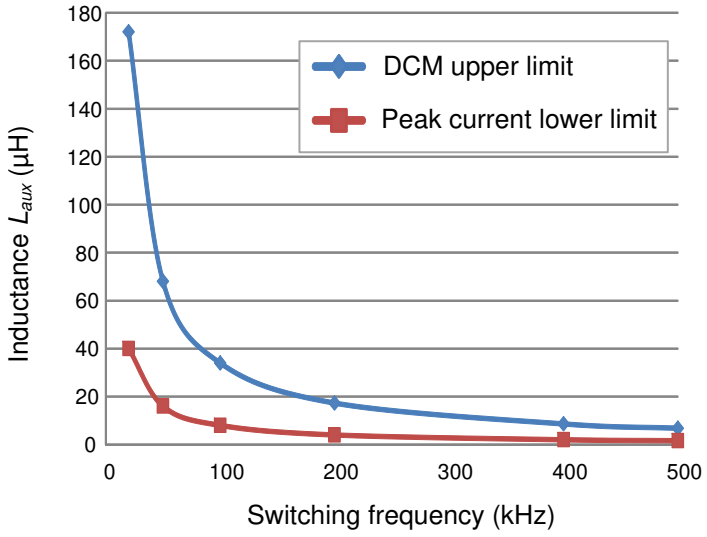


Fig. 5.4. Relation between inductance L_{aux} limits and switching frequency.

It is clear with higher switching frequency, the required inductance will be lower and thus, the size of the inductor can be reduced. In this thesis, L_{aux} is selected as 15 μH at 100 kHz.

As the inductor L_{aux} is used to transfer all the energy only, the capacitor C_{aux} needs to be able to store all the second-order harmonic energy from the HV battery charger dc-link. The energy stored in the capacitor is,

$$E_r = \frac{1}{2} C V_c^2 \tag{5.9}$$

The harmonic power P_{Hr} goes to the capacitor can be rewritten as,

$$P_{Hr} = P_{Ho} sin2\omega t = \frac{1}{2} C_{aux} \frac{dV_{c\_aux}^2}{dt} \tag{5.10}$$

where P_{Ho} is 6.6 kW in this case. Solving the differential equation, we can obtain the capacitor voltage V_{c_aux} as,

$$V_{c\_aux} = \sqrt{V_{c\_peak}^2 - \frac{P_{Ho}}{\omega C_{aux}} (1 + \cos 2\omega t)} \tag{5.11}$$

It is obvious that the capacitor voltage is dependent on the HV dc output power P_{Ho}, the capacitance C_{aux}, the line frequency ω, and the peak voltage V_{c_peak}. If all the harmonic energy needs to be stored in the capacitor, the peak voltage V_{c_peak} and the capacitance C_{aux} need to satisfy following requirement,

$$C_{aux} \geq \frac{2P_{Ho}}{\omega V_{c\_peak}^2} \tag{5.12}$$

Hence, with different peak voltage conditions, diverse capacitance requirements can be made shown in Fig. 5.5.

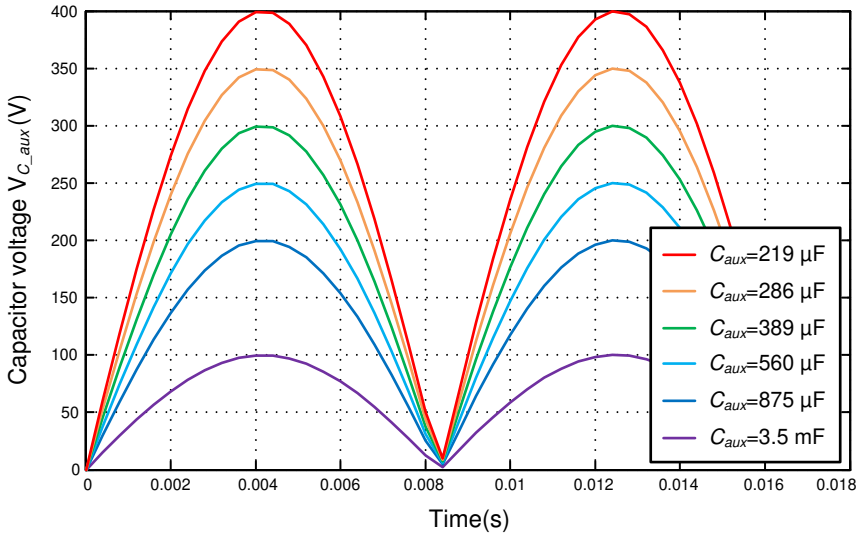


Fig. 5.5. Minimum active energy storage capacitance C_{aux} requirements at different peak voltages for 6.6 kW HV battery charger.

As the AF circuit is a buck converter, the auxiliary capacitor's voltage V_{c_aux} will always be lower than the dc-link voltage V_{dc}. In addition, from Fig. 5.5 we can see that with higher peak voltage, the required capacitance is smaller. Hence, the most desired peak voltage range is somewhere between 300 V to 400 V. In this section, 350 V is set as the peak voltage.

B. Integrated AFAPM components requirements

Based on equations (2.21), (5.3) and (5.4), the RMS current on the primary switches can be calculated for the LV APM and HV AF with different power levels. A relation between APM, AF power level and their corresponding primary switch RMS current rating can be drawn in Fig. 5.6. Clearly, if a conventional individual AF circuit is applied for the HV battery charger, the RMS current rating can reach up to 33 A for 6.6 kW HV battery charger. While if we integrate and use the full bridge as two bridges in parallel, the primary switch RMS current ratings for the 2.4 kW LV APM and 6.6 kW HV AF are almost kept unchanged. The RMS current requirement for 6.6 kW HV AF is around 16.5 A, which is slightly higher than the RMS current for the 2.4 kW APM.

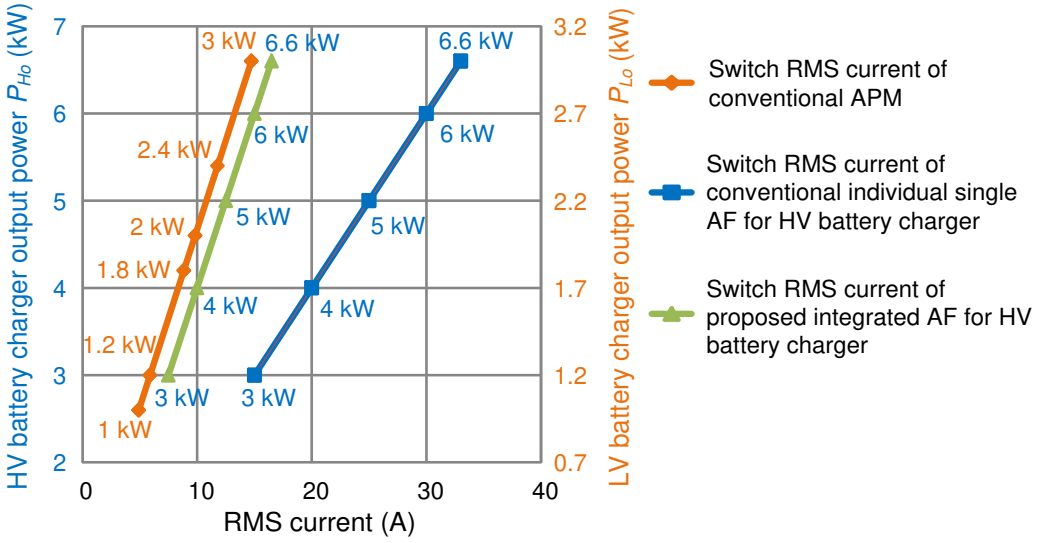


Fig. 5.6. Relation between different APM, AF power levels and primary switch RMS current ratings.

At last, for the ideal case, the switch requirements of the integrated AFAPM converter can be summarized in Fig. 5.7. Clearly, the LV battery charger APM has 400 V high-voltage stress and low-current stress on the primary; and has low-voltage stress and high-current stress on the secondary. For the AF part, the voltage stress is also equal to 400 V. If the power level of the HV battery charger is 6.6 kW, then the current rating of the primary switches need to increase slightly to meet the AF demand.

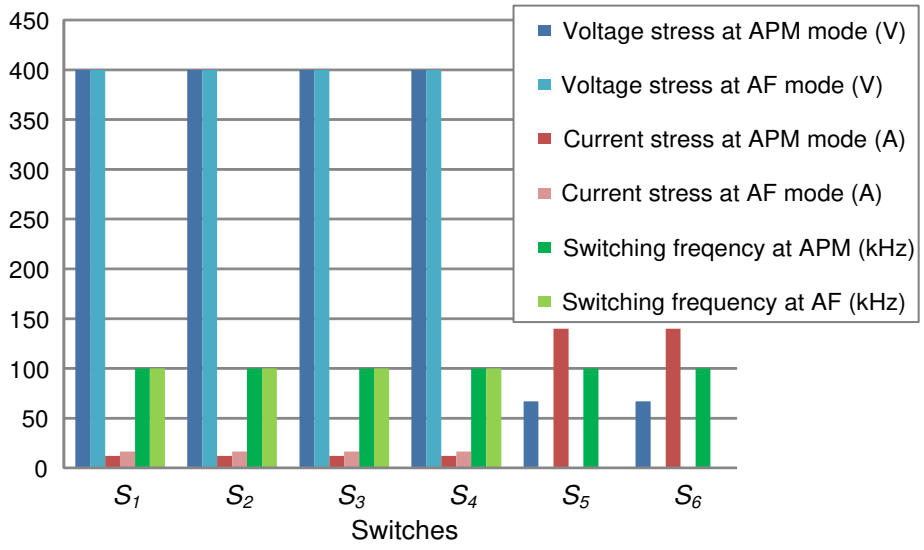


Fig. 5.7. Switch requirements of the integrated AFAPM converter for a 2.4 kW LV and 6.6 kW HV dual-voltage charging system.

With a traditional capacitor method, the dc-link capacitance calculation can be calculated from equation (3.17). For a conventional 6.6 kW HV battery charger, if the required peak-to-peak voltage ripple ΔV_{dc} is set to 10 V, then the corresponding required capacitance is around 4 mF. Therefore, a main components cost comparison can be made among the traditional capacitor method, conventional additional AF method and the

proposed integrated AFAPM method as shown in Fig. 5.8. As a result, from the harmonic energy storage aspect for the 6.6 kW HV battery charger in the vehicle applications, the cost of the conventional additional AF can decrease to 70.7% of the cost of traditional capacitor method. While with the proposed AFAPM, the cost can decrease further to 47.3% of the cost of traditional capacitor method and 66.8% of the cost of conventional extra AF method.

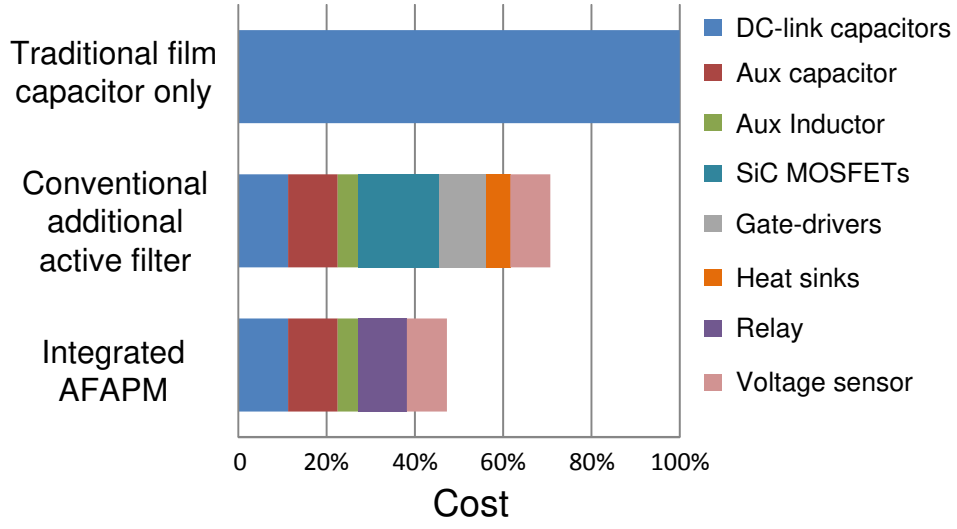


Fig. 5.8. A main components cost comparison of harmonic energy storage for 6.6 kW HV battery charger.

5.2.4 Simulation and implementation results

A. Simulation verification

A simulation is conducted in the MATLAB/Simulink. The simulation parameters' values are shown in the following Table 5.1. In order to simply the analysis in the simulation, all the parasitic inductance and parasitic capacitance are not included in the

simulation model. The on-state resistance and output capacitance of the switches are set based on the switch datasheets.

Table 5.1. Simulation parameters of the integrated AFAPM-based dual-voltage charging system.

Parameters	Value
HV battery charger output power P_{Ho}	6.6 kW
LV battery charger output power P_{Lo}	2.4 kW
Ac supply frequency f	60 Hz
Switching Frequency f_s	100 kHz
Transformer turn ratio n	12:2
Leakage inductance L_k	2.5 µH
Transformer magnetizing inductance L_m	1 mH
HV dc-link capacitance C_{dc}	300 µF
LV output capacitance C_o	14 mF
AF capacitance C_{aux}	300 µF
AF inductance L_{aux}	15 µH
Secondary inductance L_1, L_2	6 µH

Fig. 5.9 shows the simulation results of the integrated AFAPM working as a LV APM. The input voltage V_{Ho} is 250 V. The primary four switches are operating as a general phase-shift full bridge converter, and the output voltage V_{Lo} is controlled to 12 V for the LV load. The LV load resistance is set to 0.06 Ω and the output load current is 200 A. The currents of inductor L_1 and L_2 are inherently interleaved as the characteristics of current doubler.

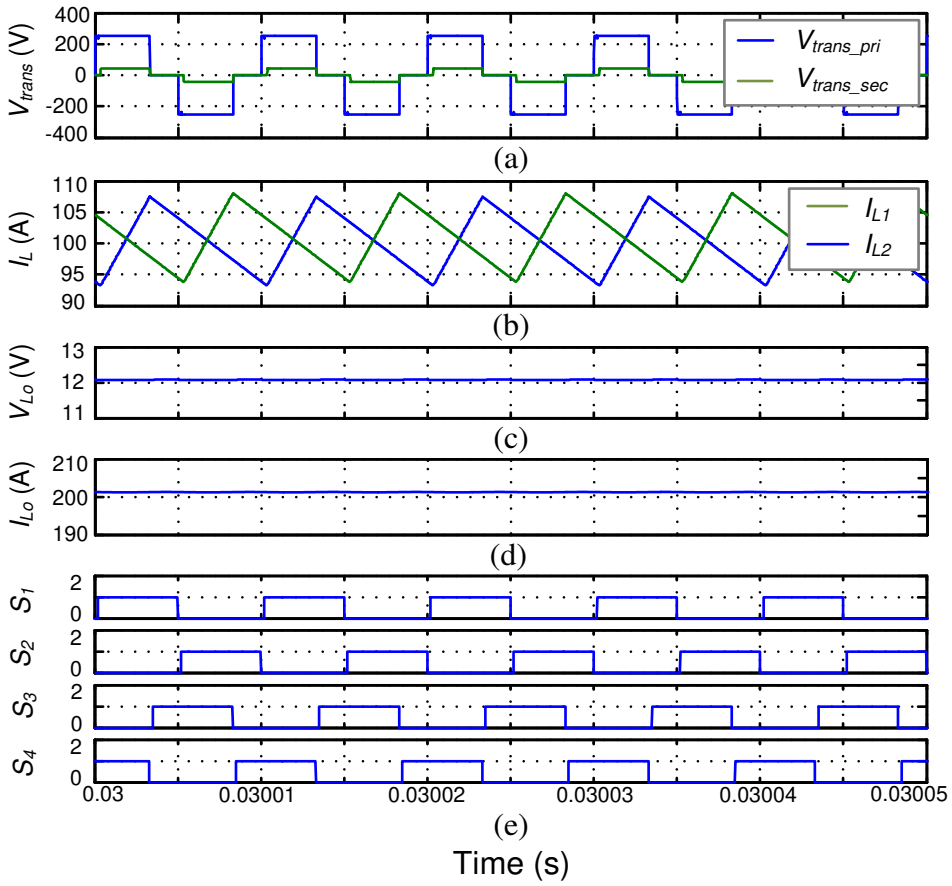


Fig. 5.9. Simulation results of the integrated AFAPM at APM mode. (a) Transformer voltage. (b) Inductor current I_L. (c) LV output voltage V_{Lo}. (d) LV output current I_{Lo}. (e) Duty cycle S_1-S_4.

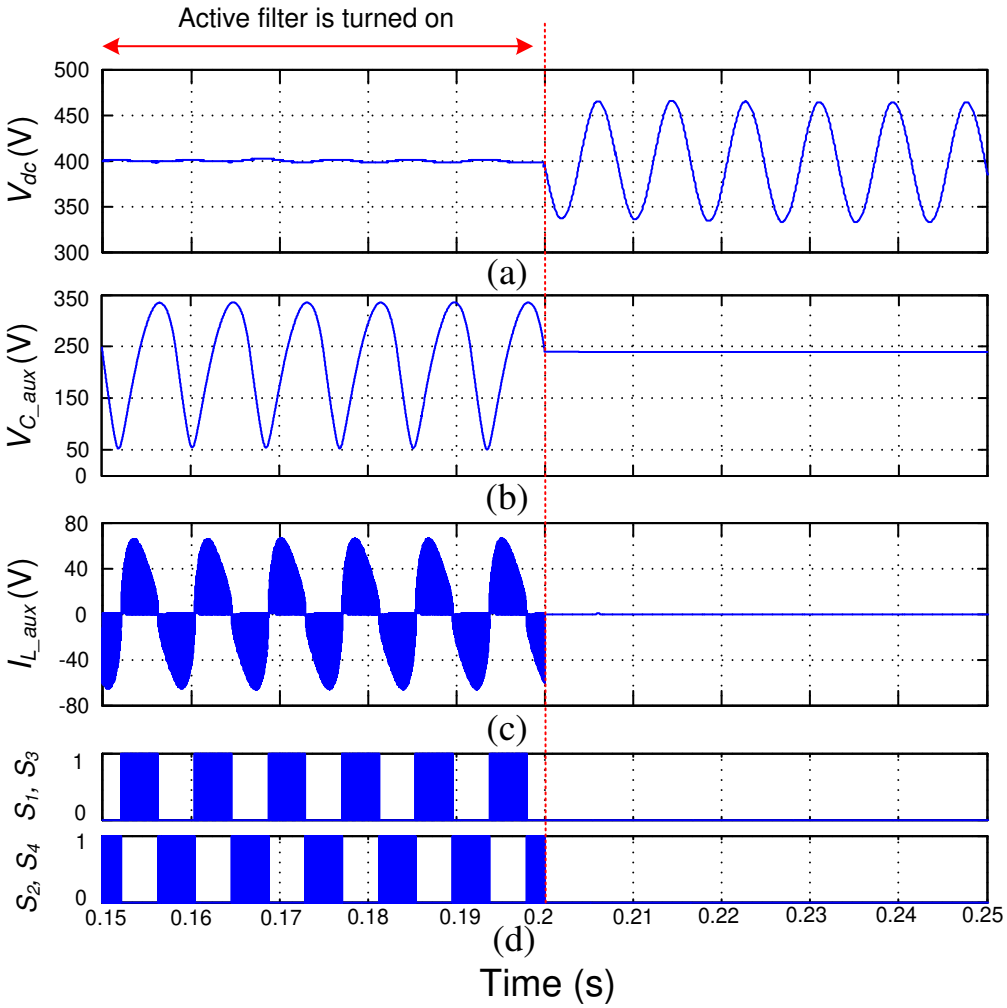


Fig. 5.10. Simulation results of the integrated AFAPM at AF mode. (a) HV output voltage V_{dc}. (b) Active capacitor voltage V_{C_aux}. (c) Active inductor current I_{L_aux}. (d) Duty cycle S_1-S_4.

Fig. 5.10 shows the simulation results of the integrated AFAPM working as an HV AF. Before 0.2 s, the AF is operating, and S_1 to S_4 are working with corresponding duty cycles. Under this condition, the dc bus voltage V_{dc} is 400 V with relatively small ripple. The second-order harmonic energy is stored in the C_{aux}. The capacitor's voltage

V_{c_aux} is fluctuated between 50 V to 340 V. The converter is operating at DCM mode and the peak current of its inductor L_{aux} is 60 A. After 0.2 s, all the switches are turned off and the large second-order harmonic current and its corresponding voltage ripple are back to the HV dc link.

B. Prototype design and test setup

A 1.2 kW 100 kHz proof-of-concept integrated AFAPM prototype has been built as shown in Fig. 5.11. It includes the main circuit and the driver circuits, but the DSP controller is not included in the picture. The rated output voltage and current on the LV side is 12 V and 100 A. The overall size of the prototype is 34 cm × 14 cm × 5 cm. The CREE's third-generation SiC MOSFET (C3M0065090D) is applied on the primary full bridge. On the secondary stage, as the current rating is relatively high, two Silicon MOSFETs (IRFP4568PBF) from Infineon Americas are connected in parallel for both S_5 and S_6. RCD snubbers are added to the SR in parallel to reduce the voltage spike and voltage oscillation on the switches [133].

The built 12:2 planar transformer is applied on this converter. The applied inductors L_1 and L_2 for the current doubler are 6 μH planar inductors from Standex Meder. The output capacitors C_o for the LV battery are 4×3300 μF electrolytic capacitors. The AF's L_{aux} is 10 μH and C_{aux} is a 22 μF film capacitor.

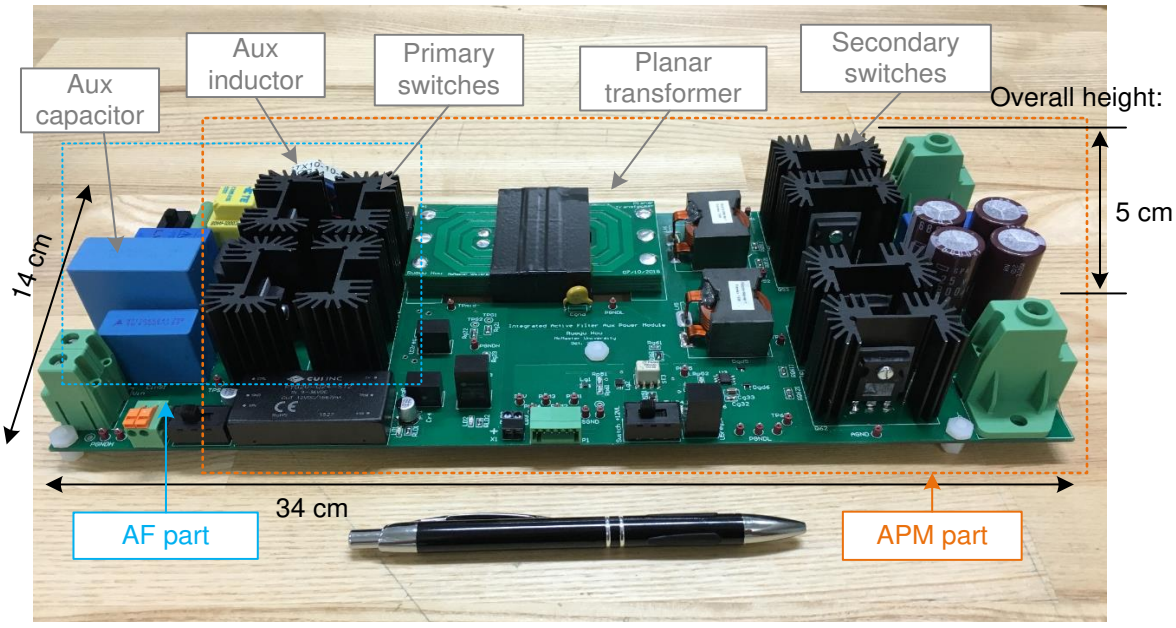


Fig. 5.11. 1.2 kW integrated AFAPM converter prototype.

In the testing, a 360 W PFC board UCC28180EVM-573 from Texas Instruments is applied as the current source for the active filtering. A 44 μF film capacitor C_{dc} is applied on the HV dc bus.

In the experiments, power for the LV battery charging mode is provided by an Ametek dc power supply QSGA330x45C and the load is a Kepco dc electronic load EL 5K-400-420. The overall control is implemented by a Texas Instrument DSP (TMS320F28335) with native floating-point support. The test setup is shown in Fig. 5.12. Test waveforms are recorded by an Agilent oscilloscope. The high-frequency ac current are recorded by a Rogowski current waveform transducer.

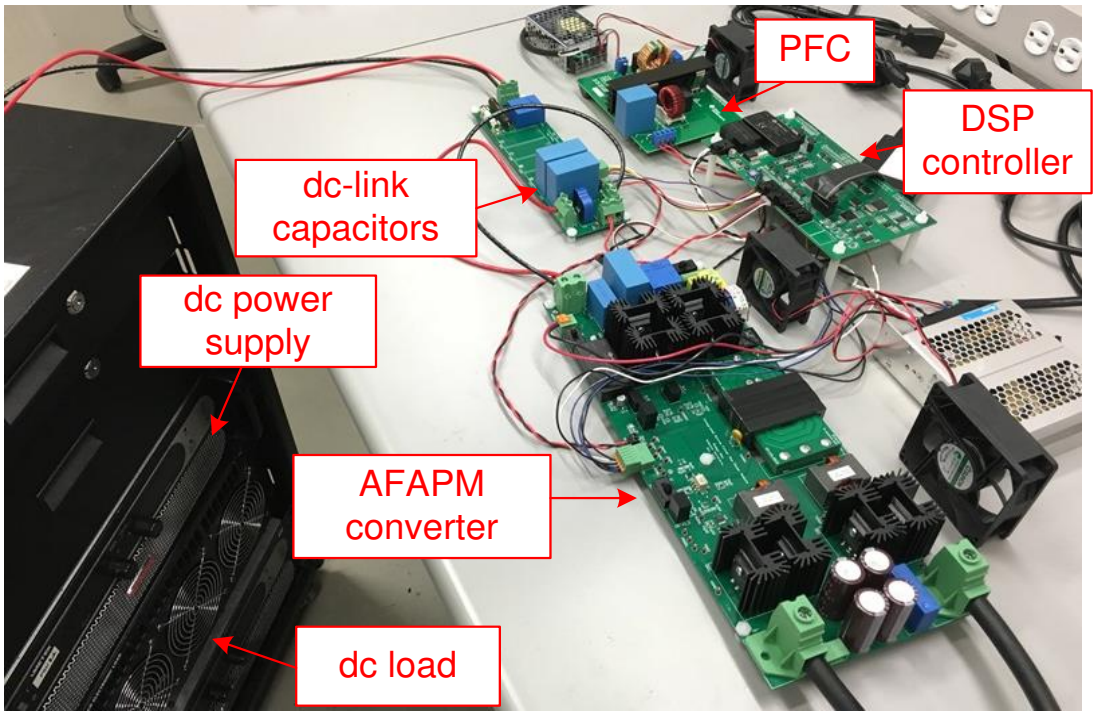
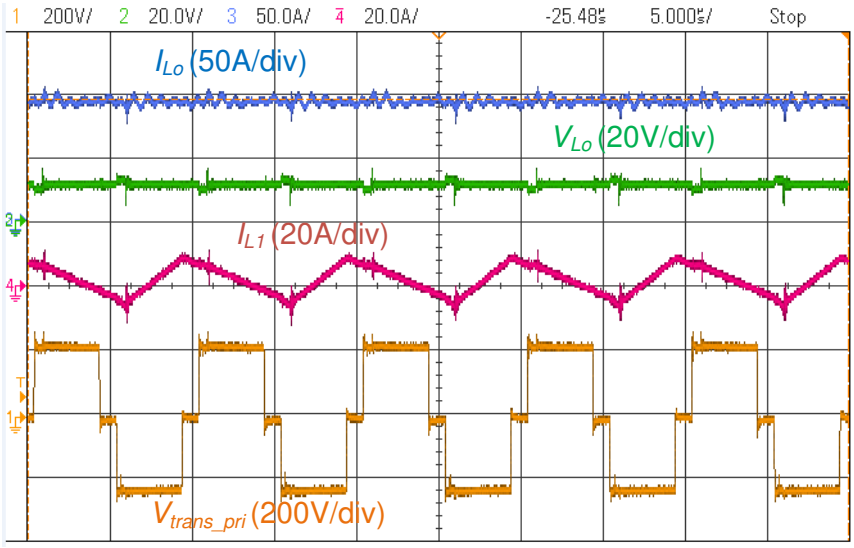


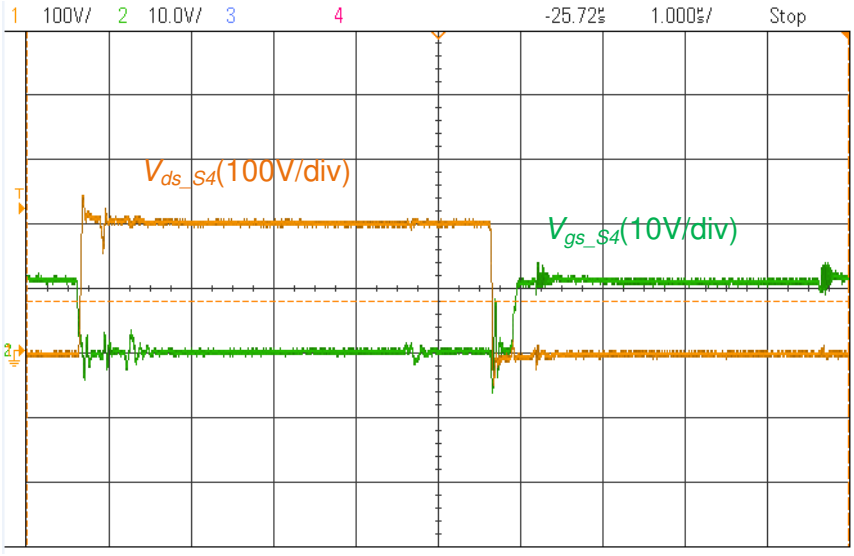
Fig. 5.12. AFAPM test setup.

C. *Experimental results*

Fig. 5.13 (a) shows the experimental waveforms of the LV battery charging mode, at the operating point where f_s = 100 kHz, V_{Ho} = 210 V, V_{Lo} = 12 V, and P_{Lo} = 1200 W. Fig. 5.13 (b) shows the experimental waveforms of drain-source voltage and gate-source voltage on the primary stage's lagging phase switch S_4. The switch S_4 is turned on after its drain-source voltage down to zero and thus, the turn-on ZVS is realized.



(a)

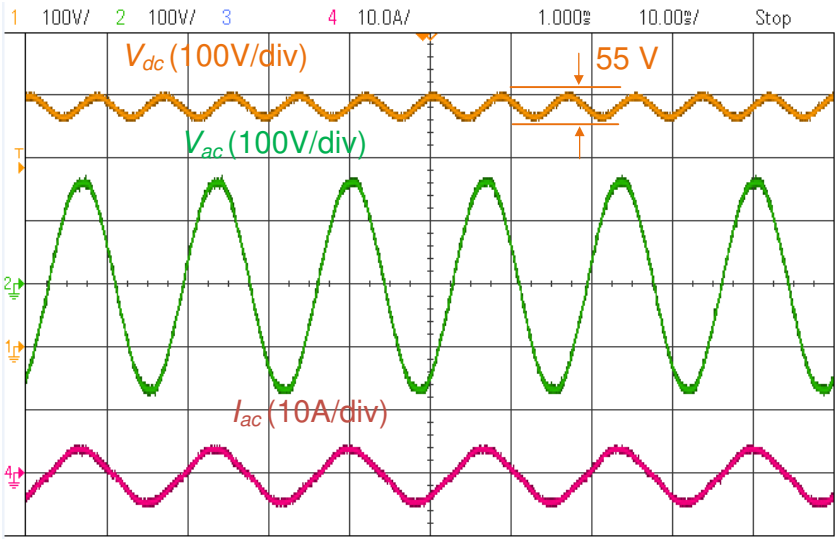


(b)

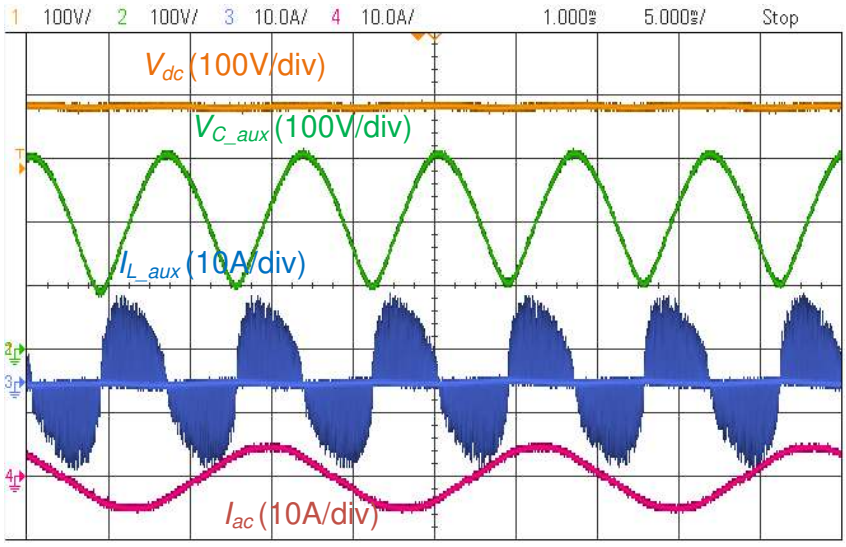
Fig. 5.13. (a) Experimental results of the LV battery charging APM mode operation. (b) Gate-to-source and drain-to-source voltage of S_4.

Fig. 5.14 is the experimental results of the AFAPM converter in AF mode. First of all, in order to present the active filtering effect of the AFAPM converter, Fig. 5.14 (a) can be used as a reference and it shows the experimental results for 360 W PFC without AF. The ac input line voltage V_{ac} is 120 V_{rms}, and its frequency is 60 Hz. The input current I_{ac} of the PFC is in phase with V_{ac}. The dc load is applied to sink the output power from the PFC. At that time, the second-order harmonic current and its voltage ripple are only filtered by 44 μF dc-link capacitors. Its dc-link voltage V_{dc} is fluctuated with a 55 V peak-to-peak.

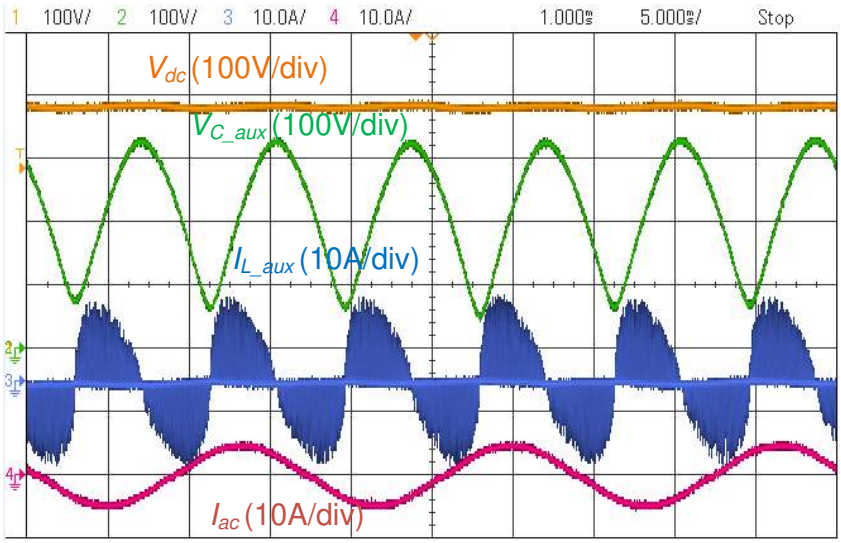
Fig. 5.14 (b) shows the experimental results with AF. In this case, the dc load is in the same condition. The AF's capacitor C_{aux} is 22 μF. The HV dc bus voltage V_{dc} is 380 V with relatively small voltage ripple and the AF capacitor's voltage V_{aux} is fluctuated between 90 V to 310 V. The AF inductor's peak current is 14 A. Fig. 5.14 (c) shows the experimental results for the AF mode with the C_{aux} = 17 μF. The HV dc bus voltage V_{dc} is still 380 V and the AF capacitor's voltage V_{c_aux} occurs a greater voltage swing which is fluctuated between 60 V to 340 V, as the capacitance C_{aux} is smaller than the former case. The AF inductor's peak current keeps the same which is still 14 A. Fig. 5.14 (d) is the zoomed experimental waveforms with C_{aux} = 17 μF. It is clear the AF is operating in the DCM mode.


1 100V/ 2 100V/ 3 4 10.0A/ 1.000ms 10.00ms/ Stop
V_{dc} (100V/div)
55 V
V_{ac} (100V/div)
I_{ac} (10A/div)

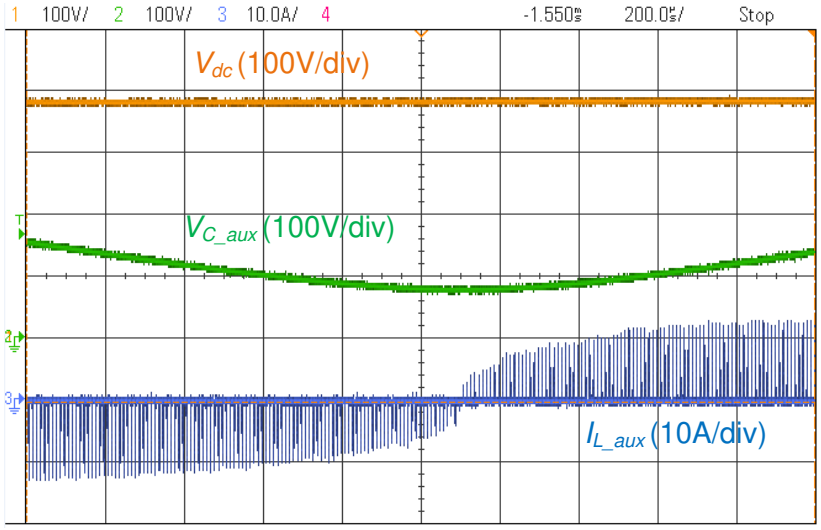
(a)


1 100V/ 2 100V/ 3 10.0A/ 4 10.0A/ 1.000ms 5.000ms/ Stop
V_{dc} (100V/div)
V_{C_aux} (100V/div)
I_{L_aux} (10A/div)
I_{ac} (10A/div)

(b)



(c)



(d)

Fig. 5.14. (a) Experimental results of the HV active filtering mode operation. (a) Without AFAPM. (b) With AFAPM (22 µF C_{aux}). (c) With AFAPM (17 µF C_{aux}). (d) Zoomed waveforms.

The measured efficiency for the integrated AFAPM during the HV AF mode is 97.8% at 360 W with 100 kHz switching frequency. The input and output voltages are fixed at 200 V and 12 V, respectively. The peak efficiency is 95.5% at 600 W. At 1.2 kW full load scenario, the converter efficiency is 90.4%. The SiC MOSFETs on the primary stage are also replaced by conventional Si MOSFETs with the same rating 900 V/36 A and same package TO-247-3. The two measured efficiency curves for the integrated AFAPM during the LV battery charging APM mode are shown in Fig. 5.15. By using SiC MOSFETs on the primary stage, in average a 1.2% point efficiency improvement over the Si-based was observed.

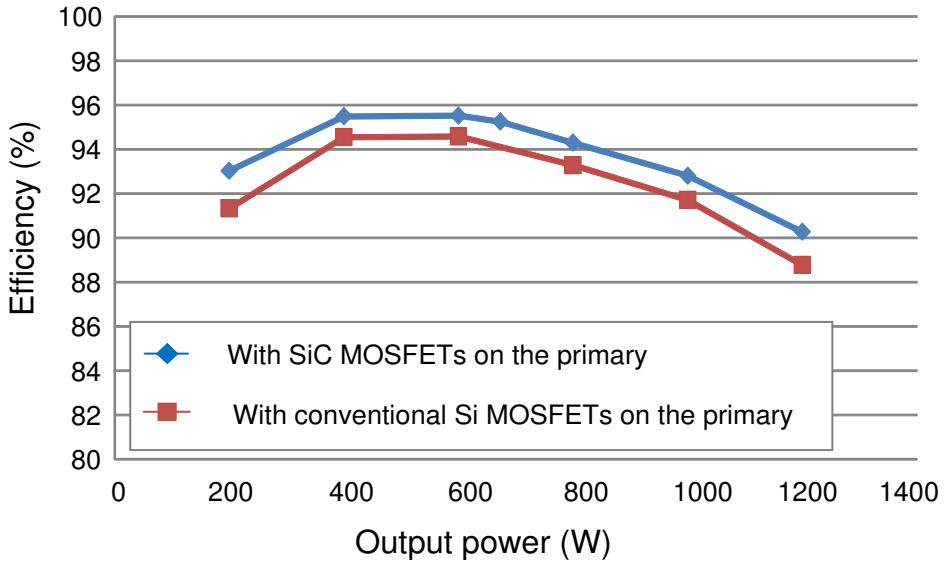


Fig. 5.15. Measured efficiency curves of the integrated AFAPM during APM mode.

The major barriers to further improve the converter efficiency are: 1) As the secondary stage of the converter needs to carry relatively high current, the conduction loss dominates during the heavy and full load conditions. Paralleling more switches on the secondary stage would be one solution to further improve the efficiency at heavy and full load scenarios. While, higher cost has to be taken into account. 2) RCD snubbers have to be applied on the secondary switches, as there are well-known significant voltage spikes on the current doubler circuit. The efficiency will be penalized by these snubbers. 3) Parasitic inductance in the circuit and also parasitic capacitance from the planar transformer will also impact the converter efficiency. A better planar transformer design will help improving the converter efficiency.

5.3 Full-integrated AFAPM converter

The first integrated AFAPM converter needs extra auxiliary inductor, capacitor and extra relay to achieve the HV AF function. It would be interesting to use the AFAPM's secondary output capacitor to store the HV second-order harmonic energy and thus eliminate or reduce the auxiliary components further. Therefore, a bi-direcitonal AFAPM converter is needed in order to sink and also source the harmonic energy. DAB is a promising topology for isolated and bi-directional power conversion due to ZVS for both primary and secondary bridges, utilization of parasitic, and fixed switching frequency [69-78]. In this section, the dual-voltage charging system with proposed DAB-based full-integrated AFAPM is shown in Fig. 5.16. The DAB converter works as a LV

battery charger when the vehicle is running; and works as an AF when the vehicle at charging station and the HV battery is charging.

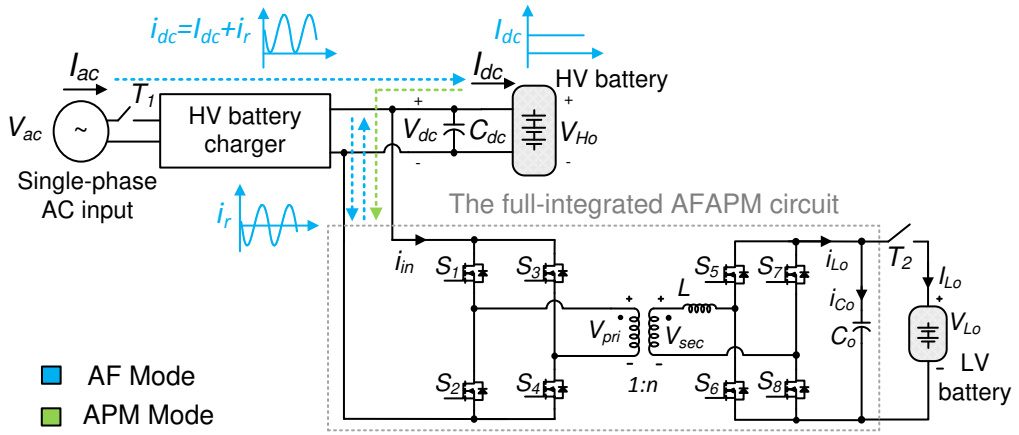


Fig. 5.16. The dual-voltage charging system with proposed DAB-based full-integrated AFAPM.

5.3.1 DAB-based APM design

The single-phase-shift (SPS) modulation is applied to the DAB for simplicity. The small signal analysis of the DAB can be found in [69, 70, 76]. Typically, when designing the DAB converter, we need to consider the transformer turn ratio and duty cycle range to achieve ZVS; and consider the leakage inductance to achieve maximum power. The DAB transformer turn ratio has been discussed in the chapter 4. 1/20 is chosen as the transformer turn ratio n.

Another important design issue is the leakage inductance L. The supplied power equation of DAB can be drawn as follows,

$$P = \frac{nV_{Lo}V_{Ho}}{2Lf_s}\phi(1-\phi) \tag{5.13}$$

where f_s is the switching frequency, ϕ is the phase shift between primary and secondary, and L is the leakage inductance referred to the secondary stage. From (5.13), it is clear that P is inversely proportional to the L. Hence, there is a trade-off between peak current and maximum output power for the leakage inductance selection.

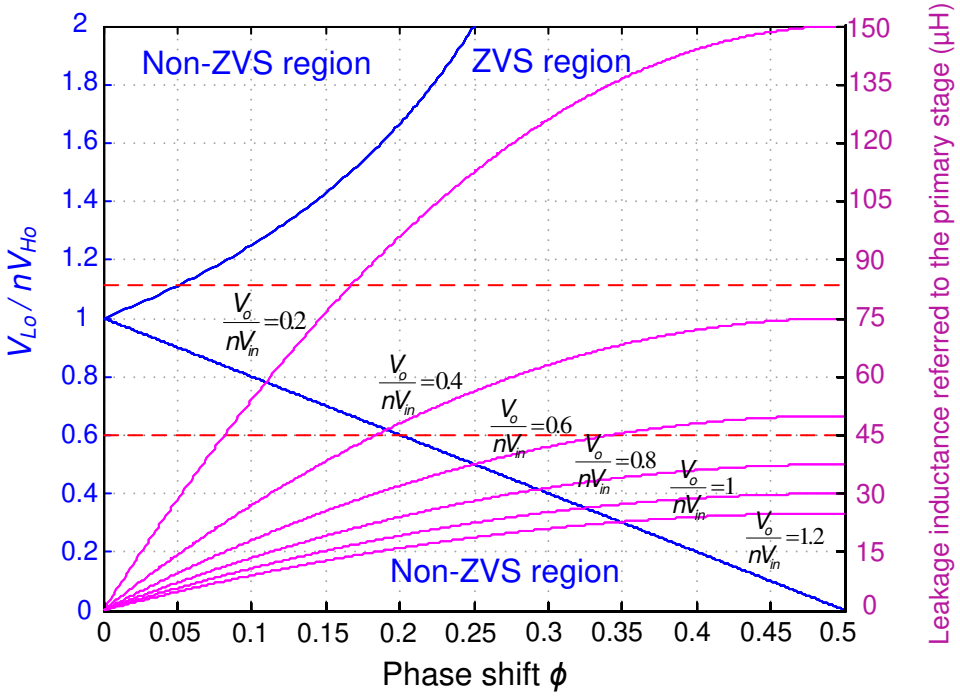


Fig. 5.17. DAB-based LV battery charger design map.

Considering both the soft switching and leakage inductance constrains, the DAB-based LV battery charger design map can be drawn in Fig. 5.17. In order to be able to

provide 2.4 kW maximum power to the LV battery, the leakage inductance *L* referred to the secondary stage is chosen as 62.5 nH.

In addition, another design consideration with SPS modulation is the well-known circulating current [73]. Typically, with smaller phase shift applying to the converter, the less circulating current will be produced. In fact, this reactive power can be eliminated by some other control methods, like dual-phase-shift (DPS) or extended-phase-shift (EPS), etc. [73-74].

5.3.2 Proposed DAB active filtering control

From equation (3.16), it is clear that the amplitude of the ripple current i_r is equal to the dc component I_{dc}. In fact, in order to assimilate the harmonic current into the AFAPM, this harmonic current i_r is exactly the input current to the AFAPM. Hence, the key to control the DAB as an AF to assimilate this harmonic is to find out the relationship between the input current and the phase shift angle, and then let the average input current equal to the harmonic current i_r.

Fig. 5.18 shows the typical waveforms of a DAB converter in the buck phase and boost phase, respectively. For both buck and boost phases, the inductor current I_1 and I_2 can be expressed as,

$$I_1 = \frac{1}{4Lf_s}[nV_{Ho}(2\phi - 1) + V_{Lo}] \tag{5.14}$$

$$I_2 = \frac{1}{4Lf_s}[nV_{Ho} + V_{Lo}(2\phi - 1)] \tag{5.15}$$

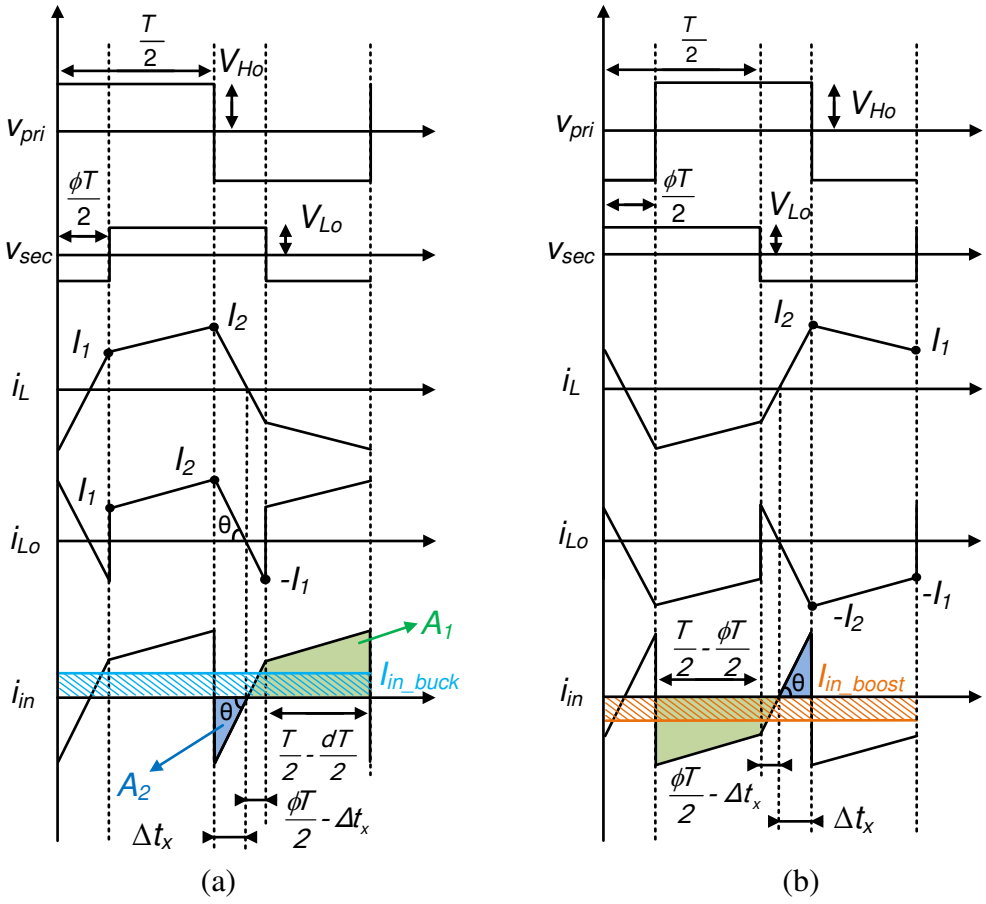


Fig. 5.18. Typical waveforms of DAB. (a) Buck charging phase. (b) Boost discharging phase.

During the buck phase, in order to calculate the average input current, the shaded areas A_1 and A_2 need to be obtained as shown in Fig. 5.18 (a). This requires knowing the expression of interval Δt_x. The $tan\theta$ needs to be calculated, and thus, Δt_x can be obtained easily. The $tan\theta$ and Δt_x can be obtained as,

$$\tan\theta = \frac{I_1 + I_2}{\frac{\phi T}{2}} = \frac{I_2}{\Delta t_x} \tag{5.16}$$

$$\Delta t_x = \frac{[nV_{Ho} + V_{Lo}(2\phi - 1)]}{4f_s(nV_{Ho} + V_{Lo})} \tag{5.17}$$

Hence, the average input current can be expressed as,

$$I_{in\_buck} = \frac{A_1 - A_2}{\frac{T}{2}} = \frac{nV_{Lo}}{2Lf_s}(\phi - \phi^2) \tag{5.18}$$

With the same procedure, the average input current during the boost phase can be derived as,

$$I_{in\_boost} = \frac{nV_{Lo}}{2Lf_s}(\phi^2 - \phi) \tag{5.19}$$

After the calculation, the phase shift for the buck and boost phase can be obtained as,

$$\phi_{buck} = \frac{1 - \sqrt{1 - \frac{8Lf_s I_{in\_buck}}{nV_{Lo}}}}{2} \tag{5.20}$$

$$\phi_{boost} = \frac{1 - \sqrt{1 + \frac{8Lf_s I_{in\_boost}}{nV_{Lo}}}}{2} \tag{5.21}$$

Then, the relationship between the harmonic current i_r and phase shift is found. During the buck charging phase, I_{in_buck} is equal to i_r and ϕ_{buck} is the phase shift; during the boost discharging phase, I_{in_boost} is equal to i_r and ϕ_{boost} is the phase shift applied to the converter.

5.3.3 Integrated output capacitor requirements

As the DAB converter is used to achieve both LV battery charging and active filtering functions, its output capacitor bank needs to meet both requirements as well. They are the ripple percentage requirement during the LV battery charging mode and active harmonic energy storage requirement during the active filtering mode. By calculating and combining these two requirements together, we can obtain the integrated output capacitor requirements.

A. Ripple percentage and capacitance requirements for LV battery charging

Part of the DAB output capacitance analysis has been done in [75]. However, the authors only discuss the condition when $V_{Lo} > nV_{Ho}$. As the V_{Lo}/nV_{Ho} is selected mostly in the region smaller than 1, the output voltage analysis for the case $V_{Lo} < nV_{Ho}$ is presented in this section. Furthermore, it is interesting to observe with the phase shift increases, and thus, the reactive power increases, the value of I_1 will be greater than I_{Lo}, as shown in Fig. 5.19. This will also affect the voltage ripple calculation. Therefore, another equation needs to be derived to calculate the voltage ripple for the scenario when $I_1 > I_{Lo}$.

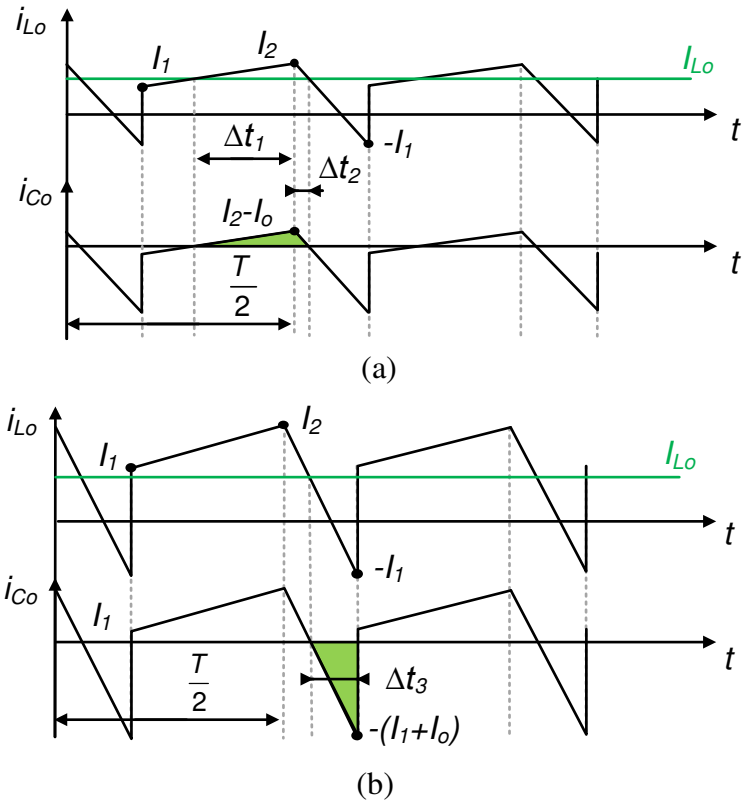


Fig. 5.19. Current ripple waveform for $V_{Lo} < nV_{Ho}$. (a) $I_1 < I_{Lo}$. (b) $I_1 > I_{Lo}$.

When $I_1 < I_{Lo}$, from Fig. 5.19 (a), the capacitor current can be obtained as,

$$\begin{cases} I_{Lo} + \dfrac{nV_{Ho} - V_{Lo}}{L} \cdot \Delta t_1 = I_2 \\ I_2 + \dfrac{(-nV_{Ho} - V_{Lo})}{L} \cdot \Delta t_2 = I_{Lo} \end{cases} \tag{5.22}$$

where the output current I_{Lo} and output voltage V_{Lo} can be found as,

$$\begin{cases} I_{Lo} = \dfrac{nV_{Ho}}{2Lf_s}(1-\phi^2) \\ V_{Lo} = \dfrac{nV_{Ho}R_{Lo}}{2Lf_s}(1-\phi^2) \end{cases} \tag{5.23}$$

where R_{Lo} is the load resistance. In the meanwhile, the voltage ripple can be derived as,

$$\Delta V_{Lo} = \frac{\Delta t_1 + \Delta t_2}{C_o} \cdot \frac{I_2 - I_{Lo}}{2} \tag{5.24}$$

Substitute (5.15), (5.22) and (5.23) to (5.24), the peak-to-peak voltage ripple percentage $\Delta V_{Lo}\%$ can be obtained as,

$$\Delta V_{Lo}\% = \frac{[2f_sL(2\phi^2 - 2\phi + 1) + R_{Lo}\phi(1-\phi)(2\phi-1)]^2}{8f_sC_o\left[4{f_s}^2L^2R_{Lo}\phi(1-\phi) - R_{Lo}^3\phi^3(1-\phi)^3\right]} \cdot 100\% \tag{5.25}$$

When $I_1 > I_{Lo}$, from Fig. 5.19 (b), the capacitor current can be obtained as,

$$I_{Lo} - \frac{nV_{Ho} + V_{Lo}}{L} \cdot \Delta t_3 = -I_1 \tag{5.26}$$

In the meanwhile, the voltage ripple can be expressed as,

$$\Delta V_{Lo} = \frac{\Delta t_3}{C_o} \cdot \frac{I_1 + I_{Lo}}{2} \tag{5.27}$$

Substitute (5.14), (5.23) and (5.26) to (5.27), the peak-to-peak voltage ripple percentage $\Delta V_{Lo}\%$ can be obtained as,

$$\Delta V_{Lo}\% = \frac{[2f_s L(4\phi - 2\phi^2 - 1) + R_{Lo}\phi(1-\phi)]^2}{32{f_s}^2 L C_o [R_{Lo}^2 \phi^2 (1-\phi)^2 + 2f_s L R_{Lo}\phi(1-\phi)]} \cdot 100\% \quad (5.28)$$

From (5.25) and (5.28), the voltage ripple percentage $\Delta V_{Lo}\%$ under different capacitances can be drawn in Fig. 5.20. If the voltage ripple percentage requirement for the LV battery is 1%, 10 mF capacitance is needed to be applied for the worst case. Actually, the output current ripple is the biggest drawback for the single-phase DAB converter. By applying three-phase DAB converter or multiple DAB converters to interleave the output current, the output current ripple can be reduced significantly and, thus, smaller output capacitor for the LV battery charger is required [72, 78].

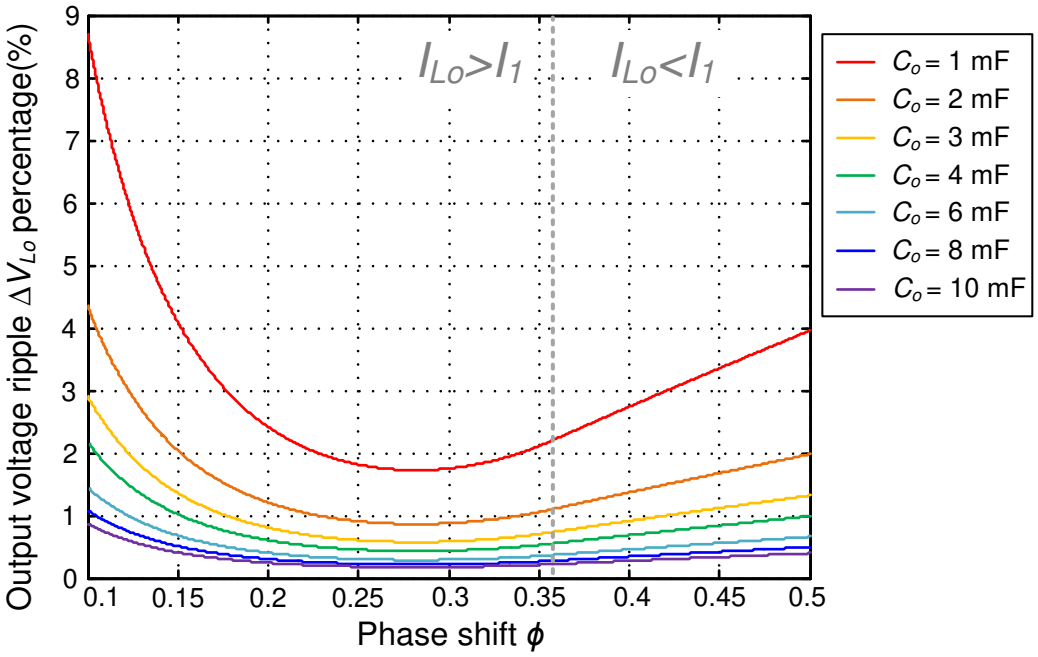


Fig. 5.20. Ripple percentage requirements for LV battery charging.

B. Active harmonic energy storage and capacitance requirements for HV active filtering

The required output capacitance equation for the HV active filtering is obtained as (5.12). For the conventional DAB-based LV battery charger, the voltage stress on the secondary stage switches is equal to the LV battery's dc link, which may varies between 11 V to 16 V. The minimum active energy storage capacitance requirements at different peak voltages for 4 kW HV battery charger active filtering is shown in Fig. 5.21.

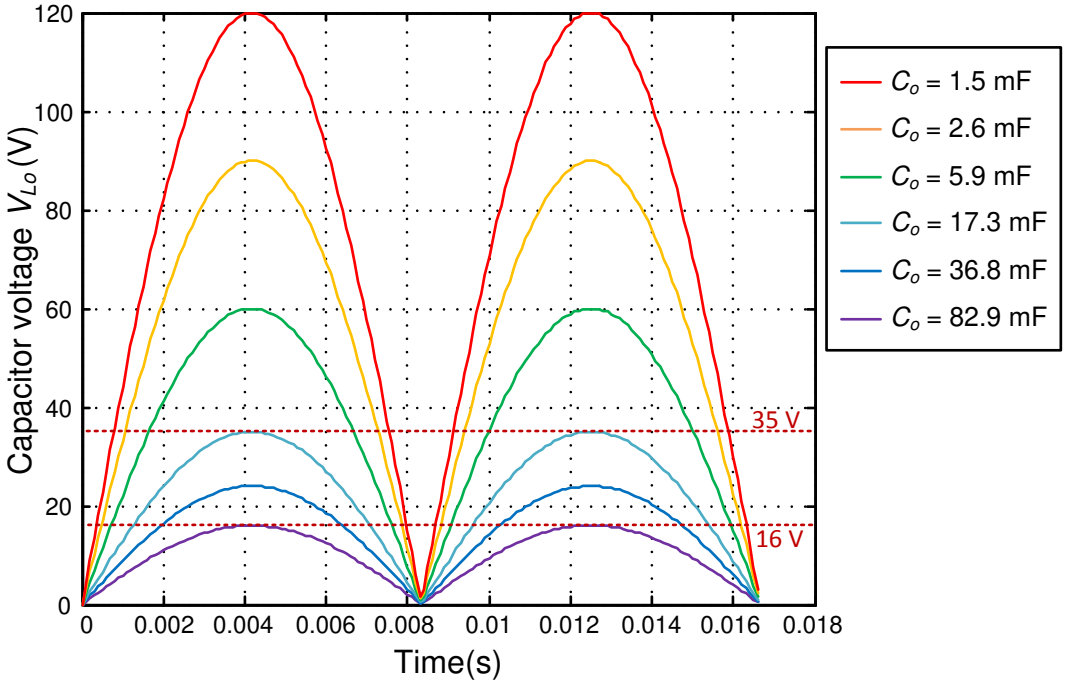


Fig. 5.21. Minimum active energy storage capacitance requirements at different peak voltages for 4 kW HV battery charger.

It is obvious that with around 16 V peak voltage, the required capacitance is relatively large. Therefore, during the active filtering mode, lifting the 16 V peak voltage is more reasonable and easy to achieve. However, the peak voltage level cannot be lifted too high. Considering the case if 60 V peak voltage ripple is selected, then secondary-stage switches with around 120 V voltage rating may need to be applied. Switch with higher voltage rating yields larger on-state resistance. As in the LV battery charging mode, the AFAPM converter needs to produce around 200 A current to the LV battery, the increase in the on-state resistance of switch will lead to higher conduction loss on the secondary stage, and thus, impact the APM converter's efficiency. In this paper, we select 60 V voltage rating switches on the secondary. Hence, around 35 V peak voltage ripple can be chosen. Then the corresponding required capacitance will be 17.3 mF.

As the peak voltage is set, the larger capacitance is, the smaller voltage ripple will be produced. The relationship between capacitance and voltage ripple can be drawn in Fig. 5.22. However, when the AFAPM works as an AF, the output capacitor is disconnected from the LV battery as shown in Fig. 5.16. Hence, there are no voltage ripple requirements on that capacitor during that time period. From volume and cost aspects, the 17.3 mF capacitor is sufficient to store all the harmonic energy regardless of the voltage ripple on it.

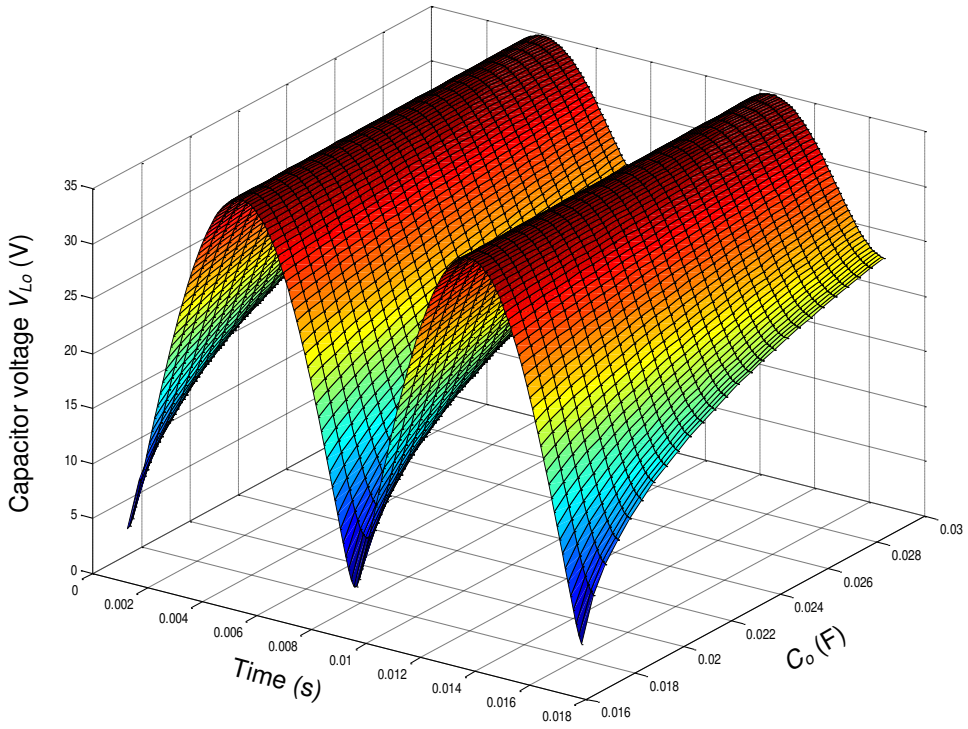


Fig. 5.22. Capacitor voltage ripple variations under fixed 35 V peak voltage.

5.3.4 Simulation results

A simulation study is conducted in MATLAB/Simulink. The dual-mode controller block diagram for the proposed full-integrated AFAPM is shown in Fig. 5.23. The SPS modulation is applied to both modes. In the DAB converter, both full bridge voltages are 50% duty cycle square wave with a phase shift ϕ between the primary and secondary. In the active filtering mode, to prevent the overcharging of the output capacitor, another voltage loop is used to control the average value of the capacitor voltage, where a low pass filter is applied. The simulation parameters are shown in the Table 5.2. A 100 μF capacitor C_{dc} is still needed on the HV dc-link to assimilate the high frequency harmonics.

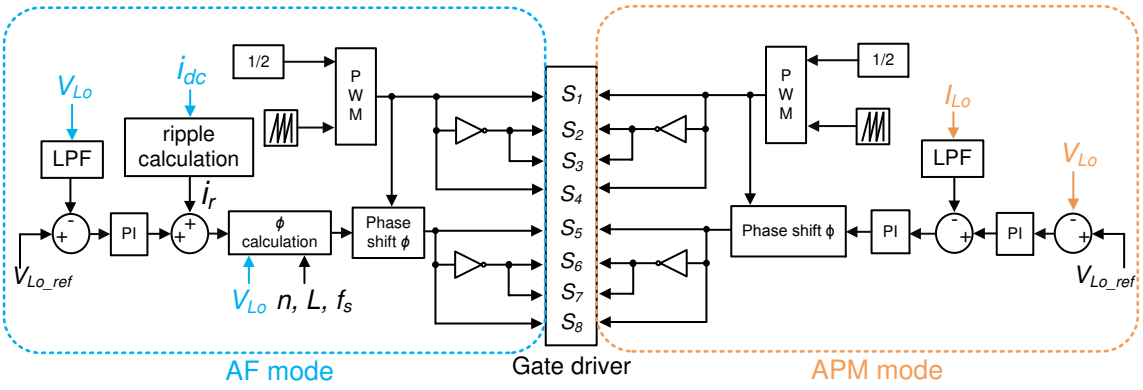


Fig. 5.23. Overall dual-mode control diagram.

Table 5.2. Simulation parameters.

Parameters	Value	Parameters	Value
Capacitance C_o	17.3 mF	Turn ratio n	1/20
Inductance L	62.5 nH	Switching Frequency f_s	100 kHz
Capacitance C_{dc}	100 µF	AC supply Frequency f	60 Hz

Fig. 5.24 shows the LV output voltage and current, when the DAB is operating at the LV battery charging mode. The output voltage V_{Lo} is 12 V and output current I_{Lo} is 200 A. As the 17.3 mF capacitor bank is applied at the output of DAB converter, this yields a relatively small charging current ripple for the LV battery.

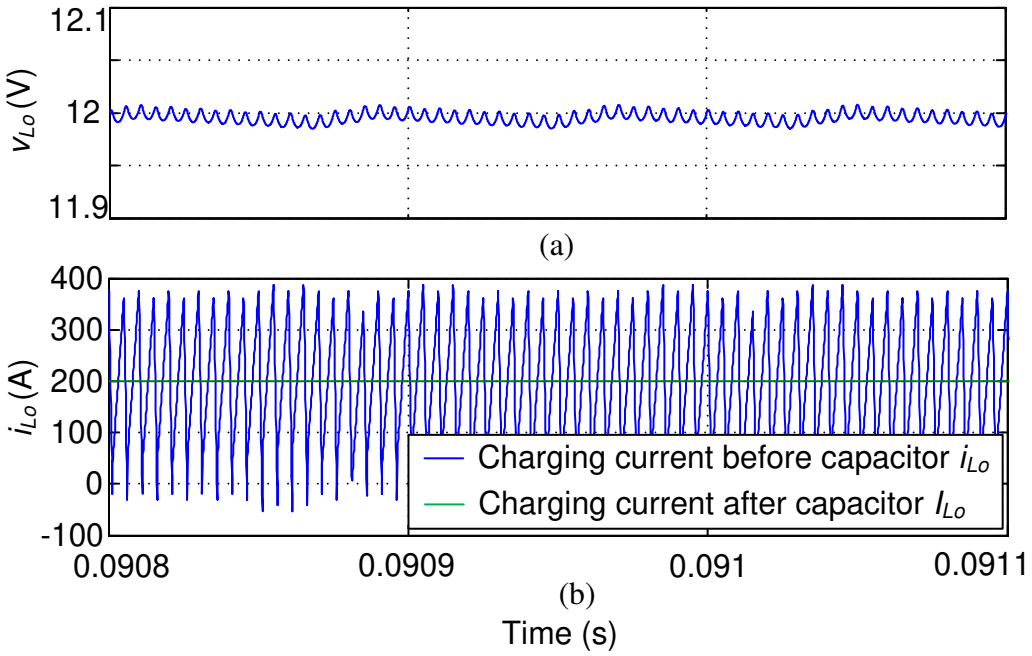


Fig. 5.24. Simulation results in LV battery charging mode. (a) Output voltage v_{Lo}. (b) Output current $i_{Lo.}$

Fig. 5.25 shows the voltage and current of the HV battery charger and DAB converter, when the DAB is operating at the active filtering mode. Before 0.5 s, the DAB is working. The voltage and current ripple on the HV battery charger's dc-link are relatively small. The second-order harmonic energy in the HV battery charger is transferred and stored into the DAB's output capacitor. The voltage on the DAB's output capacitor fluctuates between 0 V to 35 V. After 0.5 s, the DAB is turned off, and thus, all the harmonic energy is back to the HV dc-link.

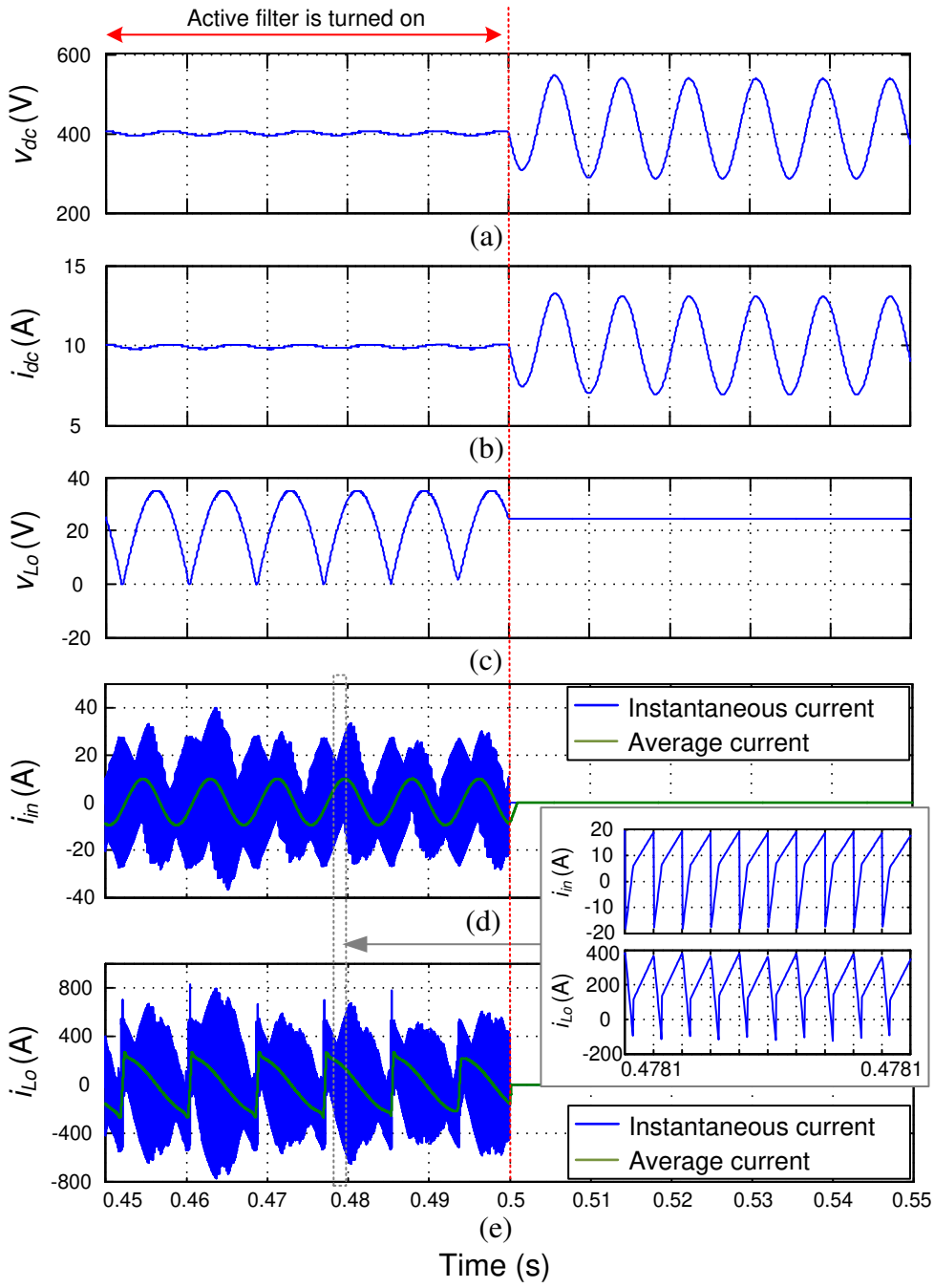


Fig. 5.25. Simulation results of active filtering mode. (a) HV output voltage v_{dc}. (b) HV output current i_{dc}. (c) LV output voltage v_{Lo}. (d) LV input current i_{in}. (e) LV output current $i_{Lo.}$

Fig. 5.26 is the switch requirements of the DAB converter at LV battery charging APM mode and active filtering mode, respectively. Clearly, for the input stage switches of AFAPM, the maximum voltage stress is 400 V for both modes; and the maximum RMS current for both would be around 10 A. Hence, the input stage switches VA ratings for AF and APM are exactly the same. However, during the active filtering mode, as we lifting the peak output capacitor's voltage to 35 V, the output stage switches voltage stress has to be lifted to 35 V rather than 16 V. Hence, 30 V MOSFETs need to be replaced by 60 V MOSFETs on the secondary stage.

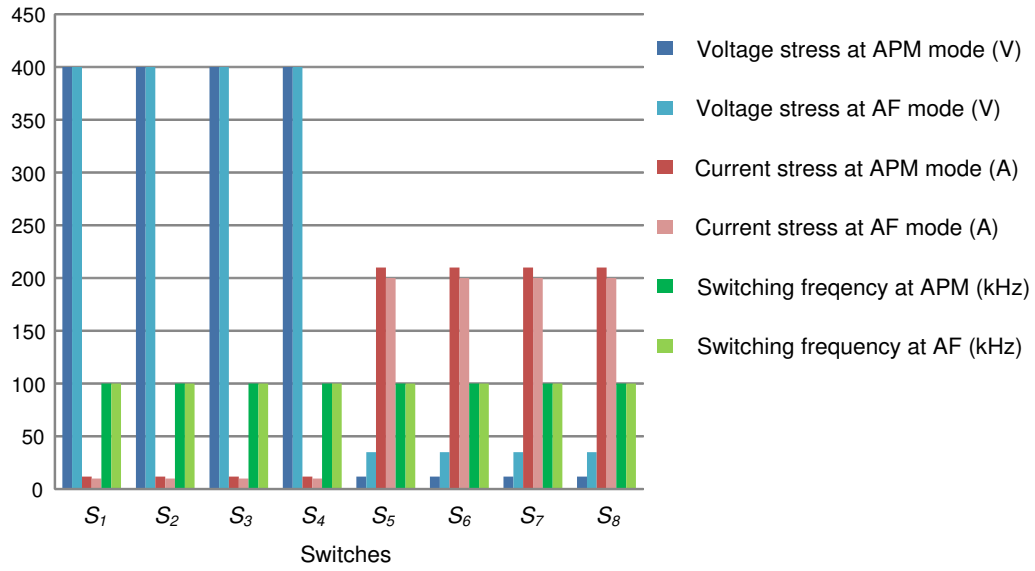


Fig. 5.26. Switch requirements of DAB-based full-integrated AFAPM.

5.4 Primary full-integrated AFAPM converter

The DAB-based full-integrated AFAPM converter uses the leakage inductor and transformer to transfer the HV harmonic energy, and utilize the output capacitor bank to store the energy. By doing so, the auxiliary components are reduced further. However, the efficiency of the converter in the HV AF mode will be relatively low as the high-voltage low-current harmonic energy needs to be converted into low-voltage high-current energy and transferred to the secondary stage. The power losses from the transformer and secondary switches have to be taken into account. In order to improve the efficiency, it would be better to still store the second-order harmonic energy on the primary stage and also eliminate the auxiliary inductors and extra relay. In this section, a primary full-integrated AFAPM converter is proposed. It is an integration between the DAB and two phase bi-directional buck AF.

5.4.1 Primary full-integrated AFAPM converter and its operation

A. Proposed primary full-integrated AFAPM converter

The dual-voltage charging system with proposed primary full-integrated AFAPM is shown in Fig. 5.27. The dual-voltage charging system specification can be found in Table 5.3.

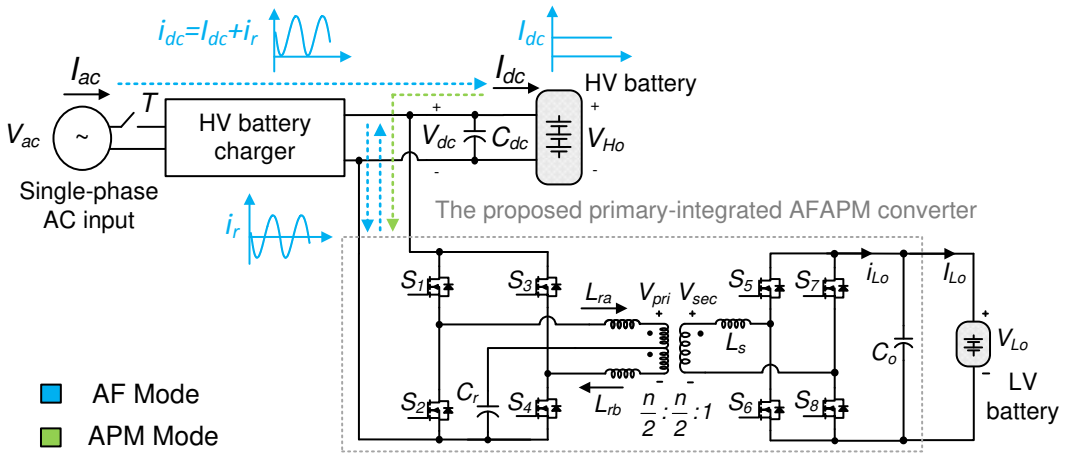


Fig. 5.27. The dual-voltage charging system with proposed primary full-integrated AFAPM.

Table 5.3. General dual-voltage charging system specification.

Parameters	Value
AC Level 2 HV battery charger output power P_{Ho} (kW)	3.3-6.6
LV battery charger output power P_{Lo} (kW)	2
AC Input voltage (V)	110-240
supply frequency f (Hz)	50-60
HV battery voltage V_{Ho} (V)	300-400
LV battery voltage V_{Lo} (V)	12-16

Note that the HV battery charger can be a single-stages or two-stage chargers containing the how-frequency harmonic current. The proposed converter is composed of a two-phase buck converter to achieve AF function for the HV battery charger, and a DAB converter to operate as the LV battery charger. The integrated AF consists of the switches S_1 to S_4, active energy storage capacitor C_r, and auxiliary inductors L_{ra}, L_{rb}. These two inductors have the same inductance L_r,

$$L_{ra} = L_{rb} = L_r \tag{5.29}$$

The switches S_1 to S_8, output capacitor C_o, auxiliary inductors L_{ra}, L_{rb}, and the transformer leakage inductance L_s form the APM. The transformer is a center-tapped transformer with a turn ratio $n/2$: $n/2$: 1. The center-tap is connected to the capacitor C_r. The lumped inductance of the DAB is L_k, which is the summation of auxiliary inductance L_{ra}, L_{rb} and transformer leakage inductance L_s,

$$L_k = L_{ra} + L_{rb} + n^2 L_s \tag{5.30}$$

The AF operates when the vehicle is connected to the grid and the HV battery is charging; the APM operates when the vehicle is running and the LV battery is charging from the HV battery. With the proposed integration method, the converter can achieve AF function with the need of an extra capacitor C_r only. Note that a small film capacitor C_{dc} is still needed on the HV dc-link. It is used to assimilate the switching ripple for the bidirectional buck converter and DAB in their corresponding modes.

B. Operating principle

The operating waveforms and equivalent circuit diagrams for the dual-mode operations are shown in Fig. 5.28 and Fig. 5.29. The deadtime is not specified on these two figures. When the converter is in AF mode, each phase of the two-phase buck converter will carry half of the total harmonic compensation current i_r. The harmonic compensation current i_r is exactly equal to the second-order harmonic current in the HV battery charger.

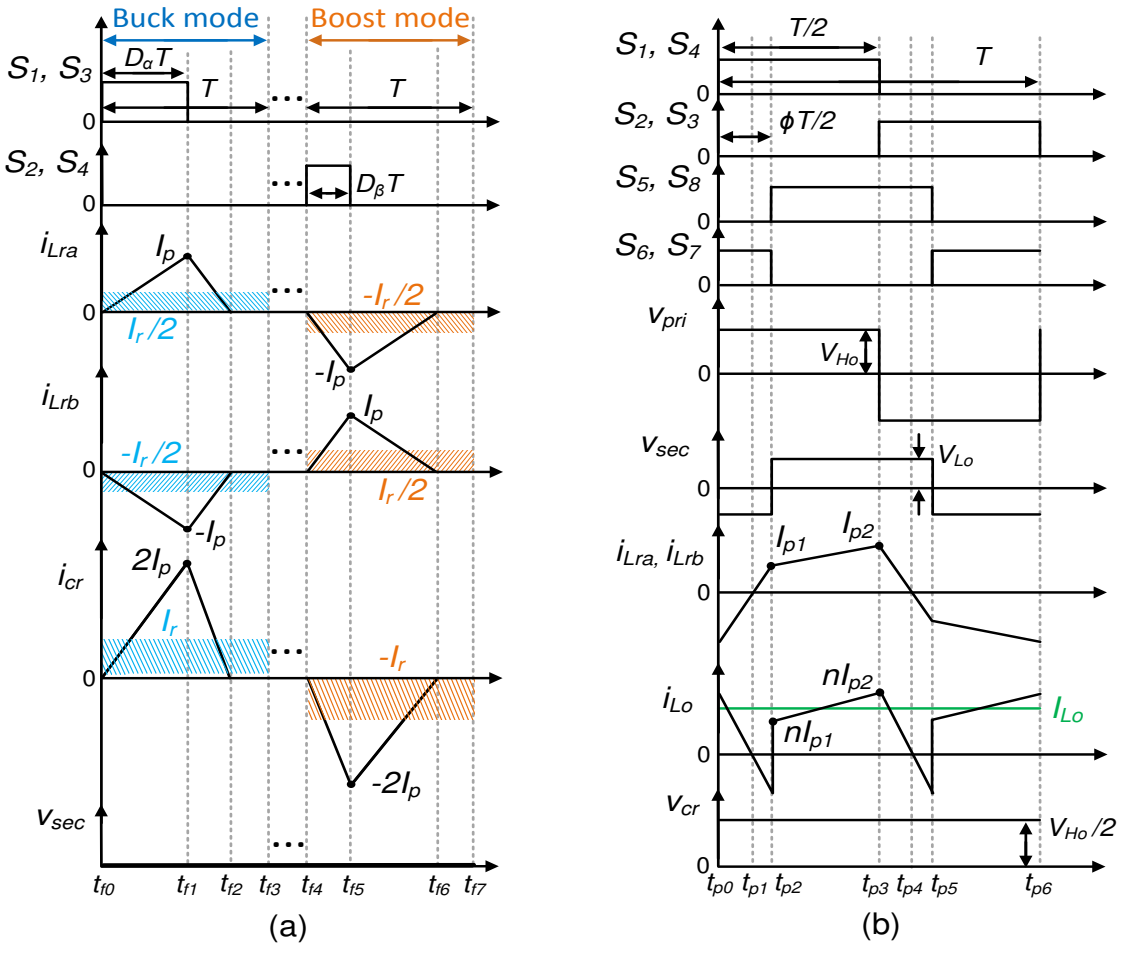


Fig. 5.28. Operating waveforms of the primary full-integrated AFAPM converter. (a) AF mode. (b) APM mode.

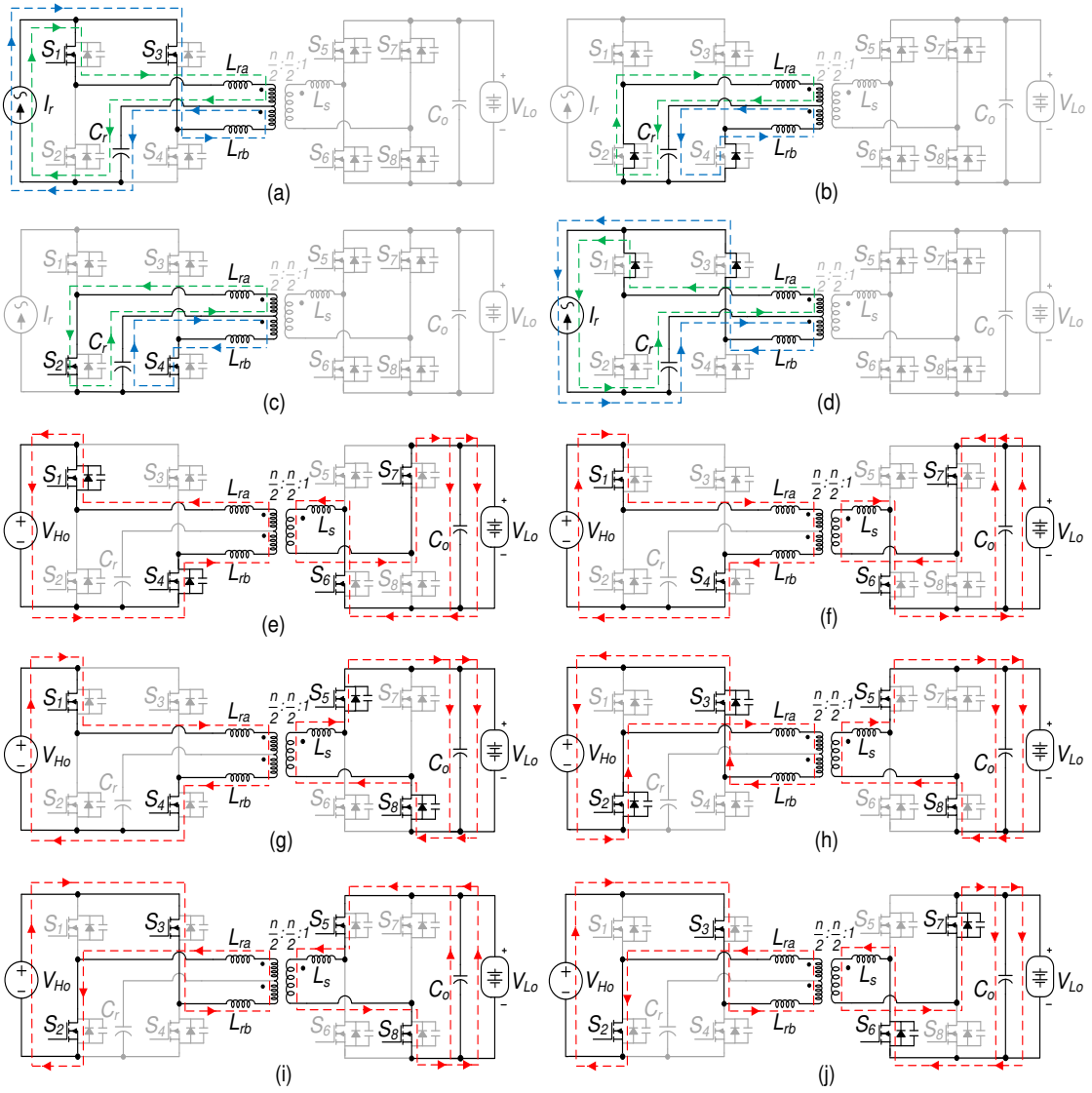


Fig. 5.29. Equivalent circuit diagrams of the primary full-integrated AFAPM converter. (a) AF Mode 1: current path between t_{f0} - t_{f1}. (b) AF Mode 2: current path between t_{f1} - t_{f2}. (c) AF Mode 3: current path between t_{f4} - t_{f5}. (d) AF Mode 4: current path between t_{f5} - t_{f6}. (e) APM Mode 1: current path between t_{p0} - t_{p1}. (f) APM Mode 2: current path between t_{p1} - t_{p2}. (g) APM Mode 3: current path between t_{p2} - t_{p3}. (h) APM Mode 4: current path between t_{p3} - t_{p4}. (i) APM Mode 5: current path between t_{p4} - t_{p5}. (j) APM Mode 6: current path between t_{p5} - t_{p6}.

When the harmonic current i_r is larger than zero, the converter works in the buck mode and the active energy storage capacitor C_r assimilate the harmonic energy. When the harmonic current i_r is smaller than zero, the converter works in the boost mode and the capacitor C_r release the harmonic energy back to the HV dc-link. Both the buck and boost operations work in the DCM as shown in Fig. 5.29 (a). The inductor L_{ra} and L_{rb} are used only to transfer the harmonic energy. This yields a relatively small inductance requirement, which is exactly the target of the inductor integration here. The feed-forward control is applied, the duty cycle is calculated directly based on the values of the harmonic current i_r, HV dc-link voltage V_{dc} and active energy storage capacitor voltage V_{cr}. The corresponding duty cycle D_α and D_β can be obtained as follows,

$$D_\alpha = \sqrt{\frac{i_r \cdot f_s \cdot L_r}{V_{dc} - V_{cr}}} \tag{5.31}$$

$$D_\beta = \sqrt{\frac{i_r \cdot (V_{dc} - V_{cr}) \cdot f_s \cdot L_r}{{V_{cr}}^2}} \tag{5.32}$$

where f_s is the switching frequency. D_α is the duty cycle applied to S_1 and S_3; D_β is the duty cycle applied to S_2 and S_4.

From Fig. 5.29 (a) to Fig. 5.29 (d), it is clear that the directions of the two phase currents on the transformer's primary winding are always opposite to each other. Furthermore, the two phase current magnitude is always equal. This yields the flux cancellation on the two center-tapped primary windings of the transformer. Hence, during

the AF mode, there will be no induced voltage on the transformer's secondary winding, and thus, no current will flow to the secondary stage.

When the converter is in APM mode, the SPS modulation is applied to the switches S_1 to S_8. The control diagram is shown in Fig. 5.30. The phase shift angle ϕ is applied between the primary full bridge and secondary full bridge as shown in Fig. 5.28 (b). The turn-on ZVS can be achieved during the deadtime for both primary and secondary stages. As shown from Fig. 5.29 (e) to Fig. 5.29 (j), the primary four switches S_1 to S_4 will always operate at a constant 50% duty cycle with complimentary control. This yields a constant voltage, whose amplitude is equal to half of the input voltage V_{Ho}, on the active energy storage capacitor C_r.

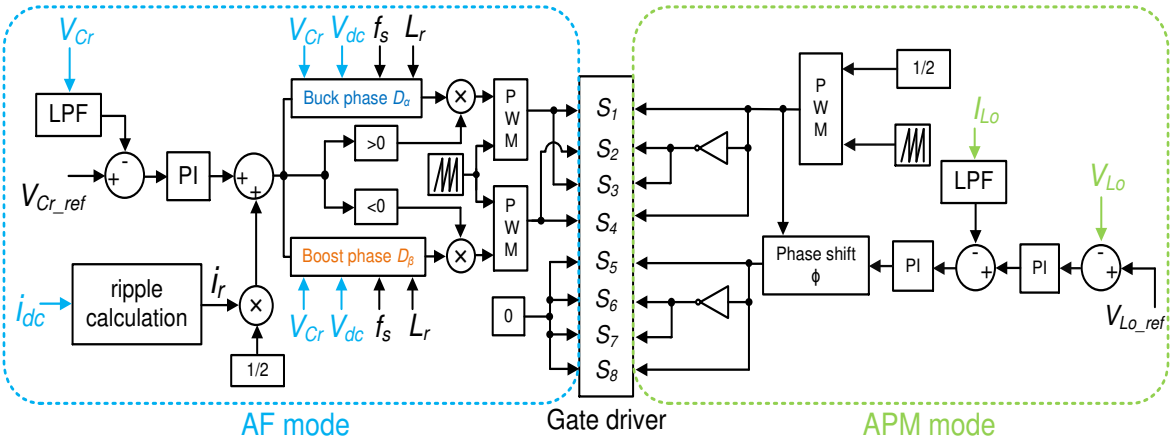


Fig. 5.30. Overall dual-mode control diagram.

5.4.2 Integrated converter design considerations

The primary switches S_1 to S_4 and the two inductors L_{ra} and L_{rb} are shared between the APM and AF modes. The integrated switch requirements have been

calculated and compared in Section 5.2. An almost same requirement can be obtained from the APM mode and AF mode respectively, which is good for a multi-functional converter integration. For the converter topology proposed in this paper, the inductors and transformer design are critical in terms of integration. This section mainly discusses the two inductor selection from the inductance and peak current aspects. As per requirement, a planar transformer with a minimized leakage is designed. The overall magnetic component design flow chart is shown in Fig. 5.31. In addition, the capacitance calculations of the capacitor C_r and C_o are also presented in this section.

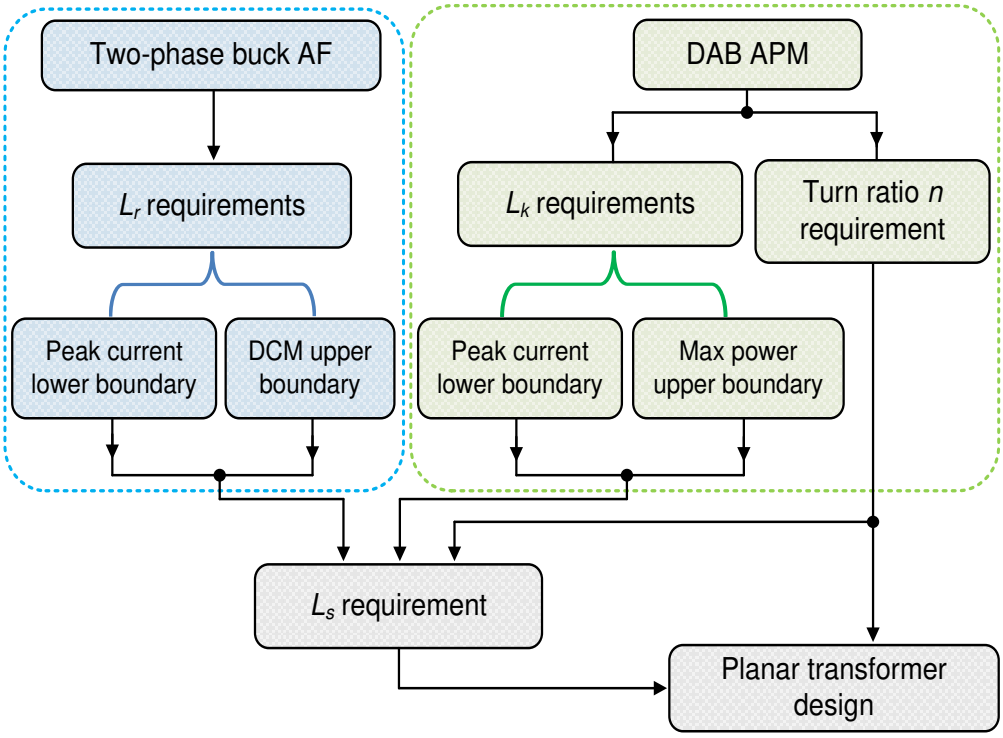


Fig. 5.31. Magnetic component design flow chart.

5.4.2.1 Integrated inductors L_r requirements

The auxiliary inductors in the AF mode have two design constrains. They are the DCM upper boundary and peak current lower boundary, which can be obtained as follows,

$$L_r \leq \frac{(V_{dc} - V_{cr}) \cdot V_{cr}}{I_{cr} \cdot V_{dc} \cdot f_s} \tag{5.33}$$

$$L_r \geq \frac{I_{cr} \cdot (V_{dc} - V_{cr}) \cdot V_{cr}}{{I_p}^2 \cdot V_{dc} \cdot f_s} \tag{5.34}$$

where I_{cr} is the average current in the capacitor C_r. If HV dc-link voltage V_{dc} is set to 400 V, the switching frequency f_s is set to 100 kHz, the peak inductor current requirement I_p is set to 50 A, and the peak capacitor's voltage is set as 350 V, based on the different power level of the HV battery charger, the corresponding inductor boundaries can be drawn in Fig. 5.32.

It is clear the inductance range between 10 to 35 μH fits for up to 6.6 kW ac level 2 single-phase HV battery charge's AF at 100 kHz. In fact, with higher switching frequency, the required inductance can be reduced further. In addition, as mentioned before, with the increase of the battery power, paralleling more integrated AFAPM converter modules will be a more effective solution for both AF mode and APM mode. This will also yield a wider inductance range for the sake of integration.

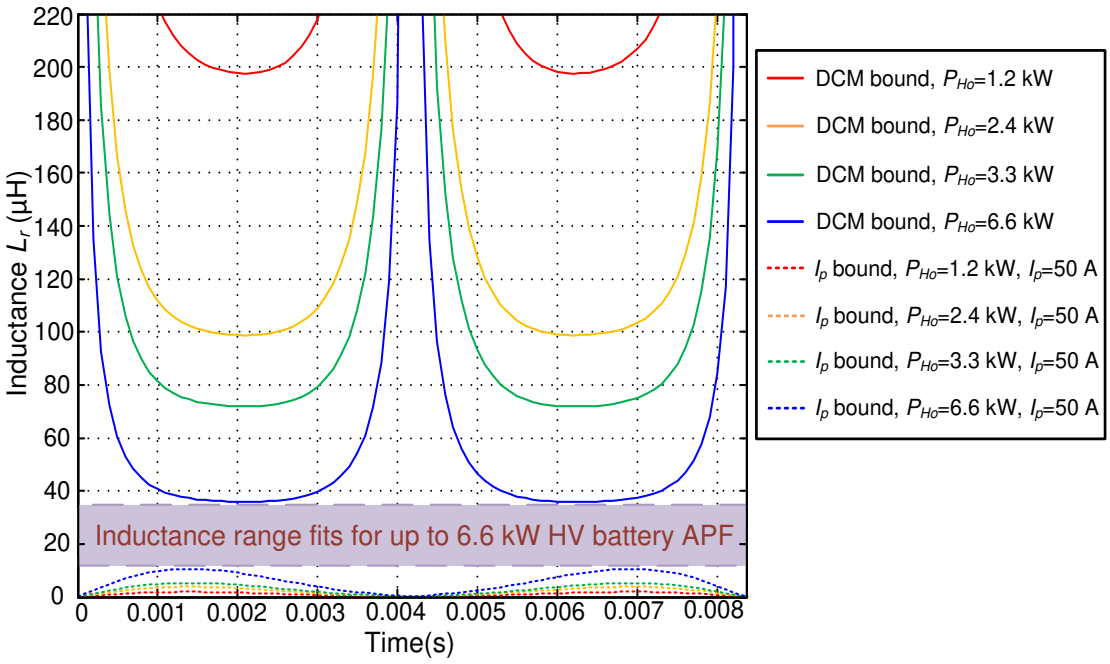


Fig. 5.32. Inductance L_r DCM upper boundary and peak current lower boundary for different power ratings of the HV battery AFs.

5.4.2.2 Integrated inductors L_k requirements

The lumped inductor L_k in the APM mode also have two design constrains. They are the maximum output power upper boundary and the peak current lower boundary. The relation between the lumped inductance L_k and the output power P_{Lo} can be drawn as follows,

$$L_k = \frac{nV_{Lo}V_{Ho}}{2P_{Lo}f_s}\phi(1-\phi) \tag{5.35}$$

In equation (5.35), it implies that L_k is inversely proportional to P_{Lo}. As the first step of the DAB converter design, the turn ratio n can be determined firstly and then the

L_k design range can be calculated based on its maximum output power and peak current requirements. The limits for the phase shift angle ϕ to maintain ZVS can be obtained as,

$$\begin{cases} \Phi > 0.5 - \dfrac{V_{Ho}}{2nV_{Lo}}, if\ V_{Lo} \geq nV_{Ho} \\ \Phi > 0.5 - \dfrac{nV_{Lo}}{2V_{Ho}}, if\ V_{Lo} \leq nV_{Ho} \end{cases} \tag{5.36}$$

In fact, the condition shown in (5.36) cannot guarantee the realization of ZVS. A more comprehensive analysis for the necessary and sufficient conditions to achieve ZVS is conducted in [70]. Briefly speaking, to realize ZVS, the inductive energy stored in the lumped inductor L_k needs to be equal or larger than the capacitive energy, which including the switches output capacitance and transformer capacitance. However, equation (5.36) is an effective method to choose the transformer turn ratio n. From the chapter 4, the turn ratio n is selected as 20.

As the turn ratio n has been selected, the next step is to obtain the range of inductor L_k. The peak current on the inductor during the APM mode can be written as,

$$I_{p1} = \frac{1}{4L_k f_s}[V_{Ho}(2\Phi - 1) + nV_{Lo}] \tag{5.37}$$

$$I_{p2} = \frac{1}{4L_k f_s}[V_{Ho} + nV_{Lo}(2\Phi - 1)] \tag{5.38}$$

Note when nV_{Lo} is smaller than V_{Ho}, the inductor current is exactly the waveform shown in Fig. 5.29 (b). The peak current is the value at I_{p2}. While if nV_{Lo} is larger than

V_{Ho}, as the voltage applied on the inductor is changed, the inductor current waveform is changed accordingly. The peak current is the current amplitude at I_{p1} instead.

Therefore, with different input voltages and required output power ratings, different inductance maximum power upper boundary and peak current lower boundary can be drawn in Fig. 5.33. If the APM maximum output power needs to reach 2 kW at the worst case 300 V input voltage, 12 V output voltage, with the turn ratio n=20, the inductance upper boundary is 45 µH. If the peak current in the APM mode is also set to 50 A, the lower boundary for the inductance L_k can be set to 20 µH. Therefore, the L_k inductance range fits for up to 2 kW APM can be set between 20 µH to 45 µH. This gives us a considerable inductance range for the transformer leakage inductance L_s design.

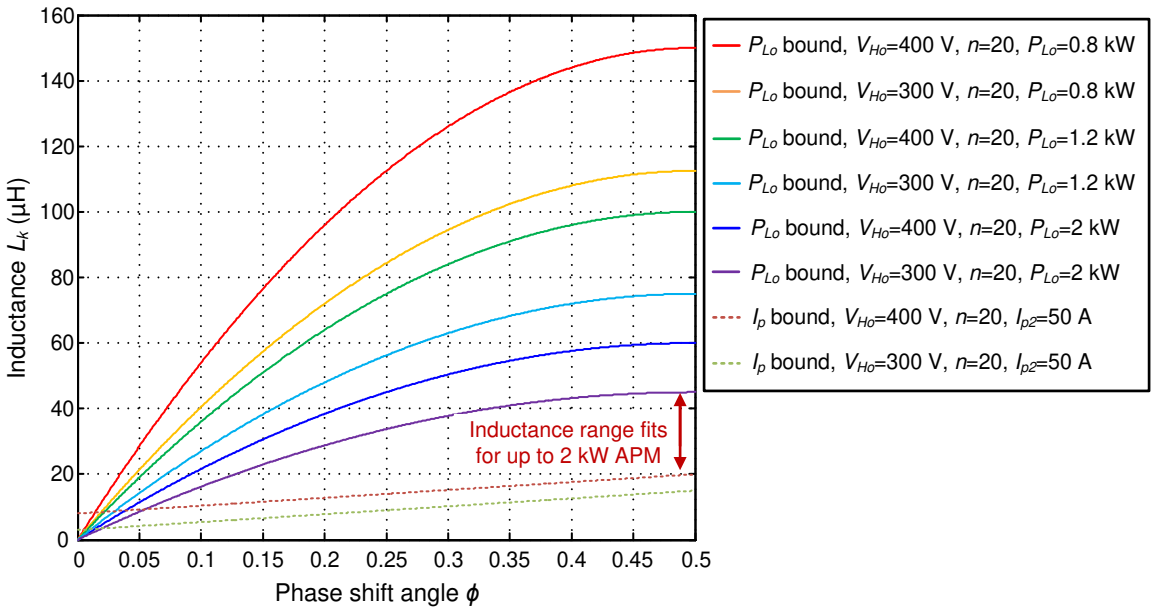


Fig. 5.33. Inductance L_k maximum power upper boundary and peak current lower boundary for different power ratings of the LV battery APMs.

5.4.2.3 Planar transformer and L_s requirements

From the aforementioned inductance analysis, it is clear a low leakage inductance from the transformer is desired. Hence, the interleaved planar transformer is exactly the objective in this paper. In addition, from the analysis in the chapter 4, the planar transformer's leakage inductance can be minimized to 31.5 nH referred to the secondary stage and 12.6 μH referred to the primary stage. This value meets the aforementioned inductance design requirements.

5.4.2.4 Capacitor C_r and C_o requirements

In order to assimilate the second-order harmonic energy fully from the HV battery charger, the requirements for the active harmonic energy storage capacitor C_r can be obtained as,

$$C_r \geq \frac{2P_{Ho}}{\omega V_{cp}^2} \tag{5.39}$$

where V_{cp} is the peak voltage on the capacitor. Hence, for a 6.6 kW HV battery charger, the capacitance C_r can be selected around 320 μF; for a 3.3 kW HV battery charger, the capacitance C_r can be chosen around 160 μF.

For the output capacitance C_o, From (5.25) and (5.28), the voltage ripple percentage $\Delta V_{Lo}\%$ with different capacitances at different power can be drawn in Fig. 5.34. If the voltage ripple percentage requirement for the LV battery is 1%, around 10 mF capacitance needs be applied for the worst case. In addition, considering the relatively high output current and also the intrinsic property of output current ripple in the DAB

converter, the relatively high peak-to-peak current ripple should also be taken into account for the LV electrolytic capacitor selection.

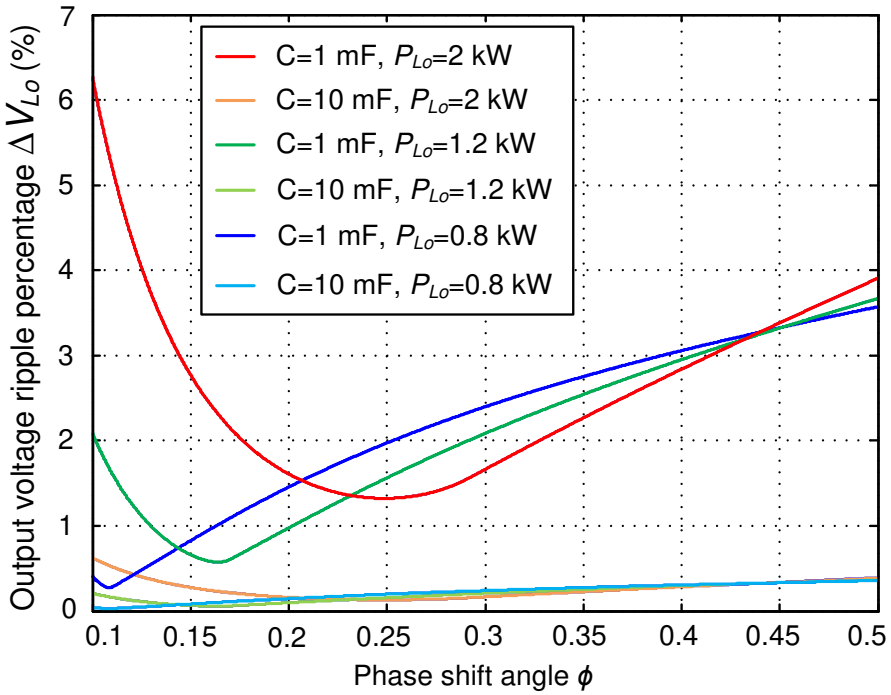


Fig. 5.34. Ripple percentage requirements for LV battery charging.

A main components cost comparison can also be made with the primary full-integrated AFAPM converter as shown in Fig. 5.35. For a conventional 6.6kW HV battery charger, the required capacitance is around 4 mF. As a result, from the harmonic energy storage aspect for the 6.6 kW HV battery charger in the vehicle applications, with the proposed AFAPM method, the cost can decrease further to 31.6% of the cost of traditional capacitor method and 44.7% of the cost of conventional active filter method.

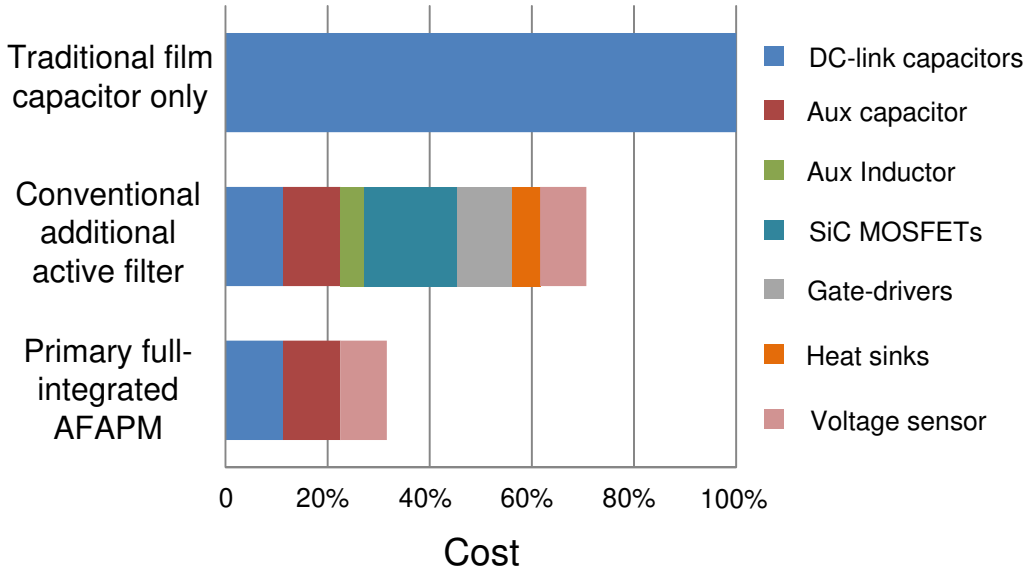


Fig. 5.35. A main components cost comparison for harmonic energy storage of 6.6 kW HV battery charger.

5.4.3 Simulation and implementation results

5.4.3.1 Simulation results

A simulation is conducted in the MATLAB/Simulink. The simulation parameters' values are shown in the Table 5.4.

Fig. 5.36 shows the simulation results in the AF mode. Before 0.037 s, the AF is turned off, the significant second-order harmonic is shown on the HV battery's dc-link Vdc. Only a 180 μF capacitor is used to assimilate the harmonic current. The peak-to-peak voltage ripple is 120 V. After 0.037 s, the AF is turned on. The harmonic energy is stored in the active energy storage capacitor V_{cr}, whose voltage is varied between 70 V to

330 V. The AF is operating in the DCM mode, and the peak current on the inductors is 40 A.

Table 5.4. Simulation setup parameters.

Parameters	Value
HV battery power P_{Ho} (kW)	3.3
LV battery power P_{Lo} (kW)	2
AC supply Frequency f (Hz)	60
Switching Frequency f_s (kHz)	100
Inductance L_{ra}, L_{rb} (μH)	10
Turn ratio n	20
Inductance L_s (nH)	40
Capacitance C_{dc} (μF)	180
Capacitance C_r (μF)	180
Capacitance C_o (mF)	10

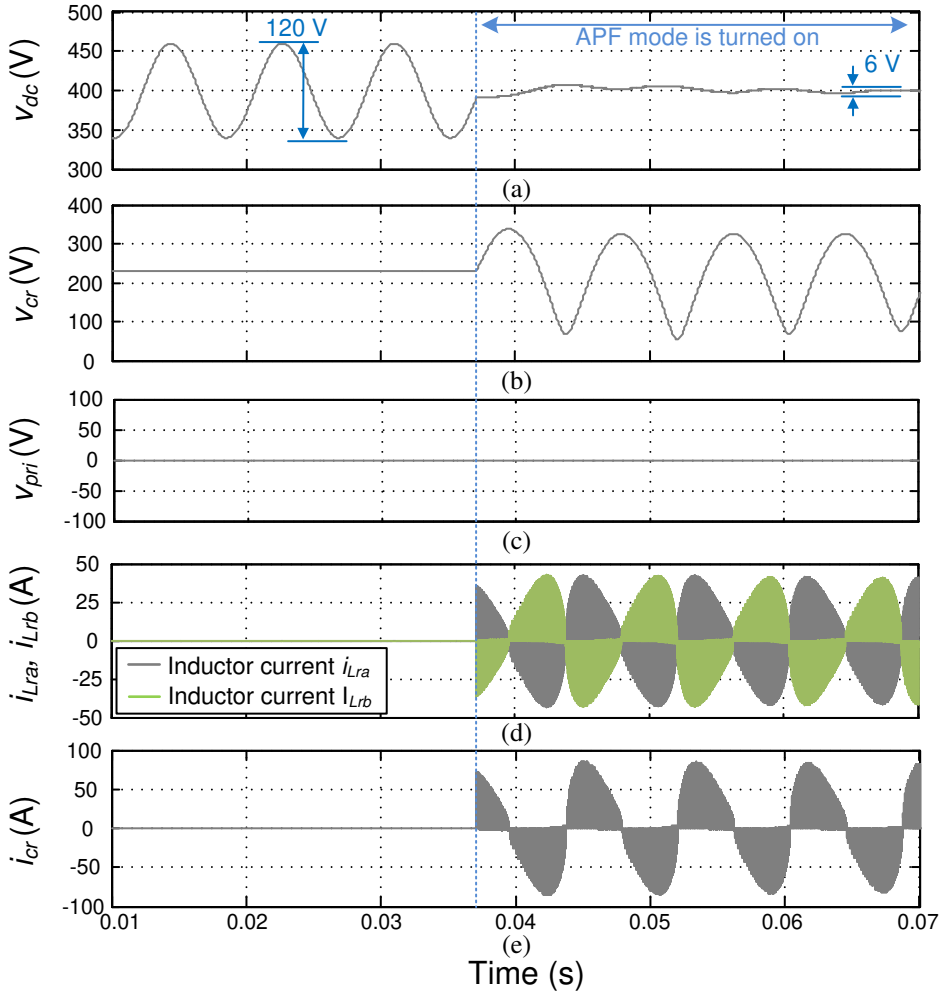


Fig. 5.36. Simulation results of AF mode. (a) HV dc-link voltage v_{dc}. (b) Capacitor C_r voltage v_{cr}. (c) Transformer primary voltage v_{pri}. (d) Inductor L_{ra} and L_{rb} current i_{ra} and i_{rb}. (e) Capacitor C_r current i_{cr}.

Fig. 5.37 shows the simulation results in the APM mode. The input voltage is 300 V. The output voltage and current are 12 V and 167 A, respectively. The voltage on the active energy storage capacitor C_r is 150 V, which is half of the input voltage. The peak current on the inductors is 14 A.

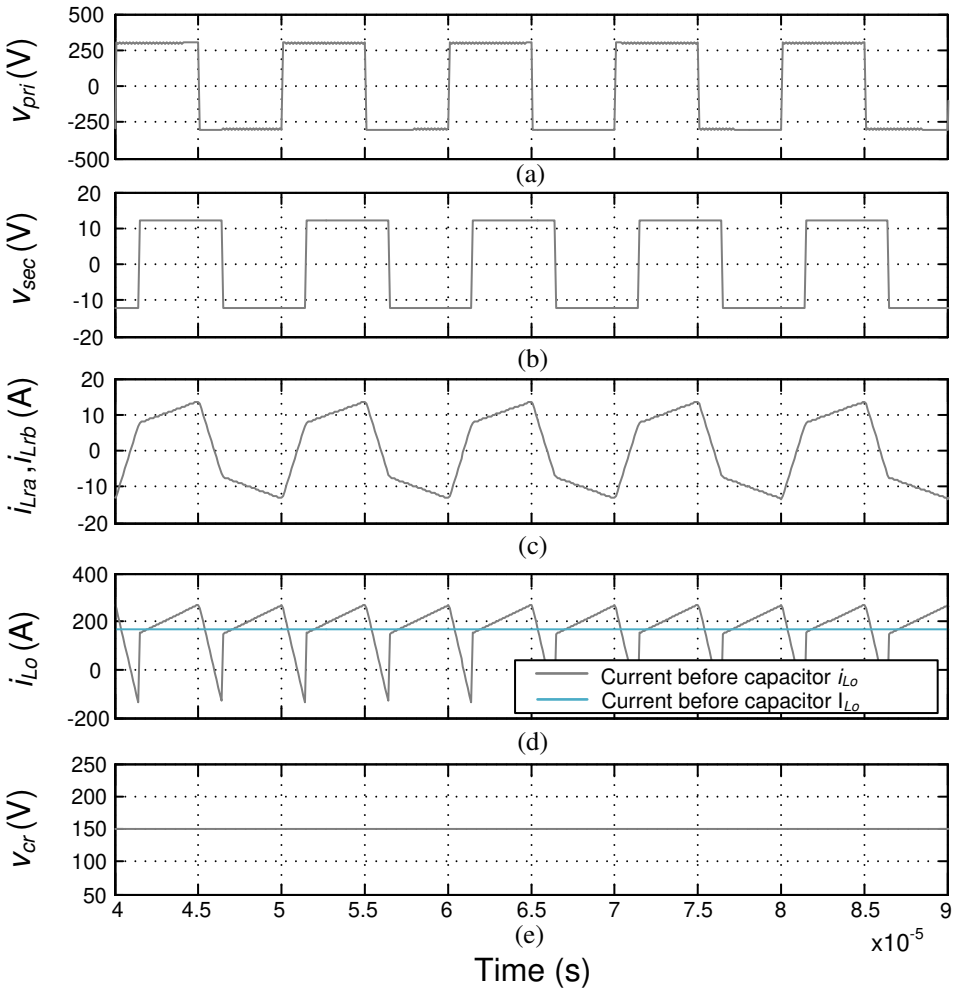


Fig. 5.37. Simulation results of APM mode. (a) Transformer primary voltage v_{pri}. (b) Transformer secondary voltage v_{sec}. (c) Inductor L_{ra} and L_{rb} current i_{ra} and i_{rb}. (d) LV output current i_{Lo}. (e) Capacitor C_r voltage $v_{cr.}$

5.4.3.2 Implementation results

A 720 W prototype has been built as shown in Fig. 5.38. Note that the gate-driver circuits are included in the prototype, while the DSP controller is not. Four CREE's third-generation SiC MOSFETs (C3M0065090D) are applied as the primary full bridge. Four Infineon Americas Silicon MOSFETs (IRFP7537PBF) are applied as the secondary full

bridge. The center-tapped 10:10:1 planar transformer is applied on this converter. Its measured L_m is 4 mH and measured L_s is 41.5 nH. The inductance of the auxiliary inductors L_{r1} and L_{r2} is 10 µH. The output capacitors C_o of the DAB are 4×6800 µF electrolytic capacitors. The AF capacitor C_r is a 22 µF film capacitor.

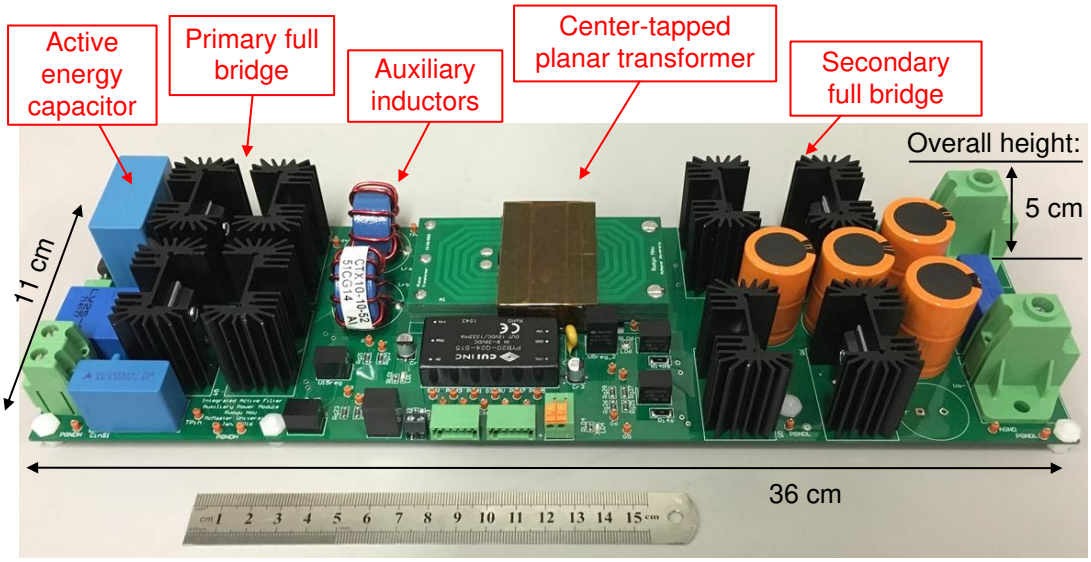


Fig. 5.38. 720 W integrated AFAPM converter prototype.

In the testing, a 360 W PFC board UCC28180EVM-573 from Texas Instruments is applied as the current source for the active filtering. A 44 µF film capacitor C_{dc} is applied on the HV dc bus. In the experiments, power for the LV battery charging mode is provided by an Ametek dc power supply QSGA330x45C and the load is a Kepco dc electronic load EL 5K-400-420. The overall control is implemented by a Texas Instrument DSP (TMS320F28335). The test rig is shown in Fig. 5.39. Test waveforms are recorded by an Agilent oscilloscope. The high-frequency ac current are recorded by a Rogowski current waveform transducer.

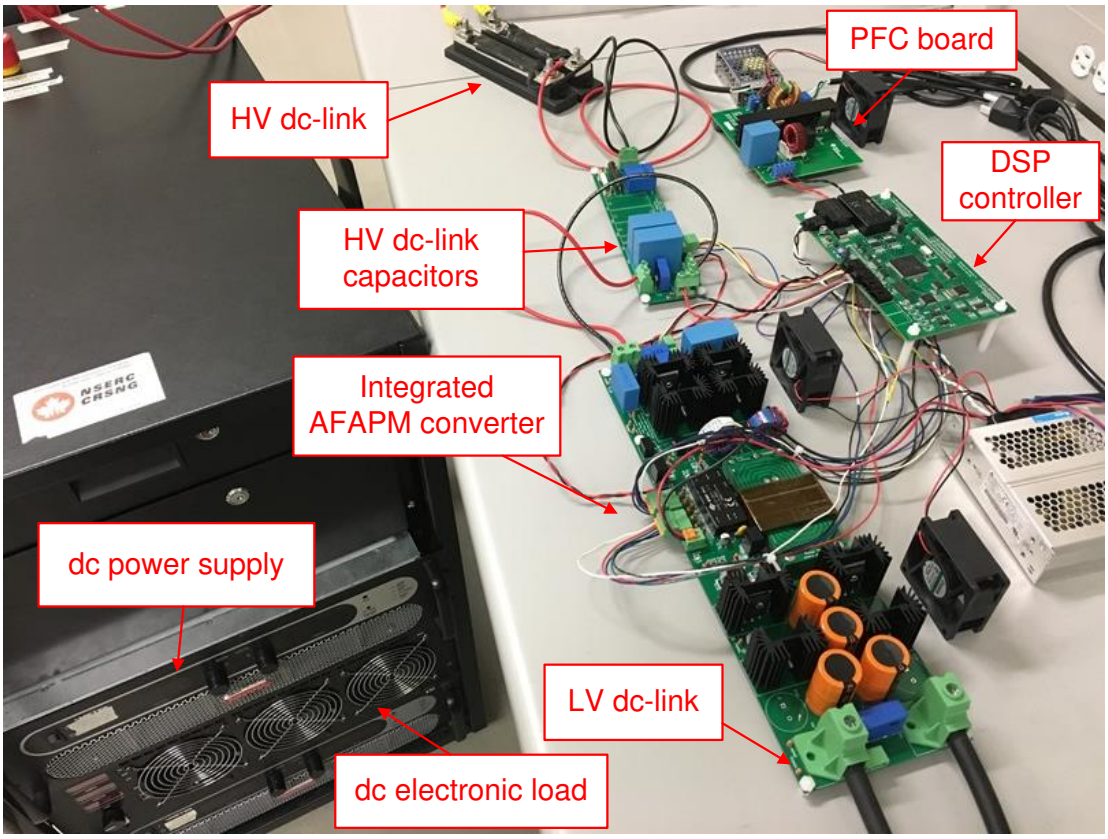
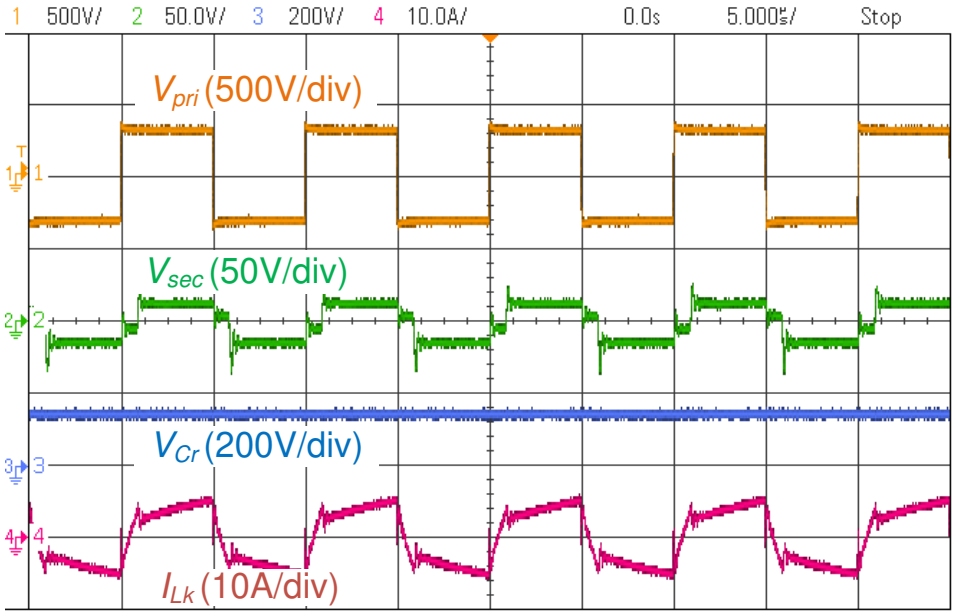
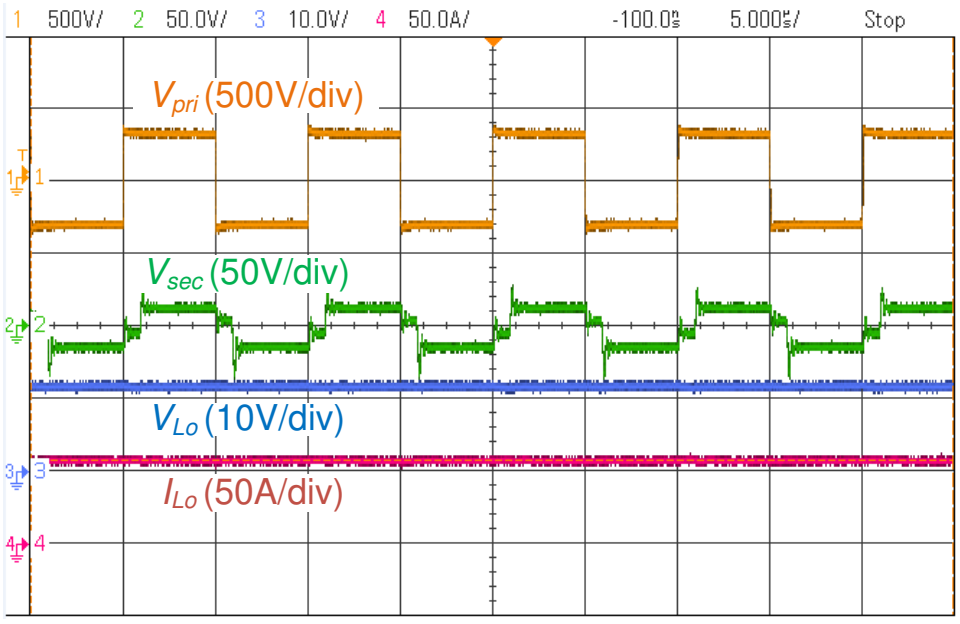


Fig. 5.39. Integrated AFAPM prototype test rig.

Fig. 5.40 shows the experimental waveforms of the APM mode, at the operating point where f_s = 100 kHz, V_{Ho} = 310 V, V_{Lo} = 12 V, and P_{Lo} = 720 W. The output current for the LV load is 60 A. As the input voltage V_{Ho} is 310 V, the AF capacitor voltage V_{cr} is equal to 155 V.



(a)



(b)

Fig. 5.40. Experimental results of the LV battery charging APM mode.

Fig. 5.41 and Fig. 5.42 show the experimental waveforms of the AF mode. First of all, in order to present the active filtering effect of the AFAPM converter, Fig. 5.41 can be used as a reference and it shows the experimental results for 360 W PFC without AF. The ac input line voltage V_{ac} is 120 V_{rms}, and its frequency is 60 Hz. The input current I_{ac} of the PFC is in phase with V_{ac}. The dc load is applied to sink the output power from the PFC. At that time, the second-order harmonic current and its voltage ripple are only filtered by 44 μF dc-link capacitors. Its dc-link voltage V_{dc} is fluctuated with a 55 V peak-to-peak.

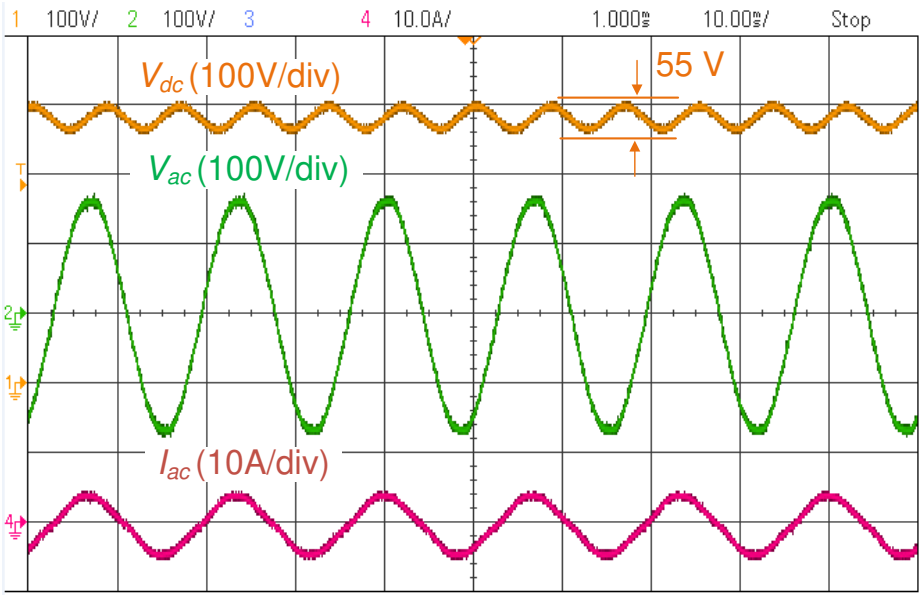
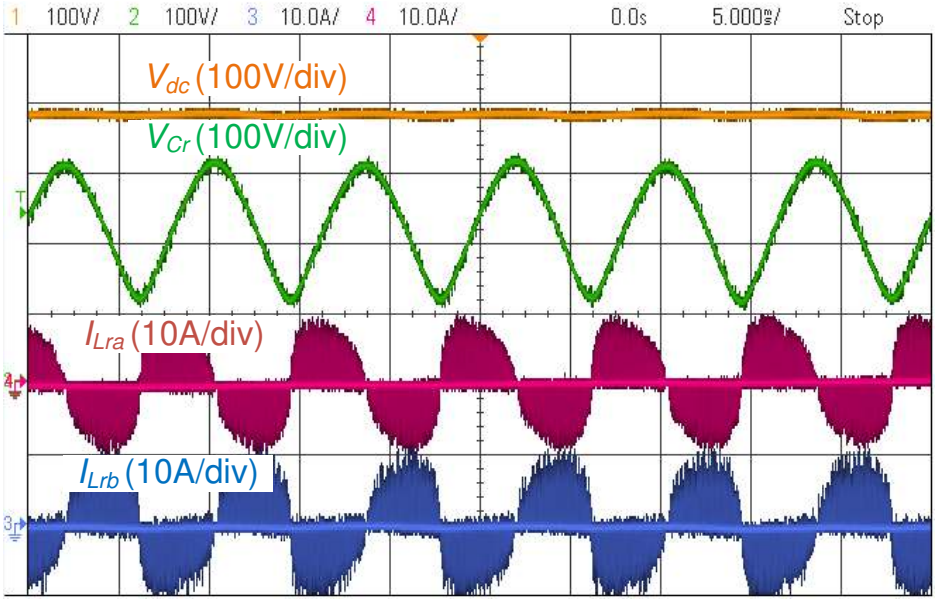


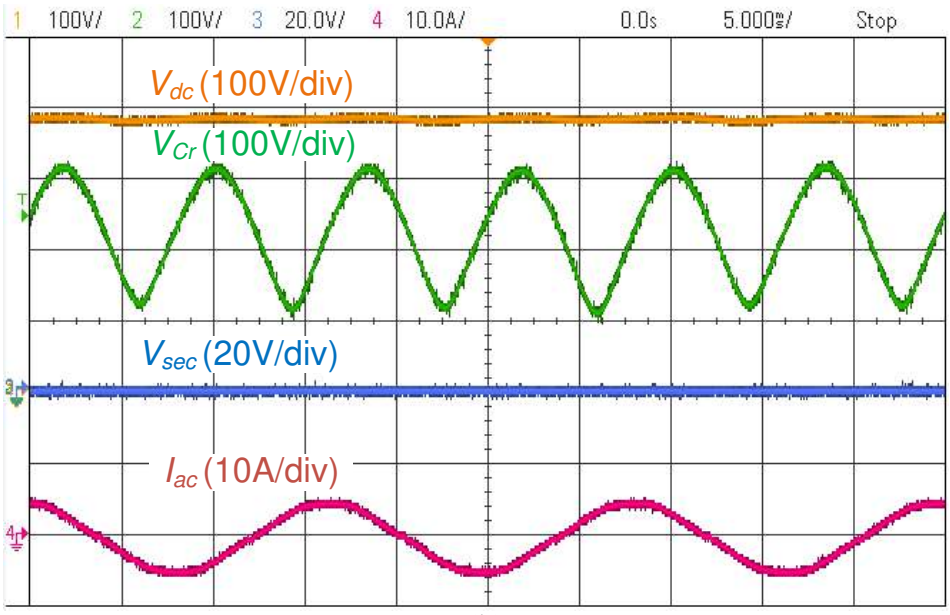
Fig. 5.41. Experimental results of the HV AF mode without AFAPM operation.

Fig. 5.42 (a) and (b) shows the experimental results with AF. In this case, the dc load is in the same condition. The HV dc bus voltage V_{dc} is 380 V with relatively small voltage ripple and the AF capacitor's voltage V_{cr} is fluctuated between 90 V to 310 V. The directions of the two inductor currents I_{Lra} and I_{Lrb} are opposite to each other. The

peak current on both inductor is 10 A. As the result of the flux cancellation, the voltage on the transformer secondary winding V_{sec} is zero.



(a)



(b)

Fig. 5.42. Experimental results of the HV AF mode with AFAPM operation.

5.5 CONCLUSIONS

In this chapter, three integrated AFAPM converters are proposed. They are not a LV battery charger, but also an AF for the HV battery charger.

The first integrated converter shares the primary full bridge. By using the two bridges in parallel, the ratings for switches between the 2.4 kW LV APM mode and 6.6 kW HV AF mode are kept almost unchanged. By reducing the current rating on the primary stage's switches, WBG devices such as SiC MOSFETs can be used and, thus, a higher switching frequency is feasible. By increasing the switching frequency on the primary switches, the size of the AF's inductor can also be reduced. Therefore, for a 6.6 kW HV battery charger, the proposed method can reduce the cost to 47.3% of the cost of traditional capacitor method and 66.8% of the cost of conventional active filter method in terms of harmonic energy storage for dual-voltage charging system in the electrified vehicles.

For the DAB-based full integrated converter, every component is shared between the AF mode and APM mode. Therefore, the required dc-link capacitance in the HV battery charger can be reduced significantly without any extra active filtering components. However, during the AF mode, the converter efficiency will be lower compare to other integrated AFAPM converters, as the high-voltage low-current harmonic energy has to be transformed into the secondary stage and converted into low-voltage high-current harmonic energy.

For the primary full-integrated AFAPM converter, a full bridge and auxiliary inductors are shared between the DAB APM converter and the two-phase buck AF converter. Only an active harmonic energy storage capacitor is needed to achieve active filtering. As a result, from the harmonic energy storage aspect for the 6.6 kW HV battery charger in the vehicle applications, with the proposed AFAPM method, the cost can decrease further to 31.6% of the cost of traditional capacitor method and 44.7% of the cost of conventional AF method.

Chapter 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this thesis, integrated AFAPMs have been presented in electrified vehicle applications.

A topological evaluation has been conducted particularly for the APM in the electrified vehicle applications. Several base primary and secondary topologies including full bridge, half bridge, Quasi-switched-capacitor bridge, center-tapped rectifier, and current doubler have been reviewed and compared in terms of VA rating and performance. A multiple input/output topology configurations including single-input-multiple-output, multiple-input-multiple-output have been compared in terms of different connection configuration and control schemes. The MOSFET loss analysis has been presented. Based on the MOSFET loss analysis, the input-series-output-parallel full bridge current doubler presents better performance based on the switch efficiency and cost analysis.

It has been proven that the power switch devices and capacitors are the most vulnerable components in the power electronic systems. In the meanwhile, film capacitor takes up large volume in the traction inverter and HV battery charger. A capacitor-less

design is relatively urgent for the next generation electrified vehicle application. AF is one promising solution to reduce the corresponding dc-link capacitance. However, additional components are required which increases the system complicity. Hence, it would be great to integrate the AF into the LV battery charger for the vehicle applications. In terms of power switch requirements, evaluations of the AFAPM have been done for traction inverter and HV battery charger, respectively. The results show that the size of the dc-link capacitor in the traction inverter is determined by the switching ripple. In addition, the power rating of the traction inverter is much higher than the LV battery charger in a typical electrified vehicle. Hence, the AFAPM in the traction drive system is practically challenging. While the size of the dc-link capacitor in the HV battery charger is determined by the second-order harmonic power rather than switching ripple. In the meanwhile, the power rating of the HV battery charger is similar to the LV battery charger. Therefore, the AFAPM in the HV battery charger system is feasible. Furthermore, a simple and effective dual-mode dual-voltage charging system operating principle is proposed. The integrated AFAPM converter charges the LV battery when the vehicle is running and operates as an AF when the vehicle is connected to the grid and the HV battery is charging. Hence, the low-frequency second-order harmonic current is alleviated without a bulk capacitor bank in the HV battery charger.

For magnetic design, there is a trend toward integration and planarization. Planar magnetic components intrinsically provide lower profiles than conventional wire-wound components, aiding the miniaturization of power converters. The low profile planar cores lead to a better surface-to-volume ratio. This provides a better thermal characteristic

under the heat exchange surface, and thus yields a better thermal characteristic. The step-by-step design guide for the planar transformer has been presented. The interleaving winding structure provides a small leakage inductance and also reduces the proximity effect loss. This yields a more uniformed current distribution and thus a higher efficiency. A conventional planar transformer has been designed for full bridge current doubler converter. Another planar transformer with a minimized leakage inductance has been designed for the dual active bridge converter.

Three different integrated AFAPM converters are proposed. The first integrated converter shares the primary full bridge. By using the two bridges in parallel, the ratings for switches between the 2.4 kW LV APM mode and 6.6 kW HV AF mode are kept almost unchanged. By reducing the current rating on the primary stage's switches, WBG devices such as SiC MOSFETs can be used and, thus, a higher switching frequency is feasible. By increasing the switching frequency on the primary switches, the size of the AF's inductor can also be reduced. Therefore, for a 6.6 kW HV battery charger, the proposed method can reduce the cost to 47.3% of the cost of traditional capacitor method and 66.8% of the cost of conventional additional AF method in terms of harmonic energy storage for dual-voltage charging system in the electrified vehicles. A 1.2 kW 100 kHz proof-of-concept prototype has been built with SiC MOSFETs on the primary stage. The experiments show promising results confirming the effectiveness of the proposed concept.

Second one is the DAB-based full integrated converter. As every component is shared between the AF mode and APM mode, the required dc-link capacitance in the HV battery charger can be reduced significantly without any extra active filtering components. However, during the AF mode, the converter efficiency will be lower compare to other integrated AFAPM converters, as the high-voltage low-current harmonic energy has to be transformed into the secondary stage and converted into low-voltage high-current harmonic energy. Simulation has been conducted to verify the effectiveness of the proposed converter.

The third one is the primary full-integrated AFAPM converter. The primary full bridge and auxiliary inductors are shared between the DAB APM converter and the two-phase buck AF converter. Only an active harmonic energy storage capacitor is needed to achieve active filtering. As a result, from the harmonic energy storage aspect for the 6.6 kW HV battery charger in the vehicle applications, with the proposed AFAPM method, the cost can decrease further to 31.6% of the cost of traditional capacitor method and 44.7% of the cost of conventional additional AF method. A 720 W prototype has been built and experiments show promising results confirming the effectiveness of the proposed converter.

6.2 Future work

Based on the proposed dual-voltage charging systems, other AFAPM converter topologies can be proposed. A comprehensive comparison can be made for the family of AFAPM converter topologies in terms of power density, switch rating, and efficiency.

Also, the SiC MOSFETs have been applied on the primary stage of the converter. It would be attractive to have WBG devices on the secondary stage as well. The Gallium nitride (GaN) is a promising candidate on the LV stage. It would be an attractive converter which has SiC on the HV primary stage and GaN on the LV secondary stage. In addition, the switching frequency of the implemented converters is 100 kHz. It is possible to increase the switching frequency further and thus, shrink the overall size of the converter.

The AF control strategy in this thesis is feed-forward control. It is also possible to apply close-loop control to the AFAPM converter (e.g. PR control). Other advanced control strategy can also be applied to achieve better active filtering performance.

From the magnetic design aspect, in order to shrink the converter size further, the transformer and inductor can be integrated together. An integrated planar transformer and inductors would be a promising design to increase the power density of the converter. A coupled inductor design can also be applied to the primary full-integrated converter. By doing so, different inductance values can be achieved for AF mode and APM mode. This will yield a broad inductance selection for this integrated converter.

Furthermore, one potential issue for this dual-mode dual-voltage charging system will the LV power during the HV battery charging mode. If the HV battery charging time is relatively short (i.e., within an hour), the LV battery should be able to provide the power to the nonpropulsion loads during that time. However, if the HV battery needs to be charged with a quite long time period, it is necessary to have the AFAPM converter to

provide the LV power in the HV battery mode. One of the potential solutions would be the burst mode charging. The original purpose of this charging method is to improve the converter battery charging efficiency at the light load and standby condition without any auxiliary circuits. Instead of operating the converter continuously at the light load, the converter is operated at the medium power or high power for a relatively short time period and then completely turned off for the rest of the time. Hence, several LV charging pulse current can be added during the HV battery charging time and thus maintain a LV power during the HV battery charging with a higher charging efficiency.

The second potential solution will be the modular AFAPM converter. As the output current of the conventional APM converter is relatively high. It would be attractive to have a modular structure in terms of scalability and efficiency. A modular AFAPM converter provides more degrees of freedom for the dual-voltage charging schedule. Then, considering from the HV and LV battery energy storage aspect, the dual-mode charging strategy can be optimized.

Last but not least, as the proposed dual-voltage charging systems are proof-of-concept design, the power rating is limited to around 1 kW. The HV battery charger applied in this thesis is a 360 W commercial PFC. The future work could be to implement a 6.6 kW high power HV battery charger. Then an accurate comparison can be made in terms of the size and weight with different design methods (i.e., traditional capacitor, conventional extra active filter and the proposed AFAPM method).

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