Integrated Chaos Generators

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Invited Paper

This paper surveys the different design issues, from mathematical model to silicon, involved on the design of integrated circuits for the generation of chaotic behavior.

Keywords*—*Analog CMOS, chaos, design methodology, design system, nonlinear circuit design.

I. INTRODUCTION

The design of electronic circuits with customized controllable chaotic behavior has potential interest in many application scenarios such as instrumentation, analog signal processing, and communication and ranging systems. Regarding instrumentation, chaotic circuits represent an efficient alternative for nonrepeatable pseudorandom signal generation. Such generators are useful for the implementation of noise sources—both white and colored—which are frequently employed at speech processing [1] and for testing the dynamic behavior of electronic systems [2], among many other applications [3]. On the other hand, chaos generators can be used in analog signal processing applications as a dither source to improve the performance of other blocks. For instance, dithering can be used to whiten the noise floor of $\Sigma\Delta$ modulators, as well as to reduce the (idle channel) spurious tones, which are introduced during quantization of direct current (dc) inputs (audible in voice-band applications) [4], [5]. Also, dithering can be used to improve the integral nonlinearity of high-performance Nyquist-rate analog-to-digital converters [6]. In another application, chaos generators can be used, together with certain dynamic element matching mechanisms, to make digital-to-analog errors average to zero over multiple sample instances [7]. In ranging systems, the nonperiodicity of chaotic signals, as well as the rapid decorrelation of their time-shifted sequences, make the use of chaos an interesting coding technique for high resolution radar systems [8]. Finally, chaotic circuits play a prominent role in chaos-based digital communication systems as they supply the required sample functions to which information symbols are mapped to [9]. In these systems, chaos generators, instead of conventional frequency synthesizers, provide the *communication carriers*, which are modulated by the digital information that is transmitted. Inherent to this chaotic modulation, the digital information also experiments a bandwidth *spreading* as a consequence of the wideband and noise-like spectral properties of chaos. This capability of simultaneous modulation and spreading, with an *a priori* lower system complexity than traditional *spread spectrum* techniques, is deserving a considerable research interest during the last years.

In the aforementioned applications, chaotic circuits can be realized by interconnecting discrete integrated circuit (IC) component parts on a printed circuit board. However, whenever system miniaturization and/or power consumption are issues, chaotic circuits must be realized as monolithic ICs, preferably in standard complementary metal–oxide–semiconductor (CMOS) technologies where they can be embedded with other digital and analog circuitry. The objective of this paper is, indeed, to survey the different design techniques, both at system and circuit levels, involved in the monolithic realization of chaotic ICs.

Though the design of chaotic generators can be afforded from different perspectives as, for instance, by adjusting the parameters of well-known oscillators or phase-locked loop structures [10], this paper focuses on a systematic *state-space* approach, which lead to more general solutions, based on the electronic synthesis of the system state equations. Following this approach, Section II reviews the mathematical models leading to chaotic behavior and identifies the basic building blocks required for their implementations. They are classified into linear (covered in Sections III and IV) and nonlinear (described in Section V) operators. Finally, Section VI

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presents three chaotic IC prototypes which illustrate the application of the methodological aspects and circuit concepts previously described.

II. Mathematical Models for Chaos Generation

Every mathematical model able to produce chaotic behavior has two basic ingredients: *dynamics* and *nonlinearity.* Regarding dynamics, models for chaos generation can be classified into *discrete-time* or *continuous-time*, depending on whether the system evolution is described by nonlinear difference or differential equations, respectively. Another possible classification is between *autonomous* or *nonautonomous* systems, which depends on whether the generator is able or not to self-sustain chaotic oscillations without any external driving excitation. Because this last classification has a weak impact regarding IC implementation, we will focus exclusively on the autonomous case.

In the following, we will separately review the basic features of discrete-time and continuous-time chaos generators, identifying the basic operations needed for their synthesis. As already mentioned, a systematic state-space approach will be used as the theoretical framework to express (and later to implement) the different chaotic systems.

A. Discrete-Time Chaos Generators

Autonomous discrete-time systems (or discrete maps, in short) can be generally described by the following qth (delay) order n-dimensional (n-D) finite-difference equation (FDE):

$$\mathbf{x}(k+q) = \mathbf{F}[\mathbf{x}(k+q-1), \ldots, \mathbf{x}(k); \mathbf{P}] \qquad (1)$$

where $k = 0, 1, 2 \ldots$ symbolizes the discrete-time variable, $\mathbf{x}(k) = [x_j(k)]^\dagger \in \Re^{n\times 1}$ represents the state vector of the system at the kth discrete time instant, and $\mathbf{F}(\cdot; \mathbf{P})$ is a n-D time-invariant nonlinear vector field that depends on the parameter set $\mathbf{P}$. For the purposes of signal generation, we will assume that system (1) is characterized by an *invariant set* J under $\mathbf{F}(\cdot; \mathbf{P})$, such that any trajectory starting in J remains confined to it. Additionally, the model may also include a p-D output equation defined in terms of the r most recent states of the system

$$\mathbf{y}(k+r) = \mathbf{G}[\mathbf{x}(k+r), \ldots, \mathbf{x}(k+1); \mathbf{Q}] \qquad (2)$$

where $\mathbf{y}(k) \in \Re^{p\times 1}$ is the output vector of the discrete map at the kth instant and $\mathbf{G}(\cdot; \mathbf{Q})$ is a function, in general, nonlinear and parameterized by a vector $\mathbf{Q}$.

Among the discrete maps defined by (1), first-order systems ($q = 1$) play a major role as they model most of the electronic chaos generators proposed so far. Their state equation may be written as

$$\mathbf{x}(k+1) = \mathbf{F}[\mathbf{x}(k), \mathbf{P}] = \mathbf{A}\mathbf{x}(k) + \mathbf{B}\boldsymbol{f}[\mathbf{x}(k)] + \mathbf{C} \qquad (3)$$

where $\mathbf{A} \in \Re^{n\times n}$, $\mathbf{B} = [\mathbf{b}_i] \in \Re^{n\times m}$, $\mathbf{C} \in \Re^{n\times 1}$, and $\boldsymbol{f}(\cdot) = [f_i(\cdot)]^\dagger \in \Re^{m\times 1}$ is a nonlinear time-invariant vector field ($j = 1, \ldots, n$ and $i = 1, \ldots, m$). Fig. 1 shows a block diagram for first-order discrete-maps comprising a *linear* section, a *nonlinear function* block connected in a feedback loop [11] and an output stage. The linear section, included in the dashed box of Fig. 1(a), consists of static and dynamic elements. The static elements realize the operations of summation and scaling (blocks labeled $\mathbf{A}$ and $\mathbf{B}$). On the other hand, the dynamic element performs sample-and-hold (S/H) and delay operations, as shown in Fig. 1(b). Usually, such element is implemented by a single electronic device which, hereafter, will be represented by the symbol in the inset of Fig. 1(a) and denoted as *delay element.* The clock signal fixing the sampling period of the delay element determines the iterations of the feedback loop.

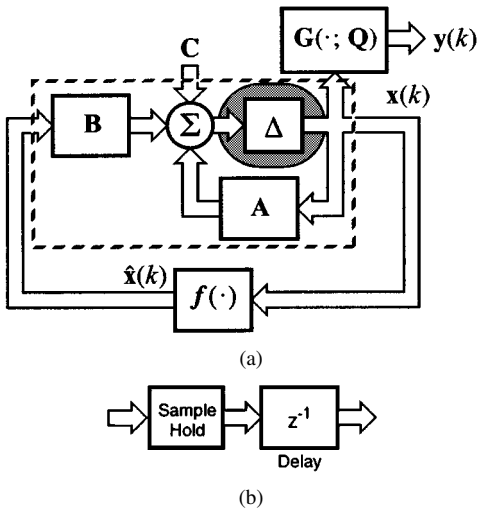


Fig. 1. (a) Block diagram of a first-order FDE-based chaos generator. (b) Operations encompassed in the Δ block [element in the inset of Fig. 1(a)].

Table 1
Short Catalog of Chaotic Discrete Maps

Discrete map	A	B	C	$f(\cdot)^{\dagger a}$
Parabolic [11]	-	$-A$	B	$x_1(k)^2$
Logistic [12][13]	-	B	$-A$	$A^2 - x_1(k)^2$
Circle [14]	1	B	-	$[1 - A\sin(x_1(k))]^{-1}$
Tent [13] [15][16][17]	-	$-B$	A	$\lvert x_1(k)\rvert$
Bernoulli [15][18]	B	$-A$	-	$sgn(x_1(k))$
Aihara [19][20]	B	$-A$	S	$sat(x_1(k), \varepsilon)$
Congruent [21][22]	B	$-2A$	-	$H(x_1(k) - A) - H(x_1(k) + A)$
Hopping [23]	B	$-C$	-	$u_-(x_1(k) + A) + u_+(x_1(k) - A)$
Henon [11][13]	$\begin{bmatrix} 0 & 1 \\ B & 0 \end{bmatrix}$	$\begin{bmatrix} -A \\ 0 \end{bmatrix}$	$\begin{bmatrix} C \\ 0 \end{bmatrix}$	$x_1(k)^2$
Lozi [11]	$\begin{bmatrix} 0 & 1 \\ B & 0 \end{bmatrix}$	$\begin{bmatrix} -A \\ 0 \end{bmatrix}$	$\begin{bmatrix} C \\ 0 \end{bmatrix}$	$\lvert x_1(k)\rvert$

a. Functions $sgn(\cdot)$, $sat(\cdot)$, $H(\cdot)$, $u_-(\cdot)$, and $u_+(\cdot)$ are defined in Table 4.

Table 1 contains a short catalog of first-order discrete maps which have been implemented in electronic form, either by means of discrete components or integrated on silicon. For

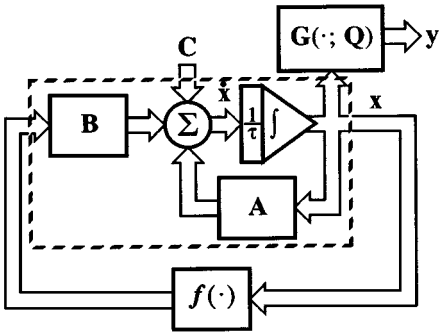


Fig. 2. Block diagram of an ODE-based chaos generator.

each entry, Table 1 shows the particular settings for $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ and $\boldsymbol{f}(\cdot)$, according to (3). The definition interval of the maps and their parameter ranges to achieve chaotic regime can be found in the references attached to the first column of Table 1.

An important conclusion that can be drawn from Table 1 is that chaotic behaviors can be obtained from very simple mathematical models. Indeed, a single state-variable is required to generate chaos, as occurs in the 1-D maps listed in the first eight rows of Table 1. Thereby, simple monolithic realizations can be expected from the use of discrete maps. In spite of this structural simplicity, the dynamic behavior of the system can be extremely rich and complicated. This will be illustrated in Section VI by means of the *Bernoulli* map defined in the fifth row of Table 1.

B. Continuous-Time Chaos Generators

As already mentioned, continuous-time chaos generators are those that can be described by nonlinear differential equations. Among them, we can further distinguish between those based on ordinary differential equations (ODEs) and those based on delay-differential equations. The latter have been recently proposed as an efficient method for the generation of high fractal dimension chaos with no substantial increase on complexity (a first order system is enough to produce chaotic behavior) [24]. Nevertheless, these systems are still far from being well understood and we will focus on ODE-based systems, for which a lot of research has been done in the last decades.

Autonomous continuous-time ODE-based chaos generators belong to the space $L_{n,m}$ of n-D dynamical systems with m nonlinear elements, defined by the state equation

$$\tau \frac{d}{dt}\mathbf{x}(t) = \mathbf{F}[\mathbf{x}(t), \mathbf{P}] = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\boldsymbol{f}[\mathbf{x}(t)] + \mathbf{C} \quad (4)$$

where τ is a diagonal matrix defining the time-integration constants of the system, $\mathbf{x}(t) = [x_j(t)]^\dagger \in \Re^{n\times 1}$ is the state vector, $\mathbf{A} \in \Re^{n\times n}$, $\mathbf{B} = [\mathbf{b}_i] \in \Re^{n\times m}$, $\mathbf{C} \in \Re^{n\times 1}$, and $\boldsymbol{f}(\cdot) = [f_i(\cdot)]^\dagger \in \Re^{m\times 1}$ is a nonlinear vector field ($j = 1, \ldots, n$ and $i = 1, \ldots, m$). Such systems can be mapped onto the analog computer concept of Fig. 2. It consists of a forward path containing a linear time-invariant subsystem (included in the dashed box of Fig. 2), a feedback path including the nonlinear elements of $\boldsymbol{f}(\cdot)$, and an additional path to synthesize the output vector $\mathbf{y}(t) = \mathbf{G}[\mathbf{x}(t), \mathbf{Q}]$. As can be seen, the only difference between the conceptual diagram in Fig. 2 and that associated to first-order discrete maps in Fig. 1(a) is the use of integrators instead of delay elements. This apparently minor change has, however, strong implications regarding system design, as will be shown next.

Table 2 includes some exemplary ODE-based chaotic systems found in the literature. Conditions on the different system parameters $\mathbf{P}$ to guarantee chaotic behavior can

Table 2
Catalog of ODE-Based Autonomous Chaotic Oscillators

Continuous-Time System	A	B	$f(\cdot)$[†a]
Canonical model with ON-OFF switching, [27]	$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ -1 & 0 & -1 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ -a \end{bmatrix}$	$f_1(\mathbf{x}) = u_+(x_2 - L) + LH(x_2 - L)$
Chaotic oscillator with Heaviside operator, [28]	$\begin{bmatrix} a & -b & -1 & b \\ 1 & 0 & 0 \\ c & 0 & -c \end{bmatrix}$	$\begin{bmatrix} d \\ 0 \\ 0 \end{bmatrix}$	$f_1(\mathbf{x}) = H(L - x_3)$
Double-Scroll-like oscillator, [29]	$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ -a & -a & -a \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ a \end{bmatrix}$	$f_1(\mathbf{x}) = sgn(x_1)$
Colpitts oscillator, [30]	$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & a \\ c & c & b \end{bmatrix}$	$\begin{bmatrix} d \\ 0 \\ 0 \end{bmatrix}$	$f_1(\mathbf{x}) = u_+(x_2 - L)$
Chaotic oscillator with convex extension operator, [31]	$\begin{bmatrix} 0 & 0 & 0 \\ 0 & a & -b \\ 0 & c & -d \end{bmatrix}$	$\begin{bmatrix} \alpha \\ 0 \\ -\alpha \end{bmatrix}$	$f_1(\mathbf{x}) = u_-(z - L) + L$ $z = x_3 - x_1$
Chua´s oscillator, [32]-[35]	$\begin{bmatrix} -c & a & 0 \\ 1 & -1 & 1 \\ 0 & -b & 0 \end{bmatrix}$	$\begin{bmatrix} -d \\ 0 \\ 0 \end{bmatrix}$	$f_1(\mathbf{x}) = sat(x_1, L)$
Modified Chua´s oscillator, [27]	$\begin{bmatrix} a & -1 & c \\ 1 & -b & 0 \\ e & 0 & -e \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ -d \end{bmatrix}$	$f_1(\mathbf{x}) = u_+(x_3 - L) - u_-(x_3 + L)$
Lorenz system, [36]	$\begin{bmatrix} -a & a & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -b \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}$	$f_1(\mathbf{x}) = (c - x_3)x_1$ $f_2(\mathbf{x}) = x_1 x_2$
Modified Lorenz system, [27]	$\begin{bmatrix} -a & a & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -b \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}$	$f_1(\mathbf{x}) = (c - x_3)sgn(x_1)$ $f_2(\mathbf{x}) = \lvert x_1 \rvert$
Hyperchaotic oscillator, [37]	$\begin{bmatrix} a & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -c \\ 0 & 0 & b & 0 \end{bmatrix}$	$\begin{bmatrix} -d \\ 0 \\ d \\ 0 \end{bmatrix}$	$f_1(\mathbf{x}) = u_+(x_1 - x_3 - L)$
Quad hysteresis oscillator,[†b] [38], [39]	$\begin{bmatrix} 0 & 1 \\ -b & -a \end{bmatrix}$	$\begin{bmatrix} d & 0 \\ 0 & c \end{bmatrix}$	$f_1(\mathbf{x}) = hyst(x_1, L)$ $f_2(\mathbf{x}) = hyst(x_2, L)$

a. Functions $sgn(\cdot)$, $sat(\cdot)$, $H(\cdot)$, $u_-(\cdot)$, and $u_+(\cdot)$ are defined in Table 4.
b. To be precise, $hyst(\cdot)$, also represented in Table 4, is not a function, but a functional which, for the sake of conciseness, has been also included in the $\boldsymbol{f}(\cdot)$ column.

be found in the references attached to the first column of Table 2. The remaining columns indicate, respectively, matrices $\mathbf{A}$, $\mathbf{B}$, and the elements of the vector field $\boldsymbol{f}(\cdot)$ in accordance to the state representation in (4) (in all cases, $\mathbf{C}$ is a null vector and τ is the identity matrix). Circuit demonstrators using off-the-shelf discrete electronic devices have been reported for all the examples in Table 2 and those in rows 3, 7, 9, and 12 have been also implemented in monolithic form.

Table 2 reveals a well-known fact: in autonomous ODE-based systems, three state variables are at least required to generate chaos if the nonlinear feedback path in Fig. 2 is memoryless. Otherwise, if the vector field $\boldsymbol{f}(\cdot)$ exhibits hysteresis, as occurs in the last row of Table 2, the jumps in the hysteretic elements correspond to additional states [36]. This is clearly in contrast with discrete maps for which single state-variable systems are enough to produce chaotic behavior.

C. General Considerations for the Design of Chaotic ICs

In the previous two sections, both the architectures and operations required for the systematic design of chaos generators using a state-space approach have been identified. One step ahead is to apply the appropriate transformations on the mathematical models to make them *suitable* for synthesis in monolithic form.

Such modifications must consider two different aspects that are related, on the one hand, to the particular nonlinear vector field $\boldsymbol{f}(\cdot)$ and, on the other, to the overall state equation of the dynamical system [defined by (3) for discrete maps or (4) for ODE-based generators].

First, let us consider the nonlinear vector field. The synthesis of arbitrary nonlinear functions in IC form can be achieved by relying to systematic representation techniques where operators are closely related to the nonlinearities available at the design primitives (details are given in Section V). Nevertheless, for the sake of reliability and also to reduce the hardware complexity of the design (and, hence, its area and power consumption), nonlinear vector fields should be made as "primitive-based" as possible in order to reduce the number of such elementary operators. It is, therefore, strongly suggested to properly alter the nonlinear vector field $\boldsymbol{f}(\cdot)$ (if it deviates too much from a simple primitive-based representation) while retaining the most relevant features of the targeted dynamic behavior. In particular, simplification strategies based on piecewise-linear (PWL) modeling are specially appealing for IC realization because of the accuracy and simplicity of their synthesis—it is ultimately based on the controled transition between the ON and OFF states of transistors, as nonlinear primitive operator. An example of piecewise linearization is given by the ODE-based systems in the rows 8 and 9 of Table 2, in which multipliers are replaced by simpler PWL nonlinearities, namely, sign inversion and absolute value operations. Another advantage of PWL modeling, in particular for high-accuracy IC implementations, is that the dynamical system becomes linear at each region of the space partition and, hence, well-defined calibration [38], [39] and tuning [40] mechanisms are readily applicable to precisely trim each of the affine characteristics.

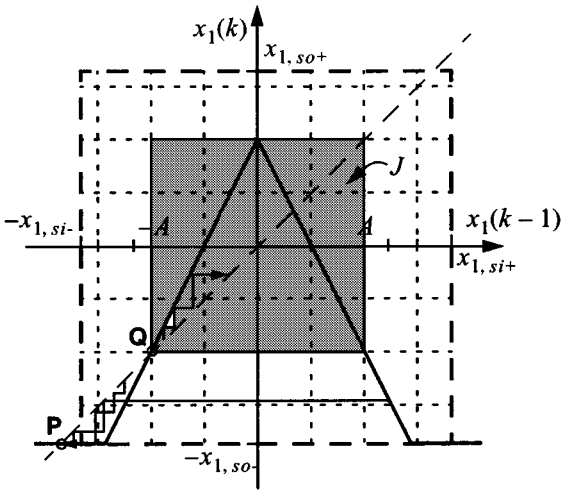


Fig. 3. Annihilation of chaotic dynamics in the tent map for $B = 2$.

Another important issue for the choice of an IC-suitable nonlinear vector field is the *robustness* of the system dynamics [22], [42]. Because of the limited accuracy of analog circuit implementations, models for chaos generators must be robust enough so that the unavoidable technological parameter deviations do not severely degrade the prescribed dynamic features. A main consequence of this fact is that some nonlinearities, which are often found in theoretical studies, must be precluded for electronic chaos generation, unless they are conveniently transformed. A typical example is offered by the tent map, defined in the fourth row of Table 1. In order to obtain a uniform distribution of the chaotic time-series, parameter B is set to 2, as illustrated in Fig. 3. In this configuration, if for some circuit impairment or noise contribution, the trajectory jumps outside the nominal invariant set J (shaded area in Fig. 3), the system evolves after a transient to the parasitic equilibrium point $\mathbf{P}$, which arises from the saturation characteristics of the circuit (long-dashed rectangle in Fig. 3). As a result, the chaotic behavior vanishes and the nominal invariant set collapses to the stable fixed point $\mathbf{P}$. To avoid this situation, the map must be transformed so that it exhibits a basin of attraction larger than its nominal invariant set, with a clearance between them determined by the maximum expected perturbations in the circuit implementation. Different strategies to achieve this goal can be found in [15], [22], [41], [42].

Let us, now, consider the overall state equation of the chaotic system. For similar reasons of reliability and cost, it should be simplified before implementation. This can be accomplished by, first, defining a family of dynamical systems that retains almost all features of the targeted model and, second, by identifying which element of such family is the most convenient from an IC perspective. Essential to the first step is the concept of *linear conjugacy*,[1] among dynamical systems [43], [44], as it guarantees that both the

[1]Two dynamics systems $\mathbf{F}(\cdot)$ and $\mathbf{H}(\cdot)$ are said to be linearly conjugated if there exists a nonsingular matrix $\mathbf{M}$ such that $\mathbf{M} \bullet \mathbf{F} = \mathbf{H} \bullet \mathbf{M}$ ("$\bullet$" denotes composition).

original model and the elements of its linearly conjugated family exhibit the same qualitative dynamics. Interestingly enough, it has been shown that for a wide class of dynamical systems, namely, those which can be represented in *Lur'e form*,[2] linear conjugacy between systems with the same vector field $\boldsymbol{f}(\cdot)$ is assured whenever the eigenvalues of corresponding matrices $\mathbf{A}$, $\mathbf{A}+\mathbf{C}\mathbf{w}^{\dagger}$ and $\mathbf{A}+\mathbf{b}_i\mathbf{w}^{\dagger}$, $i=1,\ldots,m$ are identical [44]. This implies that the family of linearly conjugated Lur'e forms built upon a given nonlinear vector field $\boldsymbol{f}(\cdot)$ can be exactly defined by n^2 less parameters than those nominally included in the representations (3) and (4)—together with vector $\mathbf{w}$. Hence, there exist infinitely many linearly conjugated elements able to reproduce the same qualitative dynamics as the original model, which allows one to establish a selection procedure aimed to determine that element most suitable for IC realization.[3] Some tailoring criteria for this selection procedure are [32].

1) *Low Complexity:* Because system parameters must be mapped into physical devices, those vector fields with a minimum number of different nonzero entries in $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{w}$—they are referred to as *canonical* elements—are *a priori* the best suited in terms of area and power consumption. In particular, those configurations with $\mathbf{B}$ proportional to a unitary vector are preferred because the vector field exhibits a single nonlinear block.
2) *Optimum Dynamic Range:* The dynamic range of a chaos generator is maximized as long as all its state variables are able to swing up to a maximum tolerable level imposed by the power supply of the circuit [1], [47]. The procedure by which this maximization can be achieved is *scaling* and basically consists on applying a convenient similarity transformation on the state vector $\mathbf{x}$. It is worth pointing out that scaling does not affect the system architecture (null entries to matrices $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{w}$ remain unaltered after scaling), but the canonical property of the original system may be lost, i.e., system parameters, initially with identical magnitude, turn to be different after scaling, thus leading to an increase on the system complexity.
3) *Reduced Mismatch:* Ratio accuracy (or matching) of similar components is enhanced as long as circuit elements are built by replicating a given unitary device [48]. Thus, if system parameters are related by integer ratios, the IC improves in accuracy and, at the layout level, in modularity and integration density. This improvement, however, reduces as the spread of system parameter values increases [48]. Thus, the unitary elements replication approach must be accompanied, in some cases, by techniques aiming to reduce the spread of system parameters [1]. Once again, this can be achieved by using a proper similarity transformation on the state variables.

A final (and critical) system-level consideration that must be addressed on the design of chaos generators is to evaluate the tolerance of the dynamic behavior against parameter deviations. Such deviations are due to the fact that physical circuit components (e.g., capacitors, operational amplifiers, comparators, etc.) deviate from nominal values or design intent because of a variety of nonidealities which can be grouped into three main categories, namely, *noise, static,* and *dynamic* [39]. Noise category basically comprises the errors due to thermal noise generated by solid-state devices. On the other hand, mismatch of ideally identical devices, which results from uncontrolled technological parameters in the fabrication process, and dc-related errors such as offset, signal-independent charge injection, and finite dc gain of active components can be grouped as static nonidealities. Saturation characteristics that result from the upward limited dynamic range of the circuit elements can be also seen as an static nonideality. Finally, dynamic errors sums all frequency dependent nonidealities such as signal-dependent charge injection, limited dynamic accuracy in comparators, limited slew-rate, and limited gain-bandwidth product in amplifiers.

In order to tie the degradation of the chaotic dynamics to the above nonidealities, each of the error sources must be conveniently modeled and incorporated in the nominal representations (3) or (4) [22], [32]. Then, a worst-case analysis, together with exhaustive simulations of the system including all nonideal effects, must be made to determine the specifications for the different building blocks of the architecture. This bridges the system and circuit levels in the design route of the chaos generator. Of course, there may be cases in which the calculated block requirements are beyond the limitations imposed by the technological process. This occurs either when the specifications for the chaos generator (usually given in terms of output statistics) are too restrictive or when the system architecture shows a large *sensitivity* to some parameter variations, making it impractical for silicon implementation. In this last case, if the mathematical model belongs to a family of linearly conjugated systems, a new element that is less sensitive to parameter inaccuracies must be found. In general, there is not a simple way to link chaotic system perturbations and deviations on statistic performance other than by long-run simulations. Only for PWL chaotic models, where the system behaves linearly at each region, a classical sensitivity analysis [49] on the eigenvalues pattern—which determines the qualitative dynamics of the generator—with respect to the circuit components can be useful to estimate how far the dynamic behavior deviates from the nominal one [32].

D. Concluding Remarks

In this section, we have explored different alternatives of chaos generators, given selection criteria for high-level optimization, and identified the basic operations involved in their implementation. Such operations can be classified between

[2]Dynamical systems in Lur'e form are systems defined by (3) and (4) in which the vector field $\boldsymbol{f}(\cdot)$, assumed memoryless, depends on $\mathbf{w}^{\dagger}\mathbf{x}$, where $\mathbf{w}\in\Re^{n\times 1}$. For our purposes, it will further assumed that Lur'e forms are *observable* in the classical sense of control theory [45].

[3]It is worth noting that multidimensional PWL representation with parallel boundary planes [46] can be also expressed in Lur'e form and, hence, they are also suitable for system level optimization—an additional advantage on the use of PWL models for chaos generation.

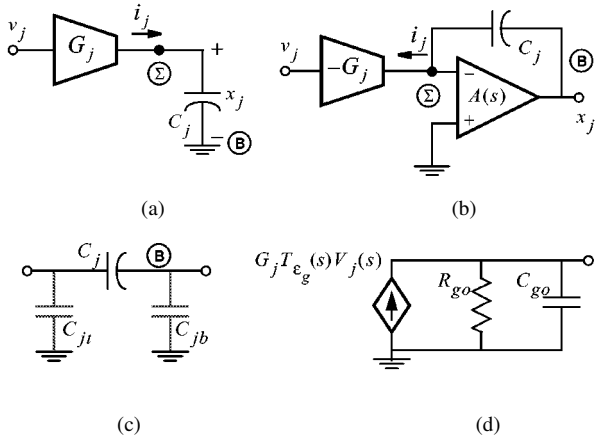


Fig. 4. Basic concepts for the continuous-time dynamics. (a) Open-loop integrator. (b) Miller integrator. (c) Parasitics of integrated capacitors. (d) First-order frequency-domain model of a transconductor.

linear and nonlinear and within the first group, between dynamic (continuous-time integrators and delay elements) and static (signal weighting and summation) operators.

In the following sections, we will present some general ideas and concepts for the IC realization of these operations, paying special attention to the nonidealities which affect them, as they ultimately determine the accuracy and operation speed of the chaos generator.

III. Linear Operators for Continuous-Time Generators

A. Integrators

Because monolithic inductors are only feasible at very high frequencies,[4] capacitors are the basic dynamic primitives of ODE-based chaotic ICs. State variables are, hence, voltages and the dynamic updating of these voltages is realized by driving the state capacitors through currents. Fig. 4 shows two alternative implementations of this dynamic updating: the open-loop [see Fig. 4(a)] and the Miller [see Fig. 4(b)] structures. In both cases, the excitation i_j is obtained for convenience as the result of a linear voltage-to-current transformation—using a transconductor—from an intermediate voltage v_j, i.e., $i_j = G_j v_j$. Ideally, both circuits obtain

$$\tau_j \frac{dx_j}{dt} = v_j \tag{5}$$

which corresponds to the behavior of an integrator with nominal time constant $\tau_j = C_j/G_j$ (j stands for the jth state variable of the system).

The differences between these alternative realizations arise when parasitics are accounted. In the foregoing analysis, considered parasitics are the following.

[4]Interestingly enough, some (integratable) classical oscillators based on passive resonant circuits, such as the Colpitts oscillator [28], can exhibit chaotic behavior upon proper parameter setting, thus giving the possibility of generating chaotic signals in the gigahertz range.

Table 3
Time-Constant Error and Approximated Poles of the Open-Loop and Miller Structures

	Open Loop	Miller
$\varepsilon_{\tau j}$	$\frac{C_{go}+C_{jt}}{C_j}$	$\frac{G_{go}}{C_j\omega_{ua}} + \frac{C_j+C_{go}+C_{jt}}{C_jA_0}$
$p_{\mathrm{L}j}$	$\frac{G_{go}}{C_j+C_{go}+C_{jt}}$	$< \frac{G_{go}}{C_jA_0}$
$p_{\mathrm{H}1j}$	-	$> \frac{C_j\omega_{ua}}{C_j+C_{go}+C_{jt}}$

1) Those associated with the capacitor [see Fig. 4(c)], consisting of two additional capacitors (bottom and top plates).
2) The first-order small-signal parasitics of the transconductor, namely: output resistance $R_{go} \equiv G_{go}^{-1}$, output capacitance C_{go}, and frequency-dependent transconductance $G_j(s) \equiv G_j T_{\varepsilon_g}(s)$ [see Fig. 4(d)].
3) The small-signal parasitics associated to the op-amp. Obviously, these are dependent on the op-amp architecture. Here, we assume that the op-amp is internally compensated, has low output impedance (negligible for analysis purposes), and can be modeled as [48]

$$A(s) = \frac{A_0\omega_a}{s+\omega_a} \equiv \frac{\omega_{ua}}{s+\omega_a}. \tag{6}$$

First of all, note that in the structures of Fig. 4(a) and (b), the capacitor terminal labeled $\mathbf{B}$ is connected to a *low-impedance* point (a point where the voltage changes only slightly for large current ranges). In Fig. 4(a), the terminal $\mathbf{B}$ is directly connected to an alternating current (ac) ground, while in Fig. 4(b), the low-impedance feature is achieved by the op-amp output node. Consequently, the two structures are insensitive to C_{jb}, i.e., the parasitic has virtually no influence on the circuit behavior.[5] Let us now separately analyze the circuits of Fig. 4(a) and (b).

In the structure of Fig. 4(a), the parasitic capacitors C_{jt} and C_{go} are connected in parallel with the nominal capacitor C_j. This makes the integrator time constant to deviate from its nominal value as $\tau_j \to \tau_j(1+\varepsilon_{\tau j})$, where the time-constant error $\varepsilon_{\tau j}$ is given in Table 3.

In addition, the parasitic resistances connected to the node Σ produce losses in the integration and, hence, the dynamic behavior deviates from the nominal one represented by $1/(s\tau_j)$. The actual transfer function is

$$\frac{X_j(s)}{V_j(s)} = \frac{1}{s\tau_j(1+\varepsilon_{\tau j})} T_{\varepsilon_g}(s) \frac{\frac{s}{p_{\mathrm{L}j}}}{\left(1+\frac{s}{p_{\mathrm{L}j}}\right)} \equiv \frac{T_{\varepsilon j}(s)}{s\tau_j(1+\varepsilon_{\tau j})} \tag{7}$$

where $p_{\mathrm{L}j}$ is the low-frequency pole created by the parallel connection of G_{go} and $C_j + C_{go} + C_{jt}$ (see Table 3) and

[5]This is not exactly true as this capacitor may influence the transient response of the op amp, especially when the op amp has a single-stage architecture [48].

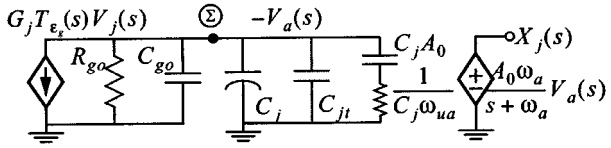


Fig. 5. Equivalent circuit for the analysis of the Miller configuration.

$T_{\varepsilon_g}(s)$ represents the transconductor frequency response.[6] The transfer function $T_{\varepsilon_j}(s)$ models the so-called *dynamic* error of the integrator. This error is negligible only for those frequencies, where $T_{\varepsilon_j}(s) \approx 1$. Neglecting at this point the influence of the transconductor, these frequencies are defined by $\omega \gg p_{\mathrm{L}j}$.

Consider now the Miller configuration of Fig. 4(b). To first order, the subcircuit formed by the op amp and the capacitor C_j can be represented by the equivalent circuit at the right of node Σ in Fig. 5—obtained by applying the Miller theorem. Analysis of this circuit obtains

$$\frac{X_j(s)}{V_j(s)} = \frac{1}{s\tau_j} \frac{s\omega_{ua}C_j/(C_j+C_{go}+C_{jt})}{(s+p_{\mathrm{L}j})(s+p_{\mathrm{H}1j})} T_{\varepsilon_g}(s) \quad (8)$$

which contains two poles at $p_{\mathrm{L}j}$ and $p_{\mathrm{H}1j}$, respectively, and displays time constant errors in the passband $p_{\mathrm{L}j} \ll \omega \ll p_{\mathrm{H}1j}$. Assuming that $p_{\mathrm{L}j}$ and $p_{\mathrm{H}j}$ are largely separated and that $C_j\omega_{ua} \gg G_{go}$, $\omega_a(C_j+C_{go}+C_{jt})$, one obtains the pole expressions shown in Table 3. Within the passband frequency range, where the circuit operates as an integrator, (8) can be approximated by

$$\frac{X_j(s)}{V_j(s)} \approx \frac{1}{s\tau_j} \frac{1}{1+\frac{G_{go}}{C_j\omega_{ua}}+\frac{C_j+C_{go}+C_{jt}}{C_jA_0}} T_{\varepsilon_g}(s)$$

$$\approx \frac{1}{s\tau_j(1+\varepsilon_{\tau j})} T_{\varepsilon_g}(s) \quad (9)$$

thus leading to the expression of $\varepsilon_{\tau j}$ given in Table 3. It shows that the time constant error is inversely dependent on the op-amp dc gain A_0 and, hence, very small.

Comparing the Miller and the open-loop configurations, the following conclusions can be drawn.

1) In the Miller configuration, the time constant error is attenuated by A_0. Hence, the Miller integrator exhibits superior performance regarding the influence of the parasitic capacitances. It is a consequence of the fact that, in the passband, the op amp exhibits very small input resistance given by $(C_j\omega_{ua})^{-1}$, which dominates over other impedances connected to this node. In the limit, as $\omega_{ua} \to \infty$, this resistance becomes null and the op-amp input becomes a *virtual ground*.
2) The low-frequency corner of the passband, given by $p_{\mathrm{L}j}$, is much smaller for the Miller than for the open loop. In the latter, the output conductance G_{go} manifests as such in the expression of $p_{\mathrm{L}j}$, while, for the Miller configuration, it manifests attenuated by $\sim A_0$. This is another positive consequence of feedback.
3) The high-frequency corner $p_{\mathrm{H}1j}$ is smaller for the Miller configuration—a negative consequence of feedback. In the open-loop configuration, the high-frequency behavior is limited by the dynamic response of the transconductor $T_{\varepsilon_g}(s)$, while in the Miller one, it is also limited by $p_{\mathrm{H}1j} \approx (C_j\omega_{ua})/(C_j+C_{go}+C_{jt})$. Assuming that the op amp and the transconductor are optimized, it is likely that the latter exhibits a frequency range wider than ω_{ua}, thus, inferring poorer frequency response for the Miller configuration than for the open-loop one.

Summarizing, the previous analysis shows that the open-loop configuration is preferable for high-frequency applications, though it may require *predistortion* to compensate for the time constant errors. On the contrary, the Miller configuration is more appropriate for low and medium frequencies, requiring no predistortion. Note, however, that the degradation of the frequency response in the Miller structure is mainly a consequence of the model used for the op amp. High-frequency advantages of the open-loop structure are not so evident if custom op amps without internal compensation are used [51]. In addition, frequency response of Miller structure may perhaps be enhanced by active compensation techniques [49] to properly shape the integrator high-frequency response and, thus, combine the features of accuracy, small losses, and large frequency bandwidth into a single structure.

Another comparison between the two configurations concerns their suitability for IC implementation. Specifically, the fact that ac grounded capacitors (i.e., those that have one of their terminals tied to either the positive or the negative power supply) are better suited than floating capacitors.

B. Signal Summation

The circuits of Fig. 4(a) and (b) can be extended to perform summing integration by routing all the voltage-to-current transformation outputs (each associated with a summing term) to node Σ and letting Kirchoff current law (KCL) to work. In this way, the basic structure to implement (4), conceptually shown in Fig. 6(a), is defined. Note that every summing term has an output conductance and an output capacitance. Hence, at node Σ, the equivalent conductance and capacitance are given, respectively, by

$$G_{go\Sigma} = \sum_{c=1,\,M} G_{goc} \approx M \cdot G_{go}$$

$$C_{go\Sigma} = \sum_{c=1,\,M} C_{goc} \approx M \cdot C_{go} \quad (10)$$

where G_{go} and C_{go} are mean values of the individual conductances and capacitances, respectively, and M is the number of excitations [according to (4) $M \leq n+m+1$]. After substituting G_{go} by $G_{go\Sigma}$ and C_{go} by $C_{go\Sigma}$ in the expressions of Table 3, we notice that $\varepsilon_{\tau j}$ increases proportionally with M for the open-loop configuration. The same enlargement is observed in the Miller integrator. However, the whole error for this configuration is still attenuated

[6]To first-order analysis, the frequency dependence of transconductances can be modeled by using a single pole $T_{\varepsilon_g}(s) \approx (1+s/\omega_g)$. This model can be valid for frequencies up to tens of megahertz. For more detailed models, see [50].

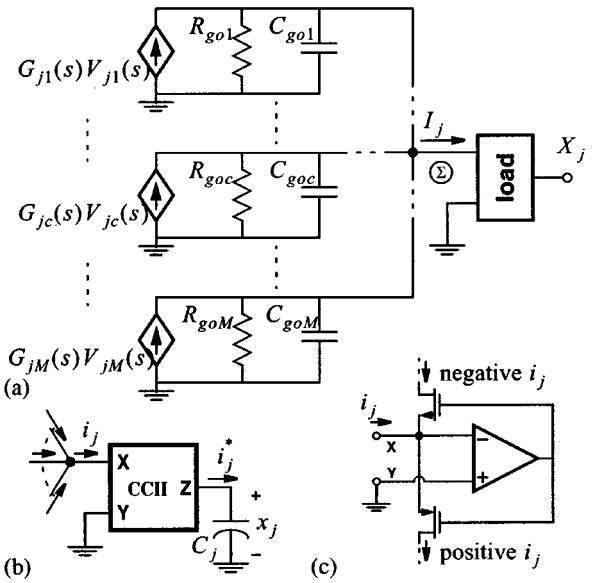


Fig. 6. (a) Obtaining the state variable updating current as the summation of M current components. (b) Using a second-generation current conveyor to isolate the summing node from the state variable node. (c) Concept for the realization of current conveyors.

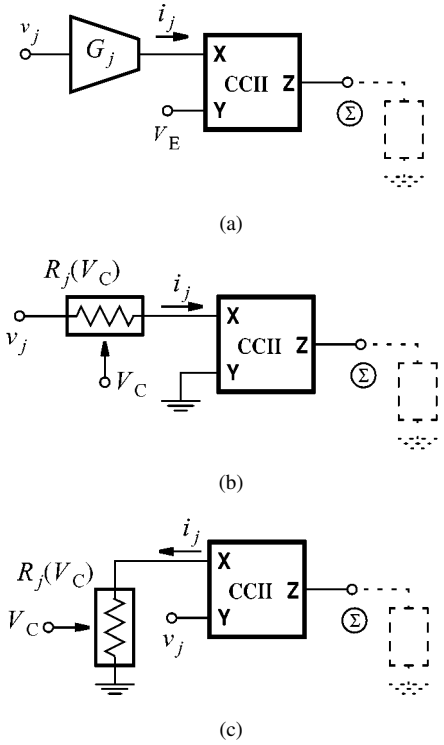


Fig. 7. Structures for voltage-to-current conversion in the case of (a) low output resistance, (b) floating self-coductor, and (c) grounded self-conductor.

by A_0. As a counterpart, the frequency behavior of the open-loop integrator remains virtually unchanged, while the value of $p_{\mathrm{H}1j}$ for the Miller configuration decreases inversely proportional to M.

A strategy to attenuate the errors caused by the summation of signals is to isolate the node where the currents are aggregated from that where the resulting current is applied to the state capacitor. This is represented in Fig. 6(b) for the open-loop configuration, although it can be used with the Miller configuration as well. The "glue" component is a *current conveyor* [52]. Actually, the current conveyor in Fig. 6(b) is of the so-called second generation, whose ideal behavior is described by

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}. \tag{11}$$

On the one hand, it creates a virtual ground between the terminals $\mathbf{X}$ and $\mathbf{Y}$. On the other, it realizes a current follower operation between the terminals $\mathbf{X}$ and $\mathbf{Z}$. Depending on the polarity of the current transfer between the $\mathbf{X}$ and $\mathbf{Z}$ terminals, the conveyor can be positive (CCII+) or negative (CCII-), which correspond respectively to the plus and minus signs in (11). In practice, the input terminals of the current conveyor can be realized by arranging two MOS transistors in feedback configuration around an op amp, as depicted in the conceptual circuit of Fig. 6(c). Then, the negative and the positive components of the input current can be rooted to the output node by using current mirrors [52]. Obviously, the current conveyor produces new errors that must be taken into consideration for proper design. First-order analysis of these errors can be found in [53].

C. Basic Strategies for Voltage-to-Current Transformation—Signal Weighting

Along this section, voltage-to-current transformation has been modeled through a transconductor, i.e., a component whose output resistance—modeled through R_{go} in Fig. 4(d)—is large by construction. Also, the transconductor input resistance has been implicitly assumed infinite and, consequently, loading errors at the transconductor driving node have been disregarded. However, in practice, voltage-to-current transformation is sometimes realized using circuits whose input and/or output resistances are not large by construction—for instance, MOS transistors operating in the ohmic region under strong inversion [54].

For transformation circuits having low input resistance, the only way to attenuate loading errors is driving the input node with low output resistance. On the other hand, for those having low output resistance, the loading problems can be attenuated by resorting to one of the structures of Fig. 7. In Fig. 7(a), the output node is clamped at a fixed value V_{E}, thus annulling spurious current contributions to i_j due to node voltage fluctuations. On the other hand, Fig. 7(b) and (c) is appropriate whenever the voltage-to-current transformation is realized by exploiting the self-conductance $G_j = 1/R_j(V_{\mathrm{C}})$ of either an active, i.e., composed of MOS transistors, or a passive resistor.

Other important issues on the design of voltage-to-current transformation circuits are briefly reviewed in the following.

Programmability: It basically refers to the possibility of scaling transconductances through electrical control

variables. For instance, the transconductance of a MOS transistor in the saturation regime under strong inversion depends on the large-signal transconductance factor β and on the gate voltage overdrive $V_{od} = V_g - V_{T0} - n_p V_s$ (see Fig. 12 in Section V for details). Two possible controlling scenarios, hence, arise:

1) taking advantage of the dependence of β on transistor geometry and of the MOS transistor operation as an analog switch to realize digitally controled β values;
2) taking advantage of the dependence on biasing conditions to realize analog-controled transconductance values.

It is worth pointing out that programmability is the basic mechanism for signal weighting and, hence, for the implementation of the coefficients of $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C}$ in (4).

Linearity: Another important issue regarding signal weighting is to guarantee linearity of the overall input–output characteristics. Because primitive components are essentially nonlinear (see Fig. 12), linearity on transconductances must be achieved by properly combining different elements. Many different strategies have been proposed for nonlinear cancellation as, for instance, by using differential configurations, by applying feedback, through inverse function techniques, etc. Some of these strategies are reviewed in [52].

Scaling Factor Accuracy: Scaling factor accuracy has two faces: absolute accuracy and ratio accuracy. The former refers to exactness in absolute values of transconductances and has tolerances of around 30%. Absolute accuracy is important in cases where timing is relevant. In these cases, a tuning mechanism must be incorporated to the circuit to reduce the tolerances to about 1%–2% [40], [49].

On the other hand, ratio accuracy, which was already considered as a selection criteria in Section II-C, can be made quite good—up to 0.1%—depending on the device areas, shapes, and distances [48].

IV. Linear Operators for Discrete-Time Generators

The implementation of delay elements for discrete maps always relies on the use of capacitors for storing and retrieving information in the form of voltages, switches for charging and/or discharging capacitors in response to a control signal, and active devices for defining the conditions of charge transfer. Main difference among analog sampled-data techniques come from the physical variables which is ultimately used to convey the information. Such variables can be in the form of voltages [switched-capacitor (SC) technique [11]), currents [switched-current (SI) technique [16]], timing characteristics of a pulse train (pulsewidth [13] or pulse-position modulation techniques [17]), or phase angles (phase-locking technique [14]), among other possibilities. In this paper, we will focus on SC and SI techniques.

The SC technique requires op amps, as active devices, and linear capacitors, as holding elements [1], [56], [57]. High-quality capacitors (high linearity, reduced voltage, and temperature dependence, and good matching properties) are available in technologies that offer parallel-plate structures separated by thin oxide [58], [59]. If such structures are not available, as in pure digital CMOS technologies, capacitors are commonly implemented by exploiting the thin-oxide gate capacitance of MOS transistors [60]. MOS-based capacitors usually exhibit larger capacitance per unit area and better matching than parallel-plate structures, but suffer from significant nonlinearities and parasitic capacitances, and must be conveniently biased to guarantee a low-resistivity conducting layer under the gate. As a result, SC circuits built on digital technologies have inevitably poorer performance than those implemented on analog-oriented processes.

An alternative sampled-data approach that avoids the need for highly linear capacitors is the SI technique [61]. In this case, capacitors are simply formed by the input parasitics of transconductors, thus, rendering the approach specially appealing for standard digital processes. Unfortunately, this notable simplification is at the expense of performance degradations. Nevertheless, in applications requiring moderate accuracy, the complexity and area consumption of SI circuits is generally lower than that of SC circuits performing the same function, which makes SI technique a fallback alternative when low-cost fabrication is mandatory.

A. Switched-Capacitor Linear Operators

Consider the basic S/H structure of Fig. 8(a) [1]. Analog switches are controled by a clock with two nonoverlapping phases, as shown in Fig. 8(c). Switches labeled ϕ_1 (respectively, ϕ_2) turn ON in synchronization with the first (respectively, second) clock phase.[7] The circuit operates as follows. In the acquisition phase, switches labeled ϕ_1 are ON and the op amp is configured as a unity-gain amplifier. Assuming that the op amp is ideal, the input voltage v_j is sampled by capacitor $C_{\rm S}$. In the holding phase, switch labeled ϕ_2 is ON and the bottom plate of the sampling capacitor $C_{\rm S}$ is connected to the op-amp output. Since the top plate of $C_{\rm S}$ remains connected to the inverting input of the op amp, the output voltage during the holding phase keeps the previously sampled input. Altogether, the operation of the S/H circuit can be described by the following recursive equation:

$$\begin{aligned} x_j(k+1) &= v_j(k+1/2) \\ x_j(k+1/2) &= 0 \end{aligned} \tag{12}$$

thus providing unity-gain half-cycle delay of the input voltage during the holding phase and null output during acquisition. Full-cycle delay elements, as required by (3), can be realized by simply cascading two half-delay stages with alternating S/H clock phases.

Taking advantage of the holding operation, SC techniques allow simple realizations of the aggregation and scaling functions. Consider, for instance, the SC circuit of Fig. 8(b) and assume the op amp is ideal. During phase ϕ_1, voltages v_{jc} are sampled by capacitors $C_{{\rm S}jc}$, $c = 1, 2, \ldots, M$, while capacitor $C_{{\rm I}j}$ is discharged as a result of the virtual ground at the input terminals of the op amp. During the next phase,

[7]By convention, any arbitrary signal $s(\cdot)$ observed at the end of the first (respectively, second) clock phase will be denoted as $s(k+1/2)$ [respectively, $s(k)$] $k = 0, 1, \ldots$, where T is the clock signal period [see Fig. 8(c)].

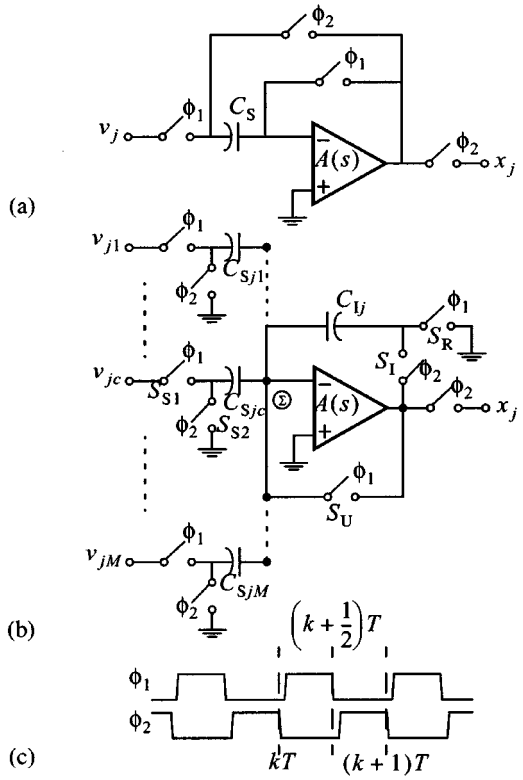


Fig. 8. (a) SC half-delay unity-gain block. (b) SC block for weighted summation. (c) Clock waveforms.

the charges stored in C_{Sjc} are fully transferred to capacitor C_{Ij}, thus, obtaining by the charge conservation principle

$$x_j(k+1) = \sum_{c=1,\,M} \frac{C_{Sjc}}{C_{Ij}} \cdot v_{jc}(k+1/2)$$
$$x_j(k+1/2) = 0 \tag{13}$$

which shows that, during the holding phase, the circuit accomplishes a weighted summation of the input voltages, as required by (3). Note that scaling factors are ideally defined by capacitor ratios $w_{jc} = C_{Sjc}/C_{Ij}$ and, hence, highly accurate. Furthermore, programmability can be quite easily incorporated to Fig. 8(b) by using digitally controled capacitor arrays [1].

Obviously, the above circuits deviate from the ideal behavior as long as parasitic effects are accounted. For simplicity, the foregoing analysis focus exclusively on the SC amplifier of Fig. 8(b) with a single input branch (subindex c is omitted for the sake of clarity). Considered parasitics are the following.

1) The small-signal parasitics associated to the op amp, as depicted in Fig. 4(d), assuming that the frequency-dependence of the transconductance is negligible. An additional parasitic input capacitance to ground C_{pa} is also considered.
2) The finite resistance of the switches in the ON state. For simplicity, it is assumed that the sampling switches S_{S1} and S_{S2} of Fig. 8(b) are identical with ON resistance R_S. ON resistances of switches S_R, S_U, and S_I are, respectively, R_R, R_U, and R_I.

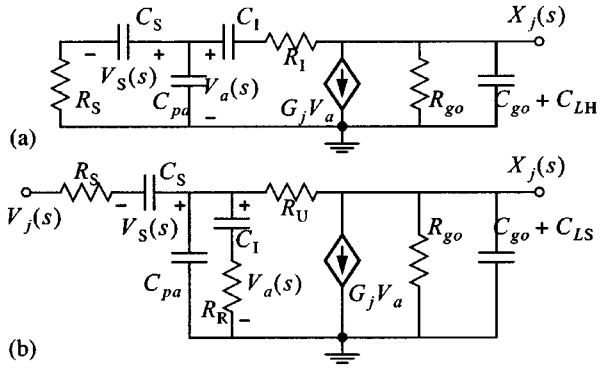


Fig. 9. Equivalent circuits for the analysis of the (single input branch) SC amplifier of Fig. 8(b) during (a) the holding phase and (b) the sampling phase.

Analysis of other nonideal effects as, for instance, op-amp offset voltage, limited slew-rate, capacitor mismatch or nonlinearities of the capacitors, switches, and op-amp dc gain can be found elsewhere [1], [62]–[65].

Fig. 9(a) and (b) shows the equivalent circuits for the SC amplifier of Fig. 8(b), valid for the holding and sampling phases, respectively. Generic loading capacitances C_{LH} and C_{LS} have been included in the models.

Let us first consider the holding phase [Fig. 9(a)] and assume that switch-ON resistances are negligible. In this case, the transfer function from the voltage stored at the sampling capacitor to the output node reads as

$$\frac{X_j(s)}{V_S(s)} = \frac{C_{Sj}}{C_{Ij}} \cdot \frac{\beta_j[sC_{Ij} - G_j]}{s[C_{TH} + C_{Ij}(1-\beta_j^2)] + G_j(1/A_0 + \beta_j)} \tag{14}$$

where $A_0 = G_jR_{go}$, $C_{TH} = C_{go} + C_{LH}$ is the total output capacitance during the holding operation mode and

$$\beta_j = \frac{C_{Ij}}{C_{Ij} + C_{Sj} + C_{pa}} \tag{15}$$

is called the feedback factor of the SC amplifier. Equation (14) shows that the dc gain of the SC amplifier stage is given by

$$w_j = \frac{C_{Sj}}{C_{Ij}} \cdot \frac{1}{1 + 1/(A_0\beta_j)} \equiv \frac{C_{Sj}}{C_{Ij}} \cdot \frac{1}{(1+\varepsilon_{gH})} \tag{16}$$

where $\varepsilon_{gH} = 1/(A_0\beta_j)$ represents the closed loop static error of the stage during holding. Further, (14) shows that, apart from a high-frequency zero at G_j/C_{Ij}, the time constant during amplification is given by

$$\tau_{jH} = \frac{C_{TH} + C_{Ij}(1-\beta_j)}{\beta_j G_j(1+\varepsilon_{gH})} \tag{17}$$

which increases as the feedback factor β_j decreases or, equivalently, as the weighting factor w_j grows.

Regarding the effect of the nonzero ON resistance of the switches during the holding phase, we will separately analyze the deviations introduced by the sampling S_{S2} and feedback S_I switches for a better understanding. Considering the sampling switch alone, it is found that for frequencies below the gain-bandwidth product of the op amp $\omega_{ua} = G_j/C_{TH}$,

the system can be still approximated by a first-order system with a time constant

$$\tau_{j\mathrm{H}} \approx \frac{C_{T\mathrm{H}} + C_{\mathrm{I}j}(1-\beta_j)}{\beta_j G_j(1+\varepsilon_{g\mathrm{H}})} + \frac{R_{\mathrm{S}} C_{\mathrm{S}j}}{1+\varepsilon_{g\mathrm{H}}} \tag{18}$$

which, compared to (17), shows that the main consequence of the nonzero resistance R_{S} is an increase on the time constant of the structure.

A more complicated situation arises when the feedback resistance R_{I} is considered. In this case, the transfer function can not be approximated by a first-order system, but must be characterized by a natural frequency ω_0 and a quality factor Q given, respectively, by

$$\omega_0 = \sqrt{\frac{\beta_j G_j(1+\varepsilon_{g\mathrm{H}})}{R_{\mathrm{I}} C_{T\mathrm{H}} C_{\mathrm{I}j}(1-\beta_j)}} \tag{19}$$

$$Q = \frac{\sqrt{R_{\mathrm{I}} C_{T\mathrm{H}} C_{\mathrm{I}j}(1-\beta_j)\beta_j G_j(1+\varepsilon_{g\mathrm{H}})}}{C_{T\mathrm{H}} + C_{\mathrm{I}j}(1-\beta_j)(1+C_{go}R_{\mathrm{I}})} \tag{20}$$

as well as by a zero located at

$$\omega_{z\mathrm{H}} = -\frac{G_j}{C_{\mathrm{I}j}(1-G_j R_{\mathrm{I}})}. \tag{21}$$

One possible strategy for sizing the feedback switch S_{I} is to choose R_{I} so that $\omega_{z\mathrm{H}}$ cancels out the closed loop pole $\omega_{p\mathrm{H}} = 1/\tau_{j\mathrm{H}}$, with $\tau_{j\mathrm{H}}$ given in (18). However, the transient response of the system can not be exactly estimated from the Q factor, due to the existence of the zero, and, therefore, sizing must ultimately rely on circuit simulations.

Let us now consider the sampling phase [see Fig. 9(b)] and assume, at first instance, that switch-ON resistances are all negligible. In this case, the transfer function from the input voltage to the voltage across the sampling capacitor C_{Sj} reads as

$$\frac{V_S(s)}{V_j(s)} = -\left[1 + \frac{sC_{\mathrm{S}j}}{G_j(1+1/A_0) + s(C_{\mathrm{I}j} + C_{T\mathrm{S}} + C_{pa})}\right]^{-1} \tag{22}$$

where $C_{T\mathrm{S}} = C_{go} + C_{L\mathrm{S}}$ is the total output capacitance of the stage during the sampling operation mode. Equation (22) shows that the time constant during sampling is given by

$$\tau_{j\mathrm{S}} = \frac{C_{T\mathrm{S}} + C_{\mathrm{I}j}/\beta_j}{G_j(1+\varepsilon_{g\mathrm{S}})} \tag{23}$$

where $\varepsilon_{g\mathrm{S}} = 1/A_0$. In most practical situations, $\tau_{j\mathrm{S}} < \tau_{j\mathrm{H}}$, i.e., the settling behavior is slower during amplification.

If the influence of the nonzero ON resistances in Fig. 9(b) are considered, the time constant takes the form

$$\tau_{j\mathrm{S}} \approx R_{\mathrm{S}} C_{\mathrm{S}j} + R_{\mathrm{R}} C_{\mathrm{I}j} + \frac{C_{T\mathrm{S}} + (1+R_{\mathrm{U}} G_j \varepsilon_{g\mathrm{S}})(C_{\mathrm{I}j}/\beta_j)}{G_j(1+\varepsilon_{g\mathrm{S}})} \tag{24}$$

which shows that $\tau_{j\mathrm{S}}$ increases due to the local time constants of the switch resistances and the associated capacitors.

The above analysis, though particularized to the SC amplifier of Fig. 8(b), is quite representative of the frequency limitations appearing in SC circuits and can be easily extended to other SC amplifier stages [57] and/or operational amplifier models [66].

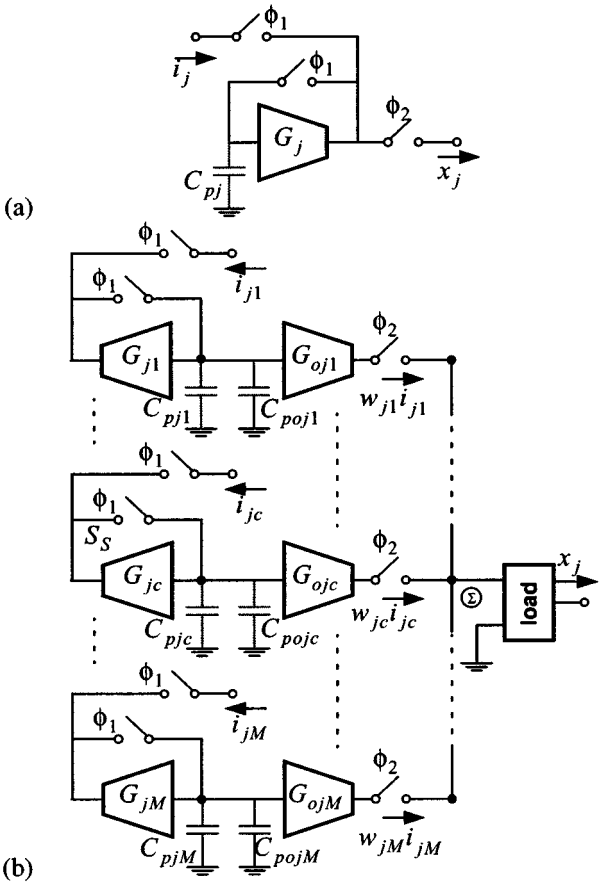


Fig. 10. (a) SI half-delay unity-gain block. (b) SI block for weighted summation.

B. Switched-Current Linear Operators

Fig. 10(a) shows a SI unity-gain S/H circuit, which is often referred to as second generation *current memory* cell [52], [61]. The transconductor can be realized by using a single transistor or a composite structure as discussed in [61]. On the other hand, the capacitor has only second-order influence on circuit performance and may simply consists on the parasitic capacitance C_{pj} at the transconductor input node—nonlinearity is not a problem provided that the clock period is long enough to guarantee that steady state is reached at each clock phase. Under ideal transfer conditions and using the clocking diagram of Fig. 8(c), the circuit of Fig. 10(a) obtains [61]

$$\begin{aligned} x_j(k+1) &= i_j(k+1/2) \\ x_j(k+1/2) &= 0 \end{aligned} \tag{25}$$

in close correspondence to (12). Again, full-cycle delay elements can be realized by simply cascading two current memory cells with alternating S/H clock phases.

Extension of Fig. 10(a) to perform aggregation and scaling functions can be accomplished with the circuit of Fig. 10(b). By exploiting KCL at the output node, Σ, it obtains

$$\begin{aligned} x_j(k+1) &= \sum_{c=1,\,M} \frac{G_{ojc}}{G_{jc}} \cdot i_{jc}(k+1/2) \\ x_j(k+1/2) &= 0 \end{aligned} \tag{26}$$

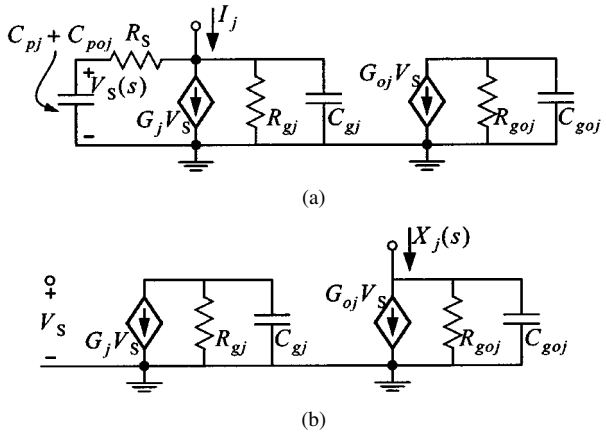


Fig. 11. Equivalent circuits for the analysis of the (single input branch) SI amplifier of Fig. 10(b) during (a) the sampling phase and (b) the holding phase.

which shows that, during the holding phase, the circuit realizes a weighted summation of the input current, as required by (3). As for SCs, ideal scaling factors $w_{jc} = G_{ojc}/G_{jc}$ are defined by similar component (transconductors) ratios and, hence, can be set with high accuracy. On the other hand, similar to ODE-based systems, programmability can be achieved through either analog control or digital control of transconductance values.

Deviations from the ideal behavior defined by (25) and (26) arises when parasitic effects are considered. The foregoing analysis focus exclusively on the SI amplifier of Fig. 10(b), assuming a single input branch (subindex c is omitted for the sake of clarity) and the following parasitics.

1) The small-signal parasitics associated to the transconductors, assuming the model of Fig. 4(d), but neglecting the reactive behavior of the transconductance.
2) The finite ON resistance of the sampling switch S_S, denoted as R_S.

Fig. 11(a) and (b) shows the equivalent circuits for the SI amplifier of Fig. 10(b), valid for the holding and sampling phases, respectively. Analysis of Fig. 11(a), corresponding to the sampling phase, yields

$$\frac{V_S(s)}{I_j(s)} = \frac{\frac{1}{G_j}\left(1+\frac{R_S G_j}{A_0}+sC_jR_S\right)}{1+\frac{1}{A_0}+s\left[\frac{C_{Tj}(1+G_{gj}R_S)+C_{gj}}{G_j}\right]+s^2\frac{C_{gj}C_{Tj}R_S}{G_j}} \tag{27}$$

where $A_0 = G_j/G_{gj}$ and $C_{Tj} = C_{pj} + C_{poj}$. This is a second-order lowpass transfer function with pole frequency and Q factor given by

$$\omega_0 = \sqrt{\frac{G_j(1+\varepsilon_g)}{C_{gj}C_{Tj}R_S}} \tag{28}$$

$$Q = \frac{\sqrt{R_S C_{gj} C_{Tj} G_j(1+\varepsilon_g)}}{C_{Tj}(1+G_{gj}R_S)+C_{gj}}. \tag{29}$$

In most practical situations, output capacitance C_{gj} is small, condition $R_S G_j \ll C_{Tj}/C_{gj}$ is met, and the SI amplifier behaves at it had a single-pole with a time constant

$$\tau_{jS} = \frac{C_{Tj}(1+G_{gj}R_S)+C_{gj}}{G_j} \approx \frac{C_{Tj}}{G_j}. \tag{30}$$

On the other hand, during the holding phase, the voltage stored in the (parasitic) sampling capacitor C_{Tj} is converted to a current according to

$$X_j(s) = G_{oj}V_S \tag{31}$$

where it has been assumed that the loading circuit of the SI amplifier performs as an ideal current conveyor so that the output impedance of the last transconductor has no influence on X_j. Taking into account (27) and (31), the overall dc current gain of the SI amplifier can be approximated as

$$w_j \approx \frac{G_{oj}}{G_j(1+(1-R_S G_j)/A_0)} = \frac{G_{oj}}{G_j}\cdot\frac{1}{(1+\varepsilon_g)} \tag{32}$$

which is similar to the expression obtained for SC circuits in (16). It should be noted, however, that simple transconductors are not able to obtain high values of A_0, indicating that more complex circuit structures are needed to reduce transmission errors and achieve a performance comparable to that of SC alternatives. Circuit techniques for increasing the ratio G_j/G_{gj} of transconductors involve the use of negative feedback either to reduce the output conductance or increase the input transconductance [61], [67].

Another aspect in which SI circuits compare unfavorably to their SC counterparts is regarding *switching imperfections* [61], [68], [69]. As we have seen, operation of both SC and SI circuits relies on the capacitor's ability to hold voltages when switches turn off. In practice, because of switching imperfections, the stored voltages suffer from deviations that are inversely proportional to the holding capacitance. Given that SI circuits use, as holding capacitors, the parasitics at the input of the transconductors—capacitances are small if transconductors with reduced sizes are used—switching imperfections are particularly problematic for this kind of circuit. Switching errors can be attenuated with several techniques. They include dummy switch compensation, fully differential architectures, and algorithmic cancellation [57], [61].

V. Nonlinear Operators

There are two basic strategies to realize nonlinear operators in IC form: 1) using signal processing or 2) exploiting some nonlinear mechanisms of the primitive components available in the technological process.

Techniques of the first category have mainly arose in the context of multipliers design, but can be easily generalized to the implementation of other functions [56], [70]. The most popular signal processing approach is based on analog pulse modulation and relies on the (nonlinear) control of some characteristic features of a pulse train (e.g., amplitude, duration, or position). Another alternative is based on the concept of temporal shaping in which the output is obtained by sampling a nonlinear waveform at an instant determined by the comparison of a given input level and an external (generally,

nonlinear) reference waveform [70]. It is worth noting that both alternatives have been already applied to the synthesis of discrete maps with chaotic behavior [13], [17].

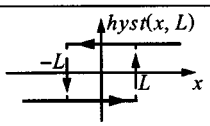
Systematic procedures and circuits to realize nonlinear functions using IC design primitives are described in [70]–[75], among others. Particularly, [70], [74], and [75] focus on CMOS technologies. In general, the design route toward the implementation of nonlinear characteristics comprises four steps [70]:

1) identification of the intrinsic nonlinearities available at the design primitives; in the CMOS case, the nonlinearities available at the MOS transistor;
2) construction of nonlinear operators (multiplication, division, logarithms, sign, absolute value, etc.) through the interconnection of primitive components;
3) realization of the elementary nonlinear functions (truncated polynomials, Gaussian functions, etc.) required by a given representation technique (splines, radial basis functions, etc.) through the interconnection of the building blocks devised in the previous step;
4) realization of nonlinear tasks through the proper interconnection of all the circuit blocks above, after solving the approximation (interpolation) problem associated to the representation technique.

Nevertheless, complex representation techniques are seldom used in the context of chaos generators and, most often, the implementation of nonlinear functions restricts to the first two steps of the nonlinear synthesis route. As an illustration, Table 4 shows some of the nonlinear operators, grouped into smooth and PWL, most commonly found for chaos synthesis—they cover all the nonlinearities (except trigonometric) listed in Table 1 and Table 2. Table 4 also makes a classification into basic and derived operators and presents some exemplary expressions that obtain the later in terms of the former. Note that such relationships can take both algebraic or implicit forms. In this last case, the targeted nonlinear operator can be generally obtained by means of feedback [70], [71]. As can be seen, few basic operators are required to span most of the nonlinear functions used for chaos generation. They are the step function, hysteresis, and extension operators, in the case of PWL functions, and the squaring and exponential operators, in the case of smooth functions. Hence, basic building blocks implementing such characteristics are essential to provide circuit solutions to many nonlinear synthesis tasks.

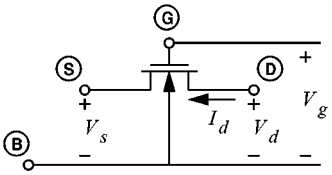
Focusing on the first step of the synthesis route, Fig. 12 outlines the nonlinear behaviors available at MOS transistors, classified, as in Table 4, in smooth and PWL. It is worth noting that these equations are first-order models and as such, only give rough approximations to actual behaviors. Therefore, nonlinear circuit designs based on these expressions will only approximate the intended functionality. Fig. 12 offers many possibilities for the implementation of nonlinear operators. Most evident, the large-signal characteristics of MOS transistors in the forward saturation region under weak or strong inversion can be exploited, respectively, for the synthesis of the exponential and squaring operators [70]. On

Table 4
Examples of Basic and Derived Nonlinear Functions

Function	Definition	Derivation
Piecewise Linear		
Heaviside or step function	$H(x) = \begin{cases} 1 & x>0 \\ 0 & x<0 \end{cases}$	Basic
Symmetric hysteresis		Basic
Concave extension operator	$u_+(x) = \begin{cases} x & x>0 \\ 0 & x<0 \end{cases}$	Basic
Convex extension operator	$u_-(x) = \begin{cases} 0 & x>0 \\ x & x<0 \end{cases}$	Basic
Absolute value	$\lvert x\rvert = \begin{cases} x & x>0 \\ -x & x<0 \end{cases}$	$u_+(x) - u_-(x)$
Sign function	$sgn(x) = \begin{cases} 1 & x>0 \\ -1 & x<0 \end{cases}$	$H(x) - H(-x)$
Symmetric saturation	$sat(x, L) = \begin{cases} -L & x<-L \\ x & \lvert x\rvert<L \\ L & x>L \end{cases}$	$\frac{\lvert x+L\rvert - \lvert x-L\rvert}{2}$
Smooth		
Squaring	x^2	Basic
Exponential	$exp(x)$	Basic
Square rooting	$\sqrt{x}$	Implicitly defined by $y,\ y^2 = x$
Logarithmic	$ln(x)$	Implicitly defined by $y,\ exp(y) = x$
Multiplication	xy	$\frac{(x+y)^2 - (x-y)^2}{4}$
Division	$\frac{x}{y}$	Implicitly defined by $z,\ x = yz$

the other hand, the linear dependence of the MOS transconductance with the voltage overdrive $V_{od} = V_g - V_{T0} - n_p V_s$ in the saturation strong-inversion region is at the very heart of the *translinear* principle [70]–[75], which allows the synthesis of current-mode circuits able to generate algebraic transformations in an essentially exact and temperature-insensitive manner. The capability of linearly controlling the self-conductance of MOS transistors in the ohmic region through the gate voltage overdrive also allows interesting solutions for nonlinear synthesis [76]. Finally, the possibility to nulling the MOS self-conductance gives a direct implementation of the rectification operation; it is simply achieved by precluding or not a current signal to flow through a circuit branch according to the value of a control variable.

A detailed description of all the above techniques is beyond the scope of this paper and readers are referred to [70]–[76]. Herein, we will restrict to give some basic ideas for the implementation of PWL operators in both current-



Smooth

Square-law characteristic of MOS transistors in the forward saturation region under *strong* inversion ($V_p \approx (V_g - V_{T0})/n_p$ is the pinch-off voltage and V_A is the equivalent Early voltage).

$$I_d = \beta_{sat}(V_g - V_{T0} - n_p V_s)^2\left[1 + \frac{V_d - V_p}{V_A}\right]$$

for $V_s < V_p < V_d$.

Exponential characteristic of the MOS transistor operating in the forward saturation region under *weak* inversion.

$$I_d = I_{D0}\exp\left(\frac{V_g - V_{T0} - n_p V_s}{n_p U_t}\right)\left[1 + \frac{V_d - V_p}{V_A}\right]$$

for $V_s, V_d > V_p$, $V_{ds} > 4U_t$.

Small-signal transconductance of a MOS transistor in saturation and strong inversion as a linear function of the gate voltage.

$$g_m = 2\sqrt{\beta_{sat} I_d} = 2\beta_{sat}(V_g - V_{T0} - n_p V_s)$$

Small-signal self-conductance of a MOS transistor in ohmic region ($V_s, V_d < V_p$) as a linear function of the gate voltage.

$$g_{ds} = \beta(V_g - V_{T0} - n_p V_s)$$

Piecewise Linear

Negligible output current for $V_s, V_d > V_p + 4U_t$.

Fig. 12. Intrinsic primitive nonlinearities. Note that voltages are referred to the bulk (local substrate) terminal $\mathbf{B}$. β is the large-signal transconductance factor—a parameter proportional to W/L, where W is the transistor width and L is the transistor length, V_{TO} is the zero-bias threshold voltage, n_P is the slope factor in weak inversion, $\beta_{sat} = \beta/(2n_P)$, I_{D0} is an specific current proportional to β, and U_T is the thermal voltage [55].

and voltage-charge domains, as they are the most extended nonlinearities in the mathematical models for chaos.

A. PWL Shaping in Voltage-Charge Domain

Fig. 13(a) shows a modification of the SC amplifier in Fig. 8(b), which realizes voltage rectification. Assume that nodes $\mathbf{A}$ and $\mathbf{B}$ are both grounded. For $v_j - V_\delta < 0$, the switch arrangement at the bottom terminal of C_{Sj} connects nodes $\mathbf{D}$ and $\mathbf{E}$ to ground. Consequently, voltage at node $\mathbf{C}$ remains unaltered from one clock phase to the next and, therefore, there is no charge flow through C_{Sj}. On the other hand, for $v_j - V_\delta > 0$, node $\mathbf{D}$ is set to V_δ, while node $\mathbf{E}$ is set to v_j. Consequently, the voltage at node $\mathbf{C}$ changes from one clock phase to the next and generates an incremental charge, which, assuming that the input voltage remains constant during each full clock cycle, results in the following output voltage:

$$x_j = w_j \cdot u_+(v_j - V_\delta) \tag{33}$$

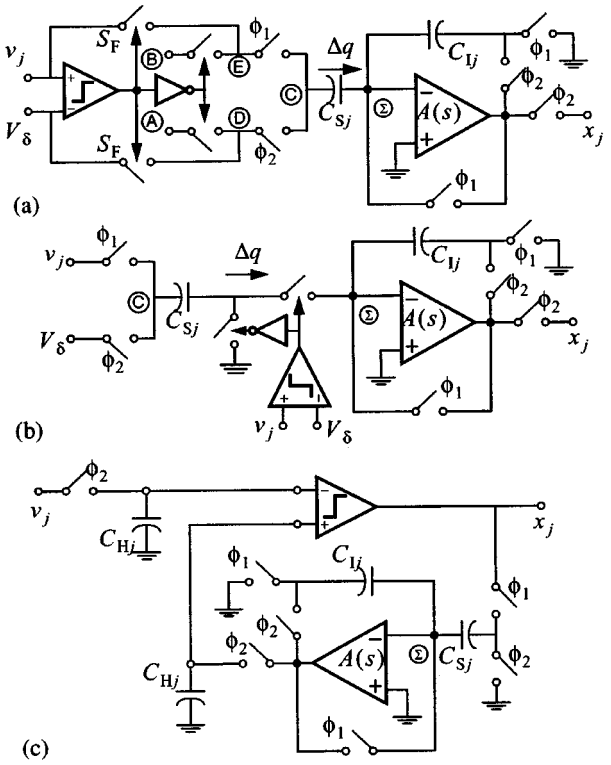


Fig. 13. (a), (b) Circuits for rectification in voltage-charge domain. (c) SC hysteresis operator.

where $w_j = C_{Sj}/C_{Ij}$. Hence, the circuit in Fig. 13(a) realizes a concave extension operator in the voltage-charge domain—it also introduces half-cycle delay. To synthesize the convex extension operator and, therefore, to make the characteristics null for $v_j - V_\delta > 0$, it suffices to interchange the comparator inputs. The technique is easily extended to the absolute value operation by connecting terminal $\mathbf{A}$ to v_j and terminal $\mathbf{B}$ to V_δ.

Another approach to the realization of PWL SC circuitry use series rectification of the circulating charge through a comparator-controlled switch [23], [70]. Fig. 13(b) shows an implementation of the concave extension operator using this technique. As for the circuit in Fig. 13(a), convex rectification is easily obtained by swapping the comparator inputs. A similar principle can be used for the implementation of the step and the sign function operators. An example is given in Section VI in connection to the electronic design of the Bernoulli map.

Finally, Fig. 13(c) shows an implementation of the hysteresis operator, formed by the positive feedback loop of a comparator and a SC amplifier [77]. Threshold levels of the hysteretic characteristics are given by $w_j V_H$ and $w_j V_L$, where w_j is the gain of the SC amplifier, and V_H and V_L are, respectively, the high- and low-logic state levels provided by the comparator.

B. PWL Shaping in Current-Mode Domain

The circuit of Fig. 14(a), called current switch rectifier, is a versatile building block for rectification operations [78]. It consists of a voltage-mode amplifier and a nonlinear resistor

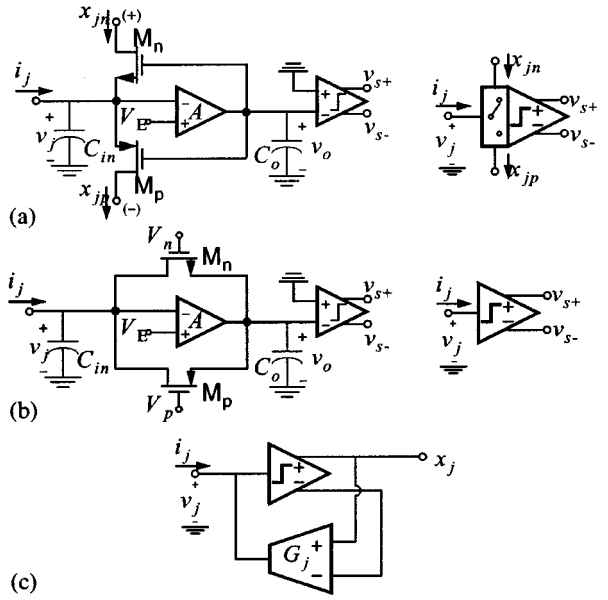


Fig. 14. (a) Current rectifier and symbol. (b) Enhanced current comparator schematic and symbol. (c) Current-mode hysteresis operator.

(formed by transistors $\mathbf{M_n}$ and $\mathbf{M_p}$) arranged in a negative feedback loop. Drain terminals of $\mathbf{M_n}$ and $\mathbf{M_p}$ are connected to appropriate low impedance nodes, which do not interfere the basic functionality of the block.

The circuit exhibits three modes of operation depending on the input current level. For positive current flows, the incoming current i_j is integrated in the input parasitic capacitor and the input voltage v_j is pulled high. The voltage difference $V_{\rm E} - v_j$ is then amplified by A (the gain of the voltage amplifier), causing v_o to go low and forcing $\mathbf{M_n}$ to the OFF state, so that $x_{jn} = 0$. In addition, transistor $\mathbf{M_p}$ turns ON and a negative feedback loop is formed around the amplifier. This feedback configuration reduces the input resistance of the current switch and obtains $x_{jp} = i_j$. A dual situation occurs for negative input currents. In this case, the input voltage v_j is pulled down and v_o goes up, turning $\mathbf{M_n}$ ON and $\mathbf{M_p}$ OFF, so that $x_{jp} = 0$. The voltage amplifier is fedback by transistor $\mathbf{M_n}$, thus, reducing the input resistance of the rectifier. Hence, $\mathbf{M_n}$ completely draws the input current and we have $x_{jn} = i_j$.

Summarizing, the circuit of Fig. 14(a) routes the input current to either the upper or the lower output terminal depending on its sign, i.e.,

$$x_{jp} = u_+(i_j) \qquad x_{jn} = u_-(i_j) \tag{34}$$

and, thus, it generates simultaneously the concave (i_{jp} output) and convex (i_{jn} output) rectified versions of the input current. Besides, the output voltage of the amplifier can be made to swing from rail to rail by using an additional amplifier stage [see Fig. 14(a)], thus, generating logical signals according to the input current sign. Namely, the output v_{s+} is $V_{\rm H}$ = "1" for $i_j > 0$ and $V_{\rm L}$ = "0" for $i_j < 0$ and the opposite for v_{s-}, thus implementing the comparison operation.

It is worth noting that due to the capacitive impedance of the circuit during transitions around $i_j = 0$, it exhibits very high resolution (only limited by leakage currents), insensitive to transistor mismatch. Additionally, the feedback loop created by the amplifier makes the voltage excursions at the input node small for a large input current range, thus, alleviating the interstage errors of the circuit.

The current switch rectifier of Fig. 14(a), however, exhibits a noticeable transient limitation that arises from the Miller effect created around the overlapping capacitor C_M, which connects input and output terminals of the amplifier—significant even for minimum sized feedback transistors, in particular for low current levels [78]. Indeed, it can be shown that the response time $T_{\rm D}$ to an input current step from a negative current level $-J_-$ up to a positive current overdrive J_+ is given by

$$T_{\rm D} \approx \frac{C_{eq}^2}{C_M} \frac{(V_{Tn} + |V_{Tp}|)}{J_+} \tag{35}$$

where $C_{eq}^2 = C_M C_{in} + C_M C_o + C_{in} C_o$. Therefore, $T_{\rm D}$ is inversely proportional to the current overdrive J_+.

Improved transient response is achieved with the circuit of Fig. 14(b) [78]. Its static operation follows principles similar to that of Fig. 14(a), however, it obtains two orders of magnitude improvement in transient behavior. In this case, the response time takes the quadratic expression

$$T_{\rm D} \approx \sqrt{\frac{2C_{in}}{\omega_{ua}} \frac{(V_p - V_n + V_{Tn} + |V_{Tp}|)}{J_+}} \tag{36}$$

where ω_{ua} is the gain-bandwidth product of the op amp. In this case, $T_{\rm D}$ is inversely proportional to the square root of the current overdrive and, therefore, better suited for comparison purposes than Fig. 14(a). Unfortunately, it does not preserve the current rectification properties and, hence, does not qualify directly for current-mode function generation.

Finally, Fig. 14(c) shows the conceptual schematic of a current-mode hysteretic operator, which takes advantage of the comparator in Fig. 14(b). The saturation current levels of the transconductor in the positive feedback loop around the comparator define, in this case, the threshold levels of the hysteretic characteristics.

VI. Examples of IC Chaos Generators

In this section, we present three IC prototypes for chaos generation that have been designed following the concepts and methodology described in the previous sections. One of them is a continuous-time chaos generator and implements the well-known Chua's oscillator (defined in the eighth row of Table 2). The other two designs implement the Bernoulli map (defined in the fifth row of Table 1) in one case using SC techniques and, in the other, SI techniques.

A. Bernoulli Map

Fig. 15 shows a SC schematic for the Bernoulli map, whose model is repeated here for convenience [15]

$$x(k+1) = F[x(k), \mathbf{P}] = Bx(k) - Asgn(x(k)). \tag{37}$$

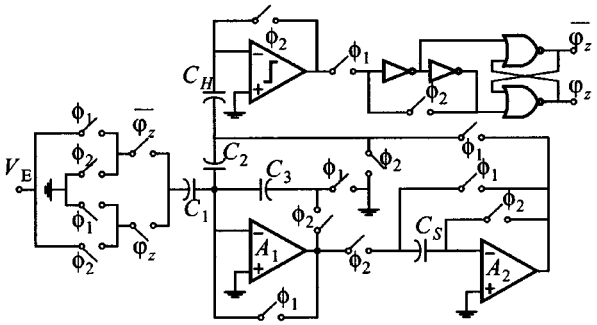
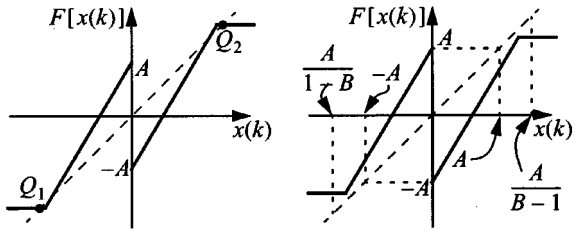


Fig. 15. SC schematics for Bernoulli map.



(a) (b)

Fig. 16. (a) Onset of parasitic stable points in the Bernoulli map due to improper setting of A. (b) Strategy to avoid locked states.

Op-amp A_1 and related capacitors perform the weighted summation in (37) and introduce a half-cycle delay. Op-amp A_2 is used to implement the remaining half delay stage and complete the concept of Fig. 1(a). Parameters in the map are controled by the capacitors C_1, C_2, and C_3 and the dc voltage $V_{\rm E}$ as follows:

$$A = \frac{C_1}{C_3} V_{\rm E} \qquad B = \frac{C_2}{C_3}. \tag{38}$$

The nonlinearity is realized via a phase-reverser switch arrangement controlled by a dynamic comparator. Depending on the value of φ_z, this arrangement makes $V_{\rm E}$ to be either added or subtracted at the input of the op-amp A_1, thereby yielding the sign operator in (37). The comparator consists of an input offset canceled amplifier, followed by a regenerative sense amplifier and a NOR-based latch [57].

Operation of the circuit in Fig. 15 is described by (37) whenever op amps work in their linear region. If any of the amplifiers enters in saturation, the circuit no longer implements (37) and locks at parasitic stable points close to the power rails. This undesirable situation can be avoided by properly setting parameter A. To illustrate this point, Fig. 16 shows the open-loop transfer characteristics of the map, including op-amp voltage saturations, for two different values of A and the same value of $B(1 \leq B < 2)$. In Fig. 16(a), parasitic stable points Q_1 and Q_2 appear at the intersections of the transfer function characteristics with the bisecting line. This makes the circuit to evolve, after a transient, to either Q_1 or Q_2, destroying any chaotic behavior. On the other hand, for Fig. 16(b) no spurious equilibria appear and chaotic waveforms are robustly generated. Necessary conditions to guarantee this last situation are

$$A < V_{sat+} < A/(B-1) \quad A/(1-B) < V_{sat-} < -A \tag{39}$$

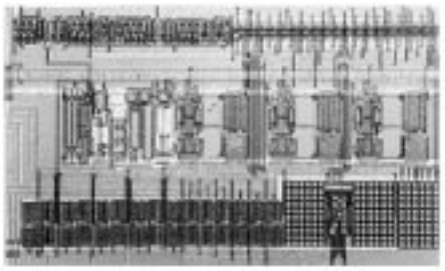


Fig. 17. Microphotograph of the SC Bernoulli map prototype.

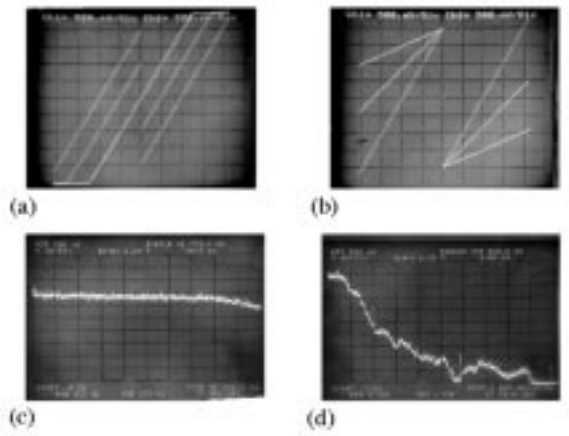


Fig. 18. Measured open-loop transfer characteristic of the SC Bernoulli map for (a) different values of A and (b) different values of B_1 and B_2. Measured spectra for different B_1, B_2 settings for (c) $B_1 = B_2 = 61/32$ and (d) $B_1 = 47/32$, $B_2 = 39/32$.

where $V_{sat+}(V_{sat-})$ denotes the op amp's positive (negative) saturation level. Interestingly enough, the condition $B < 2$ gives rise to the creation of a clearance between the invariant set of the system and its basin of attraction, which guarantees that, under small perturbations, trajectories are always reinjected into the invariant set. Other strategies to achieve this goal can be found in [15], [22], [41], and [42].

Fig. 17 shows the microphotograph of a programmable prototype of the circuit in Fig. 15 [15]. In this prototype, the slopes of the characteristic—B_1 for $x(k) < 0$ and B_2 for $x(k) > 0$—can be separately controled by means of two binary weighted capacitors with six control bits each. Also, an additional control bit can be used to selectively open or close the feedback loop.

Fig. 18(a) shows a family of curves for different values of voltage $V_{\rm E}$ and slopes B_1 and B_2 fixed at 61/32. On the other hand, Fig. 18(b) shows a set of transfer characteristics obtained for different values of B_1 and B_2 with $V_{\rm E}$ chosen so that $A = 2$ V. Measurements in closed loop were also made for all possible combinations of B_1 and B_2 values inside the chaotic regime. Fig. 18(c) and (d) show the spectra obtained for two of these combinations using a clock frequency of $f_c = 200$ kHz. Flat spectra were obtained for the cases $B_1 = B_2 = B$. This is illustrated in Fig. 18(c), obtained for $B_1 = B_2 = 61/32$. The spectrum is flat up to 75 kHz (35% of the clock frequency) with a maximum deviation of 1 dB, which renders the circuit well suited for white

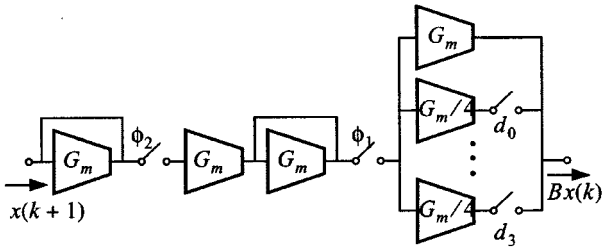


Fig. 19. Programmable current-mode scaled delay block.

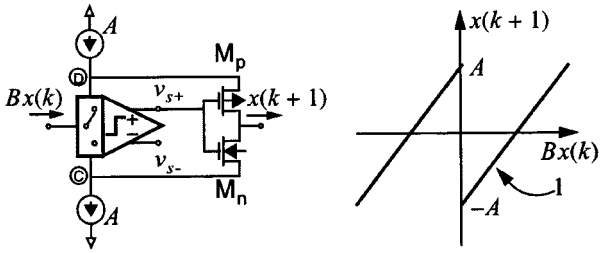


Fig. 20. Current-mode realization of the Bernoulli map nonlinearity. (a) Circuit schematic. (b) Implemented characteristic.

noise generation. On the other hand, for $B_1 \neq B_2$, generated noise becomes colored, as shown in Fig. 18(d).

Now, let us consider implementation of (37) in current-mode domain [16]. The scaled delay operation is realized as a cascade of two track-and-hold SI stages with complementary phase clocks. As indicated in Fig. 19, the rightmost transconductor has a parallel digitally programmable structure controled by a digital word of 4 bits $(d_0, \ldots, d_3)$. This makes parameter B binary-programmable from 1.0 to 2.0 at steps of 0.25—in practice, the scaling factor of the transconductor controlled by bit d_3 is made slightly less than $G_m/4$ to make parameter B lower than 2.0 and, hence, avoiding divergent orbits. Fig. 20(a) shows a conceptual schematic for the realization of the PWL characteristics of Fig. 20(b). Its operation relies on the current rectifier of Fig. 14(a). Positive input currents are routed to node $\mathbf{C}$ while, simultaneously, the voltage v_{s+} evolves to the high logic state, turning $\mathbf{M_n}$ ON and $\mathbf{M_p}$ OFF. Thus, a current $Bx(k) - A$ (obtained by KCL) is directed to the output node through the transistor $\mathbf{M_n}$—the right-hand piece of Fig. 20(b) is implemented in this manner. Similarly, negative input currents turn $\mathbf{M_p}$ ON and a current $Bx(k) + A$, obtained by KCL at node $\mathbf{D}$, is delivered to the output node.

Fig. 21 shows a microphotograph of the SI Bernoulli map prototype [16]. It includes some extra circuitry to enable testing the output current and to open or close the feedback loop.

Fig. 22(a) shows the measured PWL current transfer characteristics obtained from the prototype. Deviation from the ideal characteristic for input currents between -20 μA to 20 μA is less than 0.2%. Fig. 22(b) shows a detail of the global characteristics, in which the input current swings from -21 pA to 21 pA. It is intended to illustrate the resolution

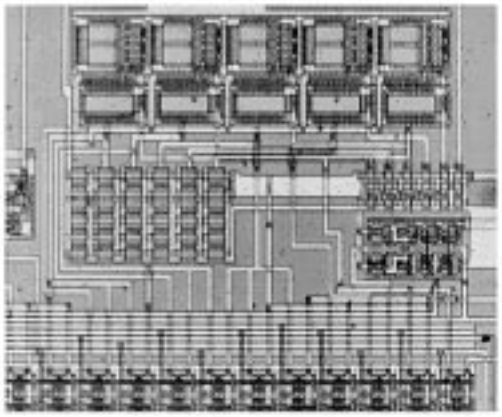


Fig. 21. Microphotograph of the SI Bernoulli map prototype.

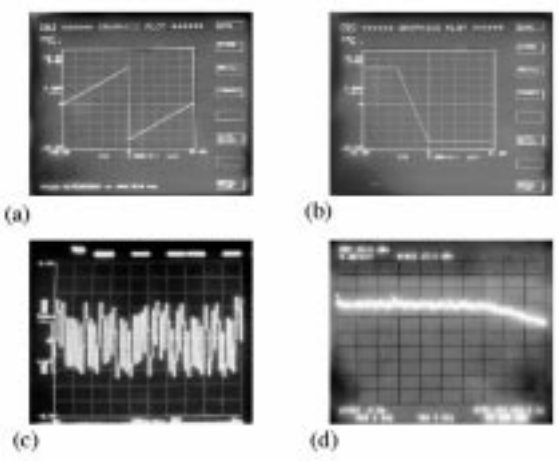


Fig. 22. (a) Measured characteristic of the nonlinear block. (b) Detail of the discrimination function. (c) Measured current waveform. (d) Power density spectrum.

achieved in the current discrimination which, as already anticipated in Section V-B, amounts to a few picoamperes.

Fig. 22(c) and (d) illustrates the closed loop operation of the prototype for a clock frequency of 500 kHz. Fig. 22(c) shows the measured current waveform at the output of the delay block for $B = 2$ (actually, a slightly lower value as mentioned before), while Fig. 22(d) shows its associated power density spectrum. The waveform of Fig. 22(c) shows that apparently coincident values of $x(k)$ result in quite different values after few iterations, thereby confirming the expected unpredictably feature. Regarding Fig. 22(d), detailed measurements shows a very flat spectrum from dc up to about 30% of the clock frequency (deviation in this range was of less than 1 dB).

It is illustrative to compare performance of this circuit to that of the SC circuit in Fig. 15. Area occupation of the SI prototype is about one order of magnitude smaller than for the SC prototype. Also, for half the power consumption, the speed of the SI prototype is about three times greater than that obtained from the SC prototype. This confirms the suitability of the SI technique for moderate system requirements.

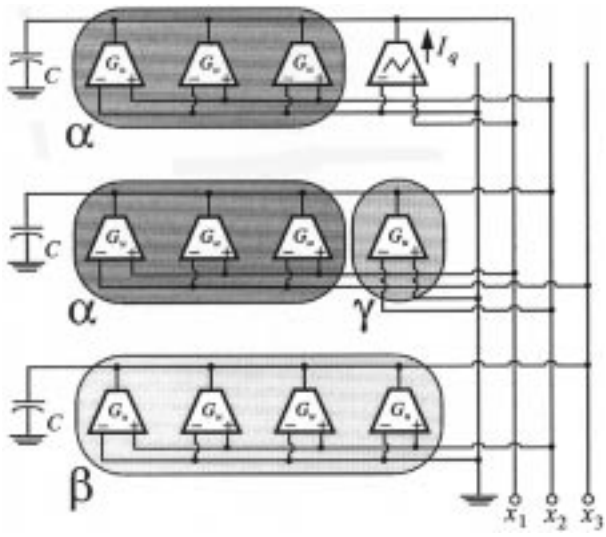


Fig. 23. Optimized *Gm-C* realization of the Chua's oscillator.

B. Chua's Oscillator

Fig. 23 shows the simplified schematic of an integrated prototype of the Chua's oscillator [32]. It implements, indeed, a modified version of such oscillator, obtained from the optimization procedure described in Section II-C. The resulting model is slightly different to that shown in Table II and defined by matrices

$$\mathbf{A} = \begin{bmatrix} s_1 & \alpha & 0 \\ \alpha & -\gamma & -\alpha \\ 0 & \beta & 0 \end{bmatrix} \qquad \mathbf{B} = \begin{bmatrix} s_0 - s_1 \\ 0 \\ 0 \end{bmatrix} \tag{40}$$

where $\mathbf{P} = [\alpha, \beta, \gamma, s_0, s_1] = [3, 4, 1, 1, -2]$. The nonlinear function is still given by $f_1(\mathbf{x}) = sat(x_1, L)$.

In Fig. 23, all the integrating capacitors are assumed identical and the linear transconductors have been implemented by building a unitary block with gain G_u and connecting in parallel as many of such units as indicated by the values of α, β, and γ. On the other hand, the nonlinear transconductor has been designed so that its output current also includes the linear term associated to the first entry of $\mathbf{A}$, i.e.,

$$I_q = G_u \left\{ s_1 x_1 + \frac{s_0 - s_1}{2} \{ |x_1 + L| - |x_1 - L| \} \right\}. \tag{41}$$

Fig. 24 shows the circuit used for the PWL function consisting of a front-end transconductor and a nonlinear circuit that operates in current-mode domain based on the high-accurate rectification mechanism described in Section V-B.

Two further circuit level aspects have been considered in the design of the schematic of Fig. 23. One is the addition of dummy devices so that all the integration nodes exhibit the same capacitance C_t by construction. Accordingly, the global time constant of the circuit τ is given by $\tau = C_t/G_u$, where C_t is the total capacitance at the state variable nodes. Since parasitics are nonlinear and depend on the operating point of the circuit, more than 80% of the total capacitance is contributed by the nominal integrating capacitance C.

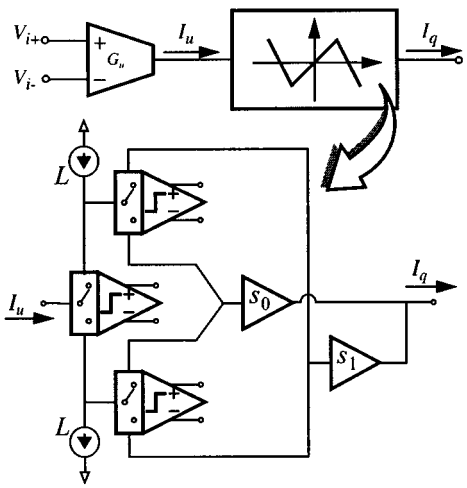


Fig. 24. Implementation of the PWL transconductor.

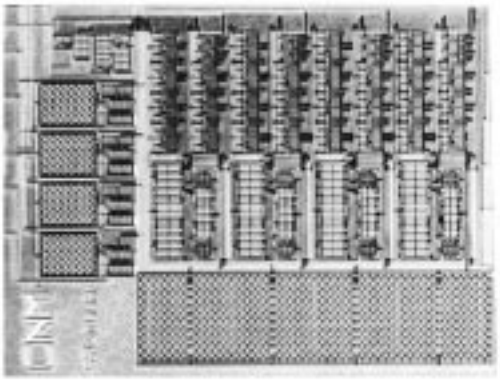


Fig. 25. Chip microphotograph.

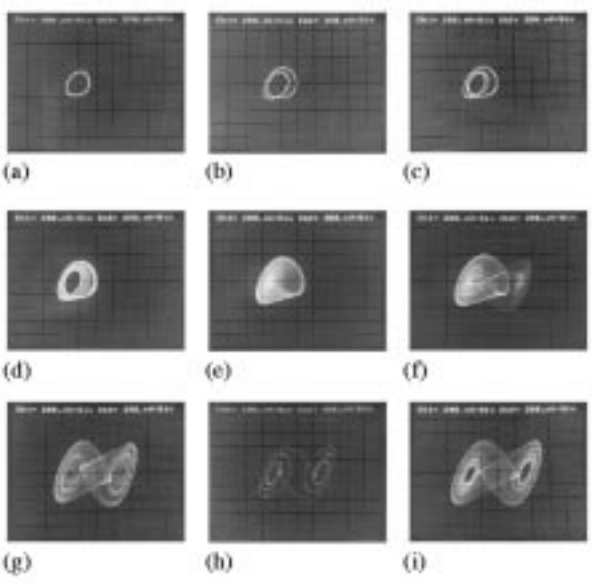


Fig. 26. Route to chaos in a silicon prototype of the Chua's oscillator. Limit cycle for (a) period 1, (b) period 2, and (c) period 4. (d) Birth of Rössler-like attractor. (e) Rössler-like attractor. (f) Birth of double-scroll attractor. (g) Double-scroll attractor. (h) Periodic window. (i) Double-scroll attractor close to saturation.

A second aspect is the introduction of a tuning mechanism [49] (not shown in Fig. 23) to reduce the absolute tolerance of the circuit time constant below 2% [32].

Fig. 25 shows a microphotograph of the chaotic oscillator, which includes the onchip tuning scheme, and other auxiliary circuitry for biasing and measurement purposes. Power dissipation is less than 1.8 mW for a symmetrical biasing of ± 2.5 V. The fabricated prototype is able to reproduce the whole bifurcation sequence leading to the chaotic attractors of the oscillator, as shown in Fig. 26 [32]. The different phase portraits (projections on the plane $x_1 - x_2$) has been obtained by progressively increasing parameter s_o, while keeping the other system parameters fixed. As can be seen, the picture book reveals a period-doubling route to chaos, including periodic windows, as well as Rössler-like and double-scroll attractors.

VII. Summary

Through proper design techniques encompassing considerations both at system and circuit levels, it is possible to design compact and robust chaotic ICs in CMOS technologies. This paves the way for the integration in silicon of many of the applications already devised for nonlinear dynamics.

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