INTEGRATED MEMS SWITCH TECHNOLOGY ON SOI-CMOS

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ABSTRACT

We describe an RF MEMS contact switch technology that has been integrated above a 0.5um silicon RFCMOS-on-SOI process. This integration strategy combines a MEMS gold cantilever contact-switch with a custom silicon-on-insulator IC platform. This IC platform provides several power management functions critical for MEMS including high voltage generation, control and analog/digital/RF circuits... The technology also includes a wafer-level-package dielectric encapsulation process for the MEMS device which is hermetic and compatible with low cost packaging processes.

INTRODUCTION

MEMS switch requirements for wireless applications

Despite early demonstrations [1][2][3] of nearly ideal insertion loss, power handling, and linearity characteristics, RF MEMS switches, be it either contact- or capacitive-type, have failed to present day to penetrate any large or medium scale application in the RF market. Despite these obvious superior RF characteristics, four major factors have prevented RF MEMS switches from widespread use when compared to conventional solid-state FET switch solutions:

1) High actuation voltages (30-100V) which are typically required for reliable MEMS switch electrostatic actuation (versus 3-5V required for FET switches) require the user to provide external high voltage supplies;
2) MEMS switches require complex and expensive hermetic packaging solutions, whereas FET switches can be packaged using very low cost plastic overmold packaging technologies;
3) RF MEMS switches are typically slow (10us to 1ms typical) compared to sub-uS switching times for a solid-state FET. This is in part due to the mechanical nature of the switch which must move a conductor across a gap before final contact is established;
4) Long term reliability, RF power degradation and general lifetime requirements are not well understood for RF MEMS switches.

These factors, coupled with the relatively low cost and high process maturity of solid state FET switches, processed in either GaAs[4] or silicon-on-sapphire (SOS) [5] technology solutions, have essentially kept RF MEMS switches from having any significant participation in large-scale commercial applications. In particular, the cellular handset puts an even higher constraint on RF switching solutions utilizing MEMS due to high volume, large number of switching events, and typically low profit margin requirements of any of its RF chain components.

With the advent of 3G and 4G cellular communications platforms, the need for a high performance and highly integrated switch module as well as an adaptive power amplifier strategy capable of covering multiple bands and standards has become extremely desirable. These are complex applications that can greatly benefit from the higher performance of RF MEMS switches and can potentially tolerate the needed overhead (such as charge pumps and voltage actuation circuitry) required.

In this paper we describe the development of RFMD's above-IC MEMS technology on SOI-CMOS. The MEMS switch is capable of meeting frequency and power (>2W) specifications needed for current cellular communication systems. This program is geared towards integrating a MEMS gold cantilever contact switch technology on a custom silicon-on-insulator IC platform to provide all of the necessary MEMS power management functions (high voltage charge pumps, control and timing signals), as well as an LDMOS silicon power amplifier and required digital and analog circuitry. This technology also includes a WLP (wafer level package) process which allows for a low cost hermetic packaging flow consistent with the industry's need to provide flip-chip solutions.

FABRICATION

SOI RFCMOS Technology

The above-IC MEMS process described in this work uses as a starting wafer a SOI (silicon-on-insulator) RFCMOS technology previously described in the literature [6]. This custom-developed technology is manufactured at JAZZ Semiconductor (Newport Beach, CA, USA). The SOI substrates used in this technology are fabricated by SOITEC (Bernin, France). The SOI silicon technology integrates on a single platform many of the necessary blocks needed for portable wireless applications, such as digital/analog mixed-mode components, solid-state power switches, as well as an RF power LDMOS transistor suitable for cellular PA operation (Figure 1).

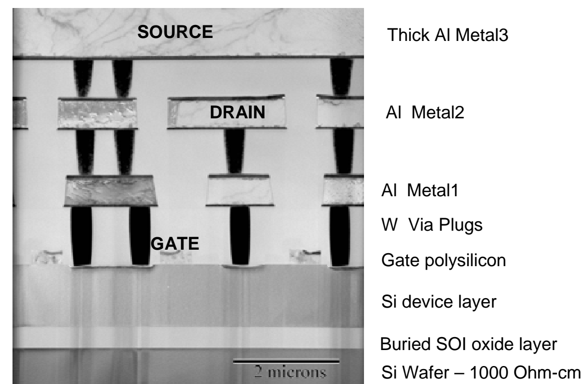

Figure 1. TEM cross-section of an LDMOS power FET built in the SOI silicon technology used as a starting wafer for our MEMS above-IC integration.

This 200mm SOI RFCMOS technology was selected for our MEMS process because of two distinct factors:

1) The handle wafer of SOI substrate utilized in this technology has a very high resistivity (1000 Ohm-cm typical), which is 2 to 3 orders of magnitude higher when compared with starting substrates used in conventional silicon CMOS technologies. The high

resistivity of the SOI silicon handle wafer yields superior RF characteristics compared with those measured on standard silicon substrates and also allows for the integration of higher Q matching components, such as inductors and Metal-Insulator-Metal capacitors.

2) The SOI technology allows for nearly ideal isolation of devices, since the different transistors and diodes do not share a common substrate terminal.

This latter feature of the SOI technology is particularly important for the development of the integrated MEMS technology, because the underlying PM (power management) block must be capable of internally boosting a 3V battery voltage to a MEMS actuation voltage > 50 V. Without the isolation provided by the SOI substrate, one would be limited to much lower charge pump voltages, typically 20-35V for commonly available CMOS technologies. The SOI technology allows for the stacking of numerous NFET, PFET, diodes and bipolar transistors to create pseudo high voltage devices capable of meeting the high voltage requirements of our MEMS technology while consuming a minimum amount of DC current from the 3V battery. The SOI configuration also allows for the development and integration of devices not available in the bulk CMOS technology, such as very high breakdown FETs (BVDSS > 100V) and SCR devices capable of triggering very high voltages with minimum amount of control charge. The suitability of SOI CMOS technology to deliver optimum power management capabilities for an integrated MEMS technology has also been identified by others in the literature [7].

MEMS Switch Technology

The R&D development of our MEMS integrated process was done at RFMD's clean room fab in Charlotte (NC, USA). Since the CMOS process is complete at this point, it is obviously necessary to maintain all processing temperatures to less than 300 C. A picture of a finished MEMS switch inside a WLP on an SOI-CMOS wafer is shown in Figure 2.

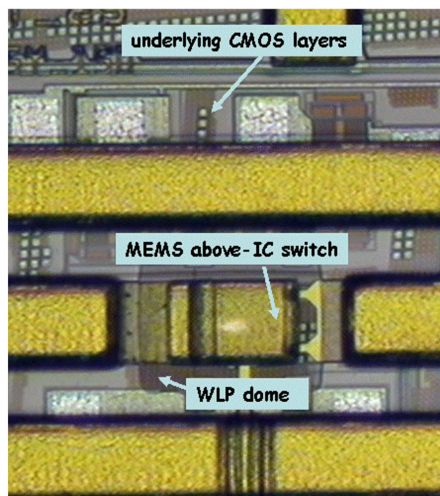

Figure 2. The above-IC MEMS contact switch technology, showing the underlying SOI CMOS layers, the Au cantilever beam and the WLP dielectric dome which encapsulates the structure.

As is typical of RFCMOS technologies manufactured in silicon foundries, the top metal layer consists of a thick final aluminum layer (3um in our case), covered with a thin final dielectric passivation layer, which has been patterned to reveal the I/O pads. This starting configuration is highly non-planar. For optimum performance and RF characteristics of the MEMS switch, it is also desirable to further isolate the MEMS structure from metallization layers utilized in the CMOS process.

The initial step in the MEMS flow therefore consists of multiple, thick PECVD oxide layer deposition and CMP (chemical-mechanical-polish) steps in order to yield a flat surface suitable for MEMS processing. Vias are then patterned and etched which will connect the CMOS aluminum layers with the top gold MEMS layers (see Figure 3).

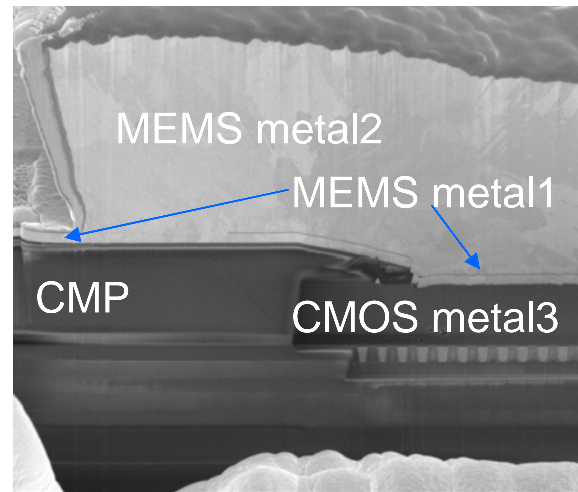

Figure 3. SEM cross-section of MEMS / CMOS vias. A thick PECVD oxide layer was deposited and planarized by CMP.

The first MEMS 0.5um gold layer is then deposited and patterned (with the appropriate adhesion layer underneath). Our MEMS flow utilizes only Au-based metallization layers due to the superior electromigration and contact reliability characteristics of Au when compared with other metals typically available. The contact metal is then deposited and patterned to form the mechanical contact region of the MEMS switch. In our case, we utilize a gold alloy metal configuration engineered to give an optimal tradeoff between contact reliability and contact resistance.

The first sacrificial layer is deposited on the wafer. We utilize a polymer-based sacrificial material which can be reflowed to yield the necessary planarity for the top cantilever Au beam. Extreme care is necessary later on to ensure complete removal of this sacrificial polymer material over the entire MEMS region in order to yield the necessary reliability figures of merit needed for our MEMS application.

The second gold layer is electroplated to form the thick cantilever for the MEMS contact switch. We utilize a very thick Au layer in order to yield the necessary stiffness for the released MEMS cantilever beam and also to provide a high quality RF metal layer which is used for transmission lines and inductor designs. The MEMS cantilever structural design and process was engineered to meet the specific requirements for our MEMS switches (see Table 1). These include a relatively fast ON and OFF actuation cycle (5us) and a high immunity to self-actuation from the large RF voltages present in a cellular PA. The stiffness of the thick gold beam also provides a much better immunity to stiction problems during the cantilever release step, which is necessary in a high yield , high volume applications.

Following the plating of the second MEMS metal, a second sacrificial layer is then deposited on the wafer which serves as the mold for the dielectric dome used in our WLP process. This

second sacrificial layer is thick enough to accommodate the height of the mechanical switch structure.

The WLP dome is formed using two low-stress PECVD depositions of silicon nitride. The combined thickness is optimized to provide a robust WLP dome as well as a short process time. The removal of all polymer sacrificial layers is done in between the first and the second dielectric depositions utilizing a proprietary patterning/cleaning process. The dielectric is then cleared over the I/O pad regions and the MEMS above-IC process is complete (see Figure 4).

Flip-chip processing is increasingly used in the wireless industry as the number of I/O's and RF intermodulation/isolation requirements increase[8]. This particular WLP process provides the low profile required..

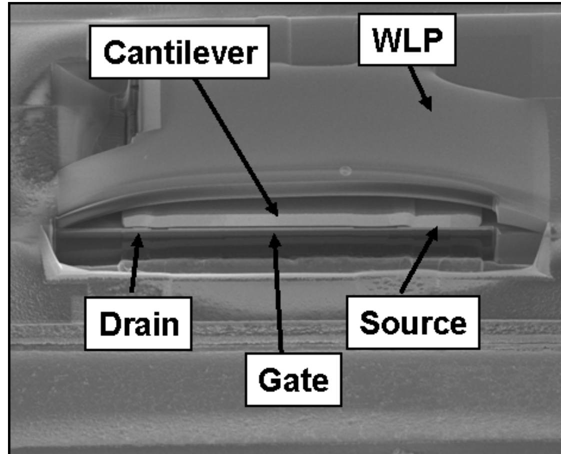

Figure 4. SEM cross-section (post FIB) of the completed MEMS contact switch, illustrating the different regions of the device. The drain corresponds to the metal contact region.

Note that in this particular WLP process, the cavity is sealed under a vacuum condition. This causes the mechanical quality factor of the switch to be very high since there is no air damping in the WLP enclosure, creating an unwanted large number of bounces for an ON transition. This effect is mitigated in our technology by a special Pulse Width Modulation (PWM) technique described in a later section.

RESULTS

MEMS Switch Requirements

In order to be used in a portable wireless application, MEMS switches have to demonstrate RF characteristics superior to solid-state FET devices, in addition to high yields and low cost. The MEMS switch must also withstand all of the required ruggedness tests associated with any RF part that is used in this application. Table 1 summarizes the measured characteristics of our MEMS contact switch.

RF Characteristics

Extensive RF small and large signal characterization has been done on our WLP MEMS switches. Our switches demonstrate the desirable loss and isolation typical of a MEMS device (see Figures 5, 6).

Table 1: Measured RFMD MEMS Contact Switch Characteristics

Parameter		Unit
RF Power Handling (0.9/2GHz) 7:1 VSWR	36/33	dBm
Insertion Loss/ Isolation (2GHz)	0.1/30	dB
2nd /3rd Harmonic (Pin=35dBm@900MHz)	<-65	dBm
DC contact resistance	1	Ohms
Actuation Voltage	<100	V
Beam Collapse Voltage	150	V
ON / OFF time (with PWM pulse)	5	uS
Ruggedness (900 MHz, 15:1 VSWR)	36	dBm
Lifetime Cycles	100E6	cycles

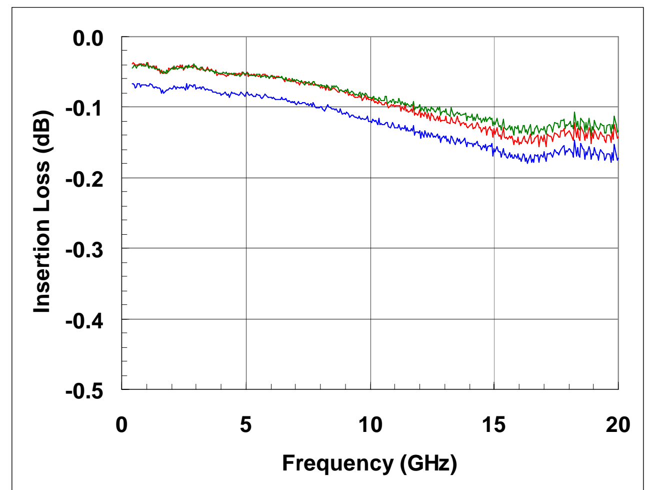

Figure 5. The insertion loss of our WLP MEMS switch is less than 0.1 dB up to 7 GHz.

As was mentioned earlier, our wafer level package is sealed under low pressure. This greatly reduces gas damping in the package and increases the Q of the MEMS switch. When the switch is actuated with a rectangular pulse the beam will bounce multiple times before settling in closed position. This behavior is illustrated in Figure 7. To mitigate this effect we employ a composite pulse actuation signal. The green trace is the high voltage signal seen by the gate and the blue trace is the switch response. The time needed for the transition from "open" to "closed" state can qualitatively be divided in three distinct segments. During the first one we apply a short pulse ("kick") to initiate movement of the mechanical structure and to transfer enough energy in the system. During the second time segment ("coast") the electrical stimulus is removed and the mechanical structure "coasts" through the remaining contact gap. Ideally, the movable structure should have zero kinetic energy when the contact is made. At this instant we apply a second actuation pulse ("hold") to latch the switch closed and to apply the force needed for low contact resistance.

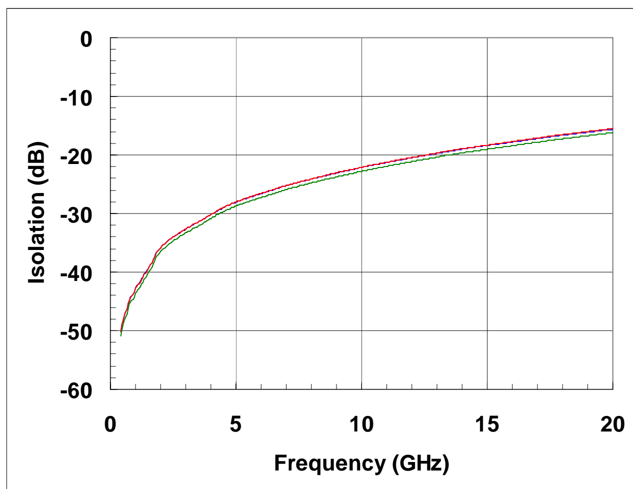

Figure 6. Isolation of our WLP MEMS switch on an SOI CMOS wafer is at least 30 dB up to 4 GHz.

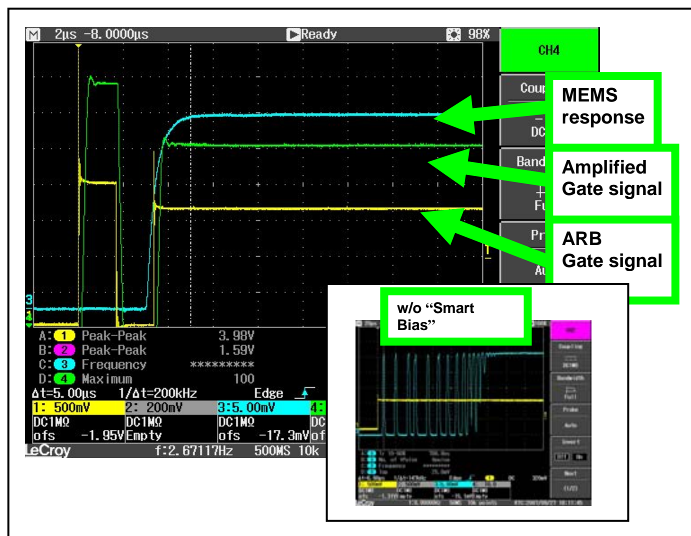

Figure 7. Pulse width modulation of switch actuation signal.

Reliability

After plastic overmold packaging, the switches have been measured and verified to retain a hermetic seal within the dielectric membrane. Package level reliability testing is on-going.

These switches have been subjected to repeated cycle testing, under both DC and RF stress. Our most recent results are shown in Figure 8. Work is continuing in this area to meet the reliability requirements of a cellular Transmit/Receive switch, which depending on the modulation and architecture of the system, may exceed 100 billion cycles.

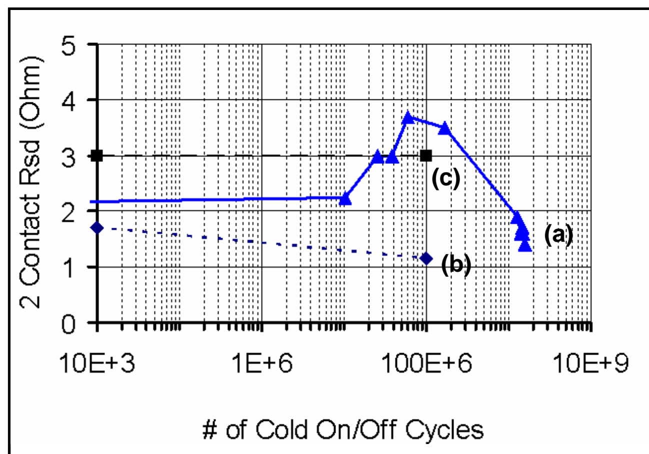

Figure 8. Cycle testing of RF MEMS switches at (a) 1 atm (without WLP), (b) 1e-3 atm (with WLP) without PWM actuation and (c) 1e-3 atm (with WLP) with PWM actuation.

CONCLUSION

We have reported the development of an above-IC MEMS contact switch technology which meets many of the requirements for use in high volume RF front end applications including timing, ruggedness, insertion loss, and isolation. The metal cantilever contact switch is hermetically sealed inside a dielectric membrane strong enough to withstand plastic overmold packaging. They have been successfully fabricated and tested on top of 0.5 um SOI-RFCMOS wafers. Work is continuing on the reliability of the switches to meet a transmit/receive level switch specifications.

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