Pure Appl. Chem., Vol. 76, No. 12, pp. 2051–2068, 2004.

Integrated nanoscale electronics and optoelectronics: Exploring nanoscale science and technology through semiconductor nanowires*

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Abstract: Semiconductor nanowires (NWs) represent an ideal system for investigating low-dimensional physics and are expected to play an important role as both interconnects and functional device elements in nanoscale electronic and optoelectronic devices. Here we review a series of key advances defining a new paradigm of bottom-up assembling integrated nanosystems using semiconductor NW building blocks. We first introduce a general approach for the synthesis of a broad range of semiconductor NWs with precisely controlled chemical composition, physical dimension, and electronic, optical properties using a metal cluster-catalyzed vapor–liquid–solid growth mechanism. Subsequently, we describe rational strategies for the hierarchical assembly of NW building blocks into functional devices and complex architectures based on electric field or micro-fluidic flow. Next, we discuss a variety of new nanoscale electronic device concepts including crossed NW p-n diode and crossed NW field effect transistors (FETs). Reproducible assembly of these scalable crossed NW device elements enables a catalog of integrated structures, including logic gates and computational circuits. Lastly, we describe a wide range of photonic and optoelectronic devices, including nanoscale light-emitting diodes (nanoLEDs), multicolor LED arrays, integrated nanoLED–nanoFET arrays, single nanowire waveguide, and single nanowire nanolaser. The potential application of these nanoscale light sources for chemical and biological analyses is discussed.

INTRODUCTION

The rapid miniaturization of electronics to the submicron scale has led to remarkable increases in computing power, while at the same time enabling cost reductions [1,2]. However, as the microelectronic industry advances toward ever smaller devices, it is believed that both physical and economic factors of current top-down silicon technology will soon limit further advances [3]. To go beyond these limits and fuel the expected demands of future society will require revolutionary breakthroughs rather than current evolutionary progress. In general terms, bottom-up assembled nanoscale electronics could provide

Pure Appl. Chem.* **76, 2051–2099 (2004). A collection of invited, peer-reviewed articles by the winners of the 2004 IUPAC Prize for Young Chemists.
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unparalleled speed, storage, and size reductions and hold the promise of powering future electronic devices that can outperform existing devices and open up totally new opportunities. To enable integrated nanoelectronics will require conceptually new device building blocks, scalable circuit architectures, and fundamentally different fabrication strategies. A bottom-up approach, where functional electronic structures are assembled from chemically synthesized, well-defined nanoscale building-blocks, has the potential to go far beyond the limits of top-down technology by defining key nanometer-scale metrics through chemical synthesis and subsequent assembly—not by lithography [4–7].

Previous studies have led to a broad range of proof-of-concept nanoscale devices including diodes and transistors based on individual organic molecules [8–12], quantum dots [13,14], or carbon nanotubes (NTs) [15,16]. However, these studies of individual nanodevices represent only an initial step toward nanoelectronic circuits. It remains a great challenge to advance from a single device level to the functional circuit level due to (1) the insufficient control of the properties of individual building blocks, (2) low device-to-device reproducibility, and (3) the lack of reliable methods for efficiently assembling and integrating building blocks into device arrays and circuits. Therefore, to move to this critical level of complexity and achieve integrated nanocircuits requires three fundamental advances, including (1) the development of rational approaches for the synthesis of nanoscale building blocks with precisely controlled chemical composition, physical dimension, and electronic, optical properties; (2) the development of rational strategies for the assembly of building blocks into increasingly complex structures; and (3) the demonstration of new nanodevice concepts that can be implemented in high yield by assembly approaches, and the development of new circuit architectures that are amenable to integration via self- or directed-assembly.

Central to the bottom-up approach are the nanoscale building blocks. One-dimensional (1D) nanostructures represent the smallest dimension structure that can efficiently transport electrical carriers, and thus are ideally suited to the critical and ubiquitous task of moving and routing charges, which constitute information, in nanoelectronics. In addition, 1D nanostructures can also exhibit critical device function, and thus can be exploited as both the wiring and device elements in future architectures for functional nanosystems. In this regard, two material classes, semiconductor nanowires (NWs) and carbon NTs, have shown particular promise. Single-walled NTs have been used to fabricate field effect transistors (FETs) [17,18], diodes [19,20], and logic circuits [21,22]. However, the inability to control whether NT building blocks are semiconducting or metallic and difficulties in manipulating individual NTs have made device fabrication largely a random event, and thus pose a significant barrier to achieving highly integrated nanocircuits.

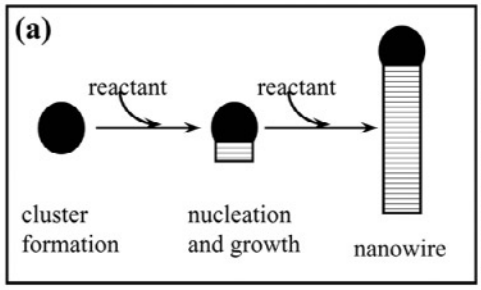
Semiconductor NWs represent another important and highly versatile nanometer-scale wire structures [23,24]. In contrast to NTs, semiconductor NWs can be rationally and predictably synthesized in single crystal form with all key parameters, including chemical composition, diameter, and length, and doping/electronic properties, controlled [25–27]. Semiconductor NWs thus represent the best-defined class of nanoscale building blocks, and this precise control over key variables has correspondingly enabled a wide range of devices and integration strategies to be pursued. For example, semiconductor NWs have been assembled into a series of electronic electronics devices including crossed NW p-n diodes [28–31], crossed NW-FETs [30], nanoscale logic gates and computation circuits [30], as well as optoelectronic devices including nanoscale light-emitting diodes (LEDs) [31] and lasers [32]. In contrast to NTs, NW devices can be assembled in a rational and predictable manner because the size, interfacial properties, and electronic properties of the NWs can be precisely controlled during synthesis, and moreover, reliable methods exist for their parallel assembly [28,33]. In addition, it is possible to combine distinct NW building blocks in ways not possible in conventional electronics and to leverage the knowledge base that exists for the chemical modification of inorganic surfaces [34,35] to produce semiconductor NW devices that achieve new function and correspondingly lead to unexpected device and system concepts.

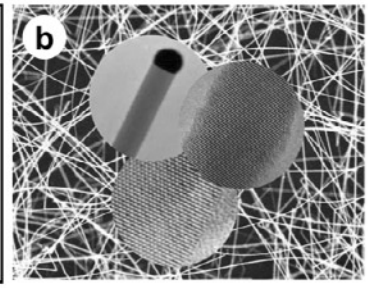
Here we review a series of key advances that defined a new paradigm of bottom-up assembly of nanoscale electronics and optoelectronics from semiconductor NWs building blocks. We first introduce

a general approach for the synthesis of a broad range of semiconductor NW building blocks with controlled properties. Next, we describe rational strategies for the hierarchical assembly of NWs into increasingly complex architectures. Lastly, we will discuss a variety of nanoscale electronic and optoelectronic devices and circuits assembled from these NW building blocks.

NANOWIRE BUILDING BLOCKS: SYNTHESIS AND PROPERTIES

Rational design and synthesis of nanoscale materials is critical to work directed toward understanding fundamental properties, creating nanostructured materials, and developing nanotechnologies [36,37]. In this regard, we have developed a general approach to controlled synthesis of a broad range of semiconductor NWs via a metal cluster-catalyzed vapor–liquid–solid (VLS) growth mechanism [38–41]. Here, the catalyst is envisioned as a nanocluster or nanodroplet that defines the diameter of the NWs and serves as the site that directs preferentially the addition of reactant to the end of a growing NW much like a living polymerization catalyst directs the addition of monomers to a growing polymer chain (Fig. 1a). Within this framework, a broad range of semiconductor NWs [38–41], typically with diameters on the order of 10 nm, and lengths extending up to tens of micrometers (Figs. 1b,c), can be rationally and predictably synthesized in single crystal form with all key parameters, including chemical composition, diameter, and length, and physical properties controlled [25–27].



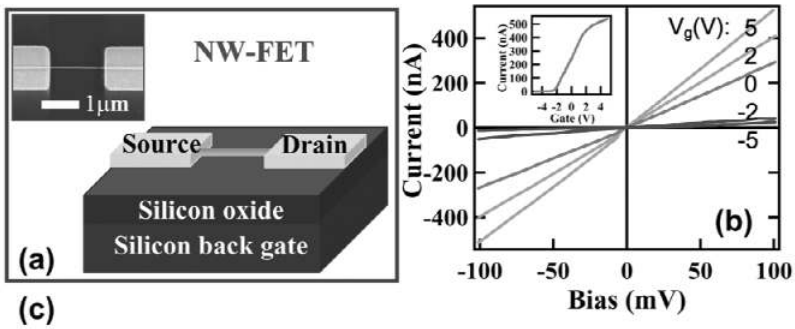


(c)

IV-IV Group	III-V Group Binary	III-V Group Ternary	II-VI Group Binary	IV-VI Group Binary
Si	GaN	$Ga(As_{(1-X)}P_X)$	ZnS	PbSe
Ge	GaP	$In(As_{(1-X)}P_X)$	ZnSe	PbTe
$Si_{(1-X)}Ge_X$	GaAs	$(Ga_{(1-X)}In_X)P$	CdS	
	InP	$(Ga_{(1-X)}In_X)As$	CdSe	
	InAs	$(Ga_{(1-X)}In_X)$ $(As_{(1-X)}P_X)$	Cd $(S_{(1-X)}Se_X)$	

Fig. 1 Semiconductor NW building blocks. (a) Schematics illustrating the underlying concept for catalytic growth of NWs. Liquid catalytic clusters act as the energetically favored site for localized chemical reaction, absorption of vapor-phase reactant and crystallization of crystalline NWs. (b) The figure shows a scanning electron microscope (SEM) image of as-synthesized semiconductor NWs. The circular insets show transmission electron microscope (TEM) images of the NWs. (c) Table summarizing NW materials grown with metal cluster-mediated catalytic approach. Adapted from [25].

The basic electronic properties of NWs can be characterized using electrical transport studies in a nanowire field effect transistor (NW-FET) configuration (Figs. 2a,b). The NW-FETs are prepared by dispersing a suspension of NWs in ethanol onto the surface of an oxidized silicon substrate, where the underlying conducting silicon is used as a global back gate [27,28,42]. Source and drain electrodes are defined by electron beam lithography followed by electron beam evaporation of metal contacts, and electrical transport measurements are done at room temperature. Current (I) vs. source-drain voltage (V_{sd}) and I vs. gate voltage (V_g) is then recorded for an NW-FET to characterize its electrical properties. Gate sweeping measurement of the NW-FET enables elucidation of important qualitative and quantitative properties of NWs. For example, changes in V_g produce variations in the electrostatic potential of the NW, and hence modulate the carrier concentration and conductance of the NW (Fig. 2b). Depending on the conductance modulation, it is possible to determine the doping type and estimate the carrier mobility in individual NWs using standard transistor formula: $dI/dV_g = \mu(C/L^2)V_{sd}$ and $C \cong 2\pi\varepsilon\varepsilon_0 L/\ln(2h/r)$, where μ is the carrier mobility, C is the capacitance, ε is dielectric constant, h is the thickness of the SiO_2 dielectric, L is the length, and r is radius of the NW [42]. In this way, we have characterized a broad range of NW materials including p-type Si, n-type GaN, CdS, and InP NWs. In all cases, the NW materials show excellent carrier mobility comparable to bulk materials (Fig. 2c) [43], which demonstrates the high quality of these materials.



(c)

Material		p-Si	n-InP	n-GaN	n-CdS
Carrier Mobility ($cm^2/V{\cdot}s$)	NW	40 - 300	400-4000	150 - 650	100 - 400
	Bulk	10-400	1000 - 3000	100 - 300	~ 200

Fig. 2 Nanowire electronic properties. (a) Schematic of an NW-FET used to characterize electrical transport properties of individual NWs. (inset) SEM image of an NW-FET; two metal electrodes, which correspond to source and drain, are visible at the left and right sides of the image. (b) Source-drain current vs. source-drain voltage for an n-type InP NW-FET. The numbers inside the plot indicate the corresponding gate voltages (V_g). The inset shows current vs. V_g for V_{sd} of 0.1 V. (c) Table summarizing carrier mobility in various NW materials in comparison with their bulk material counterpart of similar carrier concentration.

We have also carried out optical studies to investigate the photoluminescence properties of these NW materials [39,44]. Photoluminescence measurements were made on individual NWs using a home-built microluminescence instrument. Studies on a broad range of compound semiconductor NWs including GaN, CdS, CdSeS, and CdSe showed clean luminescence with spectra maxima of ~370, ~510, ~600, and ~700 nm, respectively [31], which are consistent with near band edge emission in these materials, and thus demonstrate excellent optical properties of these NW materials. Furthermore, photolu-

minescence studies on InP NWs of variable sizes showed systematic blue-shift of emission peak from ~900 to ~810 nm as the diameter of the InP NWs is reduced from 50 to 10 nm, which can be attributed to quantum confinement effect [44]. Therefore, it is possible to control the emission wavelength of these NW materials by either varying the chemical composition or physical dimension, thus offering the greatest flexibility to precisely tune the color of nano-photonic devices.

HIERARCHICAL ASSEMBLY NANOWIRES

The availability of a broad range of semiconductor NWs with controlled electronic and optical properties opens many exciting opportunities in fundamental sciences as well as technological applications. To fully explore the potential of these NW building blocks for integrated nanosystems will require the development and implementation of efficient and scalable strategies for assembling them into increasingly complex architectures. First, methods are needed to assemble NWs into highly integrated arrays with controlled orientation and spatial position. Second, approaches must be devised to assemble NWs on multiple length scales and to make interconnects between nano-, micro- and macroscopic worlds. To address these critical next levels of organization, we have focused significant effort on developing complementary strategies for hierarchical assembly of NWs on surfaces, and describe two promising approaches below.

Electrical field-directed assembly

Applied electrical fields (E-fields) can be used effectively to attract and align NWs due to their highly anisotropic structures and large polarizabilities (Fig. 3) [28]. This underlying idea of E-field-directed assembly can be readily seen in images of NWs aligned between parallel electrodes (Fig. 3b), which demonstrate that virtually all of the NWs aligned in parallel along the E-field direction. E-field directed assembly can also be used to position individual NWs at specific positions with controlled directionality. For example, E-field assembly of NWs between an array of electrodes (Fig. 3c) clearly shows that

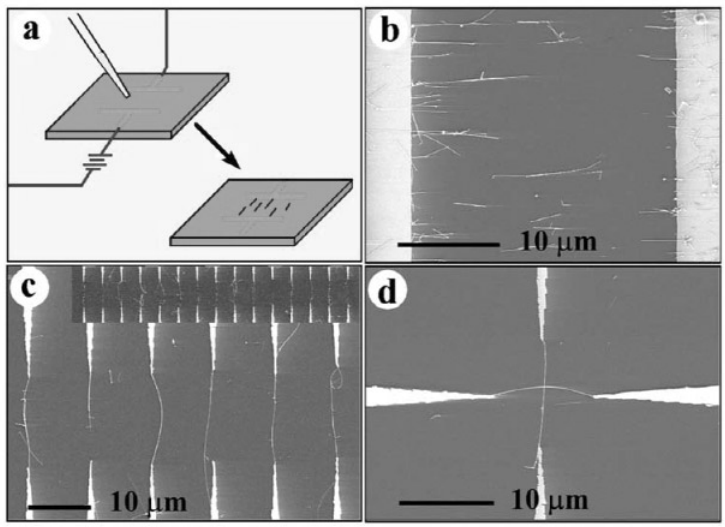


Fig. 3 E-field-directed assembly of NWs. (a) Schematic view of E-field alignment. (b) Parallel array of NWs aligned between two parallel electrodes. (c) Spatially positioned parallel array of NWs obtained following E-field assembly. The top inset shows 15 pairs of parallel electrodes with individual NWs bridging each diametrically opposed electrode pair. (d) Crossed NW junction obtained using layer-by-layer alignment with the E-field applied in orthogonal directions in the two assembly steps. Adapted from [28].

individual NWs can be positioned to bridge pairs of diametrically opposed electrodes and form a parallel array. In addition, by changing the E-field direction with sequential NW solutions, the alignment can be carried out in a layer-by-layer fashion to produce crossed NW junctions (Fig. 3d). These results demonstrate clearly that E-field-directed assembly can be used to align and position individual NWs into parallel and crossed arrays, which correspond to two basic geometries for integration, and thus provide one robust approach for rational and parallel assembly of nanoscale device arrays.

Fluidic flow-directed assembly

E-field-directed assembly, which represents the first demonstration of rational assembly of 1D nanostructures, also has limitations, including (1) the need for substantial conventional lithography to pattern microelectrode arrays used to produce aligning fields and (2) the deleterious effect of fringing electric fields at the submicron length scales. To achieve a greater flexibility in rational, parallel assembly of 1D nanostructures into integrated nanosystems, we have developed a further powerful approach based on fluidic flow [33]. In this method, NWs or NTs can be aligned by passing a suspension of NWs through microfluidic channel structures, for example, formed between a poly(dimethylsiloxane) (PDMS) mold [45] and a flat substrate (Fig. 4a). Images of NWs assembled on substrate surfaces (Fig. 4b) within microfluidic flows demonstrate that virtually all of the NWs are aligned along the flow direction. This alignment readily extends over hundreds of micrometers, and is limited only by the size of the fluidic channels used. The alignment of NWs within the channel flow can be understood within the framework of shear flow [46,47]. Specifically, the channel flow near the substrate surface resembles a shear flow, and linear shear force aligns the NWs in the flow direction before they are immobilized on the substrate.

The fluidic flow assembly approach can be used to organize NWs into more complex crossed NW structures, which are critical for building high-density nanodevice arrays, using a layer-by-layer deposition process (Fig. 4c). The formation of crossed and more complex structures requires that the nanostructure–substrate interaction is sufficiently strong that sequential flow steps do not affect preceding ones: we find that this condition is readily achieved by modifying the substrate surface with proper functional chemical groups. For example, alternating the flow in orthogonal directions in a two-step assembly process yields crossbar structures in high yield (Fig. 4d). Experiments have demonstrated that crossbars extending over 100s of microns on a substrate with only 100s of nanometers separation between individual cross-points are obtained through a very straightforward, parallel, low-cost, and fast process.

Fluidic flow directed assembly of multiple crossed NW arrays offers significant advantages over previous efforts. First, it is intrinsically very parallel and scalable with the alignment readily extending over very large length scales. Second, this approach is general for virtually any elongated nanostructure including carbon NTs and DNA molecules. Third, it allows for the directed assembly of geometrically complex structures by simply controlling the angles between flow directions in sequential assembly steps. For example, equilateral triangles have been assembled in a three-layer deposition sequence using 60° angles between the three flow directions [33]. The method of flow alignment thus provides a flexible way to meet the requirements of many device configurations in the future. An important feature of this sequential assembly scheme is that each layer is independent, and thus a variety of homo- and hetero-junction configurations can be obtained simply by changing the composition of the NW suspension used for each flow step.

To enable further control of spatial location and periodicity of assembled NW arrays, we have explored complementary chemical interactions between chemically patterned substrates and NWs (Fig. 4e). Substrates for alignment are first patterned with two different functional groups, with one of the functional groups designed to have a strong attractive interaction with the NW surface, and then following flow alignment, regular, parallel NW arrays with lateral periods the same as those of the surface patterns are produced (Fig. 4f). These experiment demonstrates that the NWs are preferentially assem-

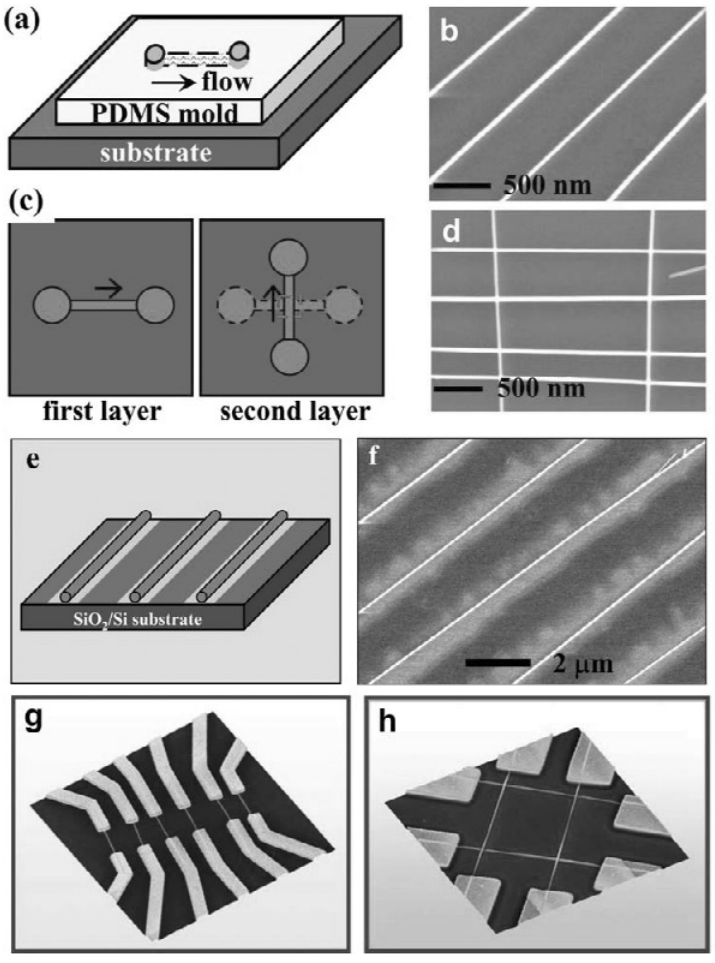


Fig. 4 Fluidic flow-directed assembly of NWs. (a,b) Schematic (a) and SEM image (b) of parallel NW arrays obtained by passing a NW solution through a channel on a substrate; (c,d) Schematic (c) and SEM image (d) of crossed NW matrix obtained by orthogonally changing the flow direction in a sequential flow alignment process. (e,f) Schematic (e) and SEM image (f) of regular NW arrays obtained by flowing NW solution over a chemically patterned surface. (g,h) Parallel and crossed NW device arrays obtained with fluidic flow assembly. Adapted from [33].

bled at positions defined by the chemical pattern, and moreover, show that the periodic patterns can organize the NWs into regular superstructures. It is important to recognize that the patterned surface alone does not provide good control of the 1D nanostructure organization. Assembly of NTs [48,49] and NWs on patterned substrates shows that 1D nanostructures align with bridging and looping structures over the patterned areas and show little directional control. Our use of fluidic flows avoids these significant problems and enables controlled assembly in one or more directions. By combining this approach with other surface patterning methods, such as phase separation in diblock copolymers [50] and spontaneous ordering of molecules [51], it should be possible to generate well-ordered NW arrays without the limitations of conventional lithography.

The above discussions clearly demonstrate that NWs can be assembled on the surface with controlled orientation and spatial location. By combining them with conventional lithography approach, a variety of integrated device structures including parallel arrays (Fig. 4g) [52] and crossed arrays (Fig. 4h) [33] can be explored. Such integrated device arrays offers a variety of opportunities for us to

investigate the fundamental properties of these NW materials and explore them for various device application. In particular, the crossed NW matrix represents an important geometrical configuration for nanocircuits, where each crossing point can function as an independently addressable nanoscale device element.

NANOWIRE ELECTRONICS

The ability to rationally synthesize NWs with controlled electronic properties and to assemble NWs into regular arrays readily enabled us to explore these NW structures for a variety of functional device arrays.

Crossed nanowire devices

Direct assembly of highly integrated functional electronic circuits based on NWs requires (1) the development of new device concepts with scalable device configuration and (2) high yield assembly of these devices with controllable functional properties. The crossed NW matrix represents an ideal configuration since the critical device dimension is usually defined by the cross-point and can be readily scaled down to nanometer level, and crossed NW configuration itself is naturally a scalable architecture and thus enables the possibility of massive system integration. Moreover, the crossed NW matrix is a versatile structure and can be configured into a variety of critical device elements, such as diodes and transistors. For example, a p-n diode can be obtained by simply crossing a p- and n-type NW as demonstrated in the cases of p-Si/n-Si, p-InP/n-InP, p-InP/n-CdS and p-Si/n-GaN materials [28–31]. Electrical measurements of such crossed junctions show clear current rectification across the junction and linear current behavior in individual NWs, demonstrating the formation of p-n diode at the crossing point (Fig. 5a). To gauge the reproducibility of these assembled NW p-n diodes, we have studied a large number of p-n junctions assembled from p-Si NWs and n-GaN NWs (inset, Fig. 5a) [30]. I-V measurements made on over 100 crossed p-Si/n-GaN NW devices show that over 95 % of the junctions exhibit current rectification with turn-on voltages of around 1.0 V. Reproducible assembly of crossed NW structures with predictable electrical properties contrasts sharply with results from NT-based device, and readily enabled us also to explore the assembly and properties of integrated p-n diode arrays. Significantly, electrical transport measurements made on a typical 4 by 1 crossed p-Si/n-GaN junction array (Fig. 5b) show that the four nanoscale cross-points form independently addressable p-n diodes with clear current rectification and similar turn-on voltages.

Nanoscale FETs can also be achieved in the crossed NW configuration using one NW as the active conducting channel and the other crossed NW as the gate electrode (Fig. 5c). Significantly, the three critical FET device metrics are naturally defined at the nanometer scale in the assembled crossed NW-FETs (cNW-FETs): (1) a nanoscale channel width determined by the diameter of the active NW (~2–20 nm depending on chosen NW); (2) a nanoscale channel length defined by the crossed gate NW diameter (~10 nm); and (3) a nanoscale gate dielectric thickness determined by the NW surface oxide (~1 nm). These distinct nanoscale device metrics lead to greatly improved device characteristics such as high gain, high speed, and low power dissipation. For example, the conductance modulation of an NW-FET is much more significant with the NW gate ($>10^5$) than that with a global back gate (<10) (inset in Fig. 5d). Moreover, the local NW gate enables independently addressable FET arrays and thus enables highly integrated nanocircuits.

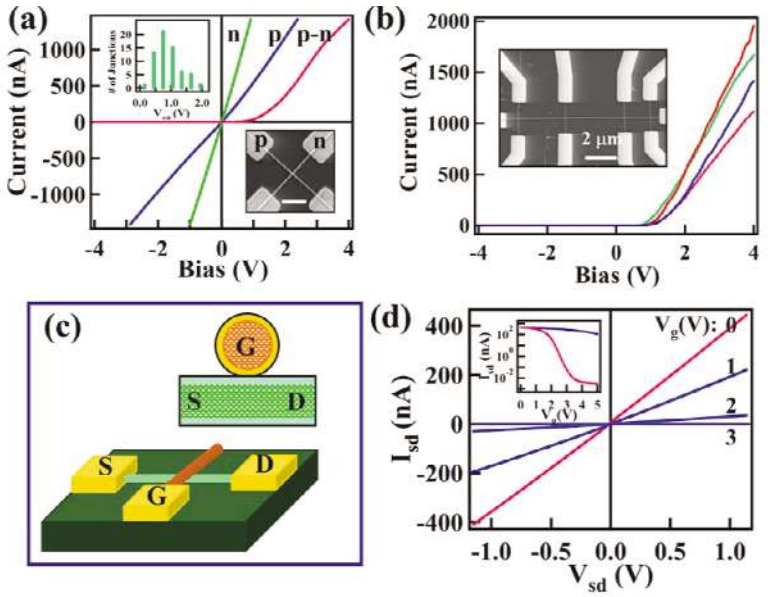


Fig. 5 Crossed nanowire devices. (a) Top, current-voltage (*I-V*) relation of the crossed p-n diode. Linear or nearly linear *I-V* behavior of the p- (blue) and n-type (green) NWs indicates good contact between NWs and metal electrodes. *I-V* curves across the junction (red) show clear current rectification. The top-left inset shows histogram of turn-on voltage for over 70 as-assembled junctions showing a narrow distribution around 1 V. The bottom-right inset shows a typical SEM image of a crossed NW p-n diode. Scale bar: 1 μm. (**b**) *I-V* behavior for a 4(p)x1(n) multiple junction array. Inset shows an SEM image of a NW p-n diode array. (**c**) Schematics illustrating the crossed NW-FET concept. (**d**) Gate-dependent *I-V* characteristics of a cNW-FET formed using a p-NW as the conducting channel and n-NW as the local gate. The red and blue curves in the inset show I_{sd} vs. V_{gate} for n-NW (red) and global back (blue) gates when the V_{sd} is set at 1 V. The conductance modulation (>10^5) of the FET is much more significant with the NW gate than that with a global back gate (<10). Adapted from [30].

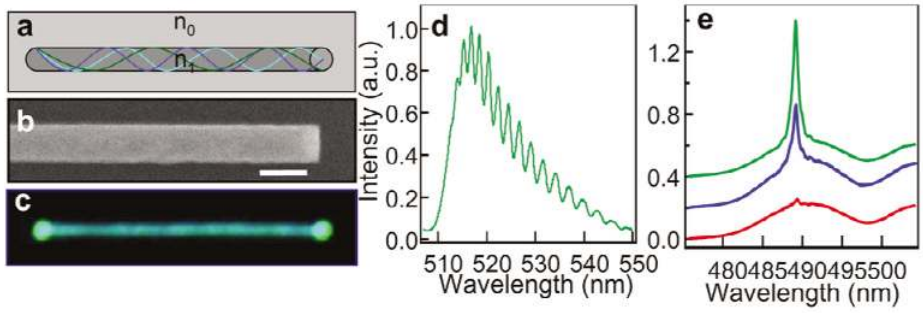


Fig. 9 Nanowire optical waveguide, cavity, and laser with optical excitation. (a) Schematic showing an NW as an optical waveguide; with cleaved ends it defines a Fabry–Perot cavity. (b) SEM image of a cleaved CdS NW end. Scale bar, 100 nm. (c) Room-temperature photoluminescence image of a CdS NW uniformly excited with a mercury lamp. (d) Photoluminescence spectrum from the NW end exhibiting periodic intensity modulation, which corresponds to the Fabry–Perot modes of the NW. (e) Emission spectra from a CdS NW end with a pump power of 190, 197, and 200 mW (red, blue, and green) recorded at 8 K show preferential gain at single mode and demonstrate laser emission. Adapted from [32].

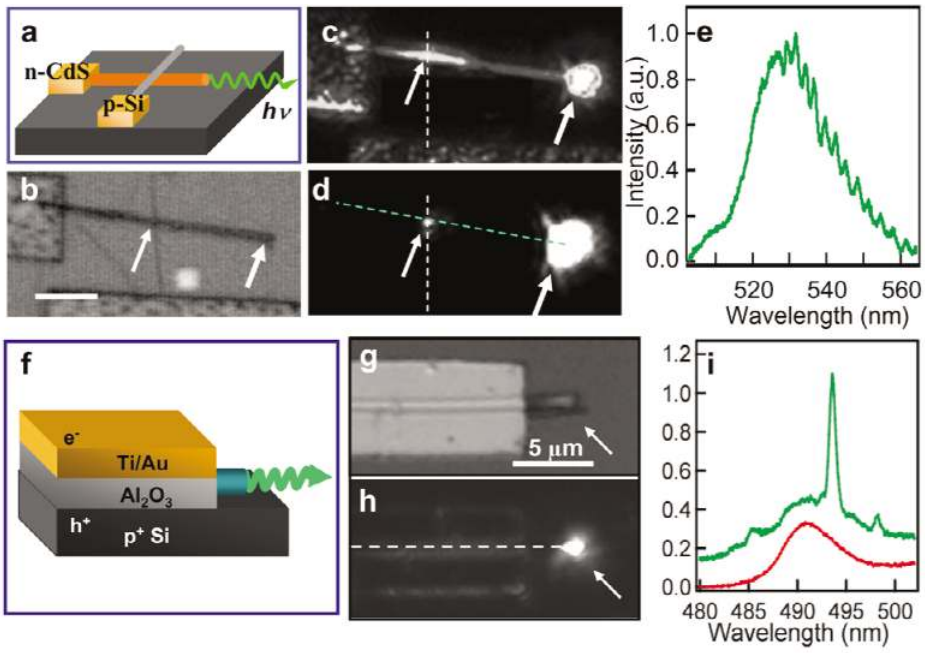


Fig. 10 Nanowire optical waveguide, cavity, and laser with electrical excitation. (a) Device schematic illustrating a p-n diode formed between p-Si and n-CdS NWs, where the CdS NW forms the cavity and active medium. (b) Optical image of a device with arrows highlighting the cross-point (blue) and CdS NW end (green). Scale bar, 5 μm. (c,d) The electroluminescence image obtained at room temperature with the device forward biased at 5 V. White light illumination is used in image (c) to show the electrodes. The two bright spots highlighted by blue and green arrows correspond to the emission from the cross-point and end, respectively. (e) Electroluminescence spectra from the NW end show periodic intensity modulation, demonstrating NW can function as optical waveguide and cavity in this injection device. (f) Schematic showing a hybrid device structure. In this structure, electrons and holes can be injected into the CdS nanowire cavity along the whole length from the top metal layer and the bottom p-Si layer, respectively. (g) Optical image of a device described in (f). The arrow highlights the exposed CdS NW end. Scale bar, 5 μm. (h) Electroluminescence image recorded from this device at room-temperature with an injection current of ca. 80 μA. The arrow highlights emission from the CdS NW end. The dashed line highlights the NW position. (i) Emission spectra from a CdS nanowire device with injection currents of 200 μA (red) and 280 μA (green) recorded at 8 K. These spectra are offset by 0.10 intensity units for clarity. Adapted from [32].

Nanoscale logic gates and computational circuits

High-yield assembly of crossed NW p-n diodes and cNW-FETs from p-Si and n-GaN materials enables more complex functional electronic circuits, such as logic gates to be produced. Logic gates are critical blocks of hardware in current computing systems that produce a logic-1 and logic-0 output when the input logic requirements are satisfied. Diodes and transistors represent two basic device elements in logic gates [53]. Transistors are more typically used in current computing systems because they can exhibit voltage gain. Diodes do not usually exhibit voltage gain, although they may also be desirable in some cases [30,53]; for example, the circuit architecture and constraints on the assembly of nanoelectronics might be simplified using diodes since they are two-terminal devices, in contrast to three-terminal transistors. In addition, by combining the diodes and transistors in logic circuits, it is possible to achieve high voltage gain, while simultaneously maintaining a simplified device architecture. To demonstrate the flexibility of these NW device elements, we have investigated both diode- and FET-based logic.

For example, a two-input logic OR gate was realized using a 2(p) by 1(n) crossed NW p-n diode array [30]. When either of the input to the p-NW is high, a high output is obtained at the n-NW as the p-n diode is forward biased; a low output is only achieved when both inputs are low; and thus realizing the same function as a conventional logic "OR" gate (Figs. 6a,b). A logic AND gate was also assembled from two p-n diodes and one cNW-FET (Figs. 6c,d), and a logic NOR gate with gain over 5 was assembled from three cNW-FETs in series (Figs. 6e,f). Importantly, logic OR, AND, and NOR gates form a complete set of logic elements and enable the organization of virtually any logic circuits. For ex-

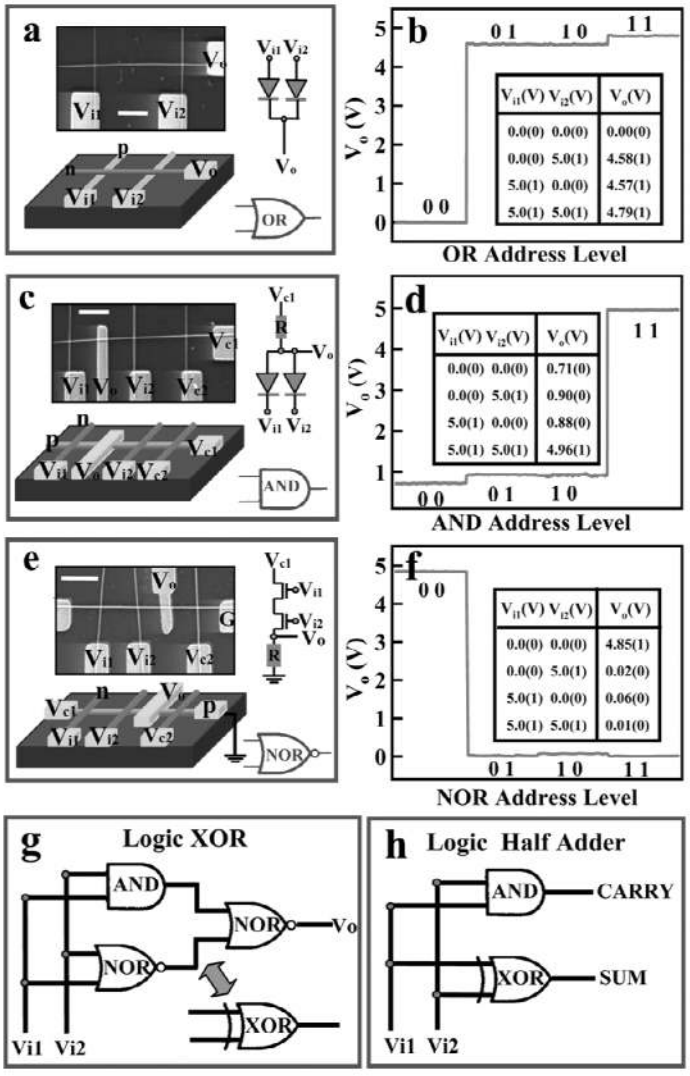


Fig. 6 Nanoscale logic gates. (a,b) Schematic and measured output vs. address level relation for a logic OR gate assembled from two-crossed NW p-n diode. The insets in (a) show the SEM image and equivalent electronic circuit of the device. The bar is 1 μm. The inset in (b) shows the experimental truth table for nano-OR gate. (c,d) Schematic and measured output vs. address level relation for a logic AND gate assembled from two-diode and one-crossed NW-FET. The inset in (d) shows the experimental truth table for the nano-AND gate. (e,f) Schematic and measured output vs. address level relation for a logic NOR gate assembled from three-crossed NW-FET. The inset in (f) shows the experimental truth table for the nano-NOR gate. (g,h) Schematics for a logic XOR gate and logic half adder realized by interconnecting individual logic gate elements. Significantly, the logic half adder assembled this way can be used to do digital computation just as conventional electronics do. Adapted from [30].

ample, NW logic gates have been interconnected to form an XOR gate and a logic half adder, which was used to carry out digital computations in a way similar to conventional electronics (Figs. 6g,h).

NANOSCALE PHOTONICS AND OPTOELECTRONICS

The availability of a wide range of NW materials readily allows us to choose materials with different properties to tailor device functions in a manner that is unique to the bottom-up assembly approach. In addition to nanoscale electronics, the broad range of optically active III-V and II-VI group compound semiconductor NW materials are attractive as building blocks for miniaturized photonic and optoelectronic devices. To this end, we have assembled of a variety of photonic devices, including nanoscale LEDs and diode array, single NW optical waveguide, cavity, and laser.

Nanoscale LED and diode array

We have previous described a p-n diode can be obtained by crossing a p- and n-type NW. In direct band gap semiconductors like InP, the p-n diode also forms the basis for the critical optoelectronics devices, including LEDs and laser diodes (LDs). To assess whether our nanoscale devices might behave similarly, we have studied the electroluminescence (EL) from crossed NW p-n junctions. Significantly, EL can be readily observed from these nanoscale junctions in forward bias. A 3D plot of the EL intensity taken from a typical NW p-n diode at forward bias (Fig. 7a) shows the emitted light comes from a point-

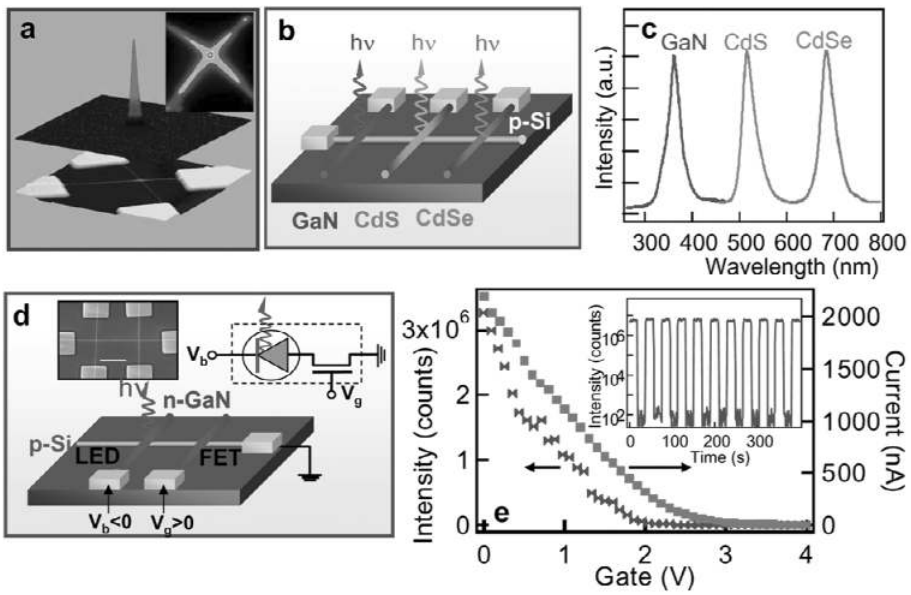


Fig. 7 NanoLED. (a) Crossed InP nanowire LED. (top) Three-dimensional (3D) plot of light intensity of the electroluminescence from a crossed NW LED. Light is only observed around the crossing region. (bottom) 3D atomic force microscope image of a crossed NW LED. (inset) Photoluminescence image of a crossed NW junction. (b) Multicolor nanoLED array. Schematic of a tri-color nanoLED array assembled by crossing one n-GaN, n-CdS, and n-CdS NW with a p-Si NW. The array was obtained by fluidic assembly and photolithography with ca. 5 μm separation between NW emitters. (c) Normalized EL spectra obtained from the three elements. (d) Integrated as a nanoFET-nanoLED array. Schematic of an integrated crossed NW-FET and LED. Inset shows SEM image of a representative device (scale bar, 3 μm) and the equivalent circuit. (e) Plots of current and emission intensity of the nanoLED as a function of voltage applied to the NW gate at a fixed bias of –6 V. (inset) EL intensity vs. time relation a voltage applied to NW gate is switched between 0 and +4 V for fixed bias of –6 V. Adapted from [31].

like source, and moreover, comparison of EL and PL (inset, Fig.7a) images recorded on the same sample show that the position of the EL maximum corresponds to the crossing point in the PL image. These data thus demonstrate that the emitted light indeed comes from the crossed NW p-n junction.

EL spectra (peaked 820 nm) recorded from the cNW-LEDs exhibit blue-shifts relative to the bulk band gap of InP (925 nm). The blue-shifts are due in part to quantum confinement of excitons, although other factors may also contribute. Furthermore, PL studies have demonstrated that the PL peak can be systematically blue-shifted as the NW diameter is decreased [44], and thus these results provide a means for controlling the color of the LEDs in a well-defined way. Indeed, EL results recorded from p-n junctions assembled from smaller (and larger) diameter NWs show larger (smaller) blue-shifts. In addition, the emission color from nanoLEDs can be further varied by using chemically distinct semiconductor NWs with different band gaps. Considering the wide range of group IV, III-V, and II-VI semiconductor NW materials available [25], it is possible to assemble a variety of NW-based nanoLEDs for different spectral regimes [31]. Indeed, we have recently demonstrated that crossing p-type Si NWs with n-type GaN, CdS, CdSeS, CdSe, and InP can produce nanoLEDs with emission spectra covering the whole spectra regime from UV to near IR [31]. In such heterostructure devices, p-Si NWs are used as the passive hole-injector, and the n-type compound NWs are used as electron-injector and active emitter, which defines the wavelength of emission.

The bottom-up assembly approaches allows flexible combination of chemically distinct nanoscale building blocks that would otherwise be structurally and/or chemically incompatible in a sequential growth process typical of planar fabrication. This capability should enable assembly of nanostructures with functions not readily obtained by other methods and open new opportunities. For example, we have exploited the ability to form nanoLEDs with nonemissive Si NW hole-injectors to assemble multicolor arrays consisting of n-type GaN, CdS, and CdSe NWs crossing a single p-type SiNW (Fig. 7b). Normalized emission spectra recorded from the array demonstrate three spectrally distinct peaks with maxima at 365, 510, and 690 nm (Fig. 7c) consistent with band edge emission from GaN, CdS, and CdSe, respectively. The ability to seamlessly assemble/integrate different materials together and independently tune the emission from each nanoLED offers substantial potential producing specific wavelength sources, and demonstrates an important step toward integrated nanoscale photonic circuits. Although lithography sets the integration scale of these multicolor arrays, it should be possible to create much denser nanoLED arrays via (1) controlled growth of modulated NW superlattice structures [54] and/or (2) selective assembly of different semiconductor materials [55].

In addition, we have assembled optoelectronic circuits consisting of integrated crossed NW LED and FET elements (Fig. 7d). Specifically, one GaN NW forms a p-n diode with the SiNW, and a second GaN NW functions as a local gate as described previously. Measurements of current and emission intensity vs. gate voltage show that (i) the current decreases rapidly with increasing voltage as expected for a depletion mode FET and (ii) the intensity of emitted light also decreases with increasing gate voltage. When the gate voltage is increased from 0 to +3 V, the current is reduced from ca. 2200 nA to an off state, where the supply voltage is –6 V (Fig. 7e). Advantages of this integrated approach include switching with much smaller changes in voltage (0 to 3 vs. 0 to 6 V) and the potential for much more rapidly switching. The ability to use the nanoscale FET to switch reversibly the nanoLED on and off has also been demonstrated (inset, Fig. 7e).

The potential of coupling the bottom-up assembly of nanophotonic devices together with top-down fabricated silicon structures has also been investigated, since this coupling could provide a new approach for introducing efficient photonic capabilities into integrated silicon electronics. To this end, a hybrid top-down/bottom-up approach was employed (1) using lithography to pattern p-type silicon wires on the surface of a silicon-on-insulator (SOI) substrate, and then (2) assembling n-type emissive NWs on top of silicon structures to form arrays consisting of p-n junctions at cross-points (Fig. 8a). Conceptually, this hybrid structure (Fig. 8b) is virtually the same as the crossed NW structures described above and should produce EL in forward bias. Notably, *I-V* data recorded for a hybrid p-n diode formed between the p-Si and an n-CdS NW show clear current rectification (Fig. 8c) and sharp EL spec-

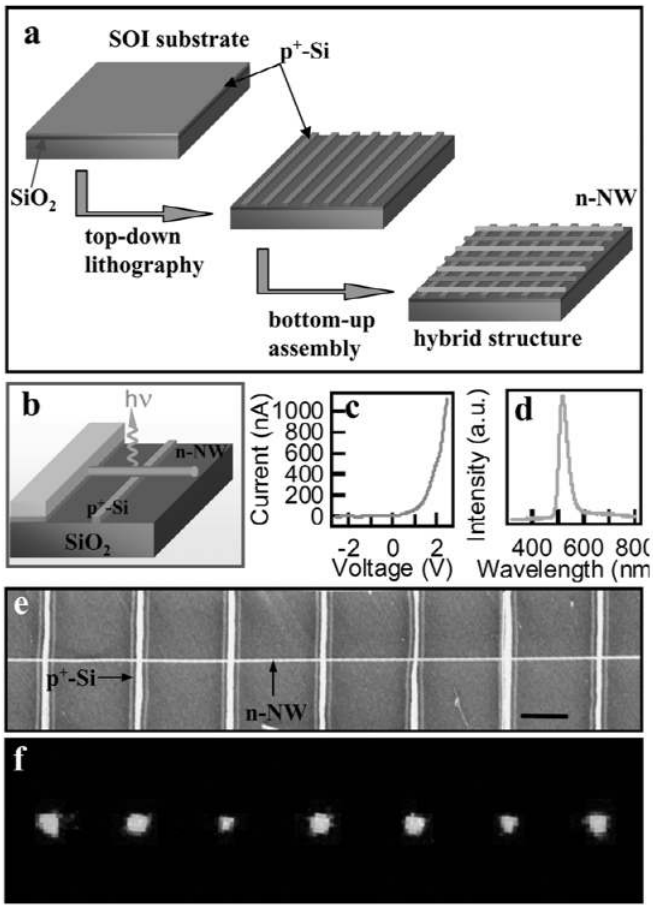


Fig. 8 Integration of nanowire photonics with silicon electronics. (a) Schematic illustrating fabrication of hybrid structures. A silicon-on-insulator (SOI) substrate is patterned by standard electron-beam or photolithography followed by reactive ion etching. Emissive NWs are then aligned onto patterned SOI substrate to form photonic sources. (b) Schematic of a single LED fabricated by the method outlined in (a). (c) *I-V* behavior for a crossed p-n junction formed between a fabricated p^+-Si electrode and an n-CdS NW. (d) EL spectrum from the forward-biased junction. (e) SEM image of a CdS NW assembled over seven p^+-silicon electrodes on an SOI wafer; scale bar is 3 μm. (f) EL image recorded from an array consisting of a CdS NW crossing seven p^+-Si electrodes. The image was acquired with +5 V applied to each silicon electrode while the CdS NW was grounded. Adapted from [31].

trum peaked at 510 nm (Fig. 8d), which is consistent with CdS band edge emission. Importantly, the photonic devices produced in this approach are highly reproducible and can be readily implemented in integrated arrays. For example, a 1×7 crossed array consisting of a single CdS NW over 7-fabricated p-Si wires (Fig. 8e) exhibits well-defined emission from each of the cross-points in the array (Fig. 8f). Similar results were also obtained for two-dimensional arrays and demonstrate clearly that bottom-up assembly has the potential to introduce photonic function into integrated silicon microelectronics.

Single nanowire waveguide, Fabry–Perot cavity and laser

In addition to LEDs, nanoscale optical waveguide, cavity, and laser are vital for the realization of highly integrated photonic circuits. Importantly, free-standing semiconductor NWs can function as stand-alone optical waveguides, cavities and gain medium to support lasing emission [32,56,57]. In general, a NW

can function as a single-mode optical waveguide much like a conventional optical fiber [58] when $1 \sim (\pi D/\lambda)(n_1{}^2 - n_0{}^2)^{0.5} < 2.4$, where D is the NW diameter, λ is the wavelength, and n_1 and n_0 are the refractive indices of the NW and surrounding medium, respectively (Fig. 9a, see color plate, p. 2059). If the ends of the NW are cleaved (Fig. 9b), they can function as two reflecting mirrors that provide optical feedback and define a Fabry–Perot optical cavity with modes $m(\lambda/2n_1) = L$, where m is an integer and L is the length of the cavity. Photoluminescence image of CdS NWs of proper diameter shows pronounced emission from both ends (Fig. 9c), clearly demonstrating waveguide effect along the NW axis. Furthermore, spectra of the emissions from NW ends show prominent periodic modulation in intensity, which can be attributed to the longitudinal modes of a Fabry–Perot cavity (Fig. 9d). For a cavity of length L, the mode spacing, $\Delta\lambda$, is given by $(\lambda^2/2L)[n_1 - \lambda(dn_1/d\lambda)]^{-1}$, where $dn_1/d\lambda$ is the dispersion relation for the refractive index. This expression provides a good description of the observed spacing when the measured nanowire length. Moreover, analysis of similar data from NWs of varying length demonstrates that the mode spacing is inversely proportional to the wire length as expected. Together, these results demonstrate that the individual NW can function as nanoscale optical waveguide and Fabry–Perot cavity. The observation of sharp modes in the uniform CdS NW gain medium suggests a single NW can support laser emission. Indeed, optical excitation at higher powers leads to preferential gain in a single mode and the onset of lasing (Fig. 9e).

The observation of laser emission with optical excitation further prompts us to investigate electrically pumped nanolasers. To achieve electrical pumped lasers requires efficient injection of both electrons and holes into the NW cavity and gain medium. Our initial studies of electrical injection into CdS NW cavities were carried out using an n-type CdS and p-type silicon (p-Si) crossed NW structures (Figs. 10a,b, see color plate, p. 2059). In forward bias, these crossed NW structures exhibit strong electroluminescence with several important characteristics. Images of the electroluminescence (Figs. 10c,d) show two points of emission: one corresponding to the n-CdS/p-Si NW cross-point and the other to the end of the CdS NW. Significantly, the intensity of the end emission is at least two orders of magnitude larger than the cross-point emission. Further more, EL spectra recorded from the CdS NW end exhibit a prominent modulation in intensity, which can be assigned to the longitudinal modes of a Fabry–Perot cavity formed in CdS NW in this crossed device (Fig. 10e). These results clearly demonstrating that the CdS NWs can function as excellent waveguides and Fabry–Perot cavity in this relatively simple device configuration, and suggest that at sufficiently high injection currents lasing should be achieved. However, the crossed NW devices are clearly not optimal for achieving high-density injection into the whole NW cavity, as high injection current invariably led to breaking down of the device at the cross-point due to the nature of localized injection.

To enable more uniform injection, we have implemented a hybrid structure (Figs. 10f,g) in which holes are injected along the length of a CdS NW cavity from a p-Si electrode defined in a heavily doped p-Si layer on a planar substrate [32]. Images of the room-temperature electroluminescence produced in forward bias from these structures (Fig. 10h) show strong emission from the exposed CdS NW end. Low-temperature measurements made on the devices have shown the preferential pumping into single mode. At low injection currents, the spectrum of the end emission (Fig. 10i) shows a broad peak with FWHM ~5 nm. Significantly, when the injection current is increased further, it was found that the emission intensity increased abruptly, and the spectrum quickly collapsed into a limited number of sharp peaks with a dominant emission line around 493 nm. Importantly, we find that the dominant mode has an instrument resolution limited line width of only 0.7 nm, demonstrating that the injection lasing is achieved in this new type of device. Using individual NWs as the laser cavity and gain medium for laser diodes represents a new and powerful approach for producing integrated electrically driven photonic devices. This basic approach, which relies upon bottom-up assembly of the key laser cavity/medium in a single step, can be extended to other materials, such as GaN and InP NWs, to produce nanoscale lasers that not only cover the ultraviolet through near infrared spectral regions, but also can be integrated as single or multi-color laser source arrays in silicon microelectronics and lab-on-a-chip devices.

Nanophotonics as excitation sources

The ability to assemble a wide variety of nanoscale light sources with tunable emission wavelength from UV to near IR regime can lead to a range of exciting opportunities in intra/inter-chip optical communication, integrated chemical/biological sensing and medical diagnostics on the chip level. For example, the localized EL from crossed NW nanoLEDs and hybrid LEDs can result in a near-field power densities greater than 100 W/cm^2, which is sufficient to excite molecular and nanoparticle chromophores. To explore this important possibility, we have used a CdS-based nanoLED to excite and record the emission spectra from CdSe quantum dots (QDs) and propidium iodide (a fluorescent nucleic acid stain) (Fig. 11) [31]. Notably, the emission of CdSe QDs and propidium iodide obtained by nanoLED excitation show essentially the same spectra (solid lines, Figs. 11a,b) as those obtained using much larger conventional excitation source (dashed lines, Figs. 11a,b). These results demonstrate that nanoLEDs could function as efficient excitation sources for integrated chemical and biological analysis.

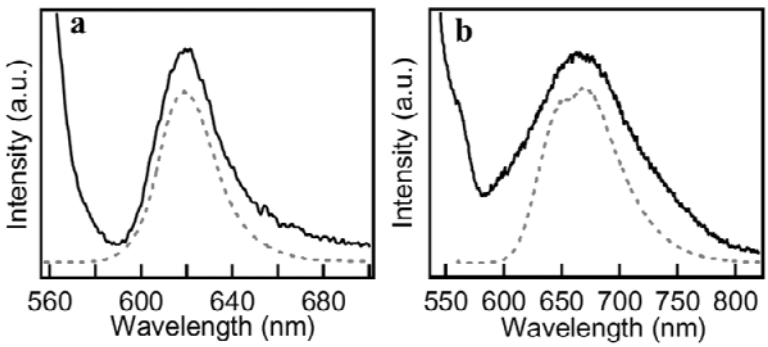


Fig. 11 Nanophotonics as excitation source. (a) Solid line is the emission spectrum recorded from CdSe QDs excited using a p-Si/n-CdS NW nanoLED; the QD emission maximum was 619 nm. The increasing intensity on the shorter wavelength side of the emission peak corresponds to the tail of the CdS nanoLED. Dashed line is the spectrum of pure CdSe QDs excited using an Ar-ion laser. (b) Solid line is the emission spectrum from propidium iodide excited using a p-Si/n-CdS NW nanoLED. Dashed line is emission spectrum of propidium iodide obtained in aqueous solution (Fluorolog, ISA/Jobin Yvon-Spex). Adapted from [31].

SUMMARY AND PERSPECTIVE

In this review, we have made a brief survey of work drawn primarily from the authors' thesis work. Overall, these examples illustrate a series of key advances that should ultimately enable nanoelectronics fabrication and manufacturing from the bottom-up. First, we have developed a general approach for the synthesis of NW building blocks with well-controlled chemical compositions, physical dimensions, and electronic properties. Second, we have developed rational methodologies to assemble NWs into integrated, increasingly complex arrays using electrical fields or micro-channel fluidics. Third, we have assembled a wide range of nanoscale electronic and optoelectronic devices and circuits from NW building blocks, which hold the promise of powering future electronic devices that can outperform existing devices and opening up totally new opportunities such as integrated, high-throughput, ultra-sensitive bioassays.

There is a very bright future for these electronically well-defined NW building blocks both in fundamental science and nanotechnologies. Specifically, we believe we have just started to explore the very edge of a broad range of opportunities, and that there remain many fascinating fundamental problems in these NW systems, such as the role of finite size and coherent states. Well-defined semiconductor NWs represent exciting systems to probe fundamental questions about localization or delocalization of electrical carriers and optical excitons in 1D. Further investigations will be not only critical to understanding fundamental issues in 1D systems, but also central to improved device characteristics

and possibly conceptually and fundamentally new types of devices such as single photon emitters and detectors, which could be critical for future quantum communication and computation. Continuing efforts will be required to develop even better control of NW synthesis and more and more sophisticated assembly approaches that can vary device functionality over multi-length scales. Lastly, developing new device concepts and integrated architectures will be increasingly essential as we move closer to ultra-high-density, integrated nanosystems.

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