Integrated Phased Array Systems in Silicon

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Invited Paper

Silicon offers a new set of possibilities and challenges for RF, microwave, and millimeter-wave applications. While the high cutoff frequencies of the SiGe heterojunction bipolar transistors and the ever-shrinking feature sizes of MOSFETs hold a lot of promise, new design techniques need to be devised to deal with the realities of these technologies, such as low breakdown voltages, lossy substrates, low-Q passives, long interconnect parasitics, and high-frequency coupling issues. As an example of complete system integration in silicon, this paper presents the first fully integrated 24-GHz eight-element phased array receiver in 0.18-μm silicon–germanium and the first fully integrated 24-GHz four-element phased array transmitter with integrated power amplifiers in 0.18-μm CMOS. The transmitter and receiver are capable of beam forming and can be used for communication, ranging, positioning, and sensing applications.

Keywords*—*Beam forming, CMOS, frequency generation, low-noise amplifiers (LNAs), phase shifting, phased arrays, power amplifier, radar, receivers, SiGe, silicon, transmitters, wireless communications.

I. INTRODUCTION

G. Moore's seminal 1965 paper [1] begins with the following prophetic passage:

> The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.
>
> Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.
>
> But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.
>
> Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Today—40 years later—we have witnessed the realization of these prophecies. Moore's law, predicting a doubling in the number of transistors on a single chip every 18 months, continues to apply. In many cases, we have access to more transistors than we are capable of using. The die area of most mixed-mode, high-speed, and/or RF ICs is not even limited by the active devices. Instead, passive components such as metal-to-metal capacitors, on-chip spiral inductors, and/or transmission lines are the primary area consumers in these ICs. Silicon-based technologies (e.g., CMOS and SiGe BiCMOS) continue to provide us with an ever-increasing number of transistors that in many cases render human creativity the primary bottleneck to further advancements.

The continued increase in the number and density of active devices is mainly fueled by scaling transistors' physical dimensions, thereby lowering the charge transit time and junction parasitic capacitances, which in turn results in an increase in the maximum usable frequency. Improved lithography techniques in conjunction with advancements in ion implantation and rapid thermal cycles have made it possible to define smaller lateral and vertical dimensions.

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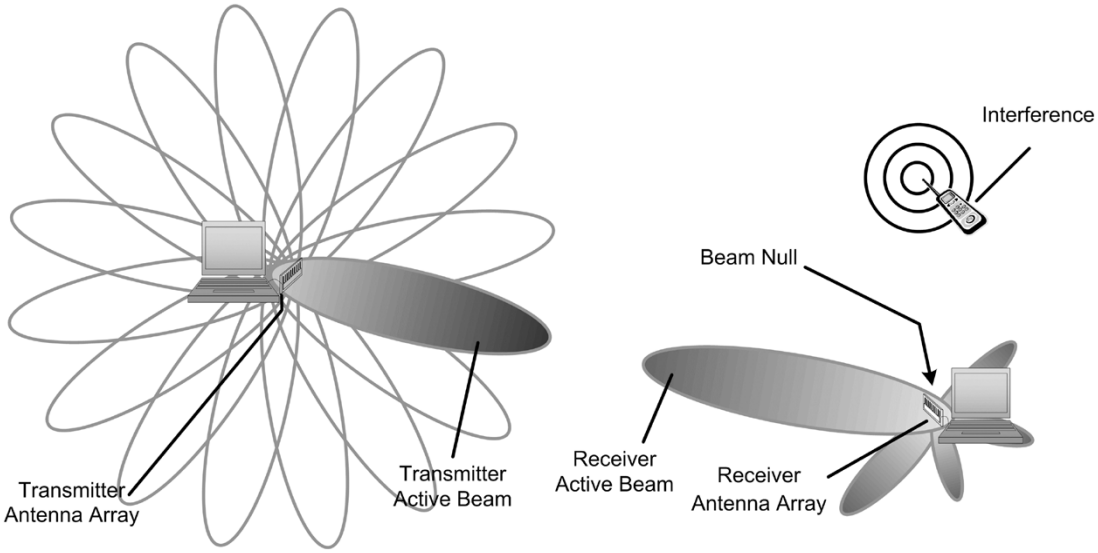

Fig. 1. Example of a phased array based communication link.

A reduction in the physical dimensions of the transistors must be accompanied by a proportional reduction in the width of the depletion regions inside the transistor to maintain its basic operation. This is achieved by an overall increase in the doping concentrations of the transistor. Unfortunately, the higher doping levels increase the electric field inside the transistor, reducing its breakdown voltages, thereby necessitating lower voltage swings and supply voltages [2]. The high substrate conductivity of silicon-based processes introduces additional inductive and capacitive energy loss mechanisms in passive components, such as inductor and transmission lines, that are extensively used in high-speed, RF, and microwave ICs.

While lower breakdown voltages and low-quality passive components may not be a major impediment for the core of digital processors and memory units, they pose major challenges for high-speed I/O as well as RF and microwave ICs. Incidentally, there has been tremendous growth in these areas in recent years, fueled by the prospects of wide-scale integration of analog, RF, and digital circuitry on the same substrate to eliminate the overhead of interface circuitry and lower the cost.

In MOSFETs, smaller dimensions result in shorter transit times and lower parasitic capacitances. Even in a velocity-saturated MOSFET, a reduction in the channel length improves the cutoff frequency by lowering the gate-source capacitance. This improvement will be eventually limited by the drain and source junction capacitors which scale sublinearly. Unfortunately, this scaling also reduces breakdown voltages.

It is desirable to improve the operation speed of transistors without an unnecessary reduction in the breakdown voltage and current handling capabilities. In bipolar transistors, one way to do this is by lowering the bandgap energy of the base region, by introducing germanium atoms in the base of a standard silicon bipolar junction transistor (BJT), thereby creating a heterojunction bipolar transistor (HBT). The lower bandgap in the base region increases the height of the potential barrier for the holes being injected back into the emitter (in an NPN transistor) improving the emitter injection efficiency γ of the transistor. The resulting higher emitter injection efficiency makes it possible to increase the doping level in the base region, lowering the physical base resistance. Additionally, the nonuniform doping profile in the base can be engineered to facilitate the charge diffusion from the emitter to the collector, thus reducing the base transit time. A higher base doping level results in a larger Early voltage V_A for the transistor and/or a reduction in the collector series resistance achieved by increasing the collector doping concentration. These modifications have made it possible to fabricate SiGe transistors with cutoff frequencies up to 200 GHz [3]–[5], which have breakdown voltages down to a few volts.

The practically unlimited number of high-frequency transistors with limited voltage and power handling capabilities necessitate a fresh look at the way we design circuits. System and circuit designers are just beginning to recognize the plethora of new possibilities that this new paradigm offers.

To deal with the limitations and opportunities of this new paradigm, it is necessary to adopt a design approach that allows for more integral co-design at the system, circuit, and device levels. In high-speed and microwave design, it seems almost inevitable that new design methodologies that take advantage of multiple signal paths, and distributed approaches will have to be applied more often [6]. One example of such multiple signal path approaches is phased array systems.

II. Integrated Phased Arrays

In the last paragraph of G. Moore's 1965 paper [1], he prophesied: "Even in the microwave area, structures included in the definition of integrated electronics will become increasingly important.…The successful realization of such items as phased array antennas, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar."

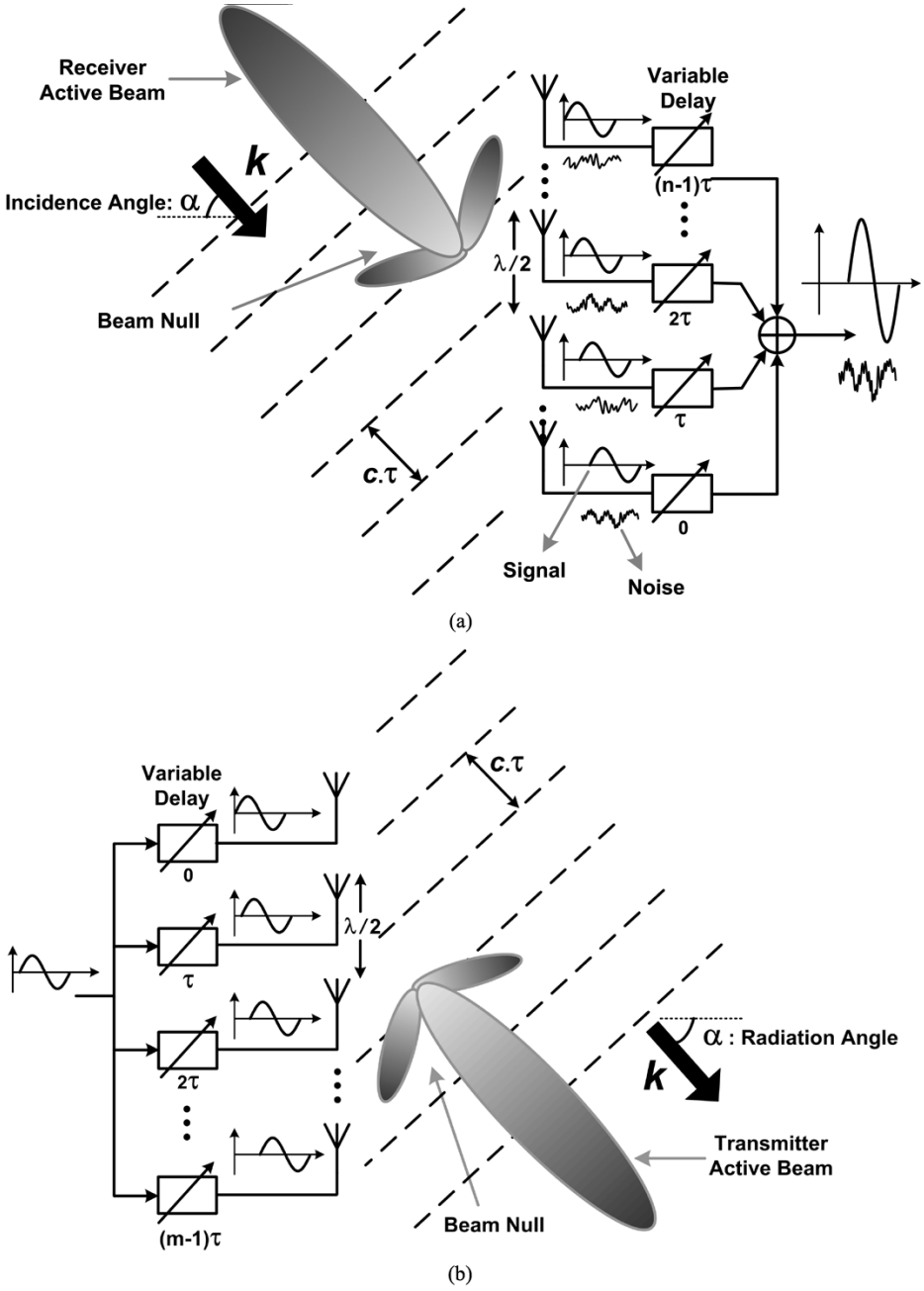

Fig. 2. Phased array transmitter and receiver. (a) Receiver improves SNR, rejects interferers. (b) Transmitter focuses radiated power.

Integration of a complete phased array system in silicon results in substantial improvements in cost, size, and reliability. At the same time, it provides numerous opportunities to perform on-chip signal processing and conditioning, without having to go off-chip, leading to additional savings in cost and power. The multiple signal paths, operating in harmony, on both the transmitter and receiver side provide benefits at the system and circuit level. The use of such phased arrays is not restricted to traditional areas such as radar alone. For example, high-frequency integrated phased array based systems will make gigabit-per-second directional point-to-point communication networks feasible. At the circuit level, the division of the signal into multiple parallel paths relaxes the signal handling requirements of individual transistors.

Higher frequencies offer more bandwidth, while reducing the required antenna size and spacing. The ISM band available at 24–24.25 GHz can be used for wireless point-top-point communications. Additionally, the 24-GHz frequency has become more attractive recently due to a 2002 FCC ruling that has opened the 22–29-GHz band for automotive radar systems, such as autonomous cruise control (ACC) [7].

In this paper, we demonstrate a complete 24-GHz phased array system, with the first fully integrated SiGe-based eight-element phased array receiver [8] and 0.18-μm CMOS four-element phased array transmitter [9], as a successful implementation of an entire microwave system in silicon. Such phased array systems can be used for high-speed

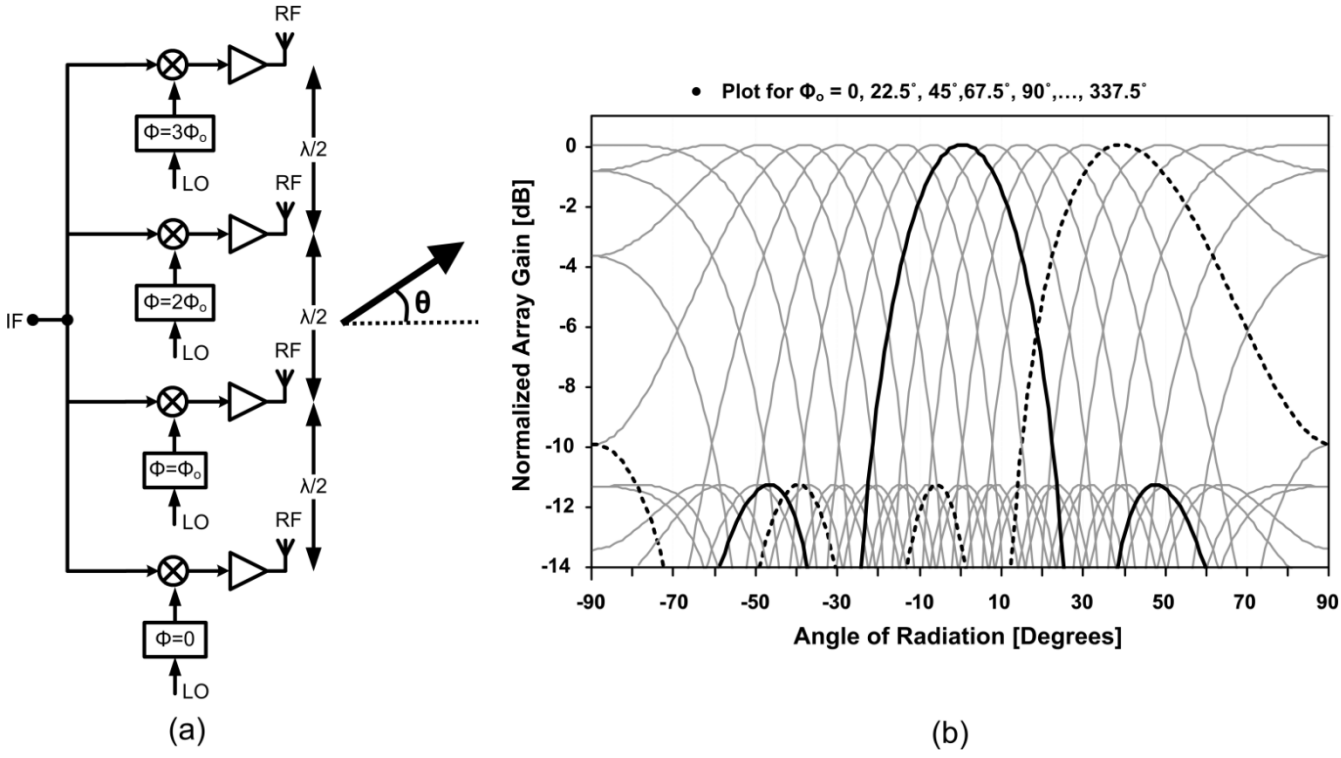

Fig. 3. Array pattern for four-element phased array with LO-path phase shift. (a) A simplified LO-path phase-shifting transmitter. (b) Four-element array pattern with 4-b phase-shifting resolution.

directional communications, as well as for ranging and sensing applications, e.g., radar. This silicon-based phased array system realizes Moore's last unfulfilled prophecy almost 40 years later.

III. System Architecture

Multiple antenna phased arrays can be used to imitate a directional antenna whose bearing can be controlled electronically [10]–[16]. This electronic steering makes it possible to emulate antenna properties such as gain and directionality, while eliminating the need for continuous mechanical reorientation of the actual antennas (Fig. 1). Additionally, the parallel nature of a phased array antenna transceiver alleviates the power handling and noise requirements for individual active devices used in the array. This makes the system more robust to the failure of individual components. In the past, such systems have been implemented using a large number of microwave modules, adding to their cost and manufacturing complexity [14], [15].

A phased array transmitter or receiver consists of several signal paths each connected to a separate antenna. The antenna elements of the array can be arranged in different spatial configurations [12]. The array can be formed in one, two, or even three dimensions, with one- or two-dimensional arrays being more common.

The principle of operation of a phased array is similar for a receiver or a transmitter. In a phased array receiver, the radiated signal arrives at different times at each of the spatially separated antennas. The difference in the time of arrival of the signal at different antennas depends upon the angle of incidence and the spacing between the antennas. As shown in Fig. 2(a), an ideal phased array receiver compensates for the time delay difference between the signals from different antennas and combines the signals coherently to enhance the reception from the desired direction(s), while rejecting emissions from other directions. Similarly, in a phased array transmitter, the signals in different elements are delayed by different amounts so that the signals add up coherently only in the desired direction(s). Incoherent addition of the signal in other directions results in lower radiated power in those directions [Fig. 2(b)].

Thus, in a phased array based system, the transmitter generates less interference at receivers that are not targeted, and the receiver is also capable of nulling out interferers as long as they do not originate from the same direction as the signal. Additionally, for a given power level at the receiver, the power that has to be generated is lower in a phased array transmitter than in an isotropic transmitter. In a transmitter with m elements, if each element radiates P watts, the total power that will be seen at the receiver in the desired direction is m^2P watts. The m^2 improvement comes from the coherent addition of the electromagnetic fields in the desired direction. In the case of our four-element transmitter, the total power radiated in the beam direction is 12 dB higher than the power radiated by each element.

At the receivers, the advantages of a phased array include better sensitivity and higher interference rejection capabilities. For a given receiver sensitivity, the output SNR sets an upper limit on the noise figure of the receiver. The noise figure NF is defined as the ratio of the total output noise power to the output noise power caused only by the source

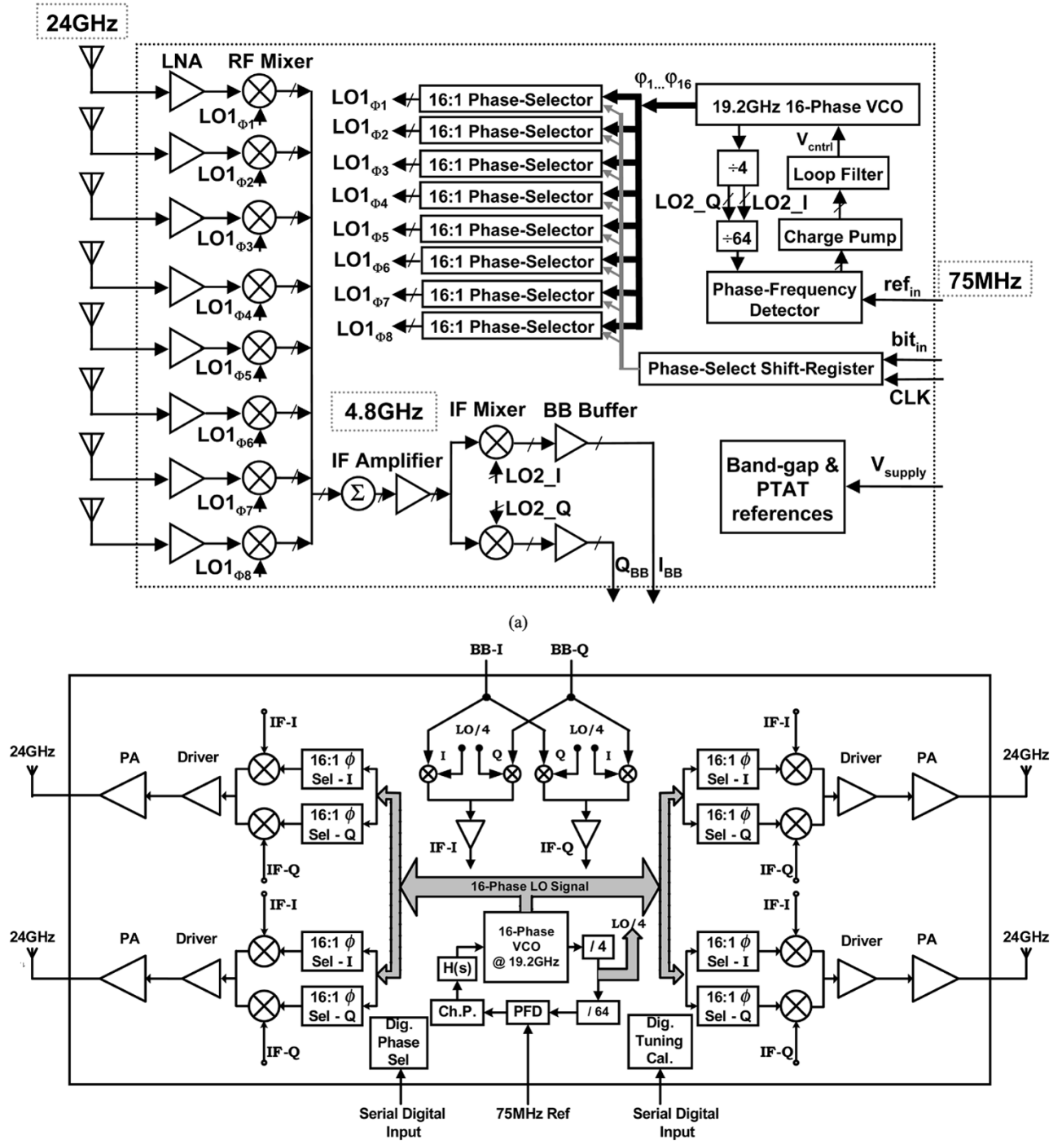

Fig. 4. Transmitter and receiver architectures. (a) Eight-element phased array receiver. (b) Four-element phased array transmitter.

[17]. Consider the n-path phased array receiver shown in Fig. 2(a). Since the input signals add coherently, the combined output is given by

$$S_{\text{out}} = n^2 G_1 G_2 S_{\text{in}}$$

where n is the number of elements and G_1 and G_2 correspond to the gains before and after signal combining. The antenna's noise temperature is primarily determined by the temperature of the object(s) it is pointed at. In general, the amount of SNR improvement in a phased array receiver depends on the nature and location of the objects in the environment that generate noise, correlation between such noise generators, multipath effects, coupling between antenna elements, input impedance mismatch, angle of incidence, and the antenna beam pattern. Assuming that the antenna noise contributions in different elements are uncorrelated, the output total noise power is given by

$$N_{\text{out}} = n(N_{\text{in}} + N_1)G_1 G_2 + N_2 G_2$$

where N_1 and N_2 are the input-referred noise contributions of the stages corresponding to gains G_1 and G_2, and N_{in} is the noise at the input of each antenna. Thus, compared to the output SNR of a single-path receiver, the output SNR of the array can be improved by up to a factor of n depending on the noise and gain contribution of different stages. The array noise factor can be expressed as

$$F = \frac{n(N_{\text{in}} + N_1)G_1G_2 + N_2G_2}{nN_{\text{in}}G_1G_2} = n\frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}}$$

which shows that the SNR at the phased array output can be even smaller than the SNR at the input if $n > F$. For a given NF, an n-element receiver can improve the sensitivity by $10\log(n)$ in decibels compared to a single-path receiver. For instance, if the noise from the antennas is uncorrelated, an eight-path phased array can improve the receiver sensitivity by 9 dB.

Thus, in a system based on phased arrays at the transmitter and receiver, the higher SNR and lower interference increases channel capacity. Furthermore, the directivity of the transmit–receive pairs can result in higher frequency reuse ratios, leading to higher network capacity.

For narrow-band systems, the true-time delay necessary in each element of a phased array can be approximated by a phase shift. This approximation leads to some signal dispersion, due to the nonconstant group delay, which increases as the bandwidth of the signal increases. This dispersion translates to a higher bit error rate (BER) in communication systems and lower resolution in radar systems [18]. However, for the bandwidths of interest in this work ($\sim$ 250 MHz @ 24 GHz), this error is not significant [19].

The phase shift necessary in each element of a phased array can be achieved at RF, at baseband/IF, or in the LO path. In this work, LO path phase shifting is adopted as the gain in each element of the transmitter or receiver is less sensitive to the amplitude variations at the LO ports of the mixers [19]. Phase shifting and signal processing at baseband (i.e., digital arrays) was not chosen due to the much larger chip area, power consumption, and the high demands placed upon the baseband digital interface, particularly for the high data-rates of interest. Also, RF phase shifters at 24-GHz RF will have a relatively high loss due to the passive components (especially inductors and varactors) and their limited self-resonance frequency. Additionally, the phase shifter's loss usually changes significantly with its phase shift, and that necessitates the use of RF variable-gain amplifiers with fine resolution to make the gain in different elements uniform [20]. In a receiver, the loss in the signal path phase shifters is particularly significant, as it degrades the receiver's overall sensitivity. Therefore, this loss will have to be compensated by providing additional gain at the low-noise amplifier (LNA) preceding the phase shifters. This additional gain comes at the cost of linearity for the same power consumption.

In comparison, the loss in the LO phase-shifting networks can be easily compensated by high-gain amplifiers (e.g., limiters) without signal-path linearity degradation and/or the need for any amplitude tuning. The reason for this is that many RF mixer implementations (e.g., Gilbert type) perform better when driven to switch with a large amplitude at the LO port, making their gain less sensitive to the LO amplitude. Moreover, multiple phases of an LO signal can be generated using methods different from those using phase shifters.

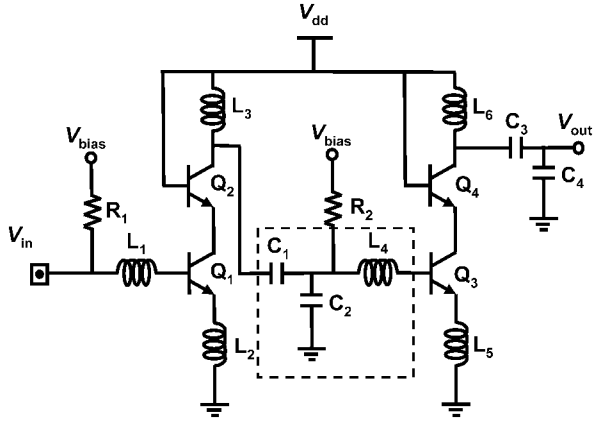

Fig. 5. 24-GHz LNA.

For the reasons detailed above, the implemented phased array system uses a LO phase-shifting architecture for beam forming. In both the transmitter and receiver chips, an oscillator core generates 16 discrete phases providing four bits (22.5°) of raw phase resolution. Phase selectors in each element apply the appropriate phase of the LO to the RF mixers to achieve desired beam direction. A simplified four-element transmitter with LO path phase shifting is shown in Fig. 3(a). As shown in the figure, the relative phase shifts in each element are multiples of ϕ_0. Fig. 3(b) shows the simulated array pattern for 16 values of ϕ_0 with a step size of 22.5° (4-b resolution), assuming omnidirectional antenna elements with a spacing of $\lambda/2$. The simulations indicate that the system is capable of steering the beam from $-90°$ to $+90°$ with a steering step size of 7.2° at the broadside. From the array pattern, it can also be seen that this LO phase shift resolution is sufficient to ensure close to peak array gain at all angles of radiation.

Fig. 4 shows the architecture of the 24-GHz eight-element phased array receiver [8] and the four-element phased array transmitter [9]. A two-step heterodyne architecture was used in the receiver and transmitter with LO frequencies of 4.8 and 19.2 GHz, allowing both LO frequencies to be generated using a single synthesizer loop and a divide-by-four. The operating state of each chip, which includes the phase-selection information (beam-steering angle) for programming the phase selectors in each element, is serially loaded into on-chip shift registers using a standard digital serial interface.

In the receiver, each of the eight RF front ends consists of two inductively degenerated common-emitter LNA stages in cascade followed by a double-balanced Gilbert-type mixer. The input of the first LNA is matched to 50 Ω, and the subsequent blocks of the front end are power matched for maximum power transfer. The outputs of all eight mixers are

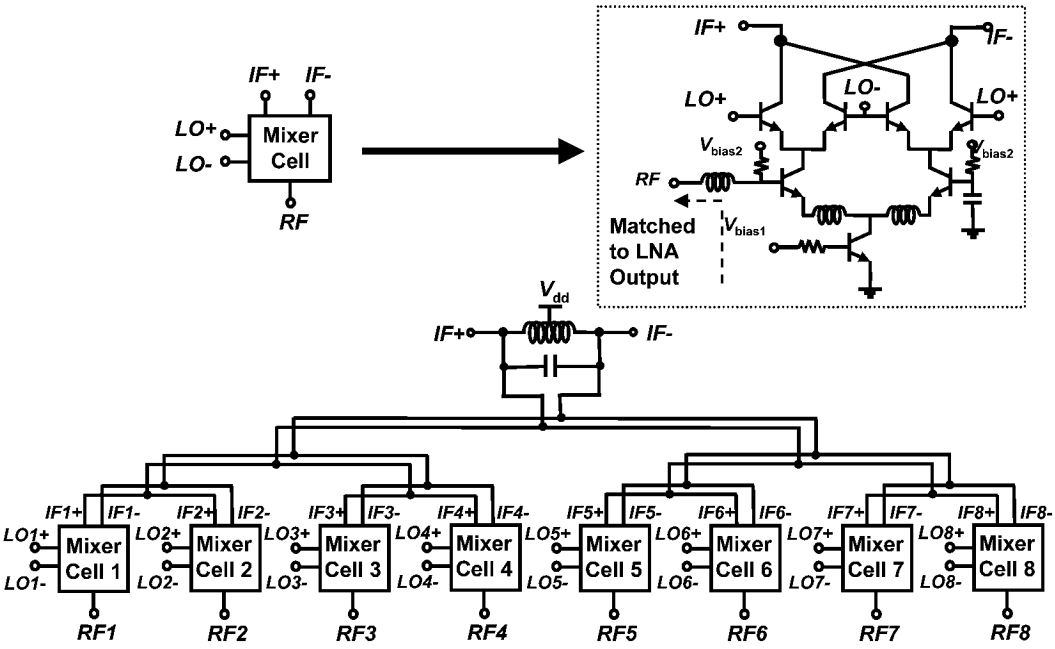

Fig. 6. RF mixers and IF combining network.

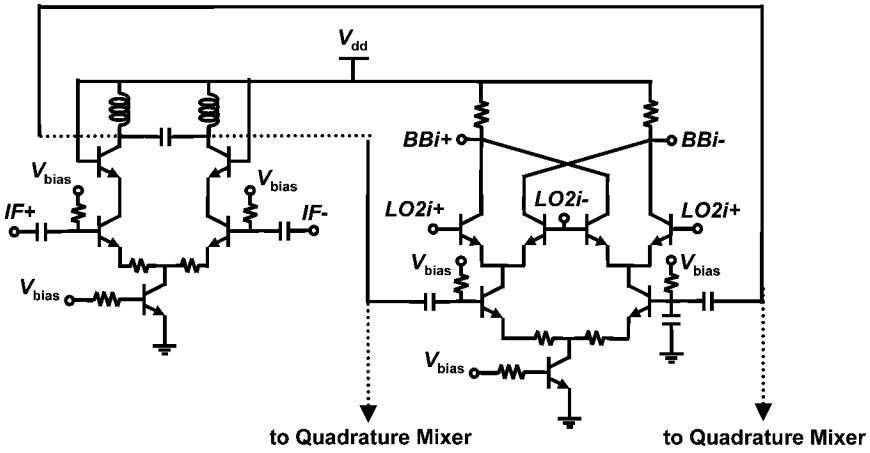

Fig. 7. IF amplifier and mixer.

combined in the current domain and terminated to a tuned load at the IF. The combined signal is further amplified by an IF amplifier and downconverted to baseband by a pair of double-balanced Gilbert-type mixers, driven by I and Q signals generated by the divide-by-four block. Two baseband differential buffers drive the I and Q outputs. On-chip PTAT and bandgap references generate the bias currents and voltages, respectively.

In the transmitter, quadrature upconversion is chosen for both upconversion steps to attenuate the image signal. The input baseband I and Q signals are upconverted to 4.8 GHz by a pair of quadrature double-balanced Gilbert-type mixers. The 4.8-GHz I and Q signals are buffered and fed to the 4.8-GHz-to-24-GHz upconversion mixers in each element. The 19.2-GHz LO I and Q signals for the 24-GHz upconversion mixers in each element are provided by the phase selectors in that element. The output of the mixers is amplified and provided to the on-chip power amplifiers. Digital tuning controls present on-chip ensure that the right center frequency is achieved for critical high-frequency blocks. The 50-Ω matching at the output of the power amplifier (PA) takes wirebond parasitic effects into account; therefore, the PAs can drive off-chip antennas fabricated on a printed circuit board (PCB).

IV. Circuits Implementation

In this section, we discuss the details of the various building blocks in the 24-GHz phased array system. We first discuss circuits that are particular to the receiver and the transmitter. We then describe the LO path circuits that are common to the transmitter and the receiver.

A. Receiver

1) LNA: The LNA is the most critical block in the receive chain in terms of sensitivity. It needs to have a low noise

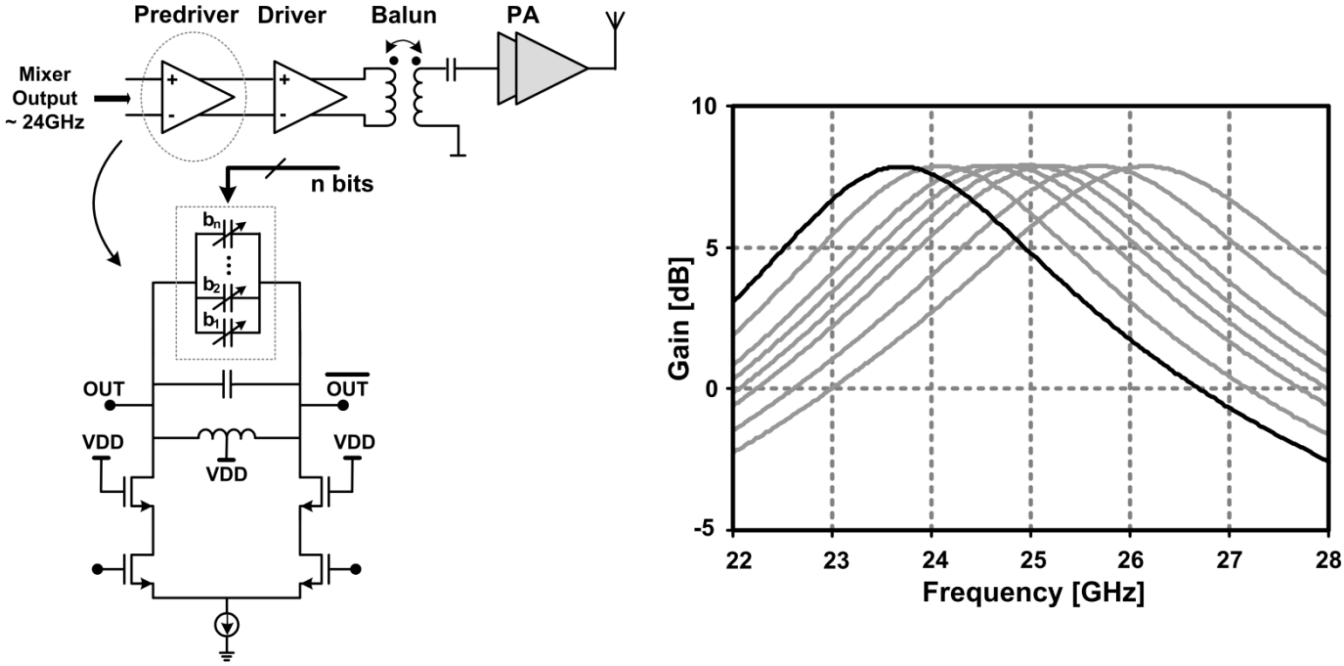

Fig. 8. Center-frequency calibration in high-frequency stages.

factor, a well-defined real input impedance (typically 50 Ω), and sufficient gain to suppress the noise of the subsequent mixer. The LNA used in a phased array system requires a particularly low power design, since multiple identical LNAs are operating concurrently in the system.

Recent advances in the silicon CMOS and SiGe BiCMOS processes have extended the operation range of silicon-based integrated LNAs from the low gigahertz range to much higher frequency bands [21]–[24]. The inductively degenerated common-emitter topology for the LNA can provide a high gain and low noise simultaneously for a small ω_o/ω_t [22]. The process used in this work provides SiGe HBT with cutoff frequency of 120 GHz [25]; therefore, inductively degenerated common-emitter topology is adopted, as shown in Fig. 5.

The input transistor size and dc current are chosen to obtain power and noise matching simultaneously by following the steps described in [26]. After the current density associated with minimum noise figure is determined from simulations, the input transistor is scaled until the optimum input impedance for low noise has a 50-Ω real part. This optimization results in a dc current of 4 mA and an emitter degeneration inductance of 0.2 nH. The cascode transistor Q_2 is used to improve reverse isolation.

The available gain of a single stage at 24 GHz is limited by the small load inductance due to the large collector capacitance of Q_2 and the load capacitance, so an identical second stage is added. A capacitive divider formed by C_1 and C_2 transforms the output impedance of the first stage to 50 Ω, which is also the optimum impedance for the second stage in terms of power and noise. The matching network loss at 24 GHz is simulated to be lower than 0.25 dB.

At 24 GHz, the bond wire inductance has a considerable effect on the input reflection coefficient of the LNA. The LNA is designed to be well matched to 50 Ω (S_{11} less than −10 dB) on chip and can tolerate bond wire inductances up to 0.3 nH. The supply and ground lines of the LNA are bypassed on chip with an MIM capacitor resonating at 24 GHz. All the inductors used in this LNA are between 0.2 and 0.5 nH. To save silicon area, spiral inductors are used. All the spirals and interconnections are modeled by electromagnetic simulations using IE3D [27].

2) Mixer and IF Combining Network: Gilbert-type double-balanced multipliers are used to downconvert the single-ended 24-GHz RF signal to a differential signal at 4.8-GHz IF, as shown in Fig. 6. The input of the mixer is conjugate matched to the LNA output through an impedance transforming network. Inductive emitter degeneration is used to improve mixer linearity. A dc bias current of 1.25 mA is chosen for each mixing cell, which is a reasonable tradeoff between power dissipation, linearity, and noise figure. Each mixing cell has a conversion transconductance of 6.5 mS. The downconverted IF signal is subsequently combined in current domain through a symmetric binary tree and terminated to a tuned load at 4.8 GHz.

3) IF Amplifier and Mixers: The IF amplifier is the first circuit block after signal combining. It was shown earlier that the noise contribution of such blocks in the overall noise figure is not only suppressed by the single-path gain of the front-end, but also by an array gain of n. At this point, the interference arriving at the input of the IF amplifier is already attenuated by the spatial selectivity of the array pattern. Therefore, both noise and linearity requirements of the IF amplifier and subsequent blocks are relaxed as a direct advantage of the phased array. Fig. 7 shows the schematics of the IF amplifier and I and Q mixers. The IF amplifier and mixer consume 1.6 and 2.3 mA of dc current, respectively.

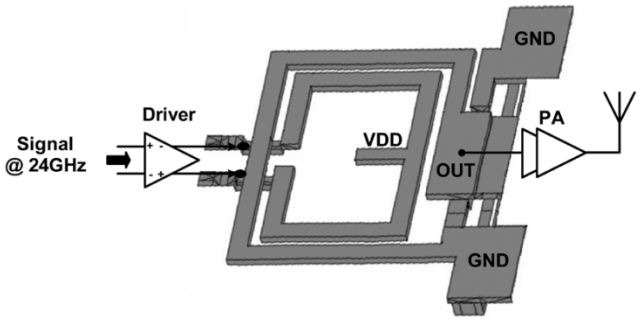

Fig. 9. Differential to single-ended conversion at PA input.

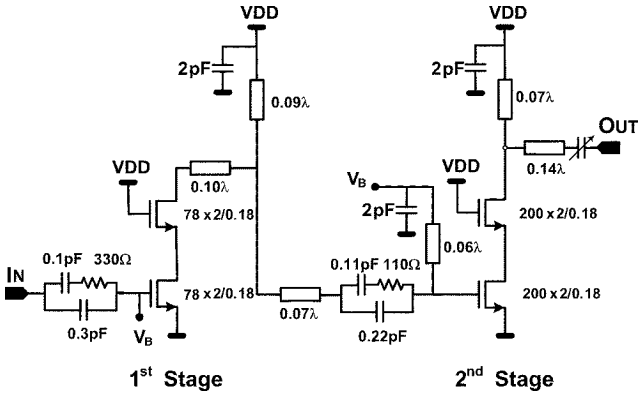

Fig. 10. 24-GHz CMOS power amplifier.

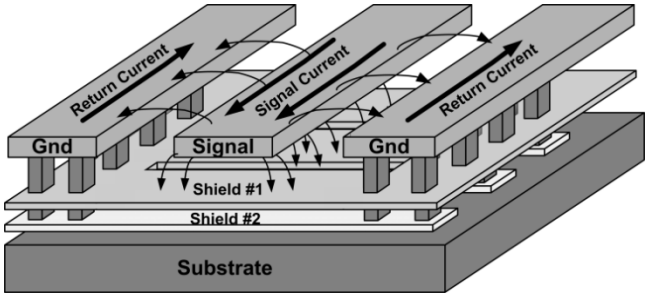

Fig. 11. Substrate-shielded coplanar waveguide structure.

B. Transmitter

1) IF and RF Upconversion Mixers: The baseband-to-4.8-GHz mixers common to all elements and the 4.8-GHz-to-24-GHz upconversion mixers in each element are Gilbert-type upconversion mixers using 0.18-μm CMOS transistors. The first upconversion mixer consumes 3.8 mA of dc current while the buffers following this consume 4.3 mA. The output of these buffers is distributed to the quadrature upconversion mixers in each element, which consume 10 mA each. The distribution of the signal is done using a symmetric H-tree structure to ensure good array performance.

2) Tunable Passive Loads at 24 GHz: There are a cascade of tuned stages in the RF path in each element. This exacerbates any off-tuning in the passive loads. To avoid the problem of gain loss due to off-tuning, switchable capacitors, controlled by programmable shift registers, were implemented at the output of some of the high-frequency stages (Fig. 8). In the predriver stage, for example, these capacitors allow the center frequency to be tuned from 23.7 to 26.3 GHz, which is sufficient to account for process variations and errors in simulation of passives.

3) PA: All the circuits up to and including the 24-GHz PA driver are differential while the PA was designed to be single ended. To avoid power and efficiency loss in the PA, a balanced–unbalanced converter (balun) was placed before the PA. This eliminates the need for an off-chip balun or a differential antenna. As shown in Fig. 9, the balun was realized with a single-turn transformer to minimize substrate loss through capacitive coupling. Electromagnetic simulations show an insertion loss of 1.5 dB for the balun when input and output parasitic inductances are tuned out with parallel capacitors.

The CMOS PA, shown in Fig. 10, consists of two gain stages [28]. Each gain stage is composed of a cascode transistor pair to ensure stability and increase breakdown voltage. To minimize the effect of gate series resistance, which can be the limiting factor for $f_{\max}$, the finger width of transistors was chosen to be 2 μm with gate contacts at both ends. All matching networks in the PA are realized with substrate-shielded coplanar waveguide structure to reduce losses [28], [29]. As shown in Fig. 11, this structure, while similar to a standard coplanar waveguide, has higher capacitance per unit length than a coplanar waveguide due to the patterned ground shield beneath the signal line. The inductance per unit length is not affected, since the return current is still forced through the coplanar ground lines as the ground shield below is patterned. As can be seen in Fig. 11, a second shield layer is placed beneath the first shield layer, with metal stripes covering the slots of the first layer, thereby completely isolating the coplanar structure from the lossy substrate. Due to the higher capacitance per unit length, this structure has a lower wave velocity and therefore shorter wavelength at 24 GHz. In the structure implemented, the wavelength is reduced by more than a factor of two when compared to a standard coplanar or microstrip transmission line on silicon dioxide. The wide signal lines in the waveguide structure result in low loss per unit length (0.9 dB/mm). This combination of short transmission lines in the matching network and the low loss per unit length, results in lower total loss in the matching networks.

A series *RC* network in the interstage matching network ensures stability of the amplifier at low frequencies. At high frequencies, the capacitor in parallel with the series *RC* network has low impedance and provides the propagation path for RF signal. However, it presents a high impedance at low frequencies, forcing the low-frequency signal through the lossy series *RC* network. This decreases the gain of the amplifier at low frequencies and makes it stable.

The matching network in the output stage is designed to convert the 50-Ω antenna impedance to the proper impedance at the drain of the transistor, maximizing output power and efficiency. The optimum impedance is chosen by load pull simulations of the cascode pair while the gate of the input transistor is driven by a large-signal source. In the matching network, a series transmission line lowers the

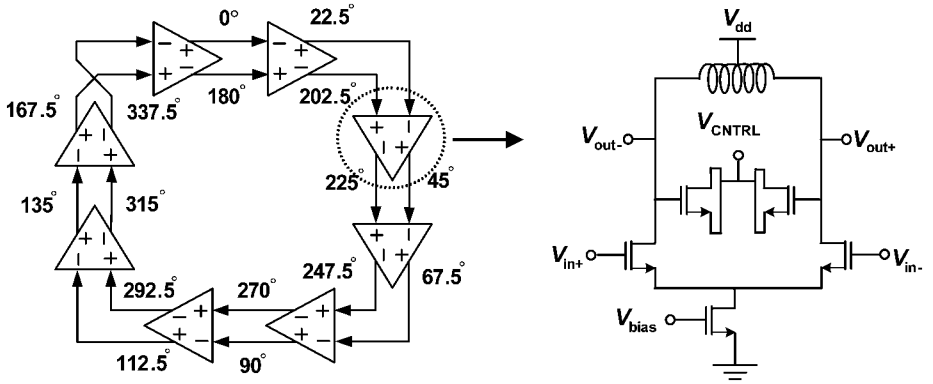

Fig. 12. 16-phase 19.2-GHz CMOS VCO.

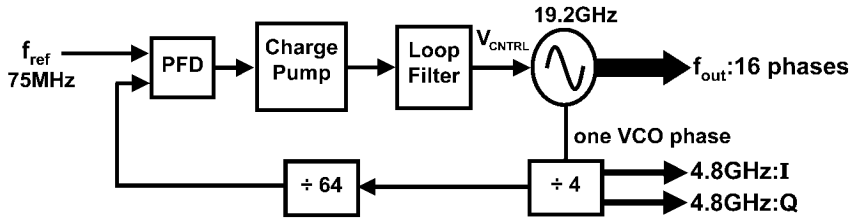

Fig. 13. On-chip PLL architecture.

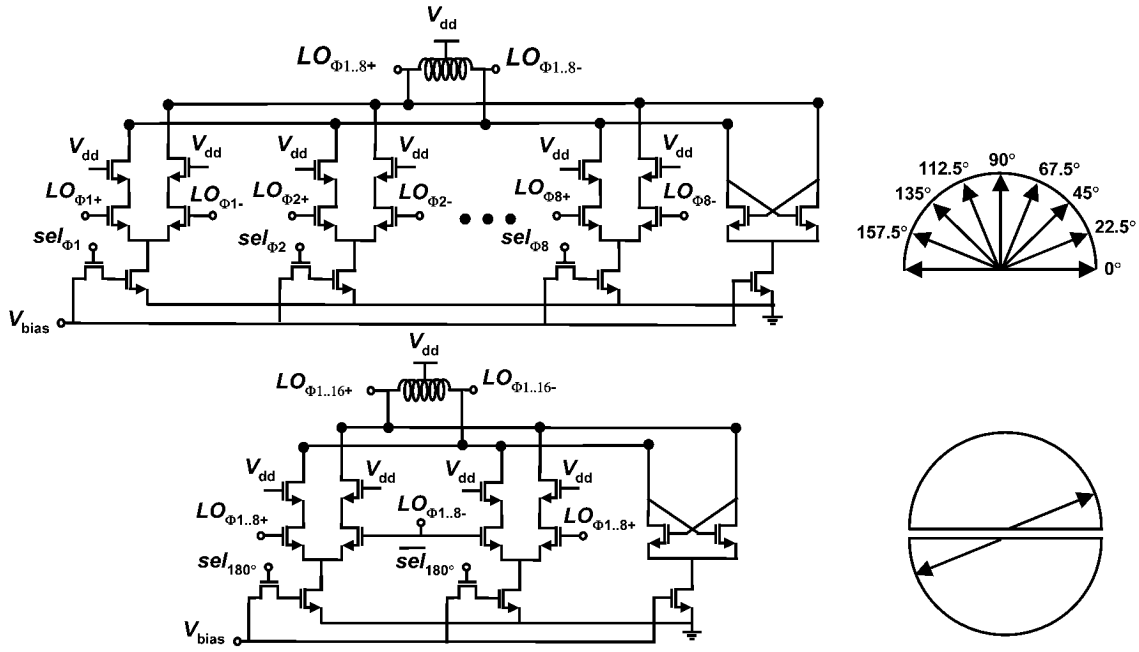

Fig. 14. Schematic of phase selectors.

50-Ω antenna impedance for a higher output power while a parallel transmission line acts as a shorted-stub inductor to resonate drain-substrate capacitance of transistor. Interstage matching networks are designed based on the same principle.

C. LO Path Circuitry

The LO path circuits are similar on the transmitter and receiver chips. In both chips, a 16-phase VCO with a center frequency of 19 GHz is used to generate the LO. The VCO is designed as a ring of eight differential CMOS amplifiers with tuned loads, as shown in Fig. 12 [30]. If no inductors are used at the amplifier outputs (e.g., differential pair with resistive load, or CMOS inverters), each amplifier will have to operate at a gain-bandwidth product close to the unity-gain frequency of transistors in the process and the reliability could be compromised [19]. However, inductors can be used to generate the necessary phase shift for each amplifier, where each stage is tuned almost at the oscillation frequency. Each of the designed amplifier stages draws less than 3.2 mA from a 2.5-V supply, resulting in a total power consumption of 63 mW for the oscillator.

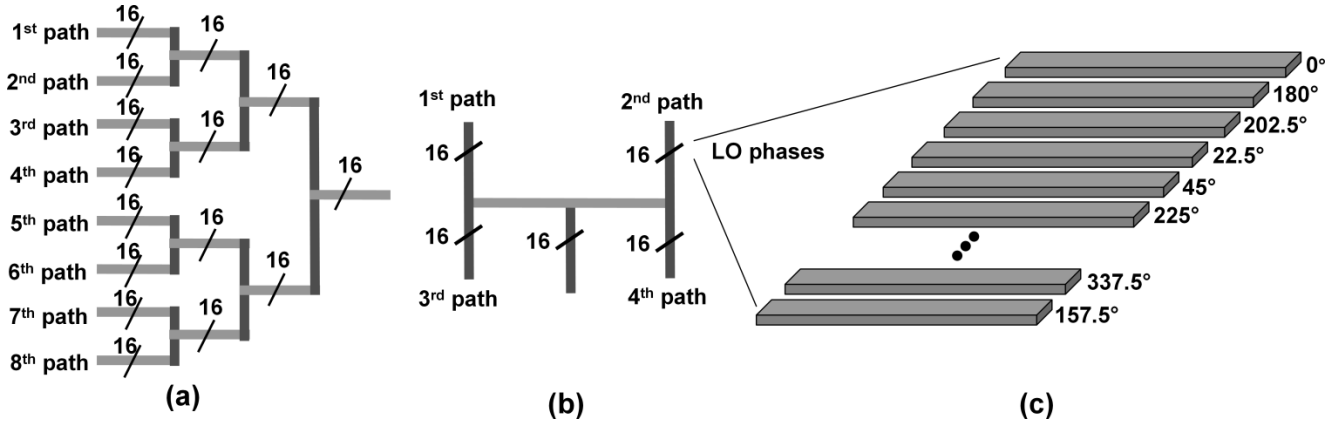

Fig. 15. Distribution of LO phases. (a) Binary-tree structure for symmetric distribution in receiver. (b) H-tree structure for symmetric distribution in transmitter. (c) Ordering of LO phases in distribution structure.

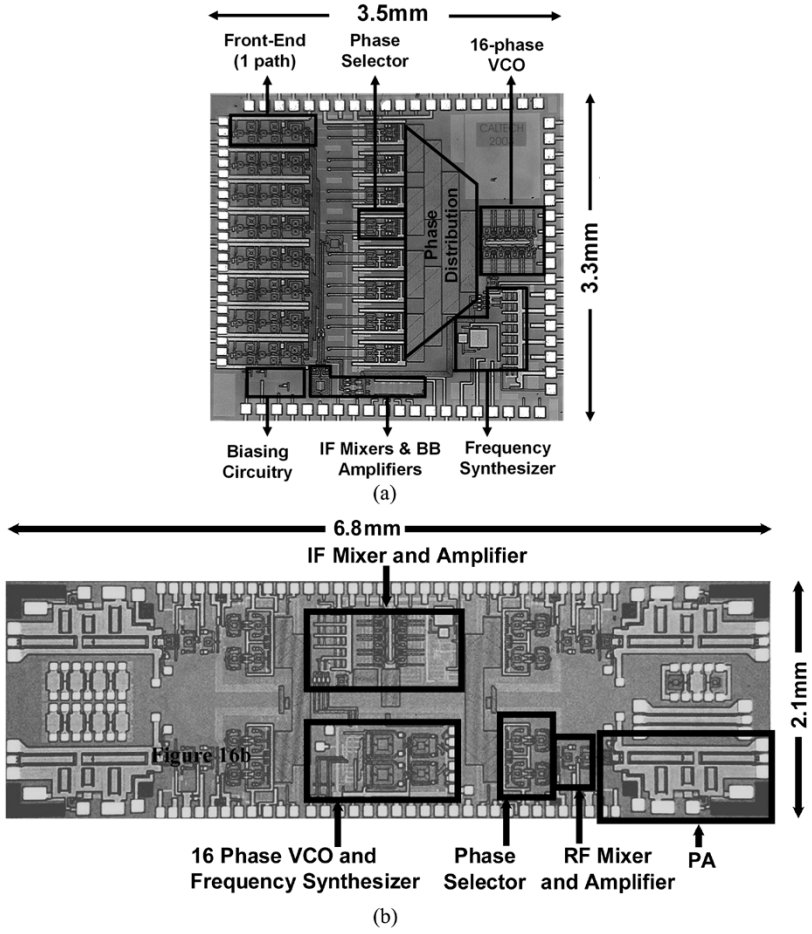

Fig. 16. Die micrograph. (a) Eight-element receiver. (b) Four-element transmitter.

The center frequency can be tuned by changing the control voltage of differential MOS varactors. In order to make the high-frequency oscillator insensitive to loading, all the eight differential outputs are buffered prior to connection to other circuit blocks. Emitter followers and differential pairs draw about 1 and 1.9 mA, respectively, from a 2.5-V supply. This results in about 9.8 mW of power consumption for each buffer.

The center frequency of the 19-GHz VCO is locked to a 75-MHz external reference signal source by an on-chip third-order frequency synthesizer phase-locked loop (PLL) with a loop bandwidth of 7 MHz (Fig. 13). The integrated synthesizer uses a standard tristate frequency phase detector and a multiswitch charge pump [31] to minimize the reference feed-through. All divide-by-two blocks use a master–slave architecture and emitter-coupled logic for high-speed operation.

In the transmitter and receiver chips, the 16 phases generated at the VCO core are distributed to local phase selectors in each element. This distribution is done in a

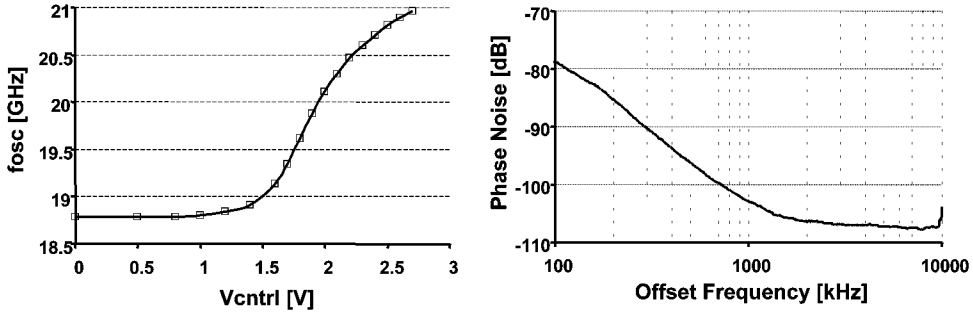

Fig. 17. VCO performance. (a) VCO frequency versus control voltage. (b) VCO phase noise (free running).

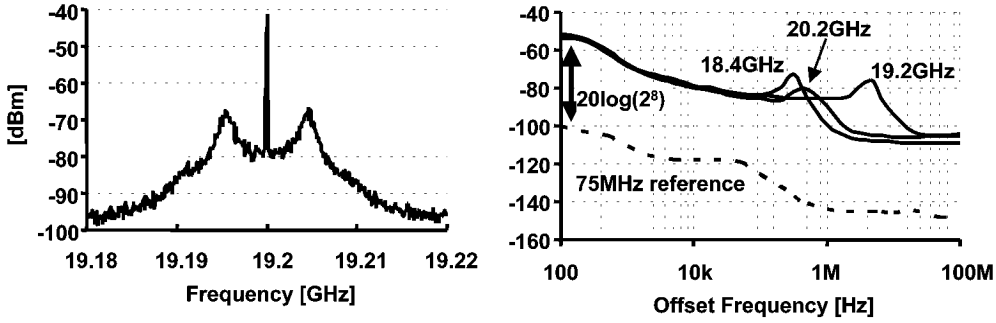

Fig. 18. Synthesizer output spectrum and phase noise.

symmetric fashion through binary trees and H-tree-based distribution networks, ensuring that each element has independent access to all 16 phases of the LO [19]. The phase selectors are equivalent to analog multiplexers, and the LO phase selection in each element is controlled independent of the phase of the other elements. The phase-selection data is serially loaded to an on-chip shift register using a digital serial interface. The LO phase selection for each element is done in two steps, as shown in Fig. 14. Initially, an array of eight differential pairs with switchable current sources and a shared tuned load selects one of the eight LO differential phase pairs. This topology accommodates phase interpolation using the appropriate digital control word. When two (or more) phase branches are selected by turning on the tail current sources associated with those phases, the current addition at the output results in interpolation between the two (or more) selected phases. By first-order interpolation between two adjacent phases, 32 equally spaced phases (5-b resolution) can be generated. A dummy array with complementary switching signals maintains a constant load on the VCO buffers and prevents variations in phase while switching. Next, the polarity (the sign bit) of the LO is selected by a similar two-to-one phase selector that is driven by the output of the first phase selector stage. The second phase-selection stage also provides additional gain to compensate the loss of the distribution network. Notably, the phase selector stages are designed to provide high gain in order to restore the amplitude of the LO signal, which is attenuated because of the loss of the distribution network and mismatch between components. Each 16 : 1 phase selector draws 12 mA. More details on the design of the multiple phase generation, distribution network, frequency synthesizer circuits, and their effects on array performance can be found in [19].

Table 1
LO Path Performance

LO Path Performance	
Synthesizer Locking Range	2GHz
Synthesizer Bandwidth	7MHz
Synthesizer Settling Time	< 50μs
VCO Phase Noise 18.7 GHz	-103dBc/Hz @ 1MHz offset
Power Consumption	180mA

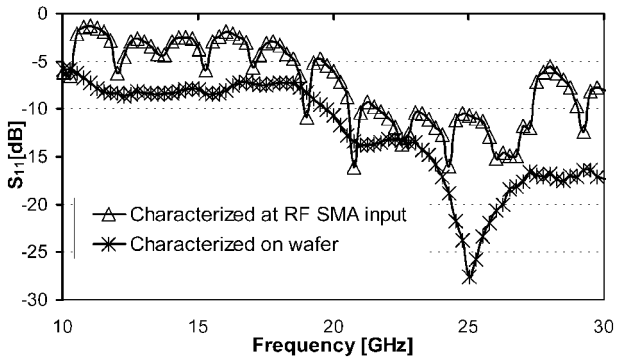

Fig. 19. Input matching at LNA.

There may be amplitude and phase variations in each path. These variations are because of the mutual coupling and the small mismatches in delivering the LO phases to different receiver paths. For example, based on electromagnetic simulations, the wavelength of a 19-GHz signal in a typical microstrip line in the silicon technology used

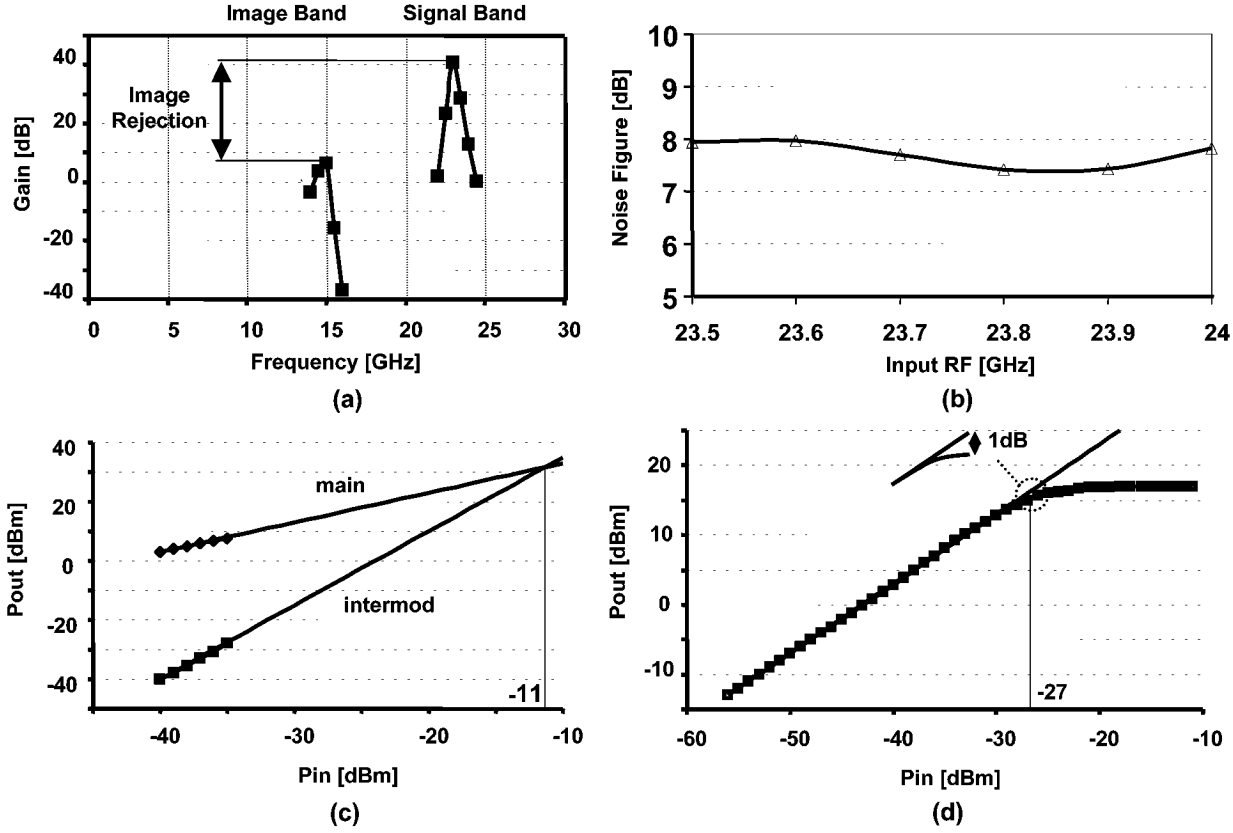

Fig. 20. Single-element receiver performance. (a) Single-element gain versus frequency. (b) Noise figure. (c) Two-tone test. (d) 1-dB gain compression test.

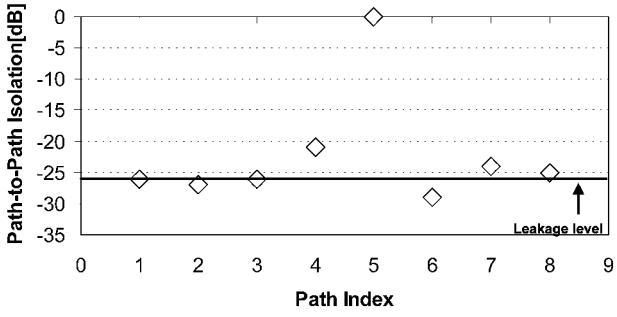

Fig. 21. On-chip path-to-path isolation in receiver.

is about 7.8 mm, and hence a length difference of 40 μm corresponds to a phase difference of 1.8°. The phase and amplitude mismatches among various paths deteriorate the side-lobe attenuation or equivalently degrade the ability of the phased array to reject interfering signals.

Fig. 15(a) and (b) shows the symmetric tree and H structures used in receiver and transmitter to transfer all 16 phases of the local oscillator signals to the phase-selection circuitry of each path with minimal mismatch between the paths. Fig. 15(c) shows the ordering of the phases in the LO phase distribution network. It was determined that this ordering minimizes the coupling induced mismatch [19]. In order to reduce the loss, the top two metal layers in the process were used for distributing multiple LO phases. The spacing between lines in the phase distribution structure is 5 μm.

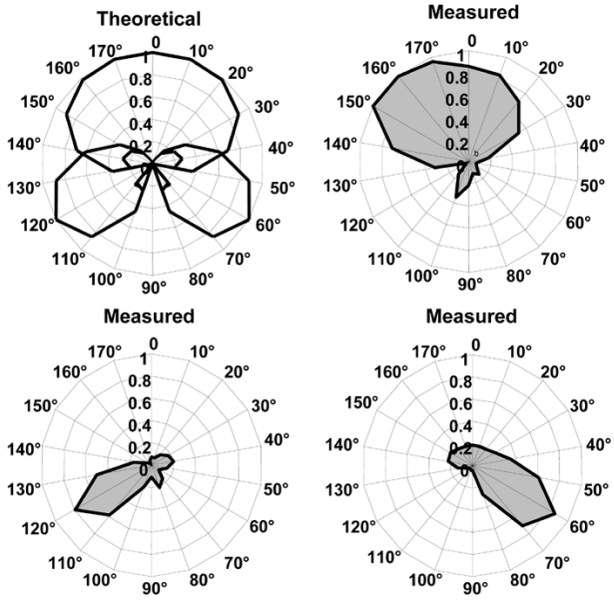

Fig. 22. Measured receiver array pattern with four-elements active.

V. Experimental Results

The phased array system is implemented in IBM 7HP SiGe BiCMOS technology with a bipolar f_T of 120 GHz and 0.18-μm CMOS transistors with an f_T of 65 GHz [25]. It offers five metal layers with a 4-μm-thick top analog

Table 2
Receiver Performance

Receiver Performance	
Signal Path Performance (per element)	
Peak Gain	43dB
Noise-Figure	7.4dB
Input-Referred 1dB Compression Point	-27dBm
Input-Referred 3rd-Order Intercept Point	-11.5dBm (2 tones 5MHz apart)
On-chip Image Rejection	35dB
S_{11}	< -10dB
Complete Receiver Performance (8 elements)	
Inferred Total Array Gain	61dB
Expected SNR Improvement	9dB
Phase-shifting Resolution	11.25°
Beam-forming Peak-to-Null Ratio	20dB (measured for 4 paths)
Power Dissipation @ 2.5V	364mA 287mA (w/o biasing and baseband buffers)
Technology	SiGe, 120GHz HBT 0.18μm CMOS
Die Area	3.5mm x 3.3mm

metal used for on-chip spiral inductors as well as for transmission lines routing the high-frequency signals. The die micrographs of the receiver and the transmitter are shown in Fig. 16. The size of the receiver chip is 3.3 mm × 3.5 mm while the transmitter chip occupies 6.8 mm × 2.1 mm of die area.

A. LO Path Performance

In order to not disturb the symmetry of VCO output phases, none of the outputs are connected to any pad for measurements. Nonetheless, we can verify the standalone VCO performance by picking up the high-frequency signal via a loop antenna placed on top of the chip. The frequency of the VCO can be continuously varied from 18.8 to about 21 GHz [Fig. 17(a)]. The slope of this transfer characteristic is about 2.1 GHz/V at 19.2 GHz and reaches a maximum of 2.67 GHz/V close to 19.6 GHz.

The phase noise of the free-running VCO at 18.70 GHz is shown in Fig. 17(b). The VCO achieves a phase noise of −103 dBc/Hz at 1-MHz offset from the carrier. The measurement at higher offset frequencies is limited by the thermal noise floor of the spectrum analyzer used to measure the phase noise. The output spectrum and the phase noise of the locked VCO are shown in Fig. 18.

As can be seen, the phase noise stays constant within the loop bandwidth as the frequency changes. Our synthesizer phase noise measurements have been limited by the phase noise of a synthesized sweeper that was used as the 75-MHz input reference signal. Better phase noise is expected if a crystal type reference is used. The frequency synthesizer performance is summarized in Table 1.

B. Receiver Performance

The input reflection coefficients S_{11} at 24-GHz RF ports are characterized both on chip and at the SMA connectors

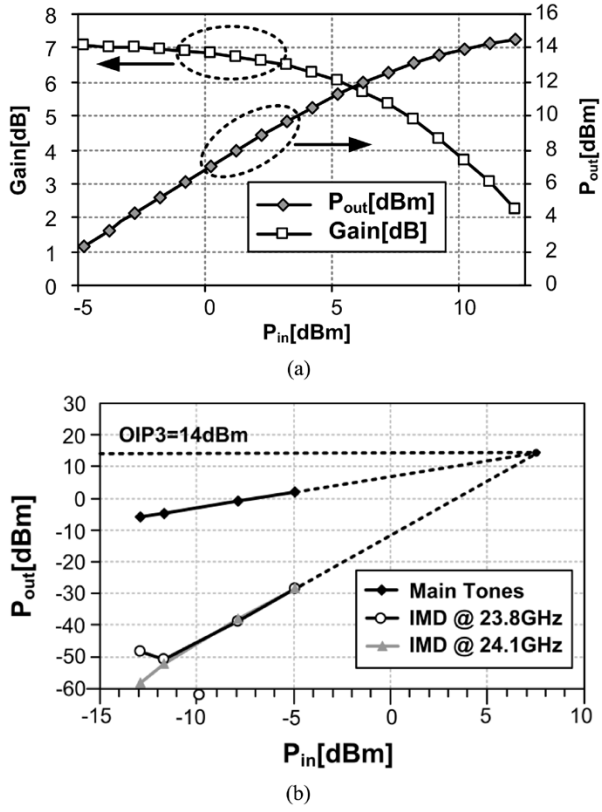

Fig. 23. On-chip power amplifier performance. (a) PA output power and gain. (b) Two-tone test.

of the RF inputs on board. The receiver demonstrates good input matching properties at frequency range of interest in both cases, as shown in Fig. 19.

Fig. 20(a) depicts the gain of a single element as a function of the input frequency, showing 43-dB peak gain at 23 GHz and 35 dB on-chip image rejection. The image signals will be further attenuated by narrow band antennas.

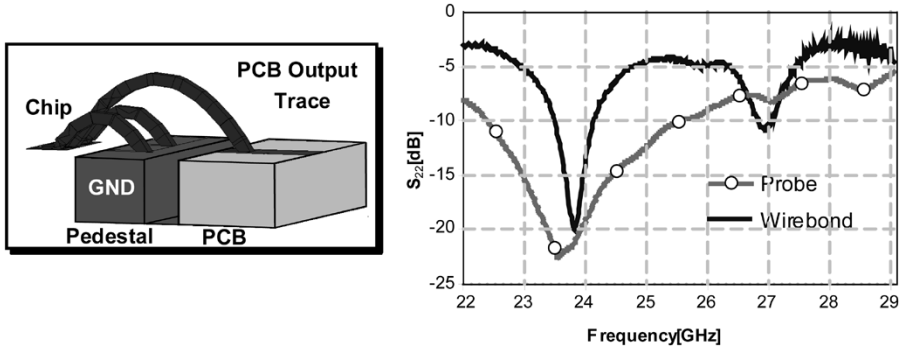

Fig. 24. Output matching in transmitter at 24 GHz.

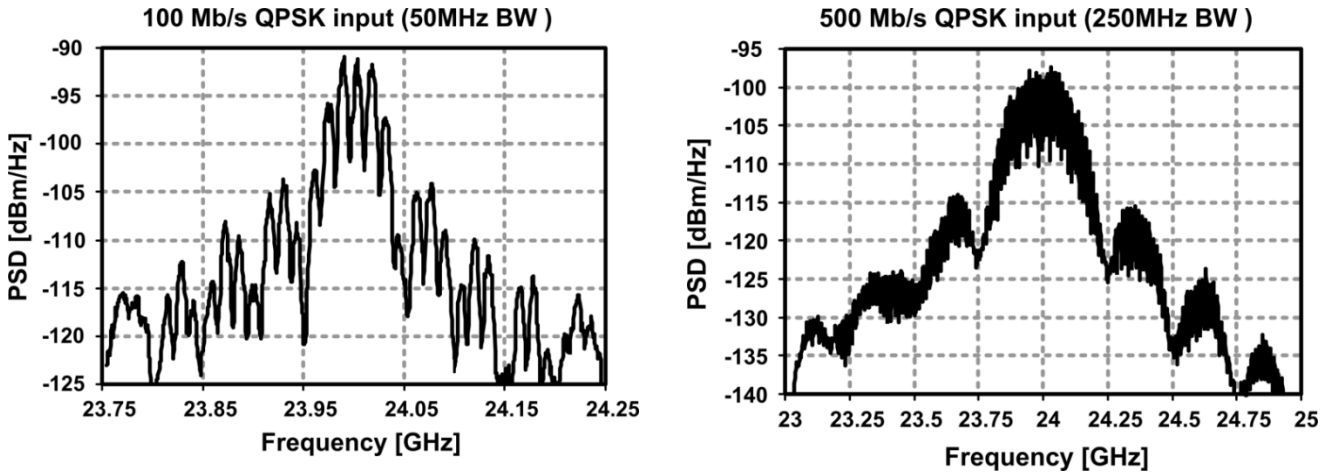

Fig. 25. Transmitter output spectrum.

A 3-dB gain variation is observed among various elements. The receiver noise figure as a function of input frequency is shown in Fig. 20(b). For a single element, a minimum double-side-band noise figure of 7.4 dB is measured over the signal bandwidth of 250 MHz. Fig. 20(c) and (d) show the measured nonlinearity of a single element. The input-referred 1-dB compression point is observed at -27 dBm, and the input-referred intercept point of the third-order distortion is -11.5 dBm.

Fig. 21 shows the on-chip isolation between different elements. The input signal is fed to the fifth path only. The phase selectors in the other elements are turned on one at a time to measure the output power due to coupling. When all phase selectors are off, the system has a -27-dB signal leakage (normalized to single element gain). The coupling is lower than -20 dB in all elements. The strongest coupling is seen between adjacent elements, e.g., the fourth and fifth elements as expected. However, when the phase selector in the fourth element is turned off and the one in the sixth element is turned on, a significantly lower output power is observed, which may due to the coexisting coupling and leakage canceling each other. The coupling between nonadjacent elements is close to or lower than the leakage level.

The array performance is assessed by generating an artificial wave front feeding the RF inputs to each receiver element via power splitters and adjustable phase shifters. This way, the array performance is measured independently of the antenna properties. The spatial selectivity of the phased array receiver is demonstrated in Fig. 22, which shows the measured array patterns with four elements operational. The measured performance of the receiver is summarized in Table 2.

C. Transmitter Performance

The complete transmitter, including four on-chip power amplifiers and on-chip frequency synthesizer, draws 788 mA from a 2.5-V supply. As shown in Fig. 23(a), each on-chip power amplifier is capable of generating up to 14.5 dBm of output power. The amplifier has a small signal gain of 7 dB and an output-referred 1-dB compression point of 11 dBm. Each amplifier draws 68 mA from a 2.5-V supply. Fig. 23(b) shows the measured two-tone performance of the amplifier.

The PCB used for testing the transmitter is a high-frequency laminate that is compatible with planar antenna design. Careful fabrication of the test setup ensured short wirebonds and therefore small parasitic inductances to the output and ground. Fig. 24 shows the output matching for one element with a probe-based measurement and with a wirebond–PCB trace–SMA connector measurement. Even though the PCB measurements show a narrow-band match, the matching over frequencies of interest is better than 10 dB.

One concern with placing multiple power amplifiers on the same die is the isolation between them. In this work, the

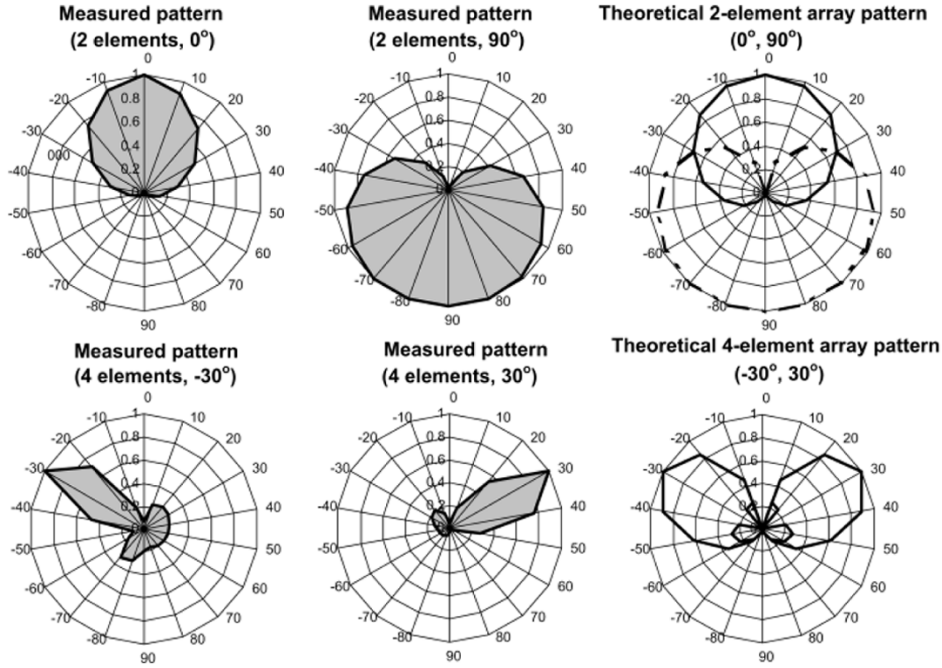

Fig. 26. Measured and theoretical transmitter array patterns with two and four elements active.

physical distance between the amplifiers and the use of transmission line based matching networks help in improving the on-chip isolation between different elements. The isolation is determined by turning on only one element and measuring the power at other elements, which are turned off by disabling all differential pairs in the phase selectors in those elements. This isolation was measured with the PCB setup and therefore includes wirebond and trace coupling. The worse case isolation between adjacent elements on the 2.1-mm side of the chip is 28 dB. The isolation between other elements pairs is more than 35 dB.

The image rejection in the first upconversion stage depends upon the quadrature matching between the inputs. Measurements showed an image signal attenuation of 24 dB. The image of the next up conversion step falls at 14.4 GHz. In addition to the image signal attenuation provided by the quadrature architecture, this image signal is further attenuated by the tuned stages at RF. Therefore, in this case, the image signal rejection was found to be better than 43 dB.

Fig. 25 shows the output spectrum of the transmitter when provided with baseband 50- and 250-MHz QPSK signals that correspond to data rates of 100 and 500 Mb/s, respectively.

To measure the array pattern, variable phase shifters are connected to the output of each element to emulate propagation delays for each element for every angle of radiation. The output of the phase shifters is combined and measured using a power meter or a spectrum analyzer. The measured array pattern with two elements and four elements active, shown in Fig. 26, when compared to theory, demonstrates the proper functioning of the phased array transmitter. To measure the performance of the transmitter for high data rate input, an external direct downconversion receiver was assembled, consisting of a passive mixer followed by an amplifier (Fig. 27). For this measurement, the LO signal that is used

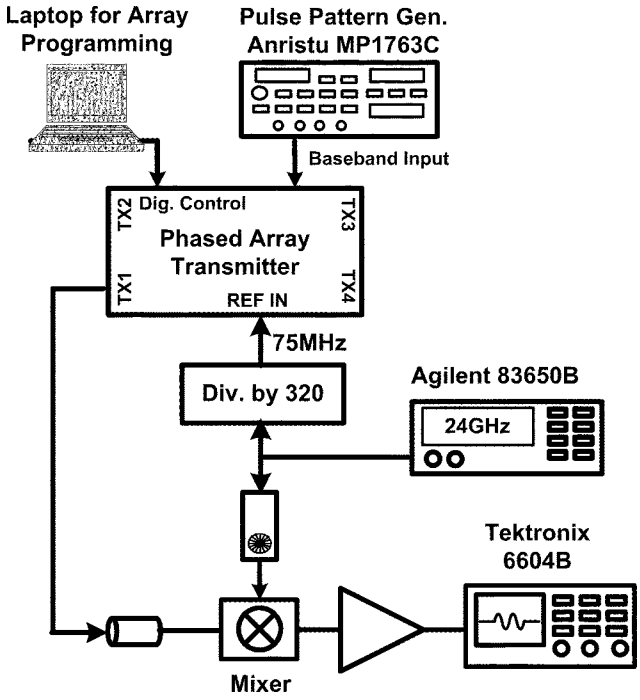

Fig. 27. Setup for direct downconversion of 24-GHz transmitter output.

for downconversion needs to be locked to the carrier signal of transmitter. Therefore, the 24-GHz LO signal to the external mixer is divided by 320 to generate the 75-MHz reference for the on-chip frequency synthesizer. The baseband input was provided to one channel using a pseudorandom bit-pattern generator, and no ISI-minimizing pulse shaping was done at the input. Fig. 28 plots the eye diagram for the downconverted baseband output for 250- and 500-Mb/s BPSK signal.

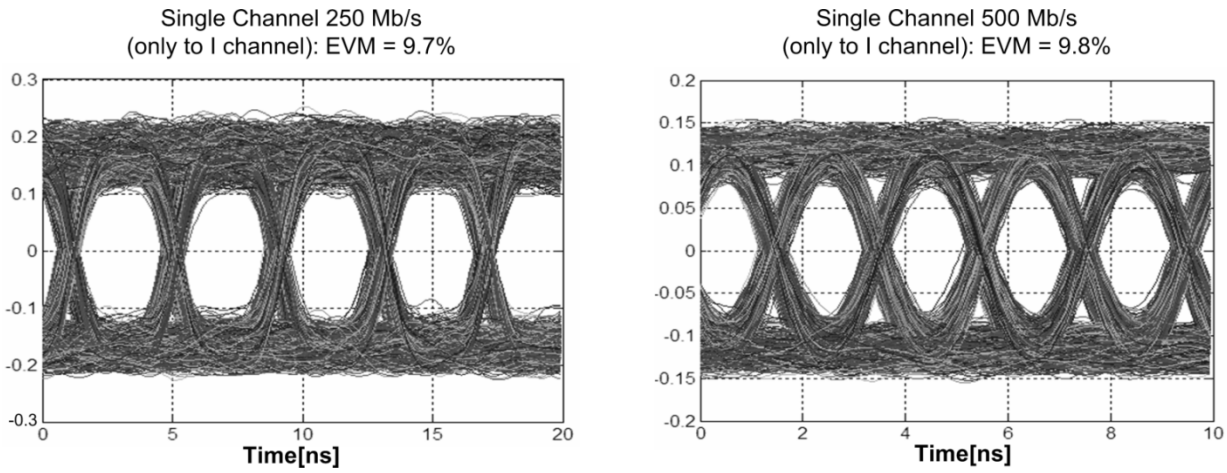

Fig. 28. Eye diagram of transmitter output @ 250 Mb/s and @ 500 Mb/s after downconversion.

Table 3
Transmitter Performance

Transmitter Performance	
On-chip Power Amplifier Performance	
Maximum saturated output power	14dBm
Current Consumption @ 2.5V	68mA
Output match @ 24GHz	-15dBm
Output referred 1dB compression point	11dBm
4-Element Transmitter Performance	
Equivalent 4-element Effective Isotropic Radiated Power	26dBm
Peak-to-Null Ratio for 4-element Array	> 23dB
Beam Steering Resolution	< 10° for normal angle of radiation
3dB Array Beam-Width @ 30° Radiation Angle	17°
Isolation between Paths (including wire bonds)	> 28dB
Image Signal Attenuation	> 24dB, first up-conversion > 43dB, second up-conversion (image @ 14.4GHz)
Transmit 3dB Bandwidth	> 400MHz
DC Current Consumption @ 2.5V	788mA
Device Technology	0.18μm CMOS in BiCMOS process
Die Area	6.8mm x 2.1mm

The measured EVM did not increase significantly with an increase in data rate, indicating that it is dominated by the noise in the external downconversion setup. Table 3 presents a summary of the measured performance of the transmitter.

VI. Conclusion

In this paper, fully integrated 24-GHz phased array transmitter and receiver were demonstrated for the first time. LO path phase-shifting architecture is used that provides a resolution of 22.5°. The eight-element SiGe receiver has a total gain (including array gain) of 61 dB and a minimum noise figure of 7.4 dB for a single element. The receiver can provide up to 9-dB improvement in SNR and has a peak-to-null ratio of 20 dB. The four-element 0.18-μm CMOS transmitter has integrated on-chip power amplifiers matched to 50-Ω output that are capable of generating up to 14.5 dBm output power each. It can support 500-Mb/s data rates (limited by the measurement setup) and has a peak-to-null ratio of 23 dB.

Acknowledgment

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REFERENCES

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, Apr. 1965.

[2] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Rev.*, vol. 26, pp. 163–163, 1965.

[3] B. Jagannathan *et al.*, "Self-aligned SiGe NPN transistors with 285 GHz $f_{\max}$ and 207 GHz f_T in a manufacturable technology," *IEEE Electron Device Lett.*, vol. 23, no. 5, pp. 258–260, 2002.

[4] T. Hashimoto *et al.*, "Direction to improve SiGe BiCMOS technology featuring 200-GHz SiGe HBT and 80-nm gate CMOS," in *Int. Electron Device Meeting Tech. Dig.*, 2003, pp. 129–132.

[5] J.-S. Rieh *et al.*, "SiGe HBT's for millimeter-wave applications with simultaneously optimized f_T and $f_{\max}$ of 300 GHz," in *IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers*, 2004, pp. 395–398.

[6] A. Hajimiri, "Distributed integrated circuits: An alternative approach to high-frequency design," *IEEE Commun. Mag.*, vol. 40, no. 2, pp. 168–173, Feb. 2002.

[7] "Federal Communications Commission,", FCC 02-04, Section XV.515.15.521.

[8] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz eight-element phased-array receiver in silicon," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2311–2320, Dec. 2004.

[9] A. Natarajan, A. Komijani, and A. Hajimiri, "A 24 GHz phased-array transmitter in 0.18 m CMOS," in *ISSCC Dig. Tech. Papers*, vol. 48, 2005, pp. 212–213.

[10] W. H. V. Aulock, "Properties of phased arrays," *Proc. IRE*, vol. 48, pp. 1715–1728, Oct. 1960.

[11] R. C. Hansen, Ed., *Significant Phased Array Papers*. Norwood, MA: Artech House, 1973.

[12] R. S. Elliott, *Antenna Theory and Design*. Englewood Cliffs, NJ: Prentice-Hall, 1981.

[13] *The RF and Microwave Handbook, Session 6.9*, M. Golio, Ed., CRC, Boca Raton, FL, 2000.

[14] D. Parker and D. C. Zimmermann, "Phased arrays—Part I: Theory and architectures," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 678–687, Mar. 2002.

[15] ——, "Phased arrays—Part II: Implementations, applications, and future trends," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 688–698, Mar. 2002.

[16] B. Kane, L. Geis, M. Wyatt, D. Copeland, and J. Mogensen, "Smart phased array SoCs: A novel application for advanced SiGe HBT BiCMOS technology," *Proc. IEEE*, to be published.

[17] "IRE standards on electron tubes: Definition of terms," *Proc. IRE*, vol. 45, pp. 983–1010, Jul. 1957.

[18] A. Hajimiri, A. Komijani, A. Natarajan, X. Guan, and H. Hashemi, "Phased array systems in silicon," *IEEE Commun. Mag.*, vol. 42, no. 8, pp. 122–130, Aug. 2004.

[19] H. Hashemi, X. Guan, A. Komijani, and A. Hajimiri, "A 24-GHz SiGe phased-array receiver—LO phase shifting approach," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 614–626, Feb. 2005.

[20] H. Zarei and D. J. Allstot, "A low-loss phase shifter in 180 nm CMOS for multiple-antenna receivers," in *ISSCC Dig. Tech. Papers*, vol. 1, 2004, pp. 392–392.

[21] G. Schuppener, T. Harada, and Y. Li, "A 23-GHz low-noise amplifier in SiGe heterojunction bipolar technology," in *IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers*, 2001, pp. 177–180.

[22] X. Guan and A. Hajimiri, "A 24-GHz CMOS front-end," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 368–373, Feb. 2003.

[23] F. Ellinger, "26–42 GHz SOI CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 522–528, Mar. 2004.

[24] S. Reynolds, B. Floyd, U. Pfeiffer, and T. Zwick, "60 GHz transceiver circuits in SiGe bipolar technology," in *ISSCC Dig. Tech. Papers*, vol. 47, 2004, pp. 442–443.

[25] A. Joseph *et al.*, "A 0.18 μm BiCMOS technology featuring 120/100 GHz $(f_t/f_{\max})$ HBT and ASIC-compatible CMOS using copper interconnect," in *Proc. BCTM*, 2001, pp. 143–146.

[26] S. P. Voinigescu, "A scalable high frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," in *IEEE Proc. Bipolar Circuits and Technology Meeting*, 1996, pp. 61–64.

[27] *IE3D Electromagnetic Simulation User Manual*, 2001.

[28] A. Komijani and A. Hajimiri, "A 24 GHz, $+14.5$ dBm fully-integrated power amplifier in 0.18 m CMOS," in *Proc. IEEE 2004 Custom Integrated Circuit Conf.*, pp. 561–564.

[29] T. S. D. Cheung *et al.*, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *ISSCC Dig. Tech. Papers*, vol. 46, 2003, pp. 396–397.

[30] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase-frequency detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 13–21, Jan. 2003.

[31] J. Craincks and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*. Norwell, MA: Kluwer, 1998.

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