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Integrated Power Management Circuit for Piezoelectronic Generator in Wireless Monitoring System of Orthopedic Implants

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1. Introduction

Wireless Monitoring System of Orthopedic Implants(WMSoOI), which is employed to detect the situations of implanted materials in patients as artificial joints, is one kind of Smart Biomedical MicroSystems(BMS). This kind of BMS is supplied by little mechanical energy. Due to the limit of input energy, there are a lot of challenges on power converter system, such as efficiency, volume, etc[1][2].
In this chapter, section 2 gives the application background of WMSoOI, and then according to the system requirements, a novel hybrid power management system is proposed in section 3. Section 4 illustrates the concrete circuit design of each block. In section 5, measurement results and simulation results are given. Finally, section 6 is a summary.

2. Application background of Wireless Monitoring System of Orthopedic Implants(WMSoOI)

Bone health is the precondition of a happy life. However, in China, 10% of the whole population suffers from osteoarthrosis, in whom many people don't have a normal life due to joint aging, joint diseases, etc. Artificial joint replacement surgery can help the patients to re-establish motor function, but there are many problems after surgery. When artificial materials have been implanted into human body, abrasion, loose and osteolysis not only affect the health and life quality of the patients, but also bother orthopedists.
In order to monitor the artificial material's situation, WMSoOI is proposed in figure 1[3]. As described, a piezoelectric(PZT) device is employed to generate electricity in an implanted bone prosthesis. When deformed by outside pressure, the PZT device can supply enough power to the whole information gathering system. In the above equipment, the PZT material not only plays a role as a sensor, but also plays a role as a generator.
In this work, a power management system is proposed to integrate several function modules into a chip to reach a small volume, which makes it possible to be implanted into human beings' body. The whole work process of the WMSoOI can be illustrated as the following. First, pressure information of artificial joint is gathered by PZT material and then

these data can be stored in non-volatile memories. Second, all of these stored data can be read by other instruments with passive RFID technologies periodically, such as a couple of days. Finally, with the information data, medical information system can monitor the real situations of those artificial materials implanted in human beings. The gathered information will help doctors to get enough information in time, mitigate the patients' pain and also can help doctors to choose proper materials to be employed in implanted artificial joint instruments.

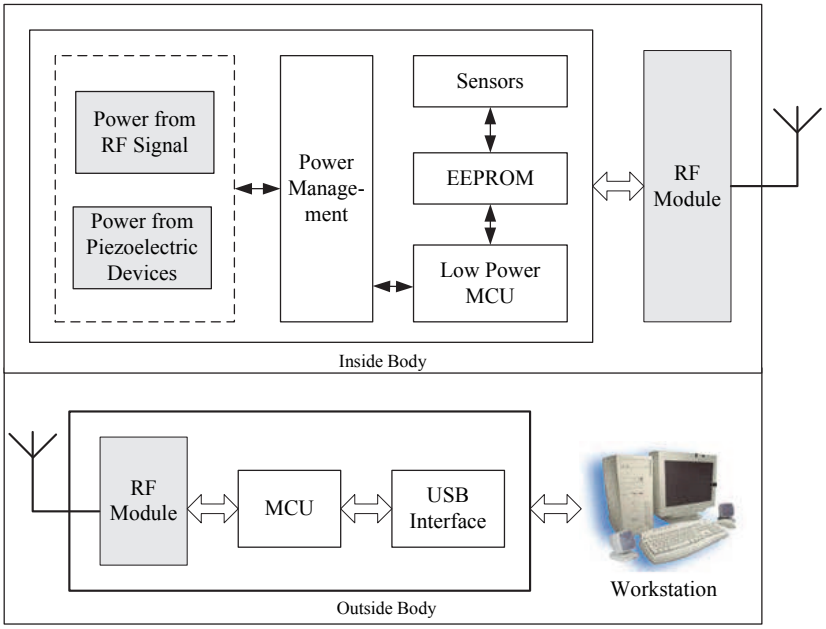

Fig. 1. Wireless monitoring system of the orthopedic implants

The difficulty to realize this integrated system lies on: PZT materials not only acts as sensors to detect the deformation of artificial joint, but also provides stable power for the functional circuits in the instrument. It is reported that the PZT device can only provide 4 mW power in a similar application background[4][5][6]. In addition, PZT materials have poor source characteristics, such as high output impedance, low output current, etc, which enhance the difficulty of designing power management circuit. In all, the power management system design of WMSoOI is a very challenging work.

3. Power management system of Wireless Monitoring System of Orthopedic Implants(WMSoOI)

In this section, in order to make full use of the energy generated by PZT materials in WMSoOI, the electrical characteristics of PZT materials and intermittent power supply mode will be illustrated first; then previous power management systems using PZT materials as power supply will be reviewed; finally, a power management system, which is suitable for intermittent power supply, is proposed to improve the convert efficiency.

3.1 Electrical characteristics of PZT material and intermittent power supply mode

Piezoelectric(PZT) materials are capable of converting the mechanical energy of compression into electrical energy. People have already used this characteristic to realize many kinds of sensors. But due to some intrinsic characteristics, such as high voltage, low current and high impedance, etc, the output power of PZT materials is very low and doesn't have the characteristics as an available power. But by now, with the advent of low power integrated circuits, it is possible to use ambient energy to provide power for an information system.

Electrical circuit model for PZT generators are typically represented by capacitors, resistors and inductance, as shown in figure 2[3][4]. F_{in} and V_{in} represent input force and input voltage respectively, and ϕ is the ratio of electrical output to mechanical input(V/N). R_e , L_e , C_e and $C_p^{'}$ are equivalent electrical circuit element parameters to reflect the mechanical element parameters. R at the right part of figure 2 is the load of the power generator.

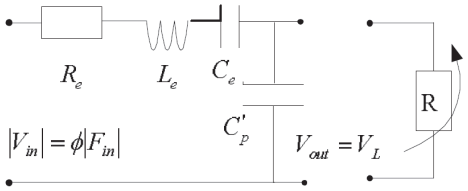

Fig. 2. Electrical Circuit Model of PZT

After being stored by power management system, the electrical energy generated by PZT materials, are converted into a stable power, which provides power for subsequent functional modules. The equivalent capacitor in the PZT generator is in parallel with the storage capacitor and the system load. There are two working situations. First, when the stored energy is not enough to provide power for the subsequent information system, the electrical energy generated by the PZT material is charged into the storage capacitor. At this time, the power consumption is just the leakage power, while the whole WMSoOI is in stand-by mode. Second, when the stored energy is enough for the whole system to finish functions, the storage capacitor is in a discharge situation, to provide power for the functional modules. The above whole process about energy convert and consumption is regarded as an intermittent work mode.

3.2 Current power management system in electrical system supplied by PZT materials

Figure 3 shows the system diagram to study the power converter of PZT materials[4]. This system is used to measure the electrical energy generated by three PZT devices in the artificial joint, where the situation is similar with the condition that human being is in a normal walking station. By diode rectifier and storage capacitor, about 4mW power is generated by these PZT devices. In [4][5][6], a big storage capacitor is employed to collect electrical energy and supply the subsequent functional circuits in each system. [4][5] use linear regulators to adjust the electrical energy in the storage capacitor to convert the energy into available power, whose converter efficiencies are 8.8% and 19%, respectively. [6] uses switcher to convert the energy stored in the capacitor, whose efficiency can reach 17.6%.

Furthermore, the systems in [4][5][6] employ commercial chips to fulfill power management functions. In rectifier circuit, because the output voltage of PZT material is very high, so the efficiency of the rectifier can reach 98%.

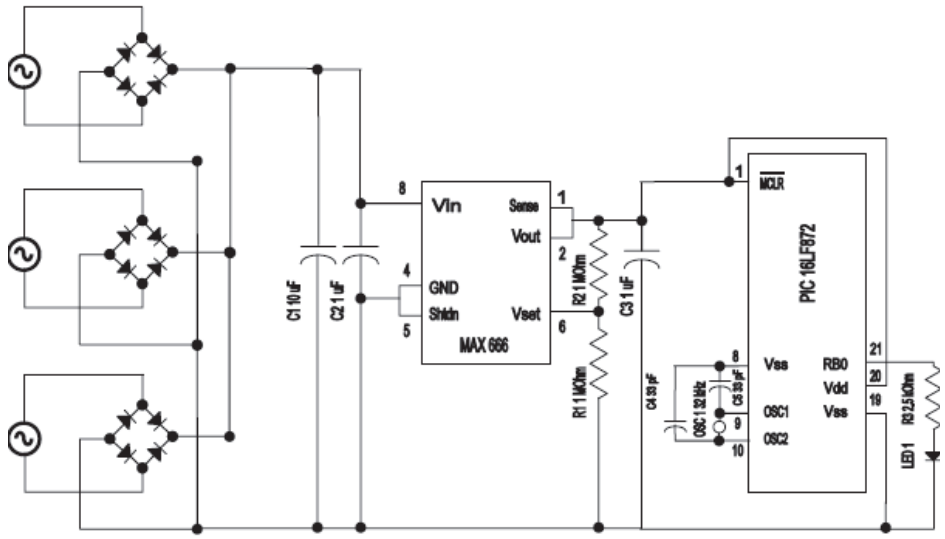

Fig. 3. Previous work of PZT generator [4]

These references prove that PZT materials have the ability to provide enough energy for microsystems and make sure that WMSoOI is feasible. But there are several problems[1]:

1. Previous works are principle experiments, without considering that the system volume when PZT materials implanted into the artificial joint.
2. The power system convert efficiency of storage capacitor is low that this little energy cannot provide enough power for the subsequent complicated function circuit, such as AD converter to sample PZT signals, MCU to process data and read-write EEPROM data circuits to interface data, etc.
3. The power system is lack of optimization. Monitoring circuit, control circuit, current limiting circuit, and other circuits are needed to improve power efficiency.

From above, a novel power management system is proposed to meet the requirements of WMSoOI in next section.

3.3 Power management system working in intermittent mode, using PZT materials as power supply

Regarding to the three problems illustrated in section 3.2, an integrated hybrid DC-DC converter is proposed to construct the main part of the power management system, which will be integrated with the rectifier, reduce the volume of the whole system and improve energy convert efficiency. In the same time, intermittent working mode is introduced to enhance the power management function to solve the technical problems in WMSoOI[1][2][7].

Due to human body's weight, PZT materials generate alternate current energy, which is rectified and then stored in the storage capacitor. Considering the output voltage ripple and convert efficiency, a 10μF capacitor is used as the storage capacitor to get a better trade-off

in capacitor value. This power management system is in an intermittent working mode, the concrete working process is as following: 5V is set to be the threshold of this power converter system. When the voltage across C_{store} is lower than 5V, the power converter will stay in a standby mode until the PZT generator charges C_{store} above the threshold voltage. Otherwise, when the output voltage across C_{store} is higher than 5V, power converter begins to work. This is one measure to improve converter efficiency in system level.

In order to further improve the energy efficiency in a circuit level, a hybrid power management system is proposed, as shown in figure 4, including rectifier circuit, storage capacitor, input voltage monitoring circuit, variable step-down ratio SC(Switching Capacitor) converter, bandgap reference, output voltage monitoring circuit, start-up circuit and voltage limit circuit, etc .

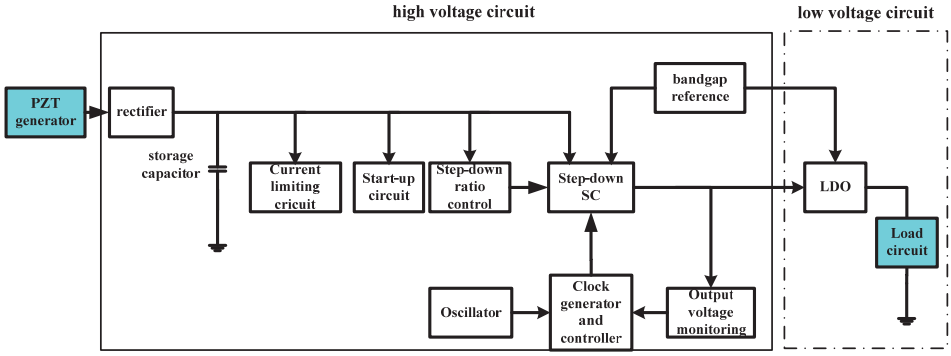

Fig. 4. Power converter system for PZT generator

The dominant blocks in the proposed power management system is serial connections of the variable step-down ratio SC converter and the low dropout linear regulator(LDO). Those circuits, surrounded by the dashed box, including bandgap reference, step-down SC, step-down ratio control circuit, oscillator, clock generator, clock control circuit and output voltage monitoring circuit, work in the high voltage supply region in this power management system, which is supplied by the storage capacitor. Oscillator, clock generator and clock controller are auxiliary parts for step-down SC circuit. Bandgap reference is employed to provide voltage reference and current reference for other modules. The LDO circuit and subsequent functional circuit, surrounded by dotted line, are supplied by the output of step-down SC circuit.

The function of variable step-down ratio SC circuit is to regulate the output voltage of storage capacitor, whose output voltage ranges from 5.5V to 15V, to 2V. The conversion ratio can be different, such as 2/3, 1/2 and 1/3. In order to realize variable step-down ratios, a SC converter with variable topology is employed. By choosing different switches, the concrete circuit topology can be set to implement different step-down ratios, which will be explained in detail in section 4.3. The function of LDO is to regulate the input voltage, which is about 2V, to 1V or even lower power supply with small ripples and high PSRR performance for analog circuits.

In the above power management circuits, those parts in high voltage region is designed in 0.35μm CMOS technology, while circuits in low voltage region is designed in 0.18μm CMOS

technology, which is suitable for the integration of LDO circuit and the subsequent functional circuits.
This power management system operates according to the following rule. By monitoring the voltage on storage capacitor and the output voltage of step-down SC converter, the power management system can control the enable signal of variable step-down ratio of the SC circuit to improve the power convert efficiency of charges stored on storage capacitor.

4. Circuit design of the power management system in WMSoOI

In this section, several important circuit designs of the power management in WMSoOI are illustrated in detail.

4.1 Rectifier circuit

Rectifier is used to convert AC(alternative current) power into DC(direct current) power. Several papers have done a lot of work in fully integrated rectifier. [8] realizes half-wave rectifier of PZT material, which is used for low input voltage applications. [9] introduces fully integrated rectifiers working at high frequencies in commercial CMOS technology.
The rectifier in this system is a full wave rectifier composed of four diodes, as shown in figure 5. Its function is to change AC electrical energy into DC electrical energy. Diodes can be easily fabricated in commercial CMOS process, although they have larger threshold voltage comparing with CMOS devices.
When voltage on side A of the PZT material is higher than that of side B, D1 and D4 are shutoff while D2 and D3 are forward turned on. This ties the low voltage side of the PZT material to ground while passing the high voltage. Situation is reversed when the voltage of side B is higher than side A.
Due to low frequency, parasitic capacitance can be ignored. Diode area is set to be 30μmx30μm, to reduce the parasitic resistor when the diode is "ON" and so to improve convert efficiency. Storage capacitor also has the ability to filter output voltage ripple. Because the transistor gate breakdown voltage is 18V, which is enough for the storage capacitor to be charged into 15V. Higher voltage across the storage capacitor will provide more energy for subsequent circuits.

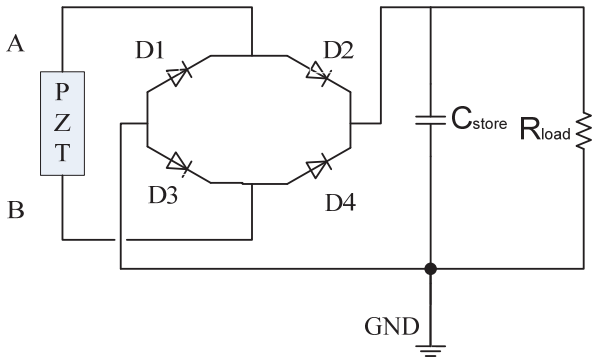

Fig. 5. Rectifier circuit

4.2 Bandgap reference

Bandgap reference circuit is a basic and important component in analog and mixed signal circuit. It not only provides precise voltage reference, but also provides precise bias currents. [10] summarizes bandgap reference circuits for low voltage operation, where current mode is often used to keep output voltage stable under conditions when supply changes. It is true that the variations of supply are small in low power supply. As far as large supply ranges are concerned, circuit topology including a voltage operational amplifier is a good solution. Figure 6 shows the system diagram of the proposed bandgap reference. In order to reduce the power dissipation of bandgap reference, transistors working in sub-threshold regions are used to reduce the supply current. At the same time, several high performance parameters of bandgap reference must be kept under different conditions such as supply voltage variations, temperature variations and different technology corners, etc. And a voltage buffer is integrated to increase the drive capacity of the bandgap reference.

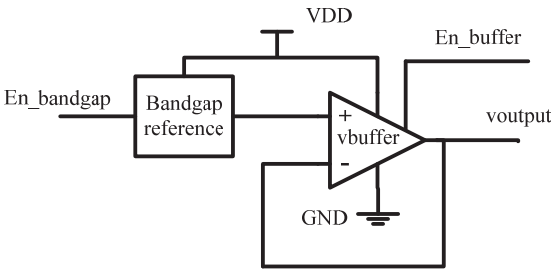

Fig. 6. System diagram of the proposed bandgap reference

Next is the principle of this bandgap reference working in subthreshold region. At the beginning, the Current performance of transistors working in subtreshold region is described. MOS transistors' drain-source current working in sub-threshold region can be expressed as

$$I_D = I_0 \frac{W}{L} e^{\frac{V_G - V_T}{n\phi_t}} \left(1 - e^{-\frac{V_{DS}}{\phi_t}} \right) \tag{1}$$

where I_0 is constant dependent on technology parameters, W and L are width and length of MOS transistors, respectively. V_T represents threshold voltage. n is a technology parameter dependent on process and ϕ_t is thermal voltage, which is about 26mV at room temperature 27℃. Equation (1) is suitable for general analysis when $V_G << V_T$. It is obvious that the drain source sub-threshold current is exponential to the minus of $(V_G - V_T)$. Therefore, sub-threshold current is sensitive to the variation of V_T.

And the transconductance of MOS transistors working in subthreshold region can be expressed as

$$g_m = \frac{I_D}{n\phi_t} \tag{2}$$

which discloses the relation between g_m and I_D in subthreshold region.

Selection of width and length of transisitor woking in sub-threshold region in the bandgap reference is explained in detail in this paragraph. Determining transistors' sizes is the key design in the process of circuit design. During this process, g_m / I_d is a very important design parameter and it represents the ratio of transconductance g_m to drain current I_D. In order to get high ratio of g_m / I_d to reduce power consumption[11][12], many people have already done a lot of work. In [13], Christian C. Enz and Eric A. Vittoz presented an EKV model for MOS transistors and this model can represent the MOS characteristics in different working regions using one equation, wherever the possible regions MOS transistors may work in. In [14], researchers proposed another MOSFET model, which has the common property that tries to use a unified model for MOS transistors in all regions, and the corresponding design methods. According to all of these papers, there are several equations available to design low power circuits.

$$I_D = 2\pi \cdot GBW \cdot C_L \cdot n \cdot \phi_t \left(\frac{1+\sqrt{1+i_f}}{2} \right) \tag{3}$$

$$\frac{W}{L} = \frac{2\pi \cdot GBW \cdot C_L}{\mu C_{ox} \phi_t} \left(\frac{1}{\sqrt{1+i_f}-1} \right) \tag{4}$$

$$V_{DS(sat)} \cong \left(\left(\sqrt{1+i_f}-1 \right)+4 \right) \phi_t \tag{5}$$

$$f_t \cong \frac{\mu \phi_t}{\pi L^2} \left(\sqrt{1+i_f}-1 \right) \tag{6}$$

where I_D is the current of MOS transistor from the drain to the source, GBW is unity-gain bandwidth, C_L is load capacitance, n is the slope factor, ϕ_t is thermal voltage, i_f is inversion level, C_{ox} is oxide capacitance per area, f_t is the cut-off frequency of MOS transistor, W is the width of MOS transistor, L is the length of MOS transistor, μ is the mobility of electron or hole, V_{DS} is the drain to source voltage of MOS transistor.

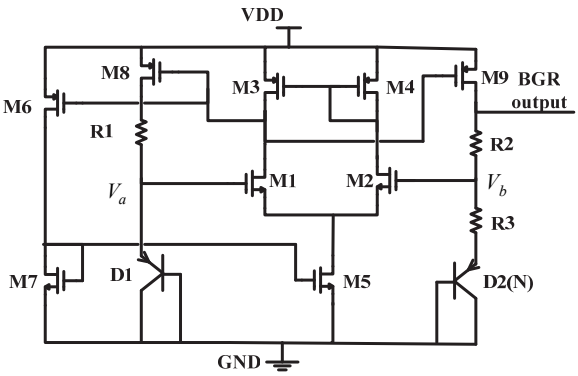

Fig. 7. Concrete circuit of the proposed bandgap reference

Figure 7 shows the concrete circuit of bandgap reference[15]. M1-M5 consist of an op-amp to keep the same voltage value of V_a and V_b . M6 and M7 provide the bias current for the op-amp. The output of op-amp is connected to the gate of M8 and M9. In order to reduce power consumption, all of these transistors are biased in sub-threshold regions or near the region to lower current consumption. Start-up circuit of bandgap reference is not drawn in figure 7.

Low current was assigned to every branch in figure 7. Every branch of the op-amp is less than 70nA and the bias current should be less than 140nA at 125℃, while the current through the resistors is less than 1.5μA. Because this system is not very stringent on circuit speed, its GBW is set to be 2.5KHz. By far the i_f parameter of transistor M1 and M2 can be obtained according to equation (3). Consequently, the W/Ls of transistors are obtained according to equation (4). At the same time, checking f_t parameters of transistors is necessary. If MOS transistors' parameters satisfy the requirement that unity gain frequency is greater than at least three times the GBW, the design space will avoid the parasitic diffusion and overlap capacitance to be of the same order of the load capacitance.

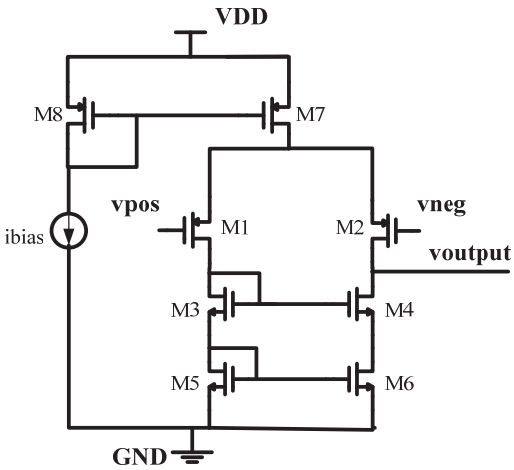

Fig. 8. Concrete circuit of the voltage buffer of bandgap reference

Voltage buffer of the bandgap reference is described in the next paragraph. Figure 8 shows the concrete circuit of the voltage buffer of the proposed bandgap reference. A traditional single stage amplifier is used as a voltage buffer to increase the drive capacity of the proposed bandgap reference. M1 and M2 are PMOS transistors as input transistors. M3, M4, M5 and M6 are used as current sources to form the active load of the input pair. ibias provides current reference for the amplifier. All the transistors in figure 8 are working in saturation region. The current through transistor M7 is about 3.2μA according to the simulation results.

4.3 Variable step-down ratio SC circuit

Circuit topology is shown in figure 9, which is illustrated in details in [16]. A and B are used to select different step-down conversion ratio. And P_1 , P_2 and P_3 are logic combinations of A, B, clk1 and clk2, as illustrated in table 1.

VDD/Vout	1/3	1/2	2/3
A	0	1	1
B	1	1	0

Table 1. Relations between control signals and step-down conversion ratio

Equation (7) depicts the relationship between P_1 , P_2 , P_3 and other signals.

$$\begin{aligned} P_1 &= (ck1)\overline{A} + (ck2)\overline{B} \\ P_2 &= (ck1)A \\ P_3 &= (ck2)B \end{aligned} \tag{7}$$

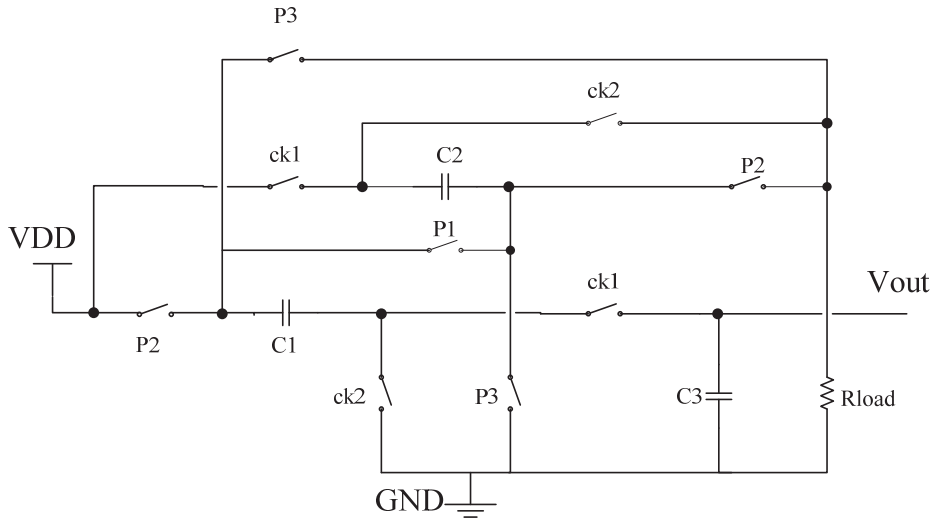

Fig. 9. SC converter circuit topology

Integrated capacitors are used to perform the DC-DC convert functions[17]. For integrated switched capacitor DC-DC circuits, there are three kinds of flying capacitors: MOS capacitors, PIP (poly-insulator-poly) capacitor and MIM (metal-insulator-poly) capacitor. Every capacitor has its own characteristics. MIM capacitors have good linear characteristic, but usually too much parasitic capacitance; PIP capacitors don't have good linear characteristic and they don't have too much parasitic capacitance; MOS capacitors have the biggest unit capacitance in CMOS technology because the distance between MOSFET gate and substrate is the smallest in the whole process. [18] compares parasitic capacitance among different kinds of integrated capacitance. After careful consideration and trade-off, MOS capacitance is preferred in this design.

One of the most important considerations of charge pump circuit design is to suppress the leakage current in the switching process. If PMOS's drain voltage or source voltage is 0.7V higher than supply voltage, the PN junction(drain or source of PMOS is regarded as p terminal, n well is regarded as n terminal) will be forward biased, which will lead to generation of leakage current.

There are two approaches to avoid leakage current generation. One is to properly set capacitors' values, second is to apply considerate clock sequence. When it comes to selection of capacitors' values, there are several considerations. The larger value the output capacitor has, the smaller output ripple the system has. At the same time, the ratio of output capacitor to flying capacitor determines the leakage current. If the ratio is large, then the voltage variation of flying capacitor will be large. This will add possibility of leakage current.

Another approach to suppress leakage current is to use proper clock sequences. 1/2 step-down conversion ratio is considered as a typical case, as shown in figure 10. After charge is delivered into C1 and C2, M1 and M3 are turned on, while M2 and M4 are turned off at this time. Then M1 is turned off to implement the redistribution between C1 and C2. If C1 is much smaller than C2, then the voltage across C1 is much larger than C2. If M2 and M4 are turned on simultaneously, the voltage at node2 is lower than ground. So during the selection of capacitor, C1 is not allowed to be much smaller than C2, although this will generate bigger output voltage ripple. In this case, C2 is set to be 10nF and C1 is set to be 1nF. In addition, if M4 is first turned on, and after several nano-seconds, M2 is then turned on. This method is named as stacked switches technique(those switches operate like stack), which will reduce the possibility of leakage current. But stacked switches technique needs complex clock sequence, figure 11 is an oscillator circuit to perform such a function.

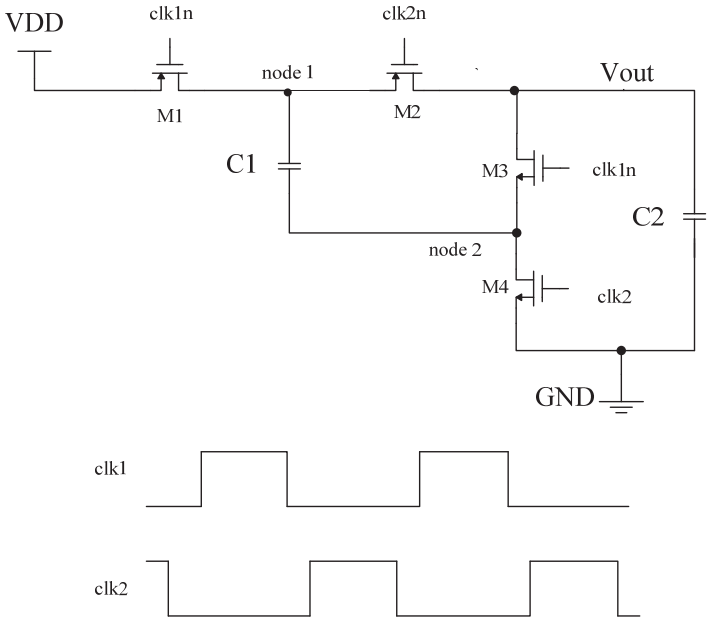

Fig. 10. 1/2 step-down conversion SC circuit

4.4 Clock generator and oscillator

Figure 11 shows the concrete circuit of the oscillator. Four comparators are used to implement the above mentioned clock scheme. Several logic operations of comparators' outputs are used to implement the clock scheme. TF, which is generated by clock output signals, is the signal to control turning on or off of M1 and M2, changing the charge stored in capacitor C and forming an oscillator. One of the advantages of this oscillator is that this scheme automatically realizes the controlled clock. When the output voltage of SC is lower than the settled value, through the control of TF signal, it will be convenient to achieve the enablement of clock, and then restart the SC converter. On the contrary, when the output of SC is higher than the settled value, clock will be disabled through the control of TF signal.

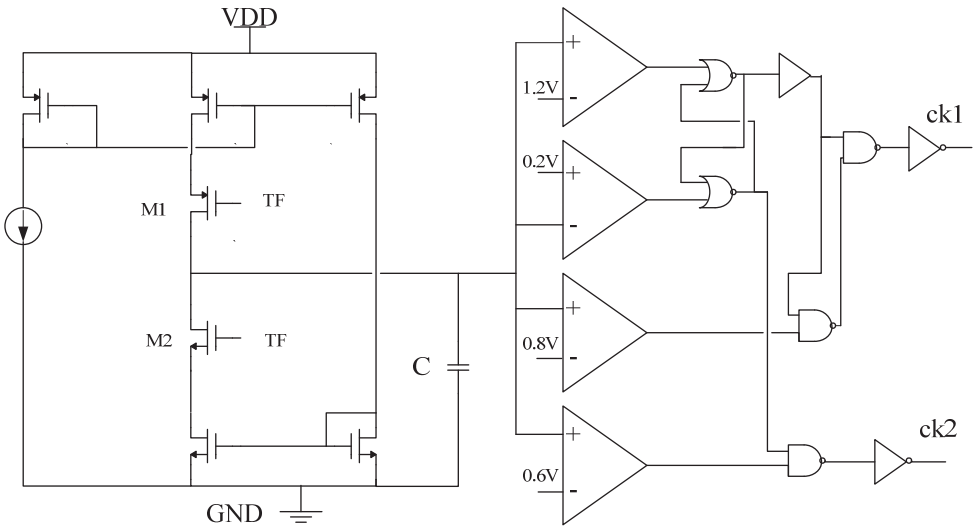

Fig. 11. Concrete circuit of oscillator

Comparators fabricated in CMOS technology have bigger DC offset. In addition, comparators working in switched capacitors are often affected by disturbance and noise. So hypothesis comparators are applied to reduce the above affects. Figure 12 shows the detailed circuit of hypothesis comparator.

The hypothesis comparator uses two-stage structure. In the first stage, M1-M7 consists of differential input stage, where M1 is the tail current, M2 and M3 are source coupled differential input pair, M4, M7 and M5, M6 are cross-coupled bi-stable current sources as load[19][20]. The ratios of width to length of M5, M6 are larger than M4, M7. M8-M11 consists of the second stage, which act as two inverters to increase drive capacity. The comparator consumes 1μA supply current when it is operating, which is a low power design, suitable for this system.

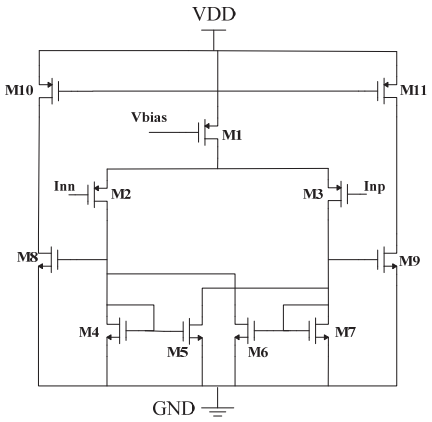

Fig. 12. Hypothesis Comparator Circuit

4.5 Step-down ratio decision circuit and output voltage monitoring circuit

The function of step-down ratio decision circuit is to monitor the voltage on storage capacitor. The output of this module is to dynamically set the step-down ratio of the SC circuit. The system block of this circuit is shown in figure 13. Vstore represents the voltage of storage capacitor.

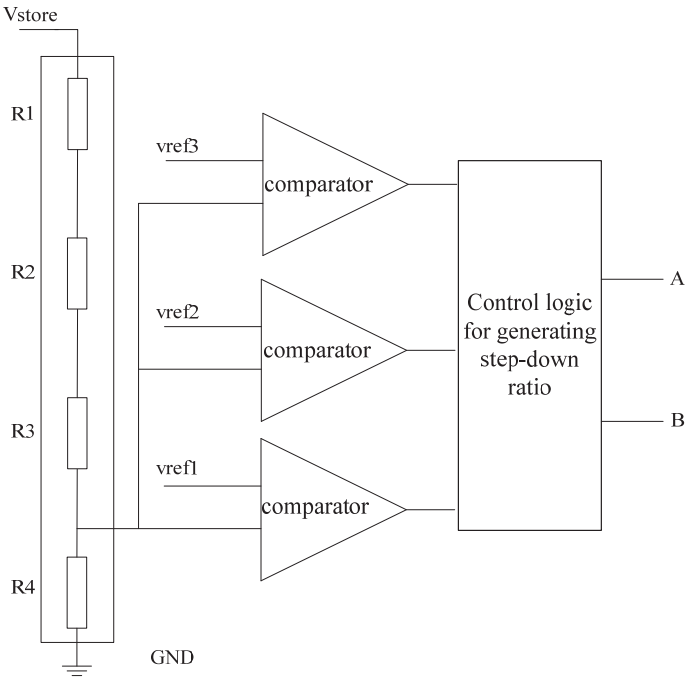

Fig. 13. Diagram of step-down ratio control circuit

The function of output voltage monitoring circuit is to detect the output voltage of variable step-down ratio SC circuit in real time. Its output determines whether enable the clock signal, in order to control the step-down SC circuit. The system diagram is shown in figure 14, where vout_sc is the output voltage of the variable step-down SC converter.

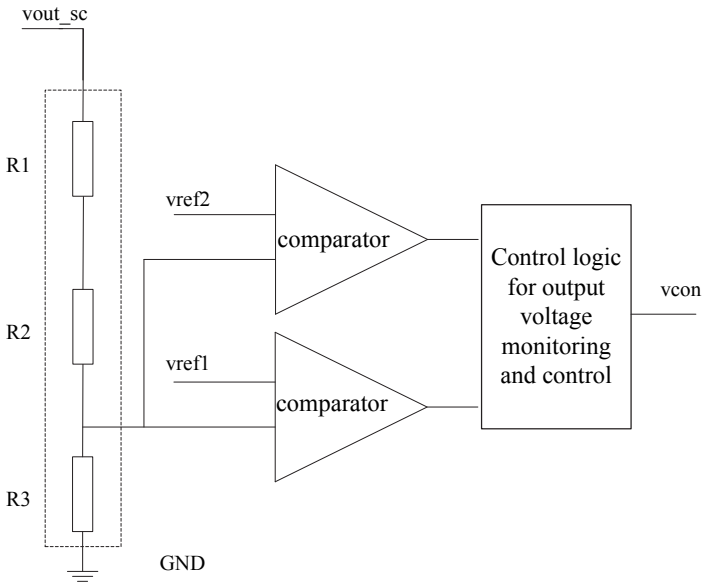

Fig. 14. Diagram of output voltage monitoring circuit

In figure 13 and figure 14, comparators are both realized by hypothesis comparator circuit, which is shown in detail in figure 12. In figure 13, 3 similar comparators are employed in the step-down ratio decision circuit while 2 similar comparators are employed in the output voltage monitoring circuit in figure 14.

4.6 LDO circuit

Traditional LDO circuit structure consists of three components: an error amplifier, a power transistor and a resistive voltage divider. The positive input of error amplifier is connected to the reference voltage and the negative one is connected to the resistive voltage divider of output voltage. The output voltage of error amplifier is to control the gate voltage of power transistor.
Because the subsequent functional circuits include analog components, such as AD converters and RF modules, PSRR(Power-Supply Rejection Ratio) of LDO is a very important characteristic, which is a measure of the ability of an output voltage to prevent noise from power supply noise. On one hand, high gain of error amplifier will lead to high PSRR; on the other hand, using PMOS transistor as power transistor will reduce power noise by offsetting power supply noise through power transistor and error amplifier [21].
In this case, error amplifier DC gain is more than 70dB and PMOS transistor is used as the power transistor. In order to suppress the supply noise from PMOS transistor, the error amplifier uses NMOS input differential pair and PMOS current-mirror load connected to the supply, as shown in figure 15.

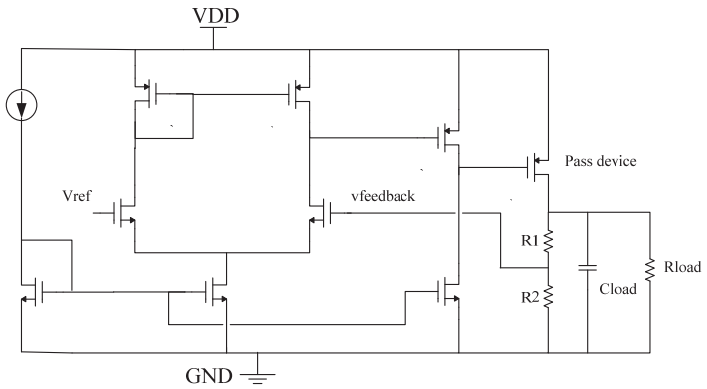

Fig. 15. Concrete LDO Circuit

5. Measurement results

Circuits of the power management circuit in high voltage region is taped out on 0.35μm CMOS EEPROM technology, while other circuits in low voltage region is to be taped out on 0.18μm CMOS technology. In this section, the measurement results of those parts in high voltage region and the simulation results of those parts in low voltage region are described.

5.1 Bandgap reference's measurement results

The proposed bandgap reference was fabricated on the above mentioned 0.35μm CMOS EEPROM technology[22]. Figure 16 shows the die photo of the proposed bandgap reference. The active area of the die is 370μm*454μm, including the voltage buffer.

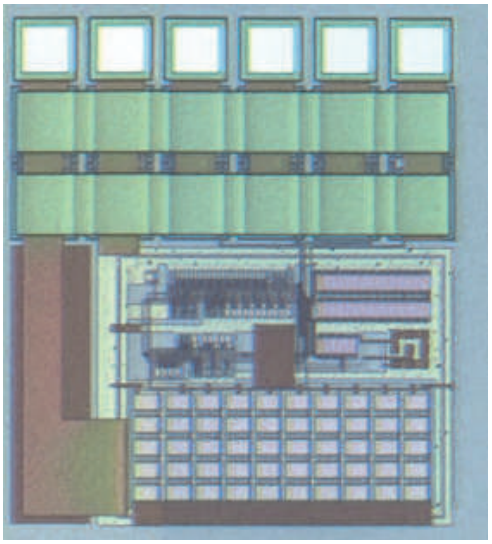

Fig. 16. Die photo of the proposed bandgap reference

Figure 17 shows the test image of the proposed bandgap reference when its supply voltage is 5V. On this typical working condition, the whole supply current is 6.87μA, including the voltage buffer, whose current is 3.6μA.

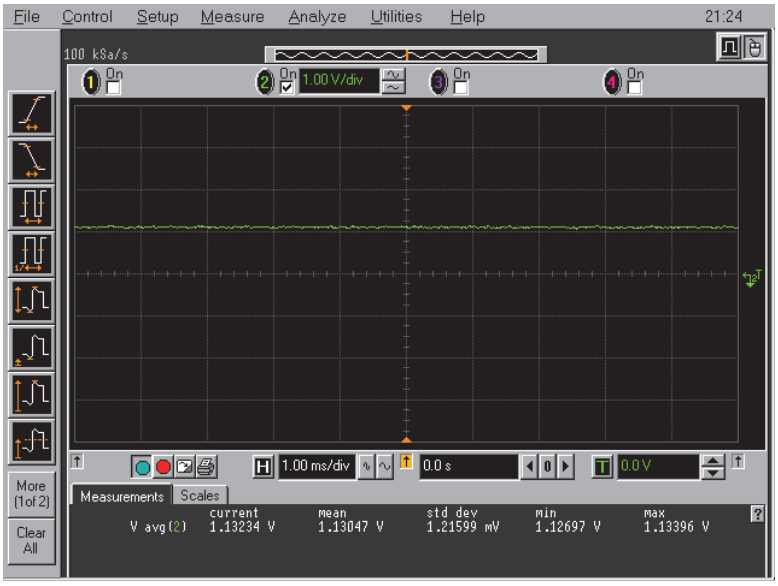

Fig. 17. Test image of the proposed bandgap reference

Figure 18 shows the output voltage characteristics of the proposed bandgap reference under different temperature. The measurement result shows the temperature coefficient is about 88.9ppm/°C at the range from 10°C to 100°C.

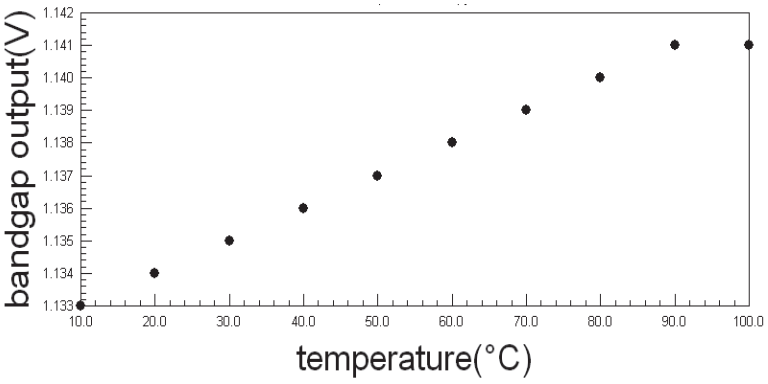

Fig. 18. Output voltage of the proposed bandgap versus temperature

Figure 19 shows the output voltage characteristics of the proposed bandgap reference under different power supply voltages. When the supply voltage changes from 3V to 11V, the output voltage of bandgap reference circuit varies about 0.875mV/V.

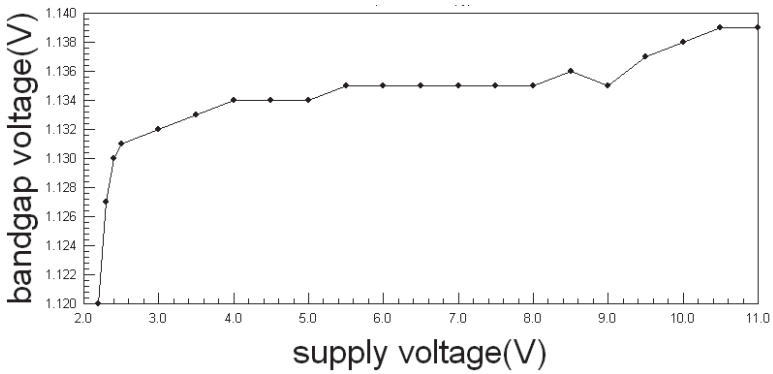

Fig. 19. Output voltage of the proposed bandgap versus supply voltage

In this system, one of the most important specifications is power consumption. All the power consumption listed below includes the power consumption of the voltage buffer. Table 2 shows the current consumption of the proposed bandgap reference at different temperature. With temperature increasing, the power supply consumption of the bandgap increases. Table 3 shows the current consumption of the proposed bandgap reference at different supply voltages. With increase of the supply voltage, the proposed circuit consumes more supply current. And the leaking current caused by PAD has been added to the total current consumption.

Temperature(°C)	10	20	30	40	50	60	70	80	90	100
supply current(μA)	6.81	6.87	6.95	7.12	7.37	7.62	7.96	8.33	8.71	9.12

Table 2. Current consumption of the proposed bandgap reference at different temperature

supply voltage(V)	3	4	5	6	7	8	9	10	11
supply current(μA)	6.54	6.71	6.87	7.04	7.26	7.62	8.14	8.79	10.56

Table 3. Current consumption of the proposed bandgap reference at different input supply voltage

This is a summary of the measurement results of the proposed bandgap reference. A bandgap working in sub-threshold region is proposed and measurement results have been shown in this paper. A voltage buffer working in saturation region has been added to increase the drive capacity of the proposed bandgap reference. When the supply voltage is 5V and at room temperature, the supply current is 6.87μA, including a voltage buffer whose current consumption is 3.6μA. The temperature co-efficiency can reach 88.9ppm at the range from 10°C to 100°C at the condition when supply voltage is 5V. And the line regulation can reach 0.875mV/V when supply voltage varies from 3V to 11V at room temperature. This design can be used widely in the power management unit in energy harvesting systems working in intermittent mode.

5.2 Variable step-down ratio SC converter's measurement results

The SC converter circuits have been taped out at the process of 0.35 μm CMOS process with EEPROM technology, provided by Chartered Corporation. The micrograph of the proposed DC-DC converter is shown in figure 20. The size of core circuit is 600 μmx800 μm[23].

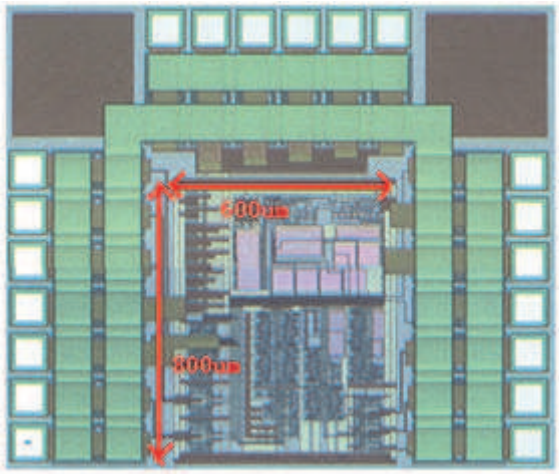

Fig. 20. The Micrograph of the proposed DC-DC converter

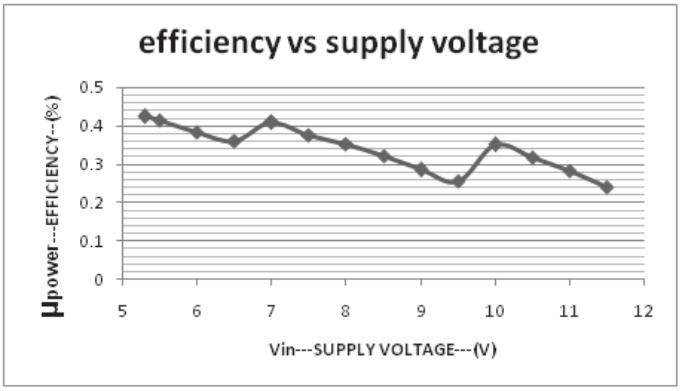

Fig. 21. The measured power converter efficiency varies with different input voltages.

It presents the measured power converter efficiency versus input voltage with the maximum load current in figure 21. The measured curve shows that the converter efficiency decreases with input voltage before changing the step-down conversion ratio. When the input voltage just exceeds the threshold voltage, the step-down conversion ratio is set to be maximum 2/3. With the input voltage increasing, the converter efficiency goes down, because system energy loss increases with supply voltage. When the input voltage reaches to the settled value, the ratio turns to 1/2 and efficiency bounces up because its no-load output voltage is closer to the load voltage desired. It also happens when the ratio changes

from 1/2 to 1/3. The maximum efficiency occurs when the input voltage is 5V. It shows the waveform of output voltage and stacked clock in different step-down conversion ratios with the same load in figure 22. The higher input voltage is, the shorter converter works for in a period.

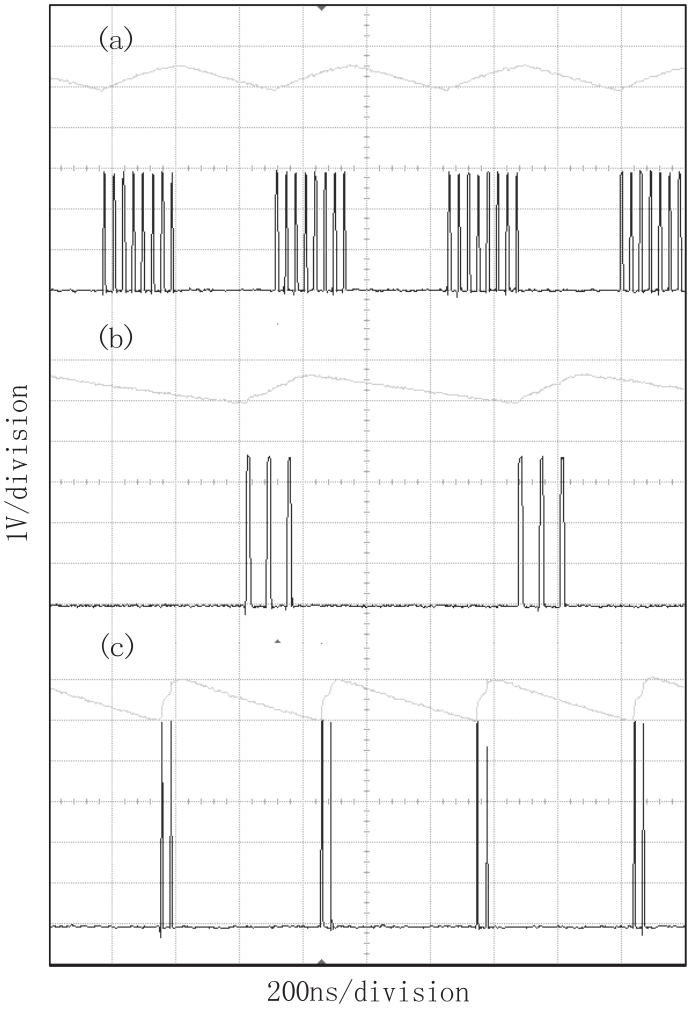

Fig. 22. The waveform of output voltage and stacked clock in different step-down conversion ratios (a) VDD=5.5V, ratio=2/3; (b) VDD=7V, ratio=1/2; (c) VDD=11V, ratio=1/3

Table 4 presents the whole circuit's performances. Measurement results show that the DC-DC converter can dynamically scale the charged capacitor supply from 5~15V to 2V and supply at least 560μA. The converter efficiency of SC converter can reach 61%, and the efficiency of the whole system is ranged from 28% to 42%, which is much higher than 17.6% in [6] and 19% in [5].

Symbol	Parameter	Testconditions	Min	Typ	Max	Units
Vin	Supply voltage	T=+27°C	5.3	9.5	14	V
Vout	Output voltage	RL=3.85KΩ	1.8		2.2	V
Iout	Supply current	5.5V<Vin<7.5V, RL=3.85KΩ		560		μA
		7.5V<Vin<11.5V, RL=3.85KΩ		580		
		11.5V<Vin<14V, RL=3.85KΩ		660		
Is	Quiescent Supply current	Iout=0mA	143		240	μA
fosc	Oscillator frequency			1	1.3	MHz
η1	SC Circuit efficiency	T=+27°C	49		61	%
η2	Total power efficiency	T=+27°C	28		42	%
Vpp	Output voltage ripple	RL=4KΩ	460		864	mV

Table 4. Measurement results of the variable step-down SC converter

This is a summary of the measurement results of the variable step-down ratio SC converter. A variable step-down conversion ratio switched capacitor DC-DC converter has been presented here to advance the converter efficiency of charge on the stored capacitor in a Wireless Monitoring System of Orthopedic Implants. The proposed converter works in intermittent mode to efficiently regulate from 15V down to approximately 2V. The SC topologies can be switched automatically to keep efficiency high over the entire supply voltage range. Stacked switches technique is also used to reduce leakage current in switching process of SC DC-DC converter. The whole converter efficiency can reach 42% including all auxiliary components' power consumption, which is far higher than previous work. This DC-DC converter could also be used in other similar intermittent energy harvesting systems.

5.3 LDO's simulation results

Table 5 shows LDO circuit's performances. Line regulation, load regulation and PSRR are important parameters for LDO design. LDO is expected to output a constant voltage even

if input voltage changes a lot. Line regulation is such a measure of the ability of the power supply to maintain its output voltage given changes in the input line voltage. Usually it is simulated by changing input voltage at the range from low power supply to high power supply using DC analysis method. In the same way, LDO is expected to output a constant voltage even if load current changes a lot. Load regulation is a measure of the ability of an output voltage to remain constant given changes in the load. And it is simulated by sweeping load current from small load current to high load current using DC analysis method. PSRR shows the ability of an output voltage to prevent noise from power supply noise. It has become an important parameter because digital circuits and analog circuits have been integrated in a single chip. Switching noise from digital circuits will greatly affect the performance of analog circuits through power supply. For example, in this design, SC converter will bring much supply noise, so PSRR is a very important parameter.

	condition	***typical***	***ff***	***ss***
Line regulation	2V<input voltage<3V	122.99μV	144.99μV	99.16μV
Load regulation	1mA<load current<5mA	180.99μV	170.73μV	207.30μV
PSRR	input voltage =2V	41.96dB@1MHz 71dB@10kHz	43.05dB@1MHz 73dB@10kHz	43.06dB@1MHz 72dB@10kHz

Table 5. Simulation results of LDO circuit

Figure 23(a) shows the dynamic response of LDO when input voltage changes between 2V and 3V in 1μs. Figure 23(b) shows the dynamic response of LDO when load current changes between 1mA to 5mA in 1μs.

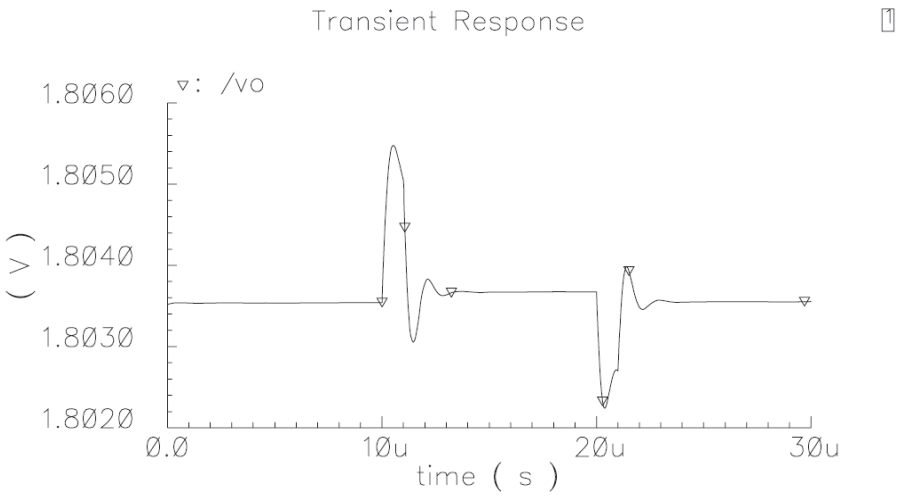

Fig. 23a. Dynamic response of input voltage

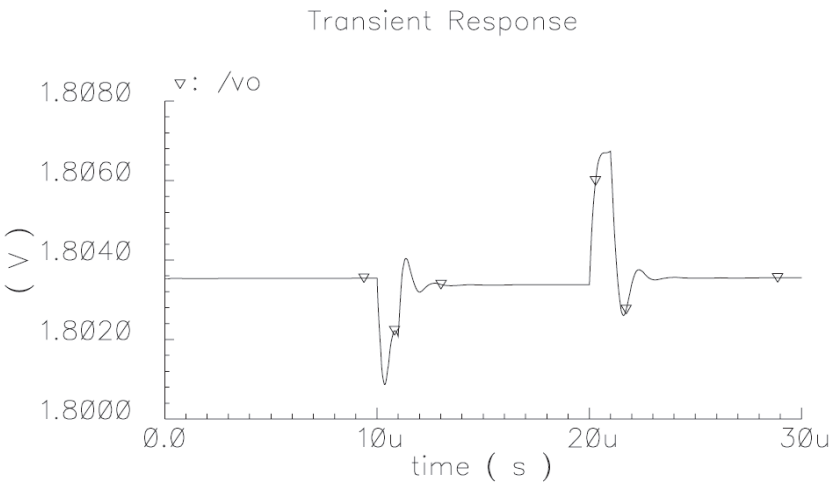

Fig. 23b. Dynamic response of load current

As is known, the efficiency of LDO is given by the product of output voltage and output current divided by the product of input voltage and input current. In this design, output voltage is 1.8V and input voltage ranges from 2V to 3V; output current is 1mA and input current is the summary of output current and the quiescent current of error amplifier, which is about 20μA. So, the efficiency of LDO ranges from 58.8% to 88.2%. If input voltage is settled less than 2.2V, then the efficiency can be larger than 80.2%.

In summary, the efficiency of whole system can be achieved by the product of the SC's efficiency and the LDO's efficiency. These components(including SC converter and auxiliary components) are working in high voltage region. According to the efficiency of the SC converter ranges from 49% to 61%, the efficiency of these parts working in high voltage region ranges from 28% to 42%. Assuming the efficiency of the LDO is 80%, the efficiency of the whole system is ranged from 22.4% to 33.6%, which is higher than 8.8%[5], 17.6%[6], 19%[4].

6. Conclusion

Based on the electrical circuit model, this paper chooses a proper storage capacitor for PZT generator. To improve converter efficiency of whole system, a hybrid DC-DC converter is proposed. A low power bandgap reference circuit working in sub-threshold region is also presented in order to reduce the power consumption of auxiliary circuits in this power system. When the supply voltage is 5V and at room temperature, the supply current is 6.87μA, including a voltage buffer whose current consumption is 3.6μA. The temperature co-efficiency can reach 88.9ppm at the range from 10°C to 100°C at the condition when supply voltage is 5V. The proposed variable step-down SC converter works in intermittent mode to efficiently regulate from 15V down to approximately 2V. The SC topologies can be switched automatically to keep efficiency high over the entire supply voltage range. Stacked switches technique is also used to reduce leakage current in switching process of SC DC-DC converter. The whole converter efficiency can reach 42% including all auxiliary components'

power consumption. A LDO circuit is proposed and the efficiency of LDO ranges from 58.8% to 88.2% under different input voltage. Assuming the efficiency of the LDO is 80%, the efficiency of the whole hybrid converter is ranged from 22.4% to 33.6%, which is higher than previous work. And the proposed hybrid power management system working in intermittent mode could also be applied in other similar energy harvesting systems.

7. Acknowledgment

The author would like to thank Wenhan Hao, Hong Chen, Chun Zhang for their many contributions to this work.

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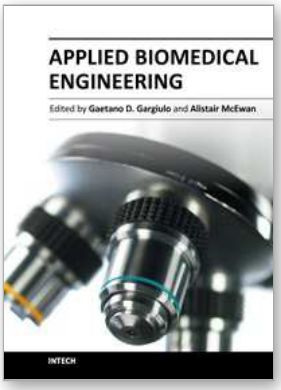

Applied Biomedical Engineering
Edited by Dr. Gaetano Gargiulo

ISBN 978-953-307-256-2
Hard cover, 500 pages
Publisher InTech
Published online 23, August, 2011
Published in print edition August, 2011

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