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Integrated Sensor Electronic Front-Ends with Self-X Capabilities

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Abstract: The ongoing vivid advance in integration technologies is giving leverage both to computing systems as well as to sensors and sensor systems. Both conventional computing systems as well as innovative computing systems, e.g., following bio-inspiration from nervous systems or neural networks, require efficient interfacing to an increasing diversity of sensors under the constraints of metrology. The realization of sufficiently accurate, robust, and flexible analog front-ends (AFE) is decisive for the overall application system and quality and requires substantial design expertise both for cells in System-on-Chip (SoC) or chips in System-in-Package (SiP) realizations. Adding robustness and flexibility to sensory systems, e.g., for Industry 4.0., by self-X or self-* features, e.g., self-monitoring, -trimming, or -healing (AFEX) approaches the capabilities met in living beings and is pursued in our research. This paper summarizes on two chips, denoted as Universal-Sensor-Interface-with-self-X-properties (USIX) based on amplitude representation and reports on recently identified challenges and corresponding advanced solutions, e.g., on circuit assessment as well as observer robustness for classic amplitude-based AFE, and transition activities to spike domain representation spiking-analog-front-ends with self-X properties (SAFEX) based on adaptive spiking electronics as the next evolutionary step in AFE development. Key cells for AFEX and SAFEX have been designed in XFAB xh035 CMOS technology and have been subject to extrinsic optimization and/or adaptation. The submitted chip features 62,921 transistors, a total area of 10.89 mm^2 (74% analog, 26% digital), and 66 bytes of the configuration memory. The prepared demonstrator will allow intrinsic optimization and/or adaptation for the developed technology agnostic concepts and chip instances. In future work, confirmed cells will be moved to complete versatile and robust AFEs, which can serve both for conventional as well as innovative computing systems, e.g., spiking neurocomputers, as well as to leading-edge technologies to serve in SOCs.

Keywords: analog-front-ends (AFE); self-X properties; universal/generic sensor interfaces; imperfect/robust observers; extrinsic/intrinsic optimization; spike-domain information presentation; adaptive spiking AFEs

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Citation: Alraho, S.; Zaman, Q.; Abd, H.; König, A. Integrated Sensor Electronic Front-Ends with Self-X Capabilities. *Chips* **2022**, *1*, 83–120. https://doi.org/10.3390/chips1020008

Academic Editor: Gaetano Palumbo

Received: 27 June 2022
Accepted: 5 August 2022
Published: 12 August 2022

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1. Introduction

The unabated surging advance in micro/nano integration and packaging technologies [1,2], and the associated advent of both a plethora of novel sensory concepts and technologies [3] and a new generation of integrated standard or reference elements (e.g., NIST-on-a-Chip, NoaC [4]) have made increasingly complex and powerful yet affordable integrated computing systems a reality. Allied with advanced information-processing technology, commonly referred to these days as AI technology, the creation of smart or increasingly cognitive pervasive systems has become feasible for an increasing domain of applications. Recent application fields include (I)IoT, AIoT, CP(P)S, Industry 4.0 [5], automation,

autonomous driving, wearable electronics, AAL/healthcare assistance systems, point-of-care-systems, etc. The aspired cognitive integrated sensory systems (CISS) for the named application fields (among others) must meet the constraints of cost effectiveness, consistent modeling, simulation and rapid design of heterogeneous systems, packaging/3D-integration issues, effective wireless or other communication, node localization, energy efficiency, and energy harvesting in their design. This already requires efficient design automation techniques from circuit and layout synthesis to automated learning or optimization of deep neural networks, e.g., [6], in particular, in their contemporary hardware manifestation [7–10], or of hybrid intelligent systems [11–15] (see Figure 1) The extrinsic optimization goals here are in finding at design time a new solution for a new problem or tune a solution to a changed problem.

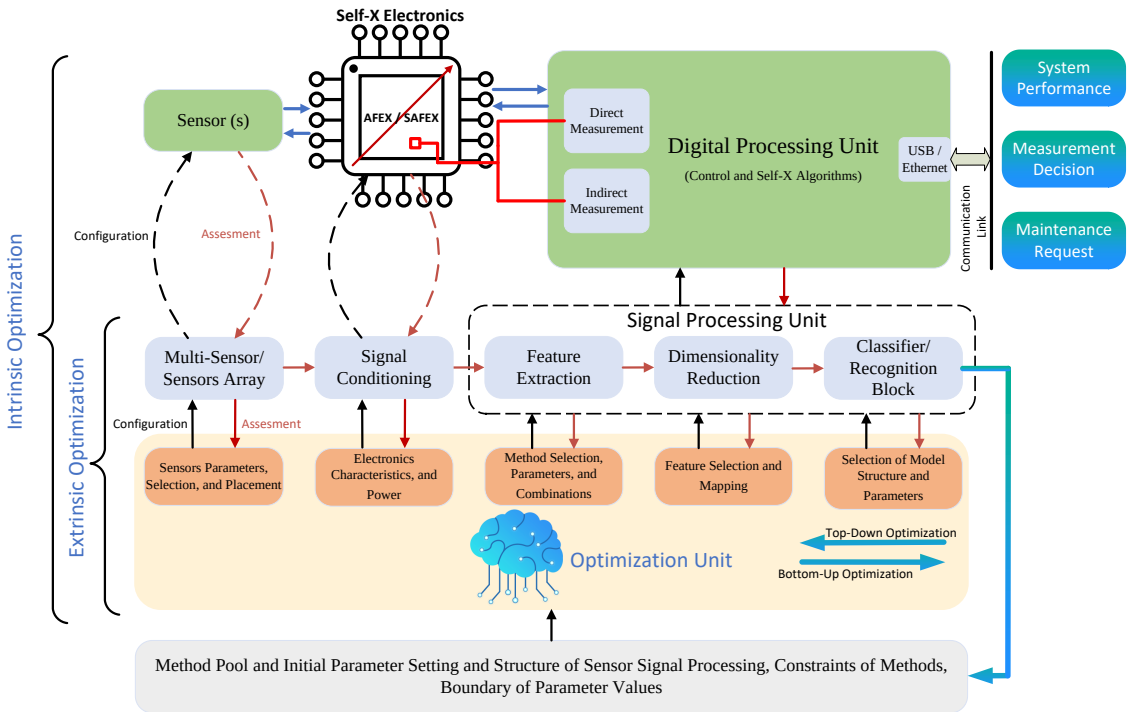

Figure 1. Hybrid intelligent system design for CISS based on extrinsic and intrinsic optimization.

In addition to the design goals, long-term system reliability, dependability, accuracy, and guaranteed uncertainty are of paramount importance. The robustness and adaptivity met in natural beings to perform in a noisy, hostile, and changing environment on an individual level and the evolutionary development on population level are properties envied and coveted by engineers for decades. However, it must be remembered that technical systems do not have a metabolism and observed regrowth of lost cells, tissues, limbs, or even a whole entity in, e.g., axolotl salamanders or planarians, and can, as of yet, only be rivaled to the extent of the redundancy supplied at manufacturing time.

Complementing activities of addressing the latter issues in the design phase (e.g., with yield optimization in mind, such as MUNEDA's WiCkeD [16]), and at a later stage in the product life cycle by repeated calibration steps, more recently the realization of life-like features in technical systems, i.e., based on so called self-X or -* features, such as self-monitoring, -calibration, -trimming, -repairing, -healing, and the self-correction of each instance, become the focus of the evolution of technical systems on all levels [17–20]. This gives rise to growing and novel design challenges from the automated design of CISS and related system, both for hybrid or deep neural architectures, with a run-time with intrinsic optimization by reconfiguration and/or adaptation [12,14] (see Figure 1).

Particular emphasis is exerted on a suitable electronics design, as the lowest and decisive system level in a self-X hierarchy (see Figure 2). In particular, integrated solutions

can benefit greatly from the realization of such an approach, as the costly one-by-one discrete calibration of systems will be replaced by an in-built redundancy, reconfiguration and correction features based on adaptation or learning/optimization techniques on various levels of abstraction. One prominent industrial example is the research of Synopsys, including the former work from Moortec, with Silicon Lifecycle Management (SLM) based on in-built sensing devices and corresponding control loops in their complex chips (SoCs) along with long-term data collection [21–24].

For CISS, sensors and sensor electronics, embodied by so-called analog front-ends (AFEs), are of major importance. Consequently, in the field of evolvable hardware (EHW) numerous approaches for robust, fault-tolerant analog and mixed-signal systems, extended by sensors, can be found, e.g., the work of Stoica et al. [25]. Related applicable concepts are, thus, established and can be extended by including sensors themselves with the help of auxiliary integrated actuation electronics in the named control loops [26,27]. The purpose of self-X approaches mainly focuses on upkeeping the functionality of a once achieved system under challenges of drift, aging, lesions or damage.

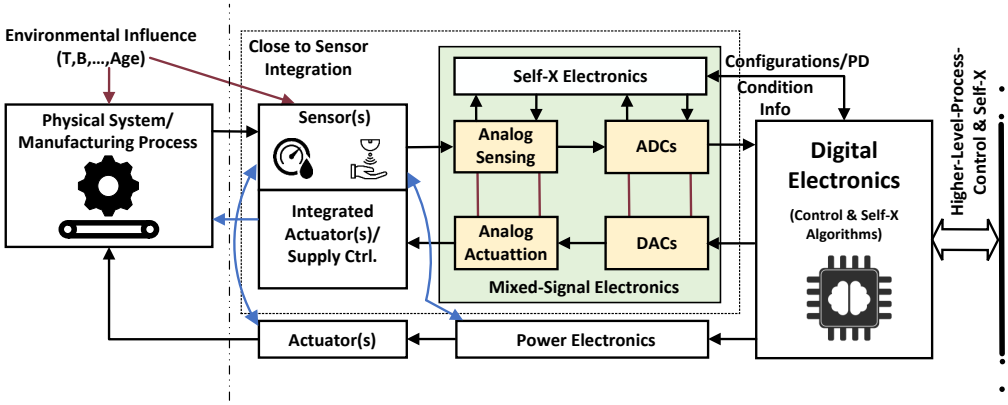

Figure 2. Sensors and sensor electronics as lowest level of self-X hierarchy.

One interesting and crucial point, which is also part of the design and result section of this paper, is the issue and realization of the observer required in the control or optimization loop, commonly established from the same 'fallible flesh' as the monitored circuits themselves. Numerous application works bypass this issue by using monitoring devices, e.g., ADCs, of better resolution and quality, than the monitored systems itself features, for instance in [28]. This actually is impractical, as for a viable system realization, the observer must be of the same make or origin as the remaining entity. Here, a relation to immune systems in general, and artificial immune systems in particular [29–33], can be observed.

Further, in modern, leading-edge integration technologies, classical analog design based on amplitude-domain information representation faces challenges that are increasingly difficult to overcome. One escape route is to follow the natural evidence once again by representing the information in the time, frequency, or spike domain, e.g., for light sensing in [34] or the Dynamic Vision Sensor (DVS) of Delbrück et al. from 2005 (see, e.g., [35]).

Time-to-digital converters have successfully established themselves [36]. Spiking AFEs (SAFEs) with adaptation features embedded in the same self-X concepts given above for their conventional counterparts are a promising and potentially technology-agnostic direction of development [37,38], interfacing to both conventional and neuro-inspired computing systems (see Figure 3).

The goals of this paper are to contribute to established amplitude-domain representation AFEs with self-X features and an emphasis of a robust and inobtrusive observer as well as a minimum of effective reconfiguration parameters, low-cost performance evaluation set-up, and optimization techniques. After a brief survey of existing AFEs, including several chips and systems of our group in Section 2, the named concepts for improved AFE with self-X properties will be described as one part of a new chip design in Section 3.

Further goals target on moving from a vulnerable amplitude domain to a robust spike-based representation of sensory information and ensuing adaptive processing. This will be outlined in Section 4 for the case of a particular adaptive neural ADC as the second part of the mentioned new chip design. In Section 5, details of the chip design and the prepared corresponding prototype system will be disclosed and discussed. In conclusion, a balance of the achieved goals and on future plans and work for robust, technology-agnostic AFEs as a base level of a self-X hierarchy will be presented.

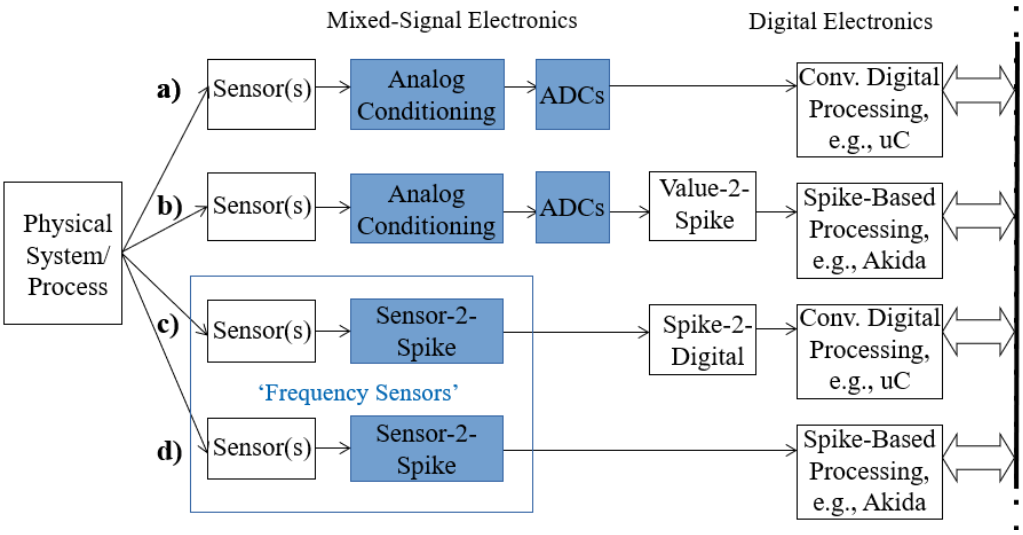

Figure 3. AFEs with Self-X capabilities for both conventional and neural computing systems.

2. Survey of AFE in Industry and Research with Self-X Extension

The decisive front-end functionality has observed a realization in different complexity and scope for industrial sensor electronics and research activities, in particular, on reconfigurable analog and mixed-signal arrays, partly with self-X extension. A most recent example is given, e.g., in [39]. Two distinct approaches can be found in the history of the field. The first one relates to fault-tolerance and circuit creation or synthesis in the widest sense and is primarily pursued in the fields of *Evolvable Hardware* and *Evolutionary Electronics* based on reconfigurable analog arrays, predominantly on transistor level granularity [40–48], combined with algorithms of evolutionary optimization to configure and reconfigure the degrees of freedom of the given hardware for continued goal or specification fulfillment [19,20,49–64]. These approaches allow both the compensation of static instance issues, e.g., defects and mismatch from manufacturing, as well as dynamic compensation of temporal phenomena such as drift, aging, or damage of defect suffered in electronics' service time. Exploiting this approach for sensory electronics has also been investigated in our group in, e.g., [28,65,66] based on two chips with reconfigurable OpAmps and InAmp in austriamicrosystems 0.35 µm CMOS technology and PSO-based optimization under the ideal observer assumption. One of the chips was employed by Tawdross in an intrisic evolution approach to both compensate static and dynamic issues by continuous self-monitoring and -reconfiguration.

In the second one, rapid-prototyping and genericness of system solutions and the AFE for interfacing a plethora of different sensors is in the focus on the level of cell level granularity, which substantially reduces the degrees of freedom to be implemented and determined by optimization. In general, in the industrial electronics community with prevalent amplitude-domain representation, the rich degree of freedom in transistor level-granularity was and is viewed as largely unrealistic due to excessive resource consumption, e.g., chip area, and side effects due to the additionally introduced parasitics. Thus, in commercial designs, only a minimum use of reconfiguration capabilities and related tuning can be found. Commonly, offset and gain issues are tackled, e.g., in instrumentation

amplifiers denoted as DigiTrim in [67], both for deviation compensation and optimum fitting measurement signal to ADC input, denoted as *Zooming ADC* [68]. Moreover, power consumption and related vigilance reconfiguration have observed implementation, e.g., by programming the vertical currents in decisive parts of the amplifiers. Last not least, additional functionality for electronics and sensor temperature tracking and related compensation can be found, e.g., in [68–78].

More flexibility and complete AFE functionality was provided by Field-Programmable-Analog-Arrays (FPAA), e.g., relevant FPAA commercial examples [79–84] and research examples [85–95], and representative AFE implementations [96–101].

As can be observed, a plethora of activities in the field has and is taking place, but linking these activities to self-X concepts and architecture is less common, e.g., in [102–105]. Thus, motivated from the obvious need in sensor and measurement systems, instrumentation, automation, IoT, and Industry 4.0, we pursued research on advanced sensor interfaces or AFEs, both generic or universal, to deal with a rich collection of relevant different sensor principles and add self-X features to these AFEs, both for stand-alone use as well as being part of a more complex self-X hierarchy, as outlined in the introduction.

For the research demonstration, magneto-resisitive sensors were selected, e.g., AMR and TMR, from the xMR options. These also offer integrated or embedded actutation devices, e.g., flip and compensation coil in the case of AMR 755b Sensitec sensors, which allows one to instantiate the self-X concepts outlined in Figure 2 with regard to including both electronics and sensors in Self-x loops as evolved and reported in [26,27]. The first chip in the family of *Universal-Sensor-Interface-with-self-X- properties* (USIX) was designed by Rober Freier [106] in austriamicrosystems 0.35 µm CMOS technology. The simplified block diagram of the USIX 1 chip is shown in Figure 4.

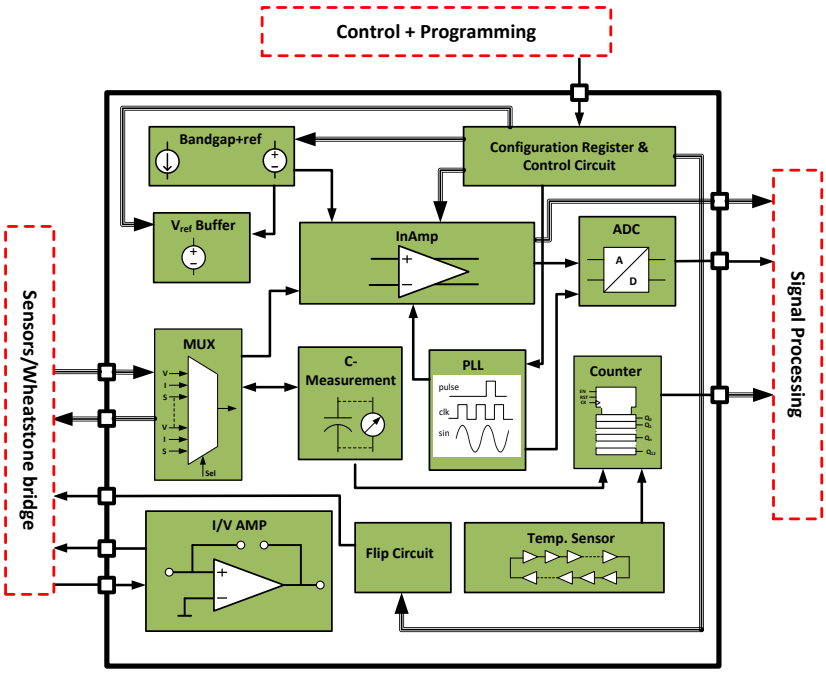

Figure 4. Simplified block diagram of the USIX 1 chip (Adapted from: [106]).

The key features are the general reconfigurability of both connectivity and analog properties as well as actuation options, e.g., the flip current control for AMR chips. Sensor sensitivity could be self-monitored, and, in case of a saturation issue, restored by a flip cycle (self-healing).

Figure 5 shows a chip photo of the fully functional design from [106]. It has observed demonstrator implementation with a dedicated Arduino set-up and applied to

activities such as foodscanner development, e.g., Lab-on-Spoon realization by USIX employment [107].

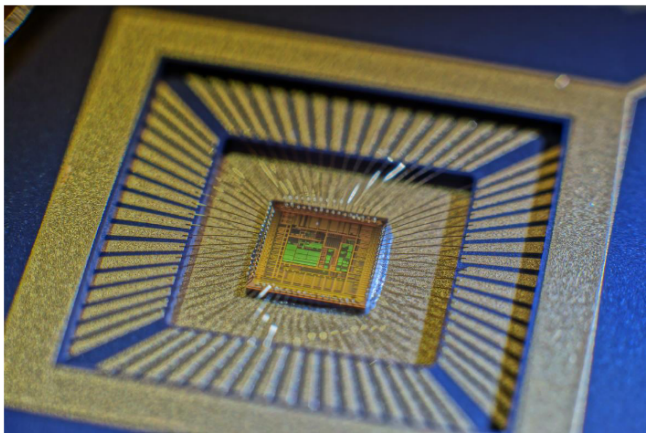

Figure 5. Chip photo of the USIX 1 chip (Reproduced with permission from Robert Freier: [106]).

The diagnostic capability and the improved integration in self-X optimization loops were open issues for that chip generation and lead to the USIX 2 chip designed by Kammara, Chinazzo, and Dobariya, as well as Gräf for the corresponding demonstrator setup [27]. The chip was also designed in austriamicrosystems 0.35 µm CMOS technology and featured 18 mm^2 area and more than 50 k transistors. The corresponding block diagram of the USIX 2 chip is shown in Figure 6.

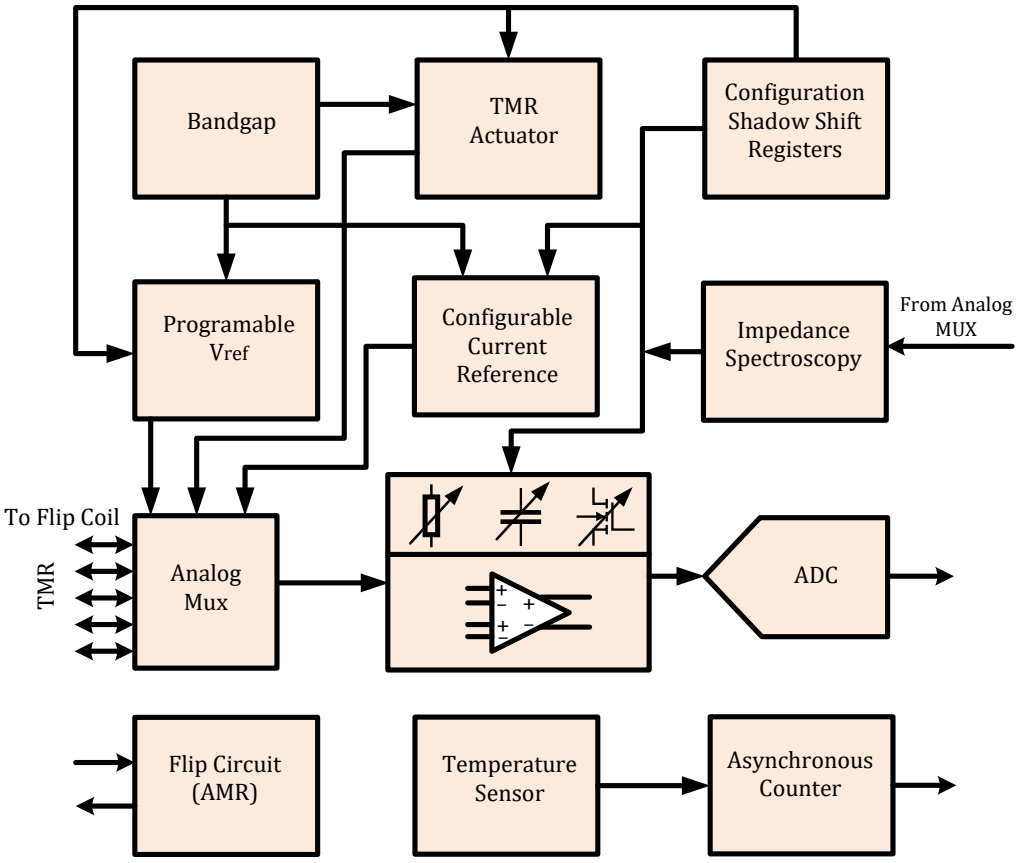

Figure 6. Simplified block diagram of the USIX 2 chip.

The USIX 2, shown in Figure 7, was enriched with features such as TMR reset actuation, more flexible connectivity generation, hotswap from up to four stored configurations, and

first extension steps towards integrated impedance spectroscopy [108], which can serve both as a measurement principle for itself or for sensor diagnosis in advanced self-monitoring.

Unfortunately, the complexity of the design under tight project timing constraints led to two major design issues, rendering the chip, beyond the simulation results, not useful in practical measurement. Though the issues were localized and a repair with the *Focused-Ion-Beam* (FIB) method from NSC at TU Kaiserslautern was tried, it unfortunately did not lead to testing success.

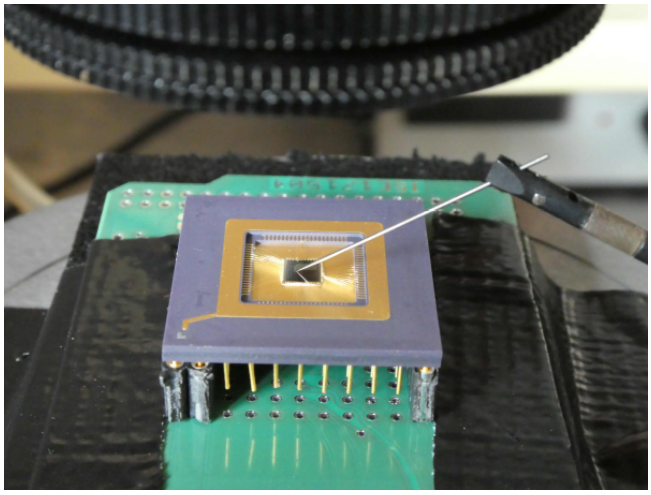

Figure 7. Photo of the USIX 2 chip on the wafer prober with test needle on FIB repair location.

In both USIX chips, several relevant technical problems for AFEs with self-X properties have not found a comprehensive and sufficiently complete answer yet. In the light of the design issues that unfortunately occurred in the USIX 2, the focus was shifted from providing a complete USIX 3 chip to elaborating in more detail solutions and advance for crucial cells and components in XFAB xh035 µm CMOS technology, validate those by a more modest design, as detailed in Sections 3 and 5, and in a following step, use the validated key cells to compile a complete USIX 3 chip. The main important issues relate to determining the minimum number and optimum location of tuning knobs, improvement of optimization techniques in the self-X loops, and last but not least, tackling imperfections and obtrusiveness in the optimizer/observer [109–119] in the named self-X loops.

Undergoing the transition from the vulnerable amplitude-domain to inherently more robust time-, pulse-, or spike-domain for future robust and technology agnostic AFEs was concurrently pursued in our group, e.g., reported in [38] with a focus on the sensor to digital conversion step and the target to integrate in the self-X-architecture described above. A first converter chip for a spiking AFE was designed by Kammara [38], as well as in the austriamicrosystems 0.35 µm CMOS technology, and the basic functionality could be confirmed from these chip samples. In Sections 4 and 5, the follow-up work including adaptation mechanisms, and their circuit embodiment will be presented and discussed.

3. Amplitude Domain AFEs with Self-X Extension

This section will present the principle of the sensor analog interfacing in the amplitude domain that belongs to part (a) of Figure 3. The major update of the recent work from the former USIX 1.0 and USIX 2.0 can be outlined in four perspectives:

- The introduction of the fully differential analog circuits.
- The limitation of the reconfigurable circuit elements to the sensitive components only.
- The incorporation of cost-effective system performance evaluation setup based on indirect measurement methods to support the automatic test equipment (ATE).
- Alleviation of the observer uncertainty, mainly due to imperfections of the sensor and/or ADCs.

The updated concept helps to reduce the overhead of implementing the self-X sensory electronics, as presented in Figure 2, which provides the possibility of achieving higher dynamic system performance due to reduction of the circuit parasitics and relaxation of the requirements of the system performance evaluation unit.

3.1. Instrumentation Amplifier

The instrumentation amplifier (in-amp) is the critical component of the AFE for signal conditioning in the amplitude domain for the sensors' interface and readout circuitry [120,121]. Compared to the operational amplifier (op-amp), the main features of the in-amp are the high input impedance and common-mode rejection ratio (CMRR), making it the best choice for conditioning weak sensor signals in a noisy environment [122]. There are three major topologies for realizing the in-amp circuits [123]; those are the capacitive coupling chopper-stabilized in-amp (CCIA) [124,125], the conventional three op-amps based in-amp, and the indirect current-feedback in-amp (CFIA) [126–128].

The CFIA utilizes the active feedback amplifier topology (AAF) [129], also known as a differential-difference amplifier (DDF) [130]. Thus, it benefits from high input impedance, high open-loop DC gain, and wide bandwidth [120,131–133]. The CFIA is more area and power-efficient than 3-opamp in-amp because the input transconductance stages share the same output driver stage [121]. The CFIA's key feature is that the common-mode voltage of the input stage is separated and isolated from the common-mode voltage of the feedback stage by utilizing two balanced differential stages [134]. Therefore, it is possible to direct the couples' sensors having a common-mode voltage distinguished from the CFIA output common-mode voltage without additional isolation or coupling techniques [129,135]. The input and feedback transconductance convert the voltage signals to current signals and reject the common-mode voltage, thus leading to higher CMRR than the 3-opamp in-amp [128,136–138]. The mismatch in the feedback resistor results only in a closed-loop gain error [139] and does not affect the CMRR performance.

Depending on the input stage type (NMOS or PMOS), the ability of the CFIA to amplify sensors' voltages that approach either of the CFIA supply rails makes it suitable to condition universal types of sensors and measurements, e.g., current sensing measurements [140,141], strain gauges [142], biomedical signals interface [139], micro-electro-mechanical systems (MEMS) interface [143,144], magnetic field sensor interface [27,145,146], electrical impedance spectroscopy (EIS) [147,148], etc. However, the CFIA suffers from two issues relevant to the DDF core amplifier; the first one is the gain inaccuracy error because of the mismatching between the input and feedback transconductance [140]. Therefore, the same type of differential transistors with extra care on layout matching has to be taken during the physical implementation; also, by using cascaded biasing currents, a better degree of matching can be accomplished [121]. The second issue is due to the limited input differential range of the input transconductance in open loop configuration [130], which especially becomes a problem when interfacing high dynamic range sensors such as the magnetoresistive sensors [149] in small node CMOS technology where the dynamic input range is already reduced.

Classical linearization solutions can be found in the literature to extend the input differential range of the CFIA [150,151], but mostly tradeoff the amplifier dynamic performance, reduce the ICMR and boost the power consumption. An innovative solution to this problem was proposed in [152], which uses the advantages of fully differential signal properties and the method to apply the negative feedback to the input and feedback transconductance stages of the DDF to create a virtual short between each pair. We proposed in [153] a fully differential CFIA based on the last solution. The reported post-layout simulations remarked on a high dynamic performance to process a large differential voltage of 1.6 V_{p-p} and achieved a total harmonics distortion (THD) of 0.95% at a signal frequency of 5 MHz, while consuming only 2.55 mW and a layout area of 0.039 mm^2.

To support self-X properties, we introduced configuration capability to the sensitive elements of the CFIA circuit and to the elements having impact control over the circuit perfor-

mance, serving as the design tuning knobs [154], as depicted in Figure 8. The configurable elements are made of digitally weighted scalable arrays controlled by the configuration bits from the optimization algorithm unit. The gate of the unselected transistor from the PMOS array is shorted to V_{DD}; similarly, the NMOS array is shorted to GND. It is important to fully shutdown the unselected transistor and avoid partial conduction due to the residual charge saved at the floating gate capacitance. Hot-swappable multi-row register-based memory is used to save the configuration pattern and allows switching between different saved solutions for supporting in situ calibration. In the proposed approach, the circuit's critical devices were first identified based on the simulation results and by considering the process, voltage, and temperature (PVT) variations, while the remaining elements are fixed to their optimum designed values. Compared to the fine-granular approach [45], where every element in the circuit is made scalable, the proposed approach reached the required flexibility in terms of circuit calibrating or changing the circuit performance according to the signal requirements with the following advantages: (1) smaller design area; (2) fewer switches parasitics, which led to improving the dynamic performance of the circuit; (3) less configuration memory; and (4) faster optimization time.

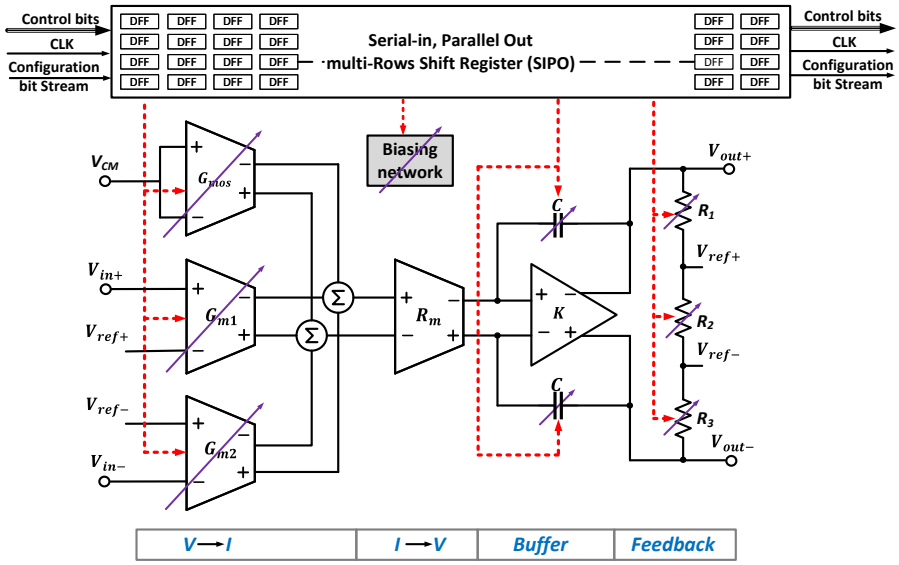

Figure 8. Reconfigurable fully-differential CFIA to support self-X properties.

Generally, the CFIA's gain-bandwidth product (GBW) is inversely proportional to the closed-loop gain (A_{CL}) [155,156] in the same fashion of the voltage-mode op-amps. Therefore, amplifying weak but high-bandwidth sensor signals demand high GBW [132], which costs more power dissipation. On the other hand, it is possible to only compensate the amplifier for the high A_{CL} using smaller compensation capacitors, which extends the CFIA bandwidth and the slew rate as well. Nevertheless, the amplifier might not be stable for low A_{CL}, especially for a unity gain buffer configuration that demands the highest compensation value. Our proposed design in [154] features GBW programmability by configuring the compensation capacitors according to the required stability of the selected gain. The gain can be programmed in eight levels, i.e., 1, 2, 4, 8, 16, 32, 64, and 128. Furthermore, by programming the biasing circuit, the −3 dB cutoff frequency (f_{-3dB}) can be tuned up to 250 MHz with unity gain configuration and to 0.5 MHz at $A_{CL} = 128$.

For precision amplification under high A_{CL}, an additional scalable transconductance stage (G_{mos}) with a scalable current source is added to the CFIA input stage to run the digital-auto zeroing (DOZ) task using the optimization algorithm. Compared to our former work implemented in [157], both minimized the offset voltage (V_{OS}) below 100 µV. However, the former design used switching-capacitor auto-zeroing, thus introducing the spikes' disturbance at the output. A total of 100 bits are used for the CFIA configuration. In the recent chip, the in-amp is further supported by an automatic digital offset calibration

scheme based on methodologies presented in [158–160], as shown in Figure 9. During the design, the statistical offset voltage (V_{OS}) of the CFIA is first concluded by running the Monte Carlo simulation with a large number of samples (500 samples) under extreme voltage, temperature, and process variation conditions. The autozeroing circuit is designed and added to the CFIA to cope with the obtained maximum absolute value of V_{OS}). Then, the MC is repeated because the autozeroing circuit itself can change the original value of the CFIA V_{OS}. The post-layout simulation gives a maximum V_{OS} of ±7 mV, while the designed automatic DOZ can treat V_{OS} up to ±14 mV. This should be enough to mitigate the additional offset due to the fabrication, packaging, and aging effect. During the calibration mode, the gain of the CFIA is set to the maximum (128). Therefore, the offset voltage of the digital loop control will be divided by this value. Figure 10 shows the offset correction under the imported worst statistical corner from MC samples. Considering the CFIA setup gain, the result proved the offset voltage down to 65 µV. The physical implementation of the complete circuit is shown in Figure 11, where the PMM stands for the power monitoring module, which will be discussed later.

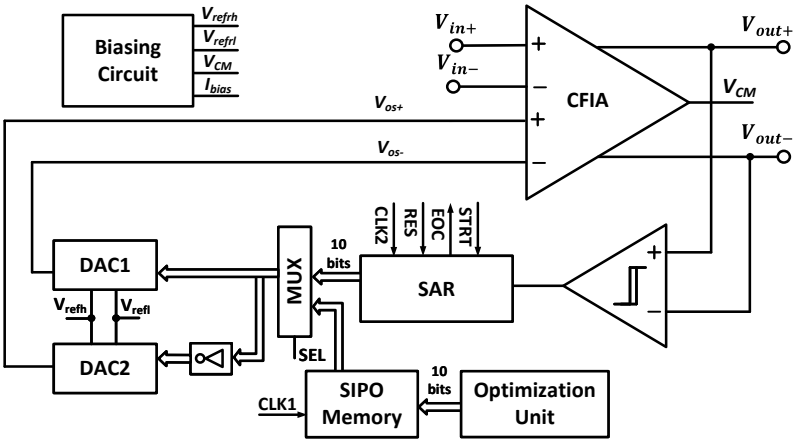

Figure 9. Proposed CFIA with programmable and automatic digital offset autozeroing.

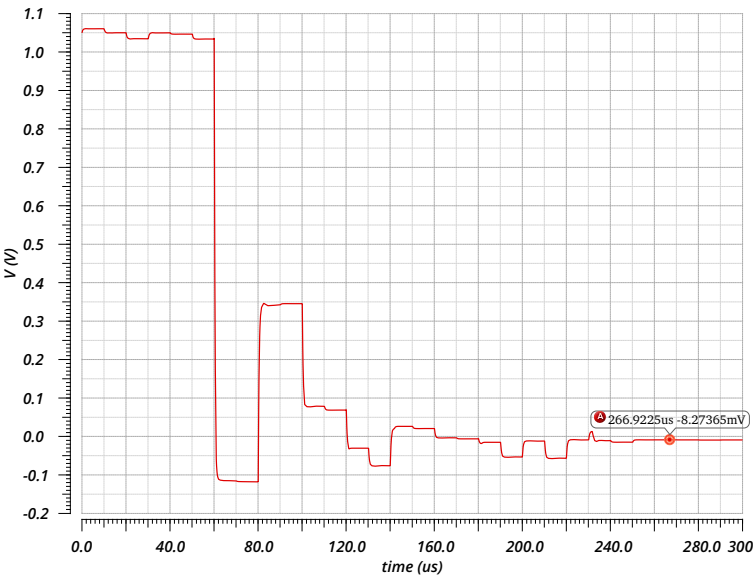

Figure 10. Digital offset autozeroing under worst statistical corner and CFIA gain equal to 128.

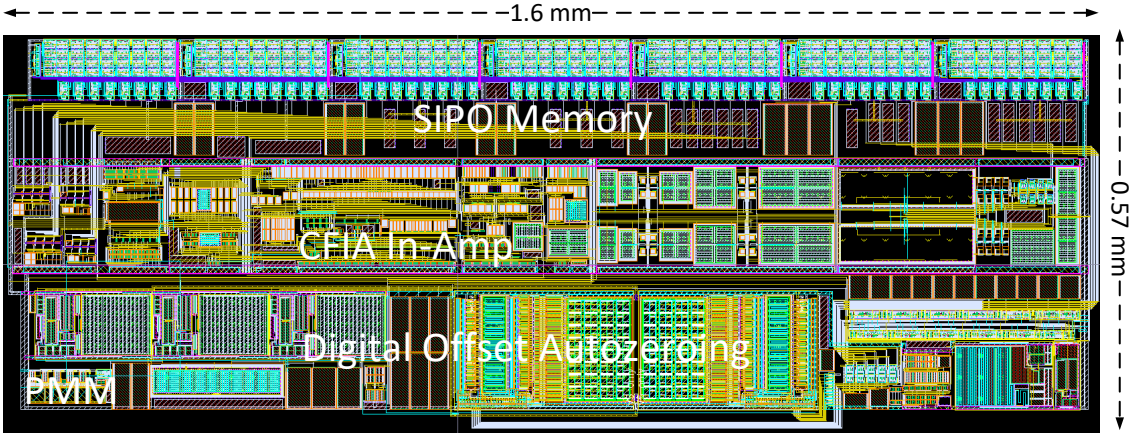

Figure 11. Layout implementation of the CFIA with the automatic digital offset automatic and power monitoring schemes.

3.2. Anti-Aliasing Filter

The anti-aliasing filter comes in the next stage of the signal conditioning chain after amplification to remove the signal noise from the Nyquist bandwidth prior the ADC converter stage. To support an extensive bandwidth range also required for EIS, we proposed in [161] a fully-differential fourth-order tunable continuous-time active low pass filter based on the Sallen–Key structure with Butterworth approximation. The post-layout simulations proved a frequency range from 30 Hz to 7 MHz with a resolution of 200 Hz, while the filter quality factor is fixed to the well-matched capacitor ratios. This range is achieved by modifying the MOS floating resistor from [162] and by varying the MOS-resistor biasing current from 50 nA to 30 µA, as shown from the schematic diagram in Figure 12. However, tuning the filter in this range is quite challenging to perform. A general optimization method can be followed, such as in [105,163] to tune the frequency bandwidth. To reduce the measurement cost of the optimization process, we proposed the indirect measurement principle based on non-intrusive sensors in our chip, as will be discussed next. The core amplifier of the presented filter is the fully-differential DFF used in the design of the CFIA. A modification is worked around to reduce the amplifier output resistance as required by the Sallen–Key topology and also to extend the GBW up to 250 MHz to cope with the required filter frequency. The filter circuit's physical implementation, including the programmable biasing current unit and the additional sensors, is shown in Figure 13.

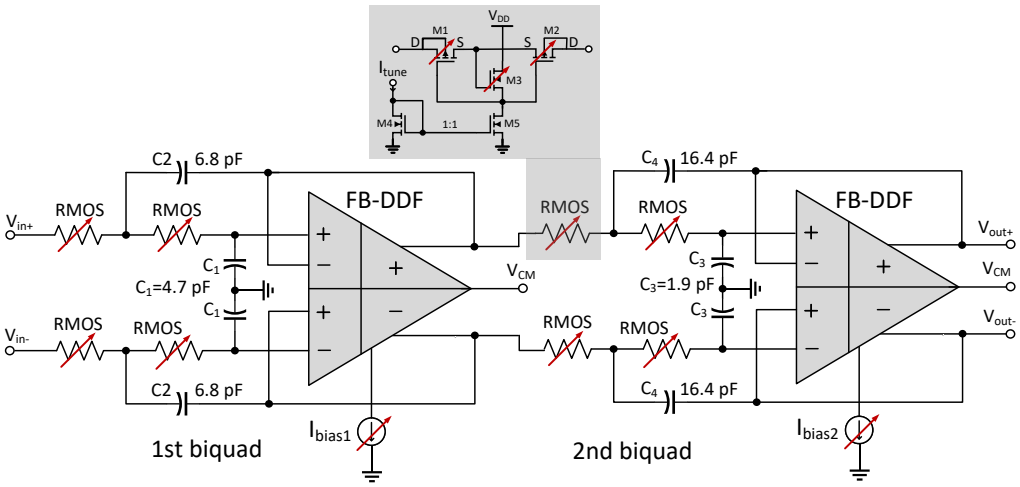

Figure 12. Simplified schematic design of the proposed anti-aliasing filter with tunable MOS resistor.

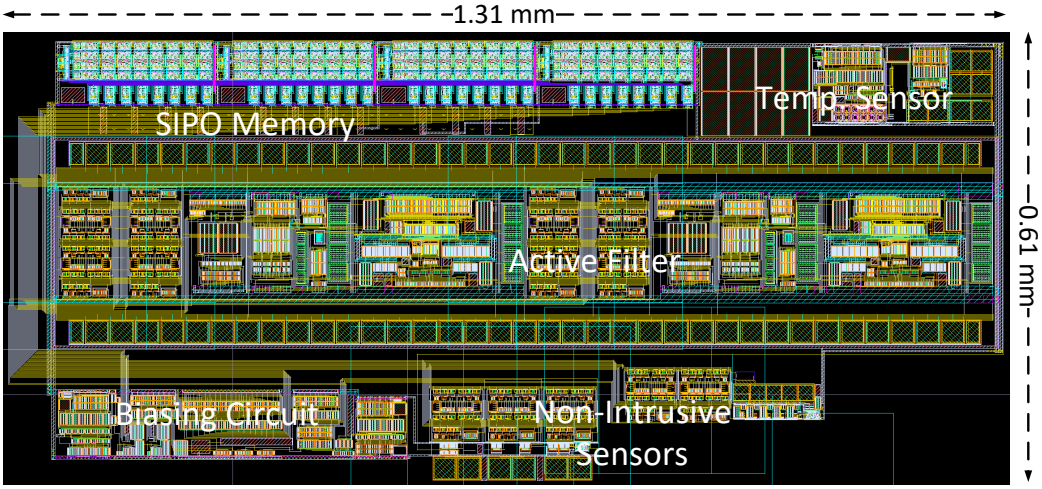

Figure 13. Layout implementation of the CFIA with the automatic digital offset automatic and power monitoring schemes.

3.3. Assessment Unit

The assessment unit consists of the essential measurement setup required for evaluating the reconfigurable hardware performance. It can be performed extrinsically, intrinsically, or mixtrinsically [164]. The extrinsic evaluation is realized by the simulation-based measurement setup, while the intrinsic evaluation is based on the real hardware measurement setup. The mixtrinsic evaluation is the combination of both the real and simulation-based measurements. The concept of mixtrinsic evolution is firstly proposed by authors in [165]. They used the genetic algorithm whose population contains both intrinsic and extrinsic individuals. In the former work at our institute [164], the concept of the mixtrinsic evaluation is extended differently by performing the complex measurements (phase margin, open-loop gain, etc.) extrinsically and executing the simple measurements (output voltage swing, and common-mode range) intrinsically, which helped to reduce the complexity of the assessment unit. However, both approaches in [164,165] rely partially on simulation-based results, which are not accurate compared to the intrinsic evaluation with real hardware. Furthermore, it drains for a considerable time, limited by the simulator's processing power, making it difficult to realize in situ calibration.

The intrinsic evaluation measurement setup cost is crucial for smart sensory electronics (SSE), especially in escalating system complexity. The performance measurement setup of the device under the test (DUT) can be divided into two fundamental categories based on the evaluation principle of the desired performance parameters. The first classification utilizes a direct performance measurement method to validate the target characteristics [105]. This category offers more accuracy and precision but raises the design complexity and physical area [166]. The second category uses the indirect measurements approach, relying on the statistical correlation between different DUT performance characteristics and low-cost test stimulation, which provides a simultaneous estimation of various DUT parameters [166–171]. We proposed in [168] a cost-effective indirect performance measurement for the smart sensory electronic system. The reconfigurable fully differential CFIA from [154] is employed as a test vehicle for the extrinsic evaluation. A sinusoidal signal with predefined amplitude and frequency is applied to the CFIA during the optimization process. Then, the THD is evaluated on the system response, which helps to predict most of the CFIA characteristics at once. It mainly relies on the fact that the design imperfection, such as slew rate, GBW, ICMR, the effective number of bits, full-power bandwidth, and signal-to-noise ratio (SNR), can be translated as a nonlinear distortion at the output of the closed-loop amplifier [172]. Unfortunately, the amplifier stability cannot be estimated from the spectrum analysis acquired by the sinusoidal response. Therefore, it is mandatory to evaluate the step response of the CFIA to predict its stability from the output response.

Compared to the optimization of digital evolvable hardware such as the field-programmable gate array (FPGA), the optimization of evolvable analog circuits at the transistor level may result in harmful solutions in terms of excessive currents that could cause a permanent failure of the DUT or reduce its life cycle. To alleviate this issue and enhance the long-term reliability, we recently embedded the low-cost indirect power monitoring module (PPM) with THD-based optimization methodology [173], as shown in Figure 14. The PPM serves two essential functions. Firstly, it helps the optimization algorithm to select the power-efficient solution. Secondly, it ensures accomplishing a safe reconfiguration pattern for the DUT. Without the presence of PPM, it is also quite challenging to constrain the acceptable current density during the optimization process without sacrificing the optimizer's exploring capabilities.

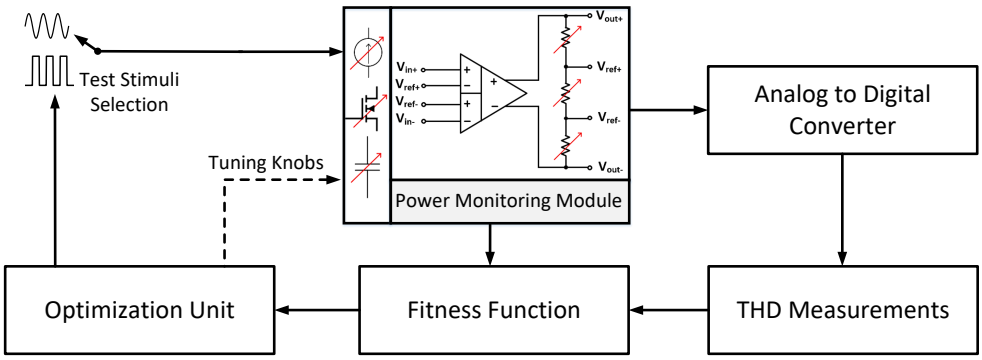

Figure 14. Block diagram of the integration of the power monitoring with THD−based optmization method.

The proposed approach mirrors a scaled-down value of the current of the power-hungry branches of the circuit into the current-starved ring oscillator, and its schematic diagram is given in Figure 15 (for simplicity, the current-starved oscillator, common-mode feedback, biasing circuit, and offset-calibration circuits are not presented in the figure). The current-starved ring oscillator [174] modulates the drawn current or the power dissipation of DUT in the form of clock frequency. This frequency is directly proportional to the consumed current; hence, this method can detect the desired power threshold level and give a fair approximation of the power consumption between various optimization solutions. Since the PPM mirrors the scaled-down current of the power-hungry branches, it has negligible effects on the overall performance of the DUT. The transistors' sizing information are listed in Table 1.

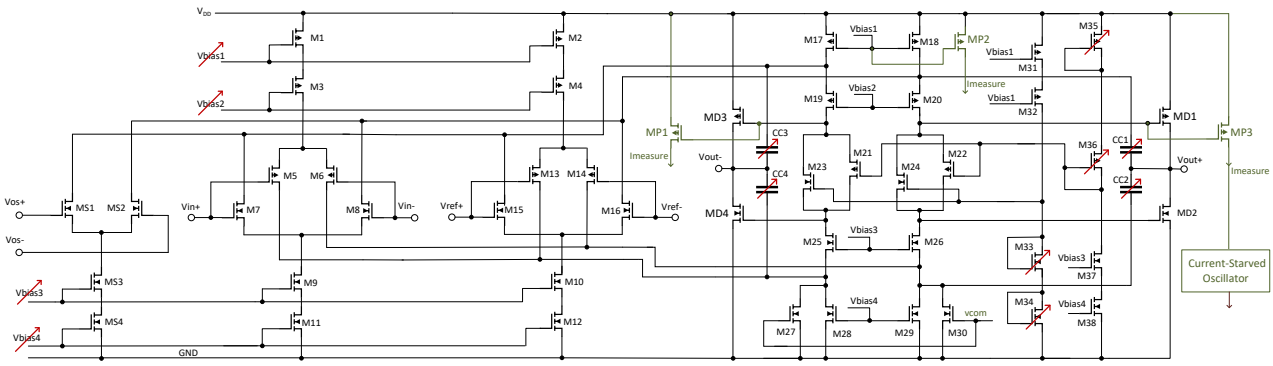

Figure 15. Transistor-level schematic diagram of CFIA along with power monitoring module.

Table 1. MOSFET size ratios of the CFIA circuit.

Tr. Nr.	W / L (μm/μm)	Tr. Nr.	W/L (μm/μm)
M1, M2	256/1	M21, M22	52/0.55
M3, M4	128/0.5	M23, M24	18/0.55
M5, M6, M13, M14	120/0.7	M25, M26	42/0.7
M7, M8, M15, M16	40/0.7	M25, M27, M30	50/1
M9, M10	40/0.5	M31	64/1
M11, M12	80/1	M32	32/0.35
M17, M18	300/1	M37	10/0.5
M19, M20	132/0.7	M38	20/1
MD1, MD3	240/0.35	M33 *, M34 *	64/0.5
MD2, MD4	80/0.35	M35 *, M36 *	128/0.5
MP1, MP3	1/0.35		

where * represents scalable devices.

Another low-cost on-chip indirect measurement method using non-intrusive sensors is presented in [166,167,175]. The non-intrusive sensors are electrically disconnected from the main DUT but placed in close proximity to the DUT. Therefore, the optimization process can be performed without interrupting the device's operation or affecting its performance. The operating conditions of these non-intrusive sensors are similar to the DUT, and their performance is designed to be highly correlated to the performance characteristics of the DUT. Hence, the DUT-targeted characteristics can be predicted from different characteristics of the non-intrusive sensors measured economically. For non-intrusive sensor design, the correlation among them should be as minimal as possible. Contrarily, their correlation with the targeted characteristics of DUT should be as maximal as possible. As observed from Figure 16, the correlation among the sensors themselves is significantly small, while it has a good correlation with the performance characteristics of the CFIA.

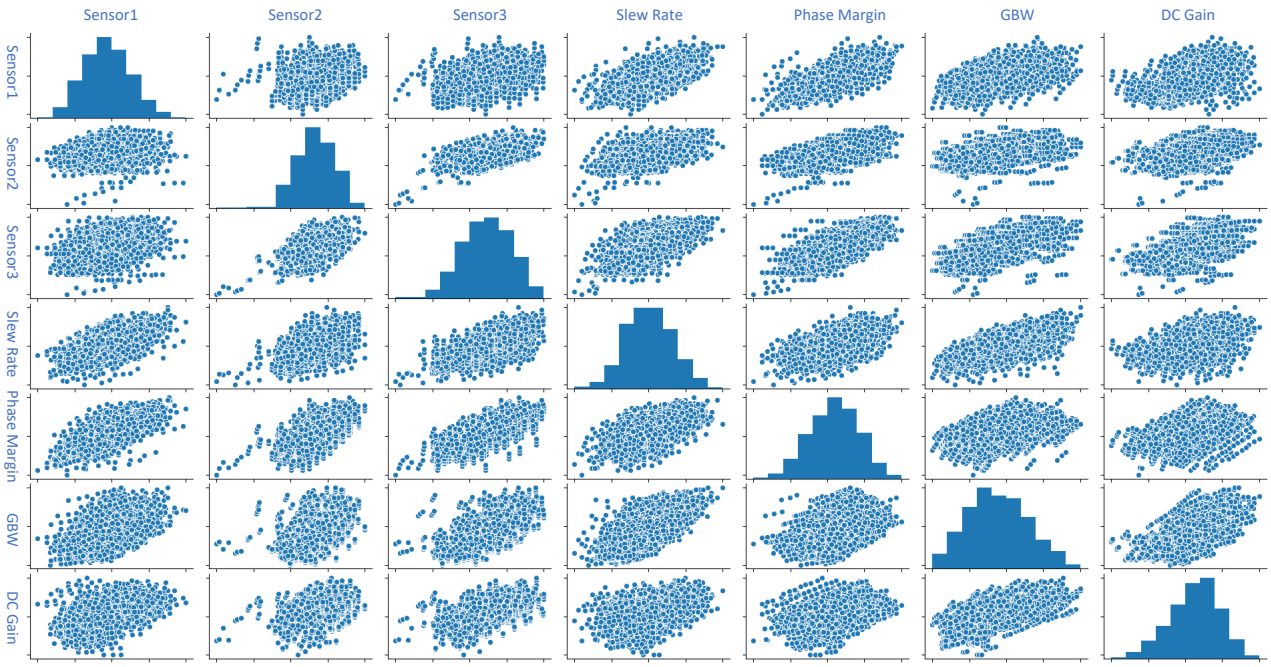

Figure 16. Correlation of the non-intrusive sensors with targeted performance characteristics of DUT.

It is a quite challenging task to model the performance characteristics of the DUT analytically [166]. Therefore, an artificial neural network is generally employed as a regressor to approximate this regression task. We proposed the indirect measurement method based on non-intrusive sensors in [175]. During the training phase, the non-intrusive

sensors and DUT are simulated and subjected to the same PVT operating conditions using the combination of Monte Carlo (MC) and worse case corners (WCC). Then, 80% of the data samples are randomly selected for the training, while the remaining 20% are used to assess the regressor performance. In the testing phase, the outputs of the non-intrusive sensors are passed to the pre-trained regressor, which indirectly predicts the performance characteristics of DUT. The achieved correlation performance metric (adjusted r squared) is 91.68% [175].

3.4. Optimization Unit

For the in-field optimization process, an AI agent is required to be embedded inside the ATE, similar to the SLM agent proposed by Synopses (Concertio) [176,177]. The AI agent can be placed at different levels of the system hierarchy, for example, at the application layer, operating system, firmware, or hardware level [23,177], as shown in Figure 17. In our proposed methodology [168], the AI agent is placed at the closest level to the DUT, i.e., at the hardware level. Regarding the selection of AI-based optimizers, derivative-based optimization techniques cannot be used because of discontinuous objective space [115]. Alternatively, meta-heuristic optimization algorithms (MHOAs) perform impressively regardless of discontinuous objective space. There are numerous types of MHOAs available in the literature [178]. We selected particle swarm optimization (PSO) as an optimization unit mainly because of its easy implementation and fast convergence speed [179]. The PSO was firstly presented in [180]. Later on, several improved modifications of the PSO algorithm have been presented in the literature [181–184] to improve its exploring capability and decrease the trapping possibility into the local optima. We recently proposed a modified PSO version, named the experience replay particle swarm optimization (ERPSO) [168]. The ERPSO extended the selection producer of the traditional PSO by introducing an experience replay buffer intending to lower the trapping probability at the local optimum. The experience replay buffer is the archive of the previously discovered global best positions, while its selection is based on an adaptive epsilon greedy approach in the velocity update equation.

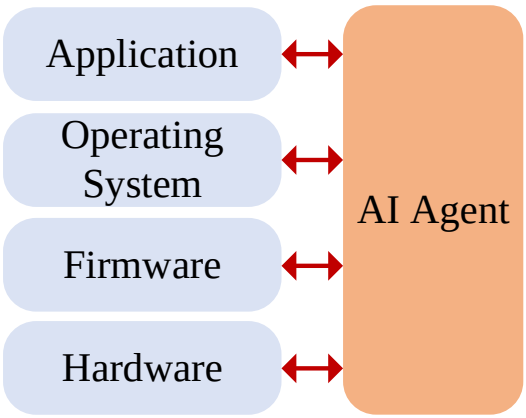

Figure 17. Possibilities of AI agent placements at different levels of the system hierarchy.

The optimized results are summarized in Table 2. The optimization is performed on the schematic level, and the solutions are evaluated on the post layout level. Though there must be a difference, as can be observed from the table, it is computationally expensive and time-consuming to run the optimization process on the post layout level due to the large netlist size with RC extractions. For this experiment, a sinusoidal signal with a frequency of 100 kHz and amplitude of 2 V_{p-p} is applied as a test stimulus for the targeted THD value of −70 dB. For the stability test, a step stimuli with a period of 1 µs and amplitude of 2 V_{p-p} is used. The power threshold is assigned to 6 mA (20 mW), as per the safe operational current range of the CFIA. As it can be observed from the table, the proposed design effectively optimizes the DUT for the targeted power and THD requirements. The optimization process is run independently five times for the typical mean condition, and its

statistical information has presented in the table. For all those independent tests, the power dissipation of the CFIA is within the safe limits, and the THD value indirectly satisfied the other performance characteristics of CFIA. With the addition of PMM, the average power consumption for the nominal operating conditions is reduced by roughly 25% compared to our previously reported work [168]. Other performance characteristics, especially slew rate and GBW, slightly declined due to lower power consumption, but they still fulfilled the desired performance requirement. The tested schematic solutions on the layout level show slight and acceptable differences. Hence the optimization on the schematic level for this circuit can be faithfully acknowledged.

Table 2. CFIA post layout characteristics based on schematic level optimization solutions.

CFIA Design Parameter	Statistical Information (Schematic Level)			Statistical Information (Post Layout Level)		
	Mean	Min	Max	Mean	Min	Max
Differential DC gain (A_{VD})	94.80 dB	92.19 dB	97.70 dB	94.73 dB	92.16 dB	97.72 dB
Gain bandwidth product (GBW)	47.75 MHz	26.35 MHz	102.18 MHz	39.41 MHz	25.1 MHz	82.32 MHz
Phase margin (PM)	73.22°	63.22°	81.32°	60.47°	47.12°	72.49°
Slew rate (SR)	±63.38 V/µs	±29.40 V/µs	±165.12 V/µs	±60.34 V/µs	±28.55 V/µs	±155.17 V/µs
PMM output frequency (f_{ck})	347.18 kHz	218.3 kHz	607.7 kHz	377.48 kHz	211.2 kHz	593 kHz
Static power dissipation (P_D)	4.17 mW	2.07 mW	8.76 mW	4.16 mW	2.06 mW	8.76 mW

The CFIA circuits have been tested on the chip level by running various optimization solutions obtained from the circuit level. As it can be visualized in Figure 18, the CFIA received two different solutions with a gain setting of 1 and 2, respectively. Initially, the CFIA is powered down, and the output of the SIPO is disabled to ground until 65 µs, whereby this time, the first row of the SIPO receives the complete optimization pattern. After that, the SIPO output from the first row is shifted to the CFIA in enabled mode, while the writing of the next optimization solution is carried out in the second row parallelly. Similarly, for the time from 115 µs, the second optimization pattern is transferred to the CFIA, which changes the gain by a factor of 2, and the writing of the next optimization solution is now performed on the third row of the SIPO. The most significant bit of the selected row of SIPO has been exposed to the chip output to debug the downloaded configuration data on the SIPO memory, as shown in Figure 19. It can also be used for handshaking or as an acknowledgement in the communication protocol between the DUT and demonstration board. In a similar approach used for the CFIA, the filter circuit is tested for two different configuration patterns to change the cutoff frequency, as shown in Figure 20.

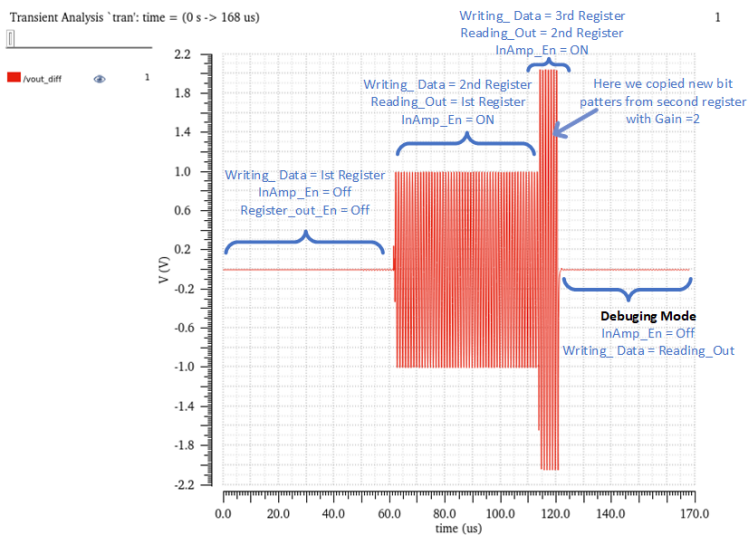

Figure 18. CFIA chip−level post layout simulation result with two different optimization solutions.

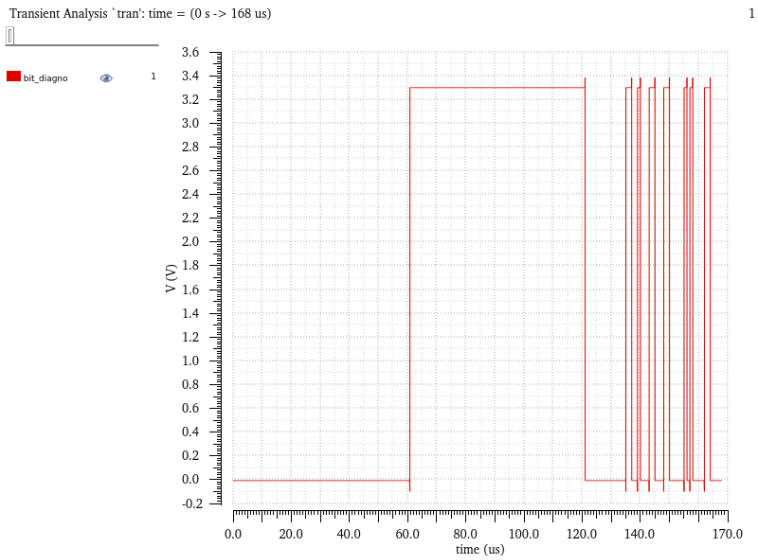

Figure 19. Chip−level simulation result of the SIPO debugging output bit.

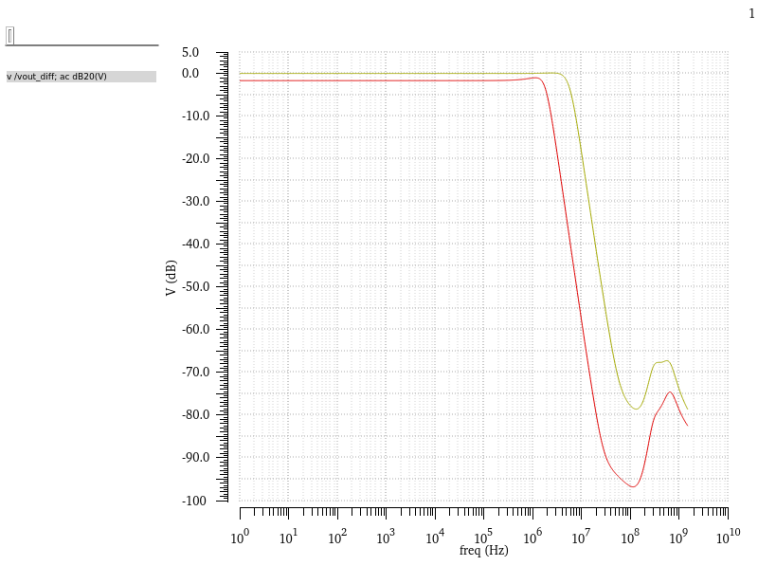

Figure 20. Filter chip−level post layout simulation result with two different configurations.

3.5. Observer Imperfections

To address the observer imperfections, we explored the concept of robust optimization in [109,110]. The robust optimization can be split into two categories [116,185]. The first category is known as archive-based robust optimization [109,185]. This approach works specifically well with the meta-heuristic optimization algorithms because of the enormous exploring capability of the searching agents during the optimization activity. However, it costs extra memory reserves. At the beginning of the optimization process, optimizer exploitation is high. The optimizer might choose a false optimum solution because of the observer's non-idealities, but as the exploration increases, it quantifies the solution's correctness with the archive's help [109]. This phenomenon is graphically illustrated in Figure 21 using the two-dimensional Griewank objective function. As the exploration of the search particles is extensively condensed around the global best position, this helps MHOAs to minimize the effects of observer imperfections with the passage of iterations.

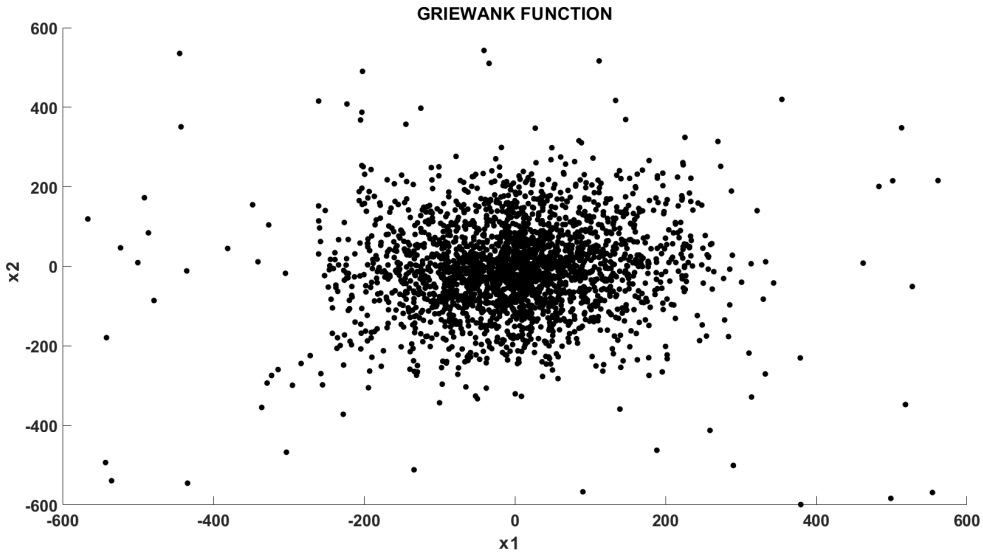

Figure 21. Visualization of the exploration capabilities of the PSO after 100 number of iterations.

The second category is based on the surrogate-based robust optimization method [185]. The famous Bayesian statistical regression process, more precisely, the Gaussian process regression (GPR) [110,117,118], falls under this umbrella. The GPR has been commonly used for error quantification and design optimization. The uncertainty is usually well modelled using GPR; hence, these models could better approximate the uncertainty [119]. Furthermore, it also provides the confidence interval for the estimated values [118]. The GPR model can be expressed as

$$f(x) \sim GP(m(x), \kappa(x, x')) \tag{1}$$

where $\kappa(x, x')$ represents the kernel function and $m(x)$ denotes the mean function. The GPR is optimized by adapting the kernel and mean value according to the training data set. Figure 22 compares the distorted output signal of the CFIA and the predicted output signal of the robust optimizer using GPR with 95% confidence intervals [110]. As observed from the figure, in addition to uncertainty level prediction, the GPR helps forecast the data, which can considerably minimize the transmission power of wireless sensor network applications. For the intrinsic evaluation of the proposed robust optimization concept, the non-idealities or uncertainty of the analog to digital converts for sampling the output response of CFIA, as shown in Figure 14, will serve as the source of observer imperfections.

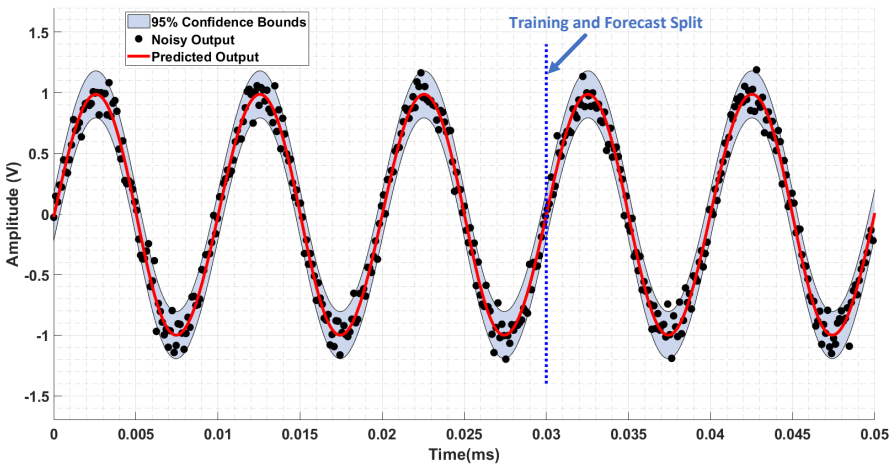

Figure 22. The predicted output with 95% confidence interval and illustration of the data forecasting capabilities by the application of GPR block.

4. Spiking AFEs with Self-X Extension

This section targets to move the AFE design from the vulnerable amplitude domain to a robust spike-based representation of sensory information, as referred to in Figure 3 part (c), with self-X properties for leading-edge integration technologies. Nevertheless, the focus is placed on the appropriate electronics design, as the system's lowest and most critical level in the self-hierarchy, as shown in Figure 2. The former sensor to spike to digital converter (SSDCα) chip introduces the SAFE inspired by human hearing acoustic localization. However, SSDCα did not make use of adaptivity as desired, e.g., to deal with challenges in advanced node CMOS technology. In this work, we pursue building blocks of the concept of robust adaptive spiking sensor systems where the essential SAFE building blocks are implemented in the recent chip. It has two different levels of adaptivity. The first level is completely local and self-adaptive, i.e., unsupervised in the classical sense. The second level is based on supervised learning and exploiting the optimization/learning using more sophisticated population-based metaheuristic algorithms.

Implementing the mixed-signal systems in the leading-edge technologies has power and speed gain advantages [186]. It is mainly due to the lower supply voltage and decreased capacitance value. On another side, many challenges imposed on the circuit design, e.g., lower supply voltage, decreased signal swing, manufacturing deviations, reduced intrinsic device gain, noise, and aggravated device mismatch [187], which complicities the signal processing in amplitude domain. Especially the complex mixed-signal system such as ADC faces the mentioned challenges when migrating to the smaller technology [186–189].

Several ADCs structures are introduced in the literature to address and attempt to overcome these challenges. One example is synthesizable stochastic flash ADC architecture, which requires many resources to implement, e.g., 3840 comparators for 5.3 bits of resolution [186,187]. However, stochastic ADCs still use amplitude-coded signals that face challenges in advanced node CMOS technology. This motivated the researchers to design electronic sensor systems using a spike or time-coded signals with a technology agnostic property, which is robust to technology scaling [37,38,190–192]. One model is the ADC-based current sensing [190]. Its architecture is based on a current-to-frequency converter implemented using the Izhikevich neuron model and frequency-to-digital conversion implemented by digital blocks. Authors in [193] proposed a scalable ADC based on the neural engineering framework. It takes advantage of parallelism inherent in neural networks. The encoder and neurons are designed in the analog domain, whilst the decoding and signal reconstruction are implemented in the digital domain. Likewise, the authors in [191,192] proposed a synthesizable ADC inspired by a neural network. It uses the resistive random-access memory (RRAM) crossbar architecture in a dual-path configuration. The overall architecture of their ADC realizes a three-layer of general neural network hardware substrate, the input, hidden, and output layer. To overcome these challenges, the former SSDCα chip has emulated the acoustic localization by using the spike timing to represent the information. The implementation of a SAFE inspired by acoustic localization needs two stages sensor-to-spike converter (SSC), and spike-to-digital converter (SDC) [38]. In the recent chip, we pursue the design of SAFE based on robust adaptive spiking electronics inspired by acoustic localization.

4.1. Natural Sensory Systems Evidence

Organisms use the time difference of the signals reaching the ears, which invoke interaural time differences (ITDs) to determine the sound source. Jeffress presented the acoustic localization in 1948 [194]. Jeffreys' theory is based on three basic assumptions: delay lines, coincidence detectors, and place map [195]. Acoustic localization is a clear adaptive spiking neural network (SNN) model, as shown in Figure 23a. We proposed SAFE with adaptation features based on the two-stage to emulate Jeffress's model [194], as shown in Figure 23b. The first stage (SSC) converts the sensor signal into two spikes with ITD, and the ITD value changes with the sensor signal. The second stage, the self-adaptive spike-to-digital converter (SA-SDC), generates digital code depending on the ITD value. The

SA-SDC has three fundamental assumptions of Jeffress's theory. These are implemented by synapses weights, an array of adaptive coincidence detection and winner-take-all (WTA) with memory. The primary goal of this work is to implement the fundamental building block of SAFE, which is SA-SDC.

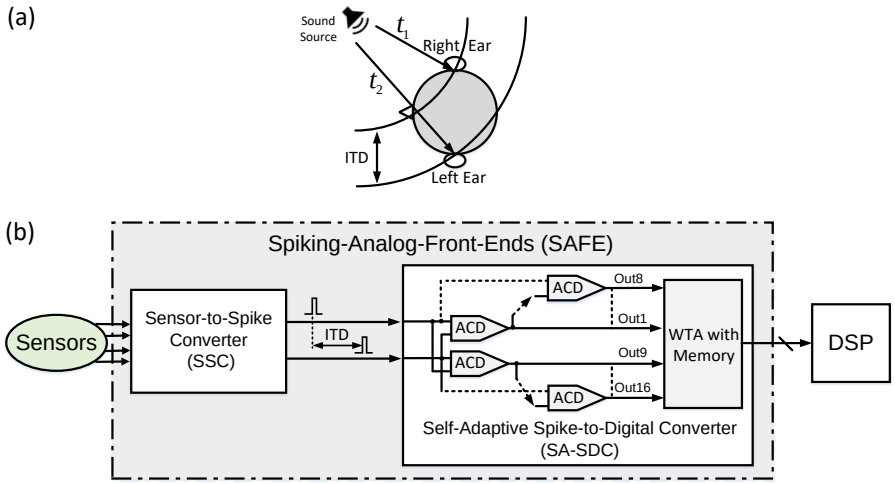

Figure 23. (**a**) Acoustic localization model. The brain locates the voice's position using interaural time differences (ITDs). (**b**) The main blocks of proposed SAFE architecture.

4.2. Proposed Self-Adaptive Spike-to-Digital Converter (SA-SDC)

The proposed SA-SDC has two parts, the self-adaptive spike-to-rank coding (SA-SRC) and winner-take-all (WTA) with memory, as shown in Figure 24. The first one generates spike orders that reflect the value of ITD. The second one is a digital circuit that converts those orders into respective digital codes. The proposed SA-SRC is implemented by sixteen adaptive coincidence detection (ACDs). The ACD has two adaptive synapses (AS) and one neuron (N). The adaptive synapse is based on the CMOS memristor, which emulates the long-term plasticity (LTP) and short-term plasticity (STP) of biological synapse [196].

Numerous neuron models are available in the literature [197]. The leaky integrate and fire (LIF) neuron model of Indiveri neuron model has components for modulating the neuron's threshold voltage, spike frequency adaptation, setting an arbitrary refractory period, membrane capacitor, positive feedback, a digital inverter for pulse generation, and a transistor for controlling the current leakage [198]. The neuron properties required for the ACD are to perform the time delay of a neural network with an inverse relationship between the incoming charge magnitude and the time of the first spike. These are the essential characteristics that are available with any neural spiking model. Indiveri's neuron model has been modified to meet the requirements of ACD, as shown in Figure 25. The proposed neuron has two variables and sixteen transistors; on the other side, the Indiveri model has four variables and twenty transistors. This results in a 20% reduction in power consumption, speed gain with the factor of eight, a 30% reduction in area, and an eight times higher rate of a spike compared to the Indivery model. During the SA-SRC design process, the transistor sizes of the neuron were initially found based on empirical results and observations from simulations. The final values are tuned again with the help of simulation to generate the spike order that works appropriately against the PVT corners, as enumerated in Table 3. The layouts of the proposed adaptive coincidence detection and self-adaptive spike-to-rank coding are shown in Figures 26 and 27, respectively. The SA-SRC consumed a total area of 0.98 mm^2 with 4-bits resolutions, while the previous work SSDCα presented by our research group consumed 8.5 mm^2 with 8-bits resolutions.

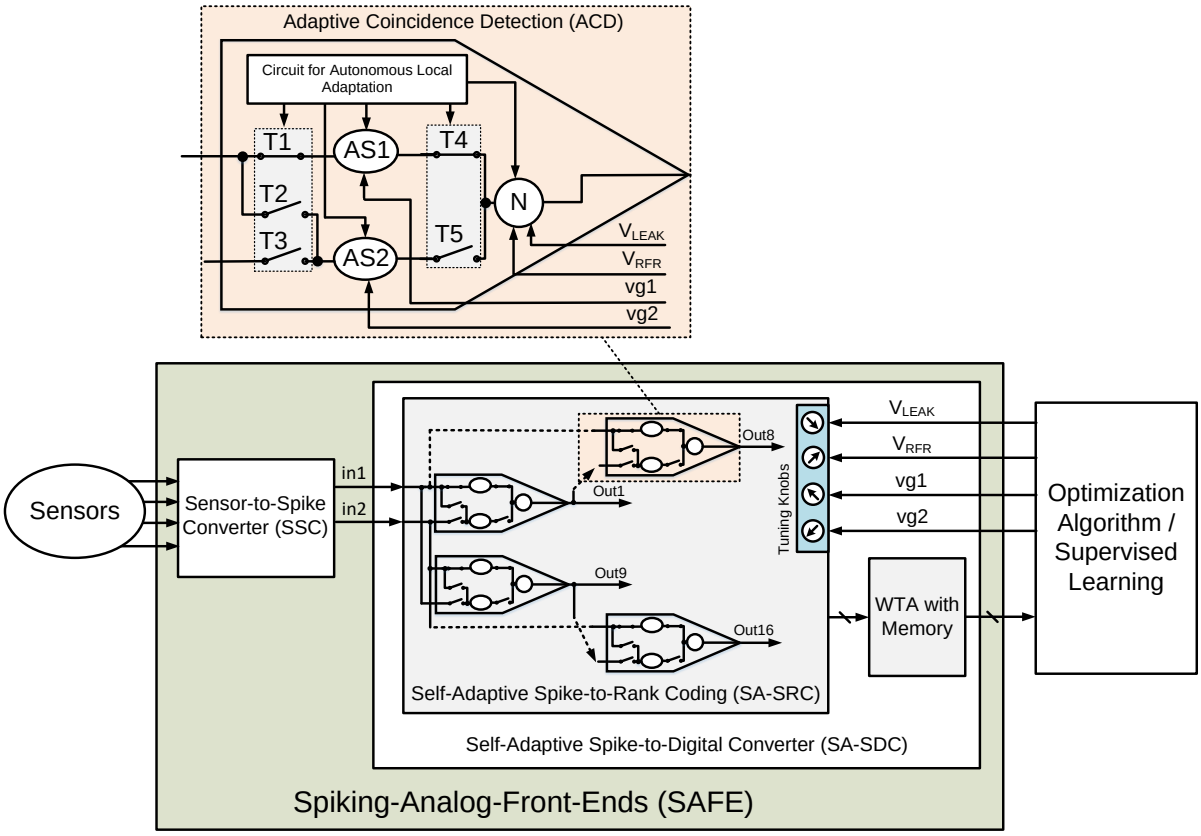

Figure 24. SAFE with self-X capabilities based on the two levels of adaptivity. The first and the second are implemented by the autonomous circuit of ACD and optimization algorithm/supervised learning, respectively. The second level used the V_{LEAK}, V_{RFR} to control the neuron and vg1, vg2 to control the synapses.

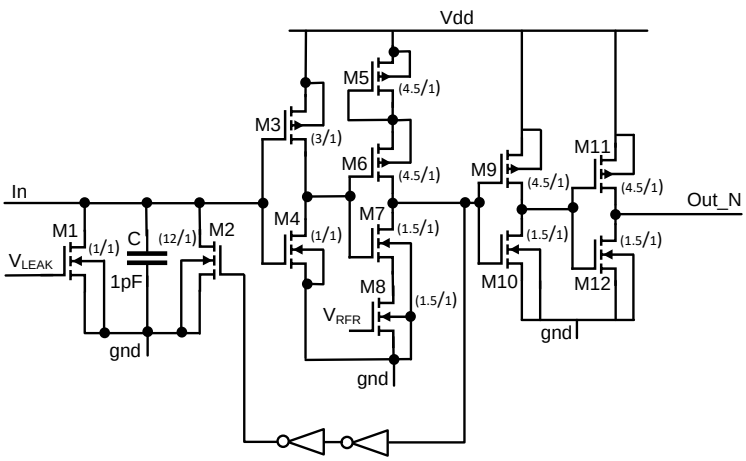

Figure 25. Proposed circuit to simplify the Indiveri's neuron (the ratio numbers represent the W/L value of the transistors in μm). It has been used in the ACD block.

We have built SAFE with two levels of adaptivity, as shown in Figure 24. The first one is at the level of ACD, and the second one is at the level of SA-SDC. The second adaptation level is responsible for adapting the variables vg1, vg2, V_{LEAK} and V_{RFR}, and it runs above the first level. For each modification in these variables; the first level participates in the adaptation process, and the second level waits until the first level completes the solution. If the solution corrects the synapse weight, the adaptation process ends; otherwise, the second level updates the variables (vg1, vg2, V_{LEAK}, V_{RFR}) and turns on the adaptation for

the next round, and so on. In the first level, the adaptation circuit is completely local and automatically adapts the synapses' weight. Moreover, in the first level, the adaption works simultaneously for all ACD. Therefore, the number of the SA-SDC variables in the second level is equal to the variables of one ACD (vg1, vg2, V_{LEAK}, and V_{RFR}).

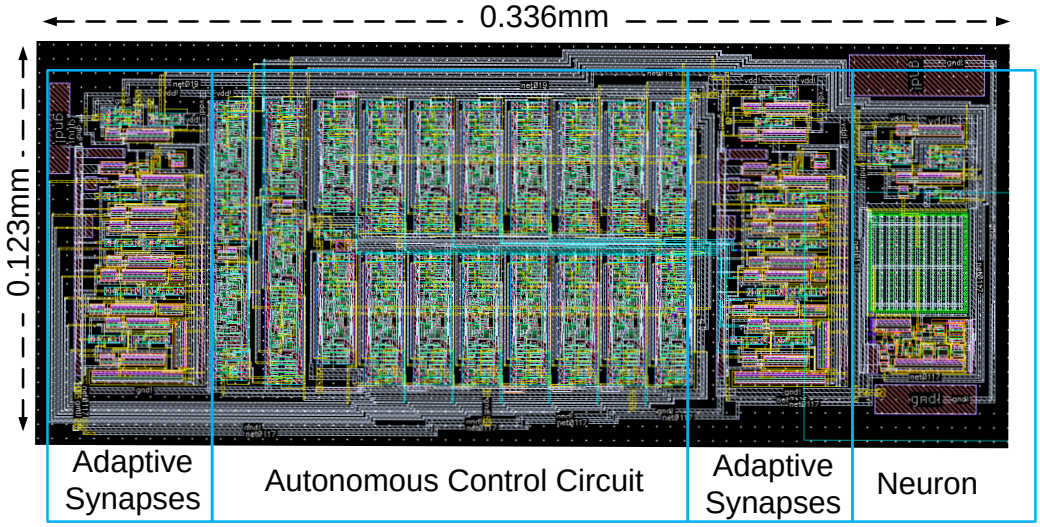

Figure 26. The layout of adaptive coincidence detection.

Figure 27. The layout of self-adaptive spike-to-rank coding.

The first level autonomous control circuit, as shown in Figure 28, uses the time of neuron fire to determine the weight of the synapse. It fundamentally relies on the fact that the timings of neuron fires depend on its input current, and the synapse's weight controls this input current. Therefore, the synapse's weight is proportional to the timing of the neuron's firing. This first level of the autonomous circuit adapts the weight of the first synapse of all ACDs simultaneously by connecting the first synapse and disconnecting the second synapse of all ACDs. Similarly, the second synapse's weight will be adapted.

The second adaptation level will explore optimization possibilities by using two different methods. Firstly, the population-based metaheuristic algorithms, more specifically,

the ERPSO proposed recently by our research group. The SAFE output will serve as the cost or fitness function for the optimization unit. Meanwhile, the four variables (vg1, vg2, V_{LEAK}, and V_{RFR}) will serve as tuning knobs for the optimization process to adjust the desired output of SAFE. The second approach will be based on supervised learning in which the pretrained regression model will be used to provide the new values of the four variables depending on the device's operating conditions. Unfortunately, these possibilities are harder to perform using cadence simulations due to the simulation time demand of the transient simulations. On the other hand, verifications of these approaches can be evaluated on the fabricated prototyping chip in a reasonable time frame. The second adaptation level will be implemented on the field programmable gate array (FPGA) board.

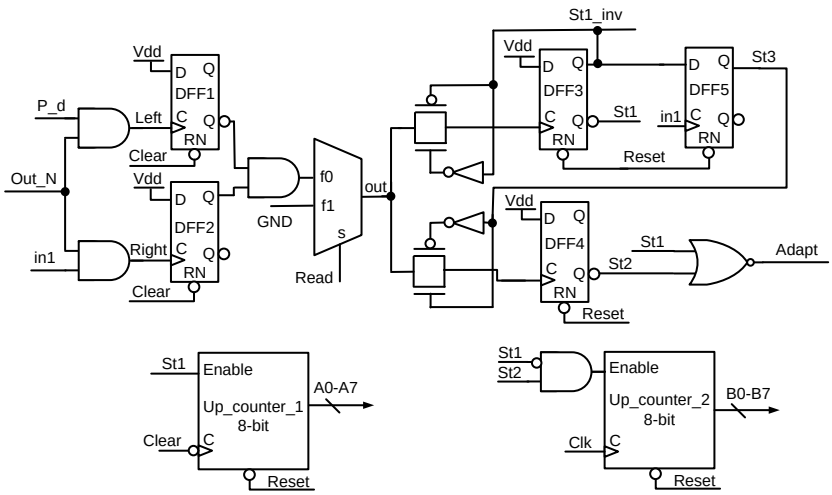

Figure 28. Autonomous control circuit. It implements the self-adaptation of the first level for the synapses' weights.

4.3. The Experimental Results

Figure 29 shows the post-layout simulation of ACD representing the basics of three states of acoustic localization. These states depend on the ITD value between the input spikes, where the ITD value determines the timing of the output spike generation. In the case of a larger ITD value (above 200 ns in this design), the output spike will not be generated.

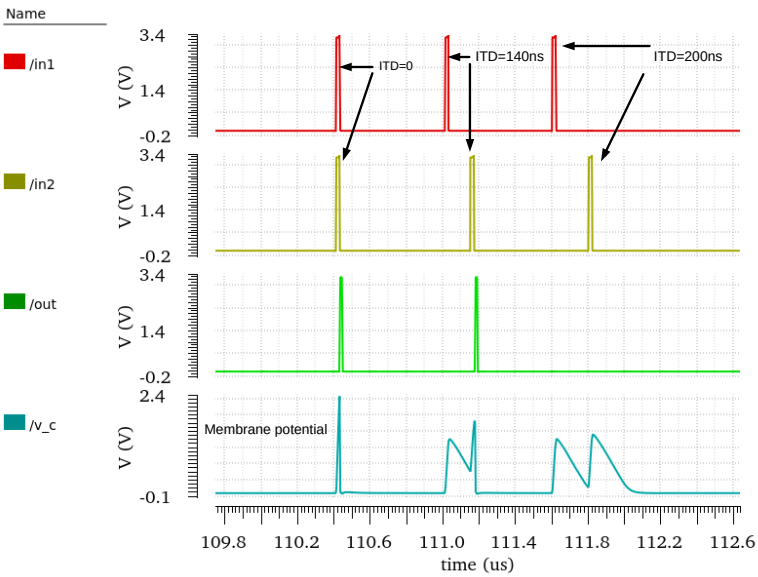

Figure 29. The post−layout simulation of the adaptive coincidence detection.

The proposed SA-SRC can generate up to sixteen different spike order codes that reflect the ITD values at its input. The value of ITD changes from −120 ns to 120 ns by the step size of 15 ns. It is equivalent to 4-bits in binary coding. The Figure 30 presents the post-layout simulation result of the SA-SRC under nominal operating conditions. For this test, two pulses are applied to the input of SA-SRC with different values of ITD. The SA-SRC generates different codes for every value of ITD. The outputs from out1 to out16 represent the one spike order code. In total, it has eight spike order codes. The numbers labelled on the output waveforms represent the spike order sequence with respect to the other outputs. The post-layout simulation of SA-SRC has been run under extreme process, voltage, and temperature (PVT) corners, as listed in Table 3. The capability of measuring ITD is increased by cascading more ACDs. The number of bits (NOB) can be calculated, as follows:

$$NOB = \frac{\ln\left(number\ of\ ACDs\right)}{\ln 2} \tag{2}$$

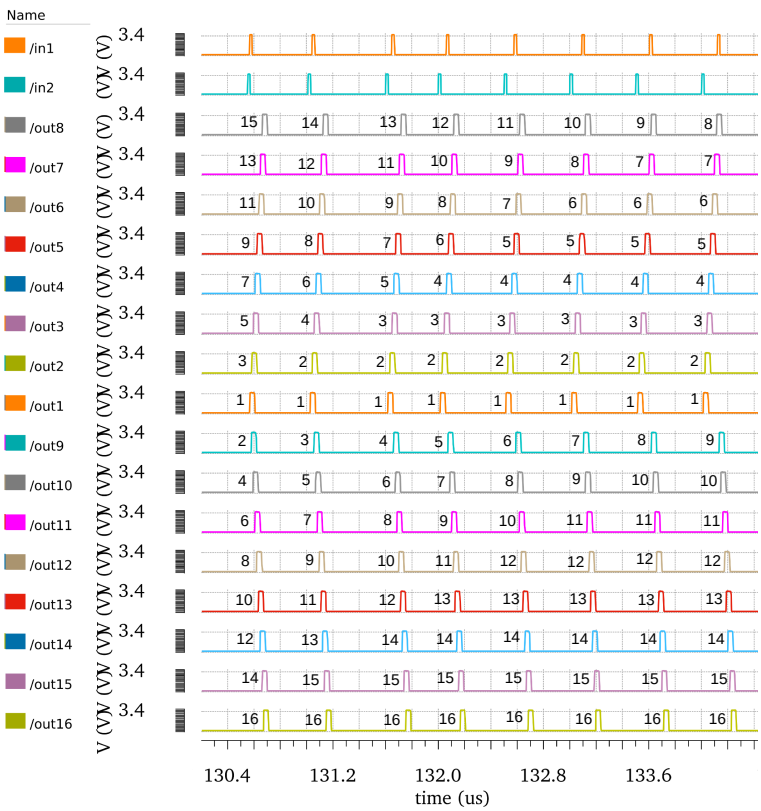

Figure 30. The simulation of SA-SRC at circuit conditions: temperature = 27 °C, Vdd = 3.3 V and on the nominal process. Every column represents one code and reflects one value of ITD.

The differential non-linearity (DNL), integral non-linearity (INL), and a number of missing codes (NOMC) parameters have been simulated under corner case number (5) in Table 3. Their values are 0.96 LSB, 4.5 LSB, and seven missing codes, respectively. However, these values are compensated by adapting the variables V_{LEAK}, V_{RFR}, vg1, and vg2, and running the automatic adaptation of the first level, as shown in corner number 5 in the table. The values of the parameters NOMC, DNL, and INL after adaptation are no missing code, 0.25 LSB and 0.44 LSB, respectively.

Table 3. The post-layout performance of SA-SRC under worst-case process corners. Where Tmax = +85 °C, Tmin = −40 °C, VDD(typ) = 3.3 V, VDD(max) = +10% VDD(typ), VDD(min) = −10% VDD(typ), WP: worst-case power, WS: worst-case speed, WZ: worst-case zero and WO: worst-case one.

Corner No.	Process	TEMP	VDD	vg1 (V)	vg2 (V)	V_leak (V)	V_ref (V)
1	TM	typical	typical	1.8	220 m	700 m	750 m
2	WO	min	max	1.8	220 m	700 m	750 m
3	WO	min	min	2.2	0	700 m	650 m
4	WO	max	max	1.8	220 m	700 m	750 m
5	WO	max	min	2.1	10 m	700 m	590 m
6	WP	min	max	1.8	660 m	700 m	700 m
7	WP	min	min	1.8	220 m	700 m	750 m
8	WP	max	max	1.8	220 m	700 m	750 m
9	WP	max	min	1.2	0	700 m	750 m
10	WS	min	max	1.2	50 m	700 m	800 m
11	WS	min	min	2.5	100 m	700 m	700 m
12	WS	max	max	2	70 m	700 m	720 m
13	WS	max	min	2.2	120 m	700 m	600 m
14	WZ	min	max	1.9	100 m	700 m	780 m
15	WZ	min	min	1.8	100 m	700 m	740 m
16	WZ	max	max	1.8	100 m	700 m	830 m
17	WZ	max	min	1.8	130 m	700 m	610 m

5. Chip and Demonstration Prototyping Board Design

The amplitude and spike domain AFEs circuits presented in Sections 3 and 4 are integrated into a single prototyping chip. For the amplitude domain AFE, two separate reconfigurable fully-differential CFIA modules have been designed, as it can be observed in Figure 31. Each module has its own hot-swappable shift registers and PMM. The shift register has D_{in} pin to shift the configuration data serially to the memory, $W_{0,1}$ for selecting the row to perform the writing operation, $R_{0,1}$ to select the corresponding row for data reading, $D_{outDebug}$ for debugging the written data, and finally En for enabling or disabling the register. The second CFIA module has an additional digital offset autozeroing scheme. This autozeroing can be performed autonomously or with the help of an optimization unit. In the next stage of AFE, the tunable anti-aliasing filter is integrated into the chip. In order to reduce the number of I/O chip pins, the register memory of the CFIA passes the data internally to the register memory of the filter. Three non-intrusive sensors, including the temperature sensor, are designed and integrated near the filter circuit to support the indirect measurement by monitoring the chip PVT conditions for the filter tuning. The output type of these sensors is in quasi-digital form. Hence, the digital processing unit, the red pitaya board in our prototype, makes it easy to demodulate the PVT information. Furthermore, the temperature sensor will also be used for the chip thermal monitoring.

The second main part of the chip is for the spike domain AFE implementation. We designed the essential SAFE blocks, neuron, synapse, ACD and SA-SRC, as shown in Figure 31. The neuron block has I/O pins and two controlling variables pins (v_{rfr}, v_{leak}) to characterize its basic operation on the physical hardware level. Likewise, the synapse cell has its basic I/O pins plus one controlling variable for adjusting the weight. The ACD cell includes the four variable voltages (v_{leak}, v_{rfr}, v_{g1},v_{g2}) that will serve as a tuning knobs for the optimization algorithm. The Adapt output signal from the ACD becomes active after completing the unsupervised adaptation of the first level. Similarly, the SA-SRC cell has four variable voltages as tuning knobs, sixteen outputs pins for generating the spikes order codes, and Adapt for indicating the adaptation end.

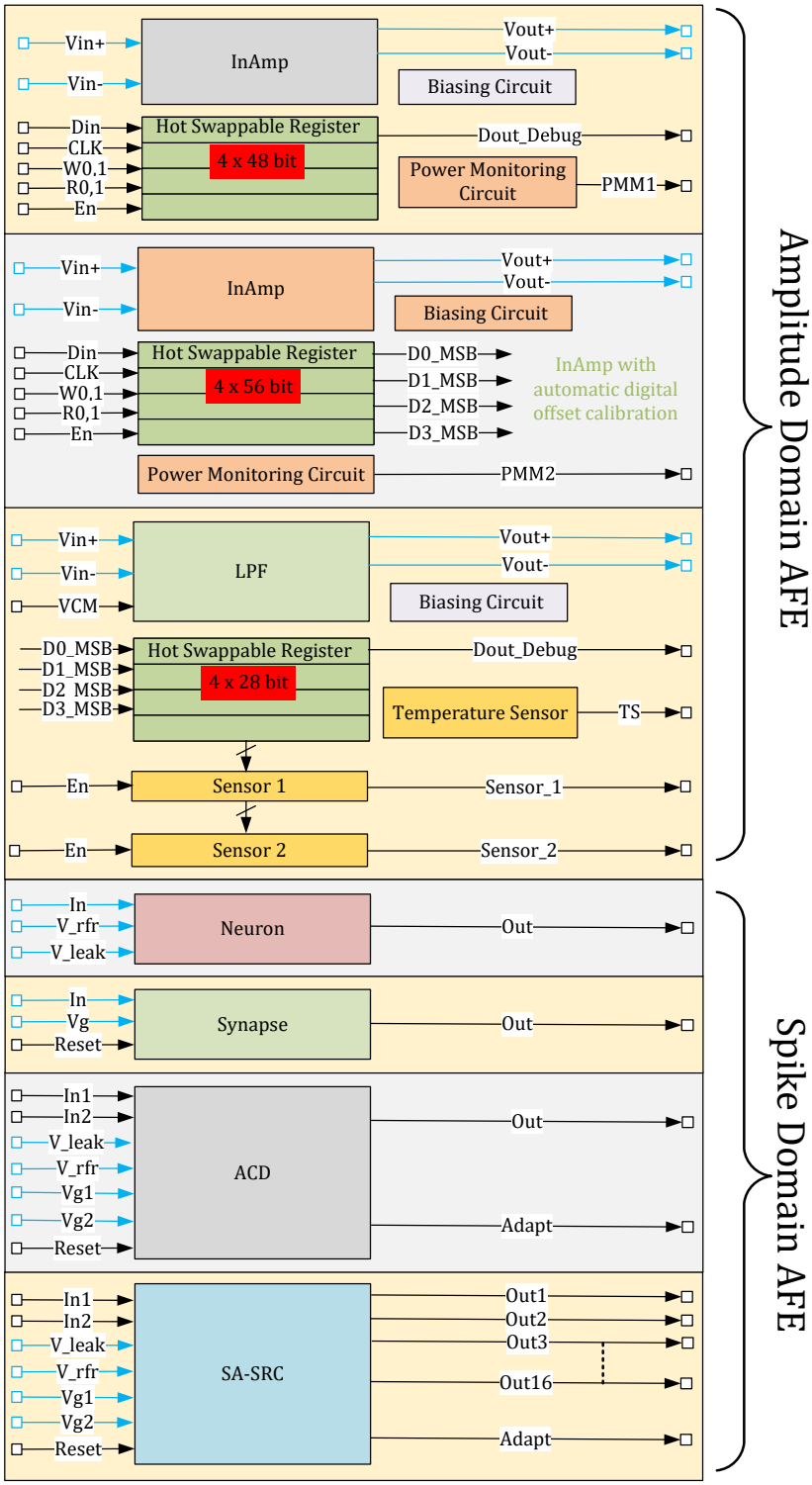

Figure 31. Simplified block−diagram of the prototyping chip layout.

The circuits were designed using the XFAB 0.35 µm CMOS NWELL technology and Cadence design tools. The chip occupies a total area of 10.89 mm^2 with 100 input/output pads, as shown in Figure 32. The former USIX 1.0 and USIX 2.0 consumed a total area of 11.59 mm^2 and 18 mm^2, respectively. These chips provide a complete solution for the sensor's interface and deal with different mixed-signal cells in the readout circuit path, while the current work is focused on essential cells for both AFEX and SAFEX in a cost-effective prototyping chip. A short description of the individual chip cells is given in Table 4.

During the layout design, matching with common-centroid interdigitation is followed for the analog cells. Four metal layers are used to complete the chip, where up to metal3 is used to layout and route the cells in the lower design hierarchy, and the thick metal4 is used to route the power rings in the highest hierarchy due to its high current density. Eleven pads are reserved for powering the chip to avoid the local IR drop on the supply rails and to avoid exceeding the driving capability of the single power pad. The substrate contacts are generously distributed between the cells to assure uniform bulk potential throughout the chip area and prevent latch-up problems. Every cell is supported with a power-down scheme to enable or disable the cell in standby mode for power energy saving. Moreover, it is necessary to keep the cells in standby mode while writing the first configuration pattern to guarantee safe operating conditions rather than passing unknown values from the SIPO memory, which might be physically harmful.

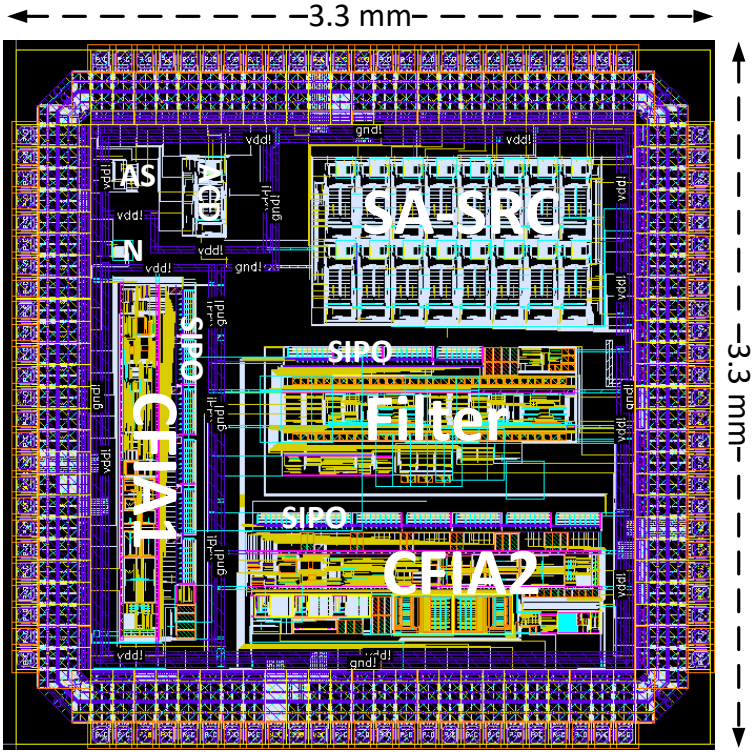

Figure 32. The physical implementation of the prototyping chip.

Table 4. Individual cells of the designed and under manufacturing chip with self-X capabilities.

Cell Nr.	Cell Label	Description
1	CFIA1	CFIA circuit with manual offset calibration
2	CFIA2	CFIA circuit with auto-digital offset autozeroing
3	Filter	Active filter circuit with non-intrusive sensors
4	SIPO	The configuration memory for the corresponding cell
5	Neuron	Modified leaky integrate-and-fire spiking model
6	Adaptive synapse	Emulated biological synapse using emulating CMOS memristor
7	ACD	Two adaptive synapses (AS) and one neuron (N)
8	SA-SRC	Self-adaptive spike-to-rank coding

For the intrinsic evaluation of the proposed indirect measurement methods, the FPGA evaluation board from red pitaya is selected as an edge computing device for the demonstration prototyping. The architecture of our demonstration board is quite similar to the ATE proposed by the Synopses for an infield optimization process [176]. The digital signal synthesizer (DSS) provided by the Xilinx Vivado IP blocks will be used to generate the desired sinusoidal and pulse test stimuli signals for the THD-based measurements. Similarly,

RF ADCs available on the red pitaya board will be used to sample the output response of the DUT. The discrete Fourier transform (DFT) IP block from Xilinx Vivado shall be used to perform the THD measurement. Since the outputs of the PPM and the non-intrusive sensors are quasi-digital, these can be directly interfaced to the programmable logic fabric of red pitaya via general-purpose digital input output pins. The ERPSO algorithm is being implemented on the FPGA by using Verilog hardware descriptive language. Additionally, a parallel-in-serial module is also designed at the output of ERPSO to transfer the parallel configuration bits generated by the ERPSO to the SIPO units of the DUT. The control module is responsible for supervising the infield optimization process, and to perform the data collection and processing. In order to perform the intrinsic robust optimization for the observer imperfections, the control module will pass the output of the ADCs to the shared random access memory (RAM) of the programmable logic (PL) and processing subsystems (PS) available on red pitaya. The concept of robust optimization using the GPR and archive-based will be performed on the PS. After performing the robust optimization, the result will be passed back to the PL, where ERPSO will take its following action based on the cost function of the current solution. In the case of optimization for block cells, 4 to 8 shown in Table 4, all outputs of the DUT are digital. Therefore, those outputs can be interfaced directly to the general purpose I/O pins of the FPGA board. Moreover, the WTA module will be implemented by Verilog language instead of the DFT IP block in Figure 33. Furthermore, the DACs available on the red pitaya board will be used to control the four voltages variables (vg1, vg2, VLEAK, VRFR) for the adaptation purpose explained in the previous section.

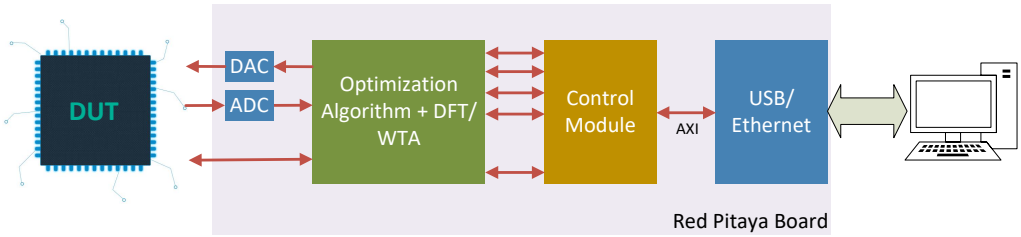

Figure 33. Demonstration board for the designed chip prototype.

Due to the current global chip shortage issue, the chip delivery is delayed; hence, the test result is not yet available. The red pitaya-based demonstration board is prepared for the chip evaluation, as shown in Figure 34a. To replace the breadboard, the PCB design is completed to attach the chip, which shall be housed using a chip zip socket provided by 3M incorporation [199] for the CPGA100 package type as shown in Figure 34b. An appropriate PCB with textool socket will extend the Red Pitaya system to complete the demonstration board, which will be used to explore the following possibilities on our prototyping chip:

- Investigation of the intrinsic optimization of our InAmp to retrieve extrinsic results for the manufactured instance.
- Applying the concept of robust optimization (archive-based and surrogate-based) for addressing the observer imperfections issues.
- Exploration of the LPF indirect performance optimization by using non-intrusive PVT sensors.
- Characterizing the basic operation of the neuron and synapse on the physical hardware level.
- Exploring the supervised and unsupervised optimization possibilities for the ACD and the SA-SRC.

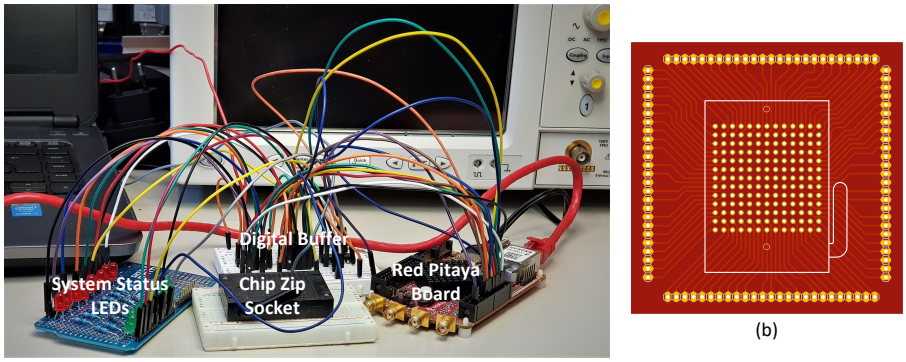

Figure 34. (**a**) Photo of demonstration board with chip zip socket, (**b**) Layout of PCB design for 13 × 13 chip zip socket for the demonstration board.

6. Conclusions

The interface to the real-world by sensors and suitable sensor electronics is of paramount importance for both conventional information processing and computing systems as well as innovative computing systems, e.g., following bio-inspiration from nervous systems or neural networks. The ongoing remarkable rapid advance in integration technologies is giving leverage both to computing systems as well as to an increasing diversity of sensors and sensor systems. Thus, both genericness and robustness as well as efficiency in the interfacing of sensors under the constraints of metrology is required.

The work reported in this paper targets on providing generic, sufficiently accurate, and robust analog front-ends (AFE) for general and intelligent (AI) application systems. Aspired robustness and flexibility are added by self-X (or self-*) properties to AFEX units as the lowest level of a self-X-hierarchy in an advanced application system design. This is pursued in two approaches, the first follows conventional amplitude-domain information representation and processing. The focus in this part of the work is on improvements of circuit assessment and observer robustness, as well as the employed supervised optimization techniques and the finding of the minimum of most sensitive and useful tuning knobs. The second follows pulse or spike domain information representation, largely inspired by nervous systems and neural networks, and introduces the concept of Spiking AFE with self-X properties (SAFEX) by employing both unsupervised neural adaptation and supervised adaptation of system parameter as in the first conventional approach. This is exemplified for the case of an adaptive spike-to-digital converter.

The concepts presented in this work, have been embodied in cells designed in XFAB 0.35 µm xh035 CMOS technology and carefully validated. Extrinsic optimization runs have been carried out, confirming the chosen approach. Essential cells for both AFEX and SAFEX have been combined in a cost-effective prototype chip. For AFEX, two fully differential CFIAs (internal and external offset calibration) and an anti-aliasing filter including the biasing circuits are implemented. It also incorporates the design of on-chip non-intrusive sensors for PVT monitoring to enable cost-effective indirect measurement. A memory size of 66 bytes is designed using SIPO registers to support hot-swappable programming for the in situ configuration/calibration of the AFEX cells. For SAFEX, we implemented the 4-bits SA-SRC to perform the main functionality of the signal conditioning in the spike domain. Furthermore, the three basic cells of the SA-SRC, i.e., neuron, synapse, and ACD are integrated on the chip to examine their characterization independently. The total chip area is 10.89 mm^2 consisting of 62,921 transistors and 100 pads. The pad frame is designed to fit the chip to the CPGA100 package with 61 digital I/O pads, 28 analog pads and 11 power pads. The chip sample is submitted for handling and ensuing manufacturing, but unfortunately will be returning with three months delay in about October. A demonstrator system, including intrinsic optimization of the AFEX and SAFEX components, has been prepared. All extrinsic activities are scheduled to be repeated in the intrinsic mode with one or several chip instances and under varying environmental conditions.

In future work, depending on the test result analysis, after possible redesign to cells, following USIX 1 and 2, a complete USIX 4.0 chip is aspired for the conventional amplitude domain representation with the new concepts and cells. For the SAFEX, as a mid to long term research activity with the potential to be technology agnostic, a complete adaptive sensor-to-spike and spike-to-digital design will be pursued for the selected sensor(s). Extensions to complete generic as well as robust and adaptive SAFEX will be pursued in ongoing and following research.

Author Contributions: Conceptualization, A.K.; methodology, A.K., H.A., S.A. and Q.Z.; software, Q.Z., H.A. and S.A.; validation, Q.Z., H.A. and S.A.; formal analysis, S.A., H.A. and Q.Z.; investigation, H.A., Q.Z. and S.A.; data curation, H.A., Q.Z. and S.A.; writing—original draft preparation, A.K., S.A., Q.Z. and H.A.; writing—review and editing, A.K.; visualization, Q.Z., H.A. and S.A.; supervision, A.K. and Q.Z.; project administration, A.K. All authors have read and agreed to the published version of the manuscript.

Funding: The funding of the named USIX 2 chip by the BMBF (German Federal Ministry of research), program: SElekt_I40, consortial project: MoSeS-Pro, subproject: 'Robuste adaptive integrierte Sensorelektronik und Informationsverarbeitung mit Self-X-Eigenschaften für zuverlässige Systeme der Industrie 4.0', grant no. 16ES0425 is gratefully acknowledged.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: The authors would like to thank the DAAD (Deutscher Akademischer Austauschdienst) for sponsoring the PhD researchers. We would also thank EUROPRACTICE for their support in providing design tools and MPW fabrication services for our prototype chip and research activity.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AFE	Analog-front-ends
USIX	Universal-Sensor-Interface-with-self-X-properties
AFEX	Analog-front-ends with self-X properties
SAFEX	Spiking-analog-front-ends with self-X properties
CISS	Cognitive integrated sensory systems
SLM	Silicon Lifecycle Management
EHW	Evolvable hardware
PSO	Particle swarm optimization
ATE	Automatic test equipment
CFIA	Current-feedback in-amp
SIPO	Serial-in, parallel-out register
PPM	Power monitoring module
MHOAs	Meta-heuristic optimization algorithms
ERPSO	Experience replay particle swarm optimization
GPR	Gaussian process regression
OIs	Observer Imperfections
SSDCα	Sensor to spike to digital converter
SSC	Sensor-to-spike converter
SDC	Spike-to-digital converter
ITDs	Interaural time differences
SA-SDC	Adaptive spike-to-digital converter
SA-SRC	Self-adaptive spike-to-rank coding
ACD	Adaptive coincidence detection
LIF	Leaky integrate and fire

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