Integrated shadow mask method for patterning small molecule organic semiconductors

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We have developed a simple and efficient method for patterning small molecule semiconductors for applications in the field of organic electronics. In our approach, a profile is created using a single layer of photoresist, defining the regions where the organic semiconductor is to be deposited. Subsequent deposition of a small molecule semiconductor results in a discontinuity of the semiconductor film at the photoresist edge. The resulting transistor characteristics have an off current that is systematically below 1 pA. We demonstrate both *p*-type and *n*-type organic thin-film transistors using this method, using pentacene and copper hexadecafluorophthalocyanine ($F_{16}CuPc$), respectively. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2182008]

Organic electronics is a field that has attracted the attention of both industrial and academic research groups. The performance of both polymeric and small molecule organic thin-film transistors (OTFTs) has improved considerably in the last few years. Several research groups have reported on pentacene OTFTs with field-effect mobilities μ higher than 1 $cm^2/V\,s$, bringing the performance of these devices at the same level as or even higher than that of amorphous silicon (*a*-Si:H) TFTs.[1–4]

Display applications are a particularly important driver for the continuing efforts in the field of organic electronics. Displays using OTFTs as the driving backplane have been realized, both on glass[5] and on flexible polymeric substrates.[6,7] In order to limit contrast degradation of the display, the off current of the driving transistor needs to be in the range of 10 pA or lower.[8] In other applications of organic electronics, like the fabrication of digital logic circuits, it is desired to be able to switch the OTFT completely off as well, for reasons of stability (reduction of cross talk) and power consumption.

Currents in the range of a few pA cannot be reached without patterning the organic semiconductor. For pentacene OTFTs, the off-current I_{off} of an unpatterned device is typically in the range of 1–10 nA. This clearly demonstrates the need for patterning the semiconductor. Patterning leads to the elimination of parasitic leakage paths, resulting in a significant decrease of I_{off}. At the same time, one should ensure that the patterning process does not lead to a degradation of the field-effect mobility μ and the threshold voltage V_T, as these parameters (among others) determine the on current of the device.

One method to pattern the organic semiconductor is by photolithographically defining a photoresist profile after the organic semiconductor deposition. This has been realized with a water-soluble poly(vinyl alcohol)-based photoresist,[9] as well as with a regular solvent-based photoresist, using parylene as a coating between the organic semiconductor and the photoresist.[10] A subsequent dry etch step results in an effective patterning of the active areas of the OTFTs.

Another method, avoiding the etch step of the organic semiconductor, consists of evaporating the semiconductor through a shadow mask.[11] Aligning the shadow mask to the existing OTFT substrate, however, requires special equipment.

In order to overcome these problems, one could create a reentrant profile prior to the deposition of the semiconductor. This in fact forms a shadow mask that is integrated with the substrate. Upon vacuum deposition, the organic semiconductor breaks across the profile, resulting in isolated OTFT active areas. This method has been demonstrated using a double-layer photoresist profile,[12] as well as using a patterned multilayer of dense SiO_2, porous SiO_2 and Si_3N_4.[13]

We have realized an integrated shadow mask by patterning one single layer of photoresist. Devices were processed on a highly doped Si wafer, acting as the substrate and the gate electrode. The gate dielectric was formed by thermally growing a layer of 100 nm SiO_2. The source and drain electrodes consist of 20 nm of Au, patterned by photolithography and lift-off. Subsequently, a layer of the negative photoresist SU-8 25 (purchased from MicroChem Corp.) was spin-coated. Processing of the SU-8 25 leads to a patterned layer of about 20 μm thickness. Subsequent to the SU-8 processing, the substrate was thoroughly cleaned and treated with octadecyl trichlorosilane and dodecanethiol self-assembled monolayers. As a last step, a layer of 30 nm purified pentacene was deposited in ultrahigh vacuum ($p=10^{-8}$ Torr). The deposition flux was 0.25 Å/s, and the substrate temperature was 65 °C.

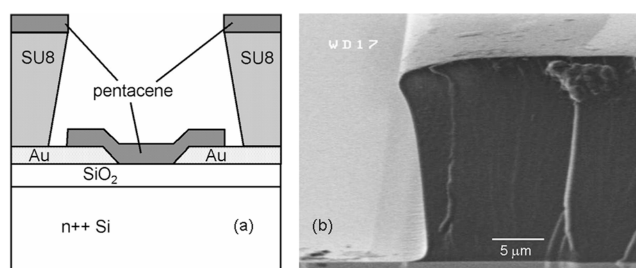

FIG. 1. (a) Schematic cross section of an OTFT with patterned pentacene layer; (b) scanning electron microscope image of a cross section of the integrated shadow mask.

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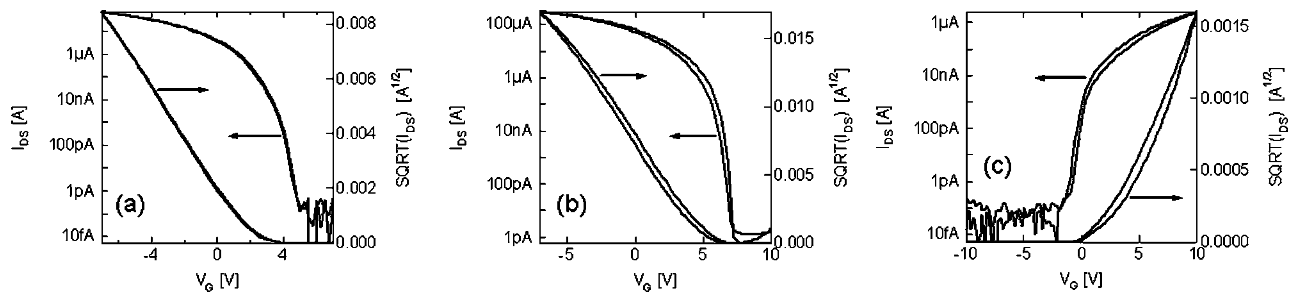

FIG. 2. $I_D - V_G$ measurement of OTFTs patterned by an SU-8 25 profile: (a) pentacene OTFT processed on Si (V_{DS}=−7 V; W/L=400/5; μ=0.67 cm^2/V s; V_T=2 V; S=0.22 V/dec; I_{on}/I_{off}=8.10^8); (b) pentacene OTFT processed on glass (V_{DS}=−7 V; W/L=5000/10; μ=0.22 cm^2/V s; V_T=5 V; S=0.17 V/dec; I_{on}/I_{off}=5.10^8); (c) F_{16}CuPc OTFT processed on Si (V_{DS}=10 V; W/L=5000/10; μ=5.10^{-3} cm^2/V s; V_T=2.5 V; S=0.44 V/dec; I_{on}/I_{off}=5.10^8).

The cross section of the device is schematically shown in Fig. 1(a). As shown by the cross-section scanning electron microscope image in Fig. 1(b), it is clear that the walls of the photoresist are slightly reentrant, which is typical for negative photoresists.[14] The cleaning and surface treatment of the substrate have no influence on the profile. The photoresist profile effectively prohibits the formation of a continuous film during the semiconductor deposition. In other words, the SU-8 25 layer breaks the semiconductor layer, resulting in patterned active areas. This can be verified in Fig. 1(b), showing a layer of 30 nm of pentacene evaporated through the shadow mask. As can be seen, the edge of the pentacene active area on the substrate is clearly visible, demonstrating the effectiveness of this patterning method. The highest temperature used in the processing of SU-8 25 is 95 °C. The low thermal budget of this patterning method makes it compatible with production on flexible substrates.

We have measured OTFTs that were fabricated following the described method. After the deposition of pentacene, the samples were transported through air and measured in a N_2 atmosphere using an Agilent 4156C parameter analyzer. The transistor parameters were extracted from the transfer curve in the saturation regime. Typical values for the field-effect mobility μ were in the range of 0.6 cm^2/V s. The threshold voltage V_T was typically 2 V. I_{off} was systematically below 1 pA, being the noise level of our measurement setup. The on-off current ratio I_{on}/I_{off} was always higher than 10^8. The average subthreshold slope was in the range of 0.2 V/dec. The hysteresis was negligibly small. Figure 2(a) shows a representative transfer curve of a pentacene OTFT in the saturation regime.

The patterning method was also applied to a pentacene OTFT processed on glass. Devices were processed on Corning EAGLE^{2000} glass substrates. The gate consists of a layer of 20 nm of TiW, patterned by optical photolithography and lift-off; 100 nm of SiO_2 was sputtered to act as the gate dielectric. Vertical interconnects were defined by wet etching. Source and drain electrodes consist of 25 nm of Au. Subsequently, the integrated shadow mask and the pentacene layer were deposited as described above. After the SU-8 processing and the pentacene deposition, not a single processing step was taken. As can be verified in Fig. 2(b), the general performance of an OTFT processed on glass is comparable to a device processed on Si. In the context of this letter, it should be specifically noted that there is virtually no difference in I_{on}/I_{off} between the two devices. Like the OTFTs processed on Si, the devices processed on glass show a remarkably steep subthreshold slope S, being systematically in the range of 0.2 V/dec. It can be noticed that the off current of this device is not limited by the noise level of our setup. This is attributed to the fact that the gate current of an OTFT processed on glass is in the range of 1–10 pA, while that of an OTFT processed on Si is below 1 pA. Indeed, thermally grown SiO_2 is superior to the low-temperature sputtered SiO_2 we used. Nevertheless, an off current in the range of 1 pA is an excellent figure.

In order to demonstrate the general applicability of this patterning method, we have also fabricated *n*-type OTFTs. The *n*-type organic semiconductor copper hexadecafluorophthalocyanine (F_{16}CuPc)[15] was deposited on a Si substrate that was prepared in the same way as for the case of pentacene, as described above. Patterned F_{16}CuPc OTFTs were measured in a N_2 glovebox, immediately after deposition. A typical transfer curve of an *n*-type OTFT is shown in Fig. 2(c). It can be seen that I_{off} is below 1 pA, showing that the *n*-type semiconductor F_{16}CuPc is patterned as effectively as the *p*-type semiconductor pentacene.

It should be mentioned that the patterning of an *n*-type organic semiconductor is difficult using a lithography and etching process, because of the rapid degradation of the semiconductor in the presence of air and moisture.[16] Hence, the patterning method proposed in this letter is a unique technology, as it allows for the patterning of small molecule *n*-type organic semiconductors with photolithographic resolution, while at the same time avoiding degradation.

In conclusion, we have demonstrated a simple method for patterning small molecule organic semiconductors. The method consists of patterning a thick and reentrant profile of a single negative photoresist (SU-8 25) prior to the semiconductor deposition. Upon deposition, it is not possible for the semiconductor to grow as a continuous layer on the photoresist walls. This effectively results in a patterned semiconductor film in the active areas of the OTFTs. The method provides a particularly simple way for patterning *n*-type small molecule organic semiconductors, since all possible sources of degradation are avoided. Finally, the thermal budget of the method is compatible with production techniques on flexible substrates.

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