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Integrated Silicon Microbeam PI-FET Accelerometer

PAU-LING CHEN, RICHARD S. MULLER, SENIOR MEMBER, IEEE, RICHARD D. JOLLY, GREGORY L. HALAC, STUDENT MEMBER, IEEE, RICHARD M. WHITE, FELLOW IEEE, ANGUS P. ANDREWS, MEMBER, IEEE, TEONG C. LIM, AND M. E. MOTAMEDI, SENIOR MEMBER, IEEE

Abstract—**Integrated accelerometers showing excellent linearity have been designed and fabricated using silicon planar technology, zinc-oxide sputtering, and anisotropic etching. Small cantilevered beam structures overcoated with piezoelectric ZnO films act as force transducers, and the electrical signal is directly coupled to the gate of a depletion-mode, p-channel MOS transistor. The accelerometers have a nearly flat response from very low frequencies until beam resonances become significant (above 40 kHz). The near-dc response results from completely isolating the piezoelectric film from electrical leakage paths. Measured performance has matched very well with theory. Theoretical analysis has been used to derive useful design tradeoffs.**

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P-L. Chen, R. S. Muller, G. L. Halac, and R. M. White are with the Department of Electrical Engineering and Computer Sciences, and the Electronics Research Laboratory, University of California, Berkeley, CA 94720.

R. D. Jolly was with the Department of Electrical Engineering and Computer Sciences, and the Electronics Research Laboratory, University of California, Berkeley. He is now with Hewlett-Packard Laboratories, Palo Alto, CA.

A. P. Andrews, T. C. Lim, and M. E. Motamedi are with Rockwell International Corporation, Thousand Oaks, CA 91360.

INTRODUCTION

EXCELLENT experimental performance has been observed on integrated accelerometer structures that were fabricated using capacitive PI-FET transducers [1] to detect strains in miniature cantilever beams. The beams are composite structures consisting of Si, SiO_2, ZnO, metal, and passivating oxide (Fig. 1). They are formed by anisotropically etching the silicon [2] from underneath the layered structures using an aqueous solution of ethylenediamine and pyrocatechol (EDP) in the manner described by Petersen [3], or else by a combination of backside and frontside etching of the wafer as described by Roylance and Angell [4]. The piezoelectric strain-sensing layers are directly coupled to depletion-type, p-channel MOS transistors. Dependent on the fabrication procedures employed, the total beam thicknesses are either below 5 μm (for top-surface etching), or else range to about 50 μm (for etching from both sides of the wafer).

Most of the previous work with thin-film ZnO transducers has been directed at SAW applications in which strain waves have characteristically very high frequencies (above 10 MHz). For an accelerometer, on the other hand, low frequency and

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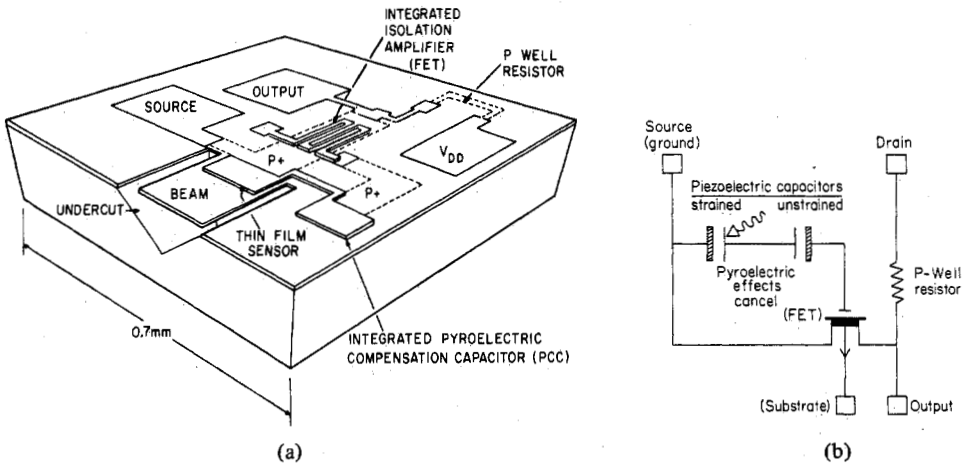


Fig. 1. (a) Integrated accelerometer formed by anisotropic etching and planar technology. The compensation ZnO capacitor is used to reduce temperature sensitivity by differentially removing the pyroelectric effect. (b) Equivalent circuit for the accelerometer shown in Fig. 1(a).

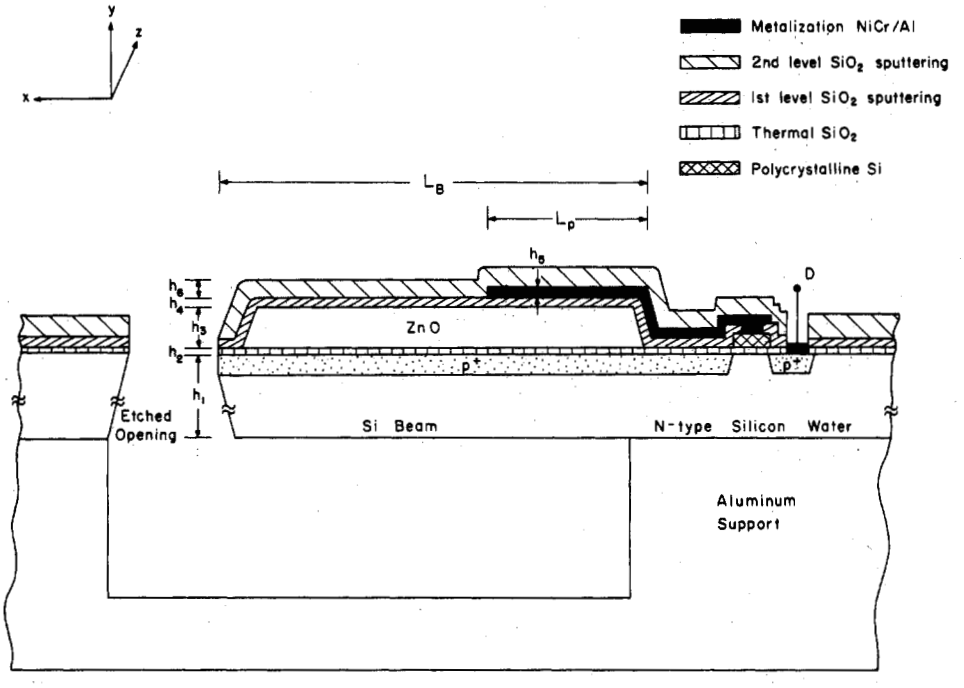


Fig. 2. Cross section of the beam portion of an accelerometer formed by two-sided etching.

even dc strain response is desirable. By encapsulating the ZnO film entirely within insulating layers that are thin relative to the Debye length within the piezoelectric ZnO, we have been able to obtain a near-dc response in the overall structure. The insulating layers consist of an underlying film of thermally grown SiO_2 and an overlaying film of sputtered SiO_2. This construction has led to a measured decay time for a stress-induced signal of approximately seven days even though the dielectric relaxation time of the sputtered ZnO is only about 1 ms [5].

Theory

A cross section of the accelerometer is shown in Fig. 2. Its operating principles can be described as follows. When an inertial force strains the cantilever beam, the piezoelectric ZnO becomes polarized. The resultant surface charge on the ZnO is coupled capacitively to the gate of the p-channel, depletion-mode FET and an amplified output voltage is then obtained at the drain. The polarized charge density can be calculated from the equation

$$D_i = e_{ikl} S_{kl} + \epsilon^s_{ik} E_k \tag{1}$$

where D is the electrical displacement, E is the field, S is the strain, and e and ϵ are the piezoelectric and dielectric coefficients, respectively. The low-frequency piezoelectric response of the ZnO capacitor in the bending mode can be modeled by the circuit shown in Fig. 3 in which C_{d1} and C_{d2} represent the two SiO_2 capacitors which are sandwiched on either side of the ZnO film. If the Si beam thickness is not much greater than the composite ZnO layer thickness, the strain within the

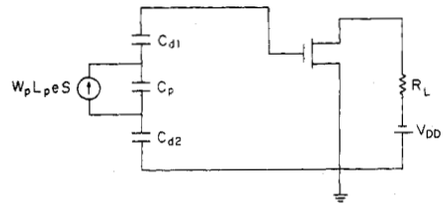


Fig. 3. Equivalent circuit of a simple (noncompensated) accelerometer.

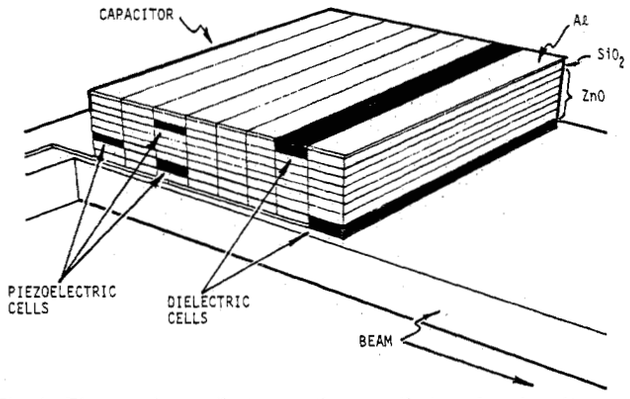


Fig. 4. Elemental contributors to the overall piezoelectric voltage.

piezoelectric film is not localized but is a function of x and y. Therefore, a distributed circuit model, as shown in Fig. 4, has to be used to analyze the structure. In Fig. 4, we divide the ZnO layer into infinitesimal cell stripes that are uniform across the beam (since the strain is uniform in that dimension). Straightforward mathematical analysis using (1) on the model of Fig. 4 and the equivalent circuit of Fig. 3 leads to the following expression for the induced piezoelectric voltage at the MOS gate:

$$V = \frac{W_P L_P e \bar{S}}{C_G + C_P + C_P C_G (C_{d1} + C_{d2})/C_{d1} C_{d2}} \tag{2}$$

where W_P and L_P are the width and length of the ZnO capacitor layer, respectively, e is the piezoelectric constant, and C_P and C_G are the capacitances of the piezoelectric layer and of the FET gate, respectively. $\bar{S}$ is the strain averaged over the thickness and length (along the beam) of the ZnO piezoelectric capacitor.

The overall expression for the averaged strain is algebraically complicated, but quite readily derived. It shows that the principal design parameters specifying sensitivity and dynamic range are: the beam thickness, the ratio of the length of the piezoelectric capacitor to the beam length, the piezoelectric-layer thickness, the overall beam length, and the position and magnitude of any proof mass that might be used. Relevant design tradeoffs derived from the theoretical investigation are described in a separate section. We confine our discussion here to mentioning one important consideration in the design of a beam accelerometer, the role of the neutral axis in the beam. Since there is a null output if the neutral axis of the beam system is situated midway within the piezoelectric film, the designer must consider and avoid this eventuality as variations are made in the thicknesses and densities of overlaying films.

A simple case occurs when the Si layer is thick compared to the total thicknesses of all other layers forming the beam. In this case, the strain at the clamped end is found to be [6]

$$\bar{S} = \frac{3\rho a L_B^2}{E_Y h} \tag{3}$$

where a is the acceleration of the beam end, ρ is the Si density, L_B the beam length, E_Y Young's modulus for Si, and h the thickness of the beam. The maximum g loading that the beam can sustain can be calculated by inserting the yield limit for Si ($S = 10^{-3}$) into (3). This maximum strain value, obtained by experiment, is roughly consistent with measurements of the fracture strength of Si [7] reported by Chen which showed a 50-percent failure probability for chemically polished Si wafers of 2.17, 2.78, and 4.96×10^8 N · m^{-2}, respectively, for twist, cylindrical bending, and biaxial stressing. The resonant frequency of the beam is given by the formula [8]

$$f \simeq 0.16 \sqrt{E_Y/\rho} \left[\frac{h}{L_B^2}\right]. \tag{4}$$

All of the beams designed for the accelerometer studies have resonant frequencies above 40 kHz which is appreciably higher than the typical frequencies of interest.

Design Tradeoffs

A desktop computer has been programmed to evaluate design tradeoffs between the various microbeam parameters. An example of the useful design information that can be extracted from these programs, which are based on the distributed model of Fig. 4, is shown in Figs. 5 and 6. The figures refer to an accelerometer design that has been extensively studied theoretically, but not yet fabricated. The design is for an accelerometer that is specified to have a nominal scale factor of $\frac{1}{3}$ mV/g (at the gate of the FET), a 300g operating range, and a linear range of 100 mV. The peak strain sensitivity, constrained in the design to be less than 0.1 ppm/g, occurs at the beam root on the outside surface.

In the tradeoff curves, shown in Figs. 5 and 6, the design conditions satisfying the scale-factor constraint are shown by solid lines. The design limits imposed by the strain-sensitivity constraint are shown by dotted lines. A "design envelope" is defined by the intersections of these two types of lines, hence the region outside this envelope is labeled "forbidden zone" in the figures. The two figures display the same data, but in alternative formats which give different insights into the tradeoffs that can be made in designing the accelerometer.

In Fig. 5, the curves correspond to differing Si thicknesses. Each solid curve shows values of beam length and thickness of the ZnO film which yield the design scale factor. The curves terminate at the heavy solid curve where they intersect the corresponding strain-limit curve (dotted). This curve represents the boundary of the design envelope. Note that this boundary is essentially horizontal on the upper right corner, which indicates that the minimum thickness of the ZnO layer is about 1.2 μm, and this limit is reached at beam lengths of about 3 mm.

A similar limiting length is apparent in the curves of Fig. 6. The solid curves on this graph correspond to the simultaneous values of the Si and ZnO thicknesses which yield the design scale factor for fixed values of the beam length. As the beam lengths decrease from 3 to 1.1 mm, the curves move to the upper right, and eventually disappear after the 1-mm curve.

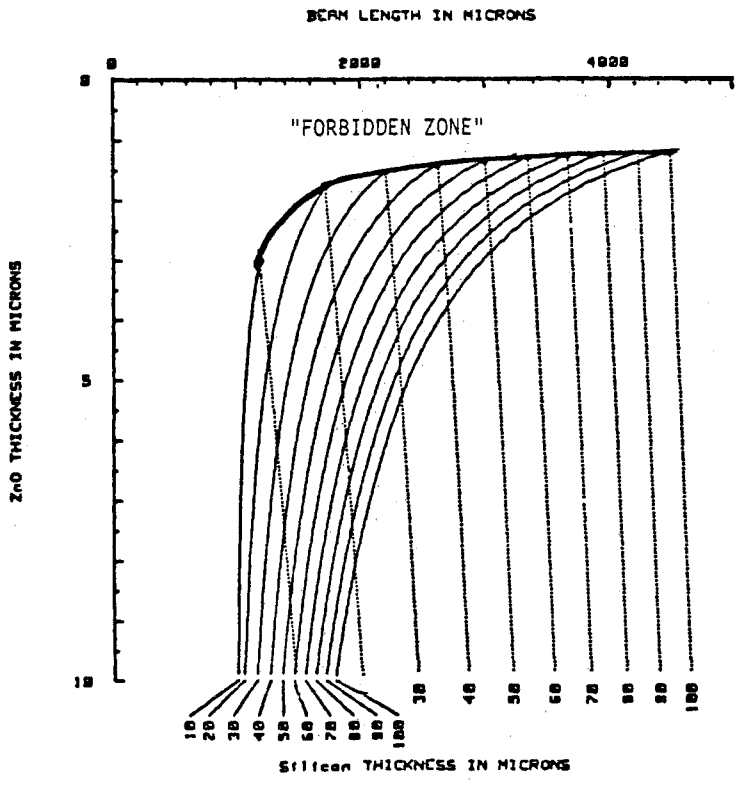


Fig. 5. Tradeoff curves illustrating the effect of variable ZnO thickness, Si-beam thickness, and beam length. All curves on the family have the same sensitivity.

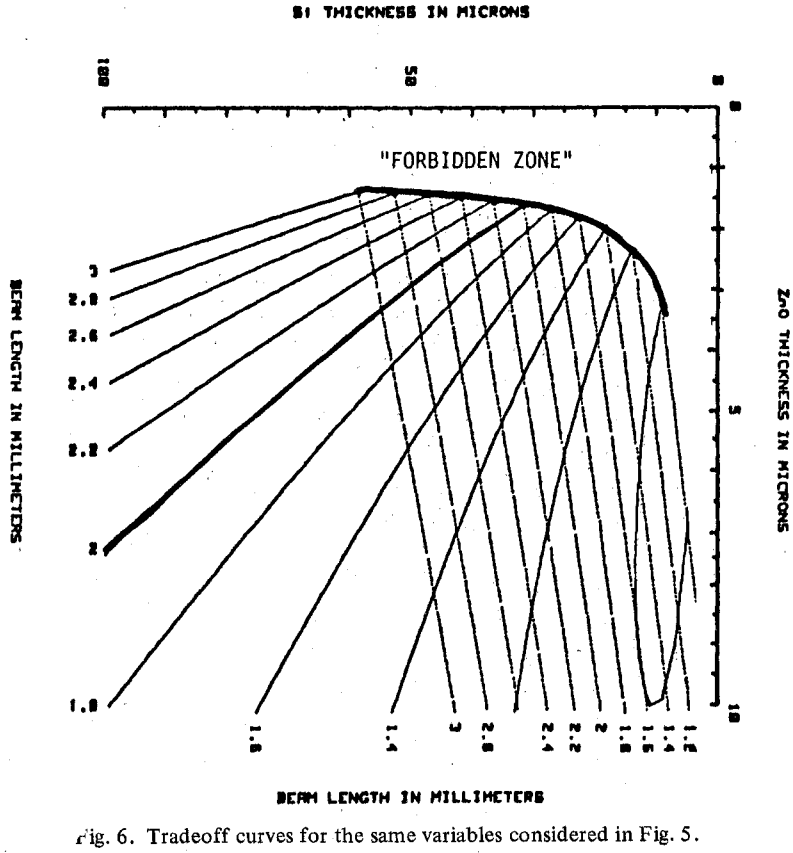


Fig. 6. Tradeoff curves for the same variables considered in Fig. 5.

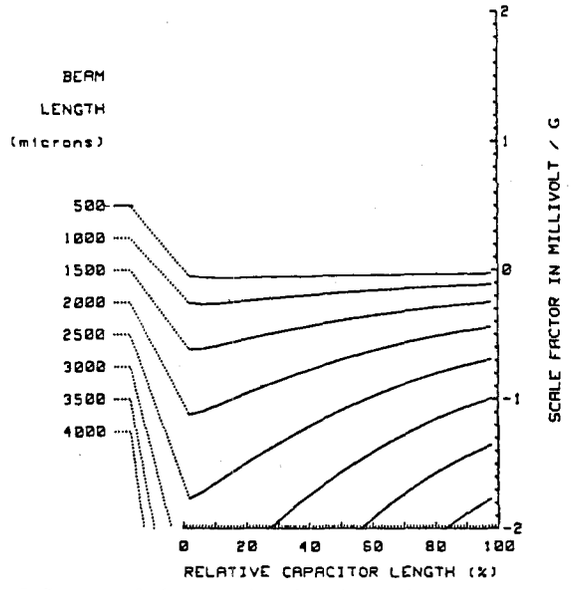


Fig. 7. Influence of the capacitor length on the accelerometer scale factor.

This indicates that there is a lower limit on the beam length between 0.8 and 1 mm for the sensitivity required in this design.

The design parameters that are not varied in these tradeoffs are shown in Table I. These constant parameters include the thicknesses of other layers in the beam and the relative surface dimensions of the beam and piezoelectric capacitor.

The influence of the length of the piezoelectric capacitor on scale factor was evaluated independently. The design tradeoff curves for capacitor size are shown in Fig. 7. The thickness of the ZnO layer was assumed to be 2 μm and the Si layer was taken to be 6.25 μm. These curves show a decrease in scale factor as the capacitor length is made an increasing fraction of the beam length. This behavior results from the extra loading on the strain-induced signal by the parasitic capacitance in the relatively nonstrained region of the cantilever toward its free end. For a capacitor design length equal to 25 percent of the beam length, the scale factor is roughly 80 percent of the maximum value, and this design has been used generally.

Fabrication

The fully integrated accelerometer structure was produced using a seven-mask IC process. Except for the ZnO sputtering and the anisotropic etching step, standard Si-gate, PMOS processing was employed. The substrate material was 10-$\Omega \cdot$ cm n-type ⟨100⟩ Si. After following the conventional MOS IC fabrication steps through field-oxide growth, windows for the gate and active sensor region are opened and thin thermal SiO_2 is grown. Following a 35-keV threshold-adjusting B implant (dosage = 1.75×10^{12}), a polysilicon gate is deposited and patterned. The next step is a heavy implant of B through the thin oxide (BF_2 dosage = 1×10^{16} at 180 keV). This implant dopes the Si surface strongly p-type in order to stop the EDP etch and also to define the source and drain regions and to dope the polycrystalline Si gate.

A 2-μm film of piezoelectric ZnO is laid down by planar magnetron sputtering [9]. The ZnO is then patterned to have a slope of about 70° at its edge using a dilute combination of acetic and phosphoric acids in order to improve step coverage by subsequent depositions. An overlying sputtered SiO_2 layer prevents leakage of charge across the surface and helps to assure nearly dc response for the accelerometer. Metal connections consisting of Al and NiCr layers are evaporated and patterned, and a final thick SiO_2 layer is sputtered and overlain with a gold layer for the purpose of EDP etch resistance and surface passivation.

TABLE I
Profiles of Beam Layers

Dimension μm	Material
(top) 1.5	Au-Ti
5.0	Sputtered SiO_2
0.4	Al-NiCr
0.5	Sputtered SiO_2
varied	ZnO
0.10	Thermal SiO_2
(bottom) varied	Si

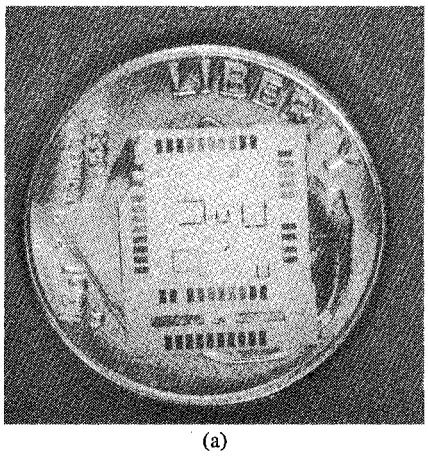
The process is IC compatible; neither the SiO_2 nor the ZnO sputtering have been observed to affect the FET parameters. Etching to delineate the Si beam [10] has been carried out in one of two ways. Direct etching in EDP results in a Si beam that is on the order of 1 to a few micrometers thick. A thicker beam can be made by using double-sided etching. For this latter process, the front surface is covered and etching begins from the back. This process continues for 2 h for a 50-μm-thick wafer and then the front pattern is uncovered so that etching proceeds from both sides until the beam is formed. The thickness of the beam is controlled by the width of the window opened to the EDP etch.

A modeling program has been found helpful to predict the shapes of EDP etch patterns in Si. The program makes use of an HP 9845 desktop computer and takes as input data the window dimensions opened to the EDP etch, the orientation of the Si wafer, and the temperature of the etch. The model was derived from experiments with different surface geometries and has been validated by stereographic SEM images. Its output is a plot of the predicted evolution of the etched surface geometry.

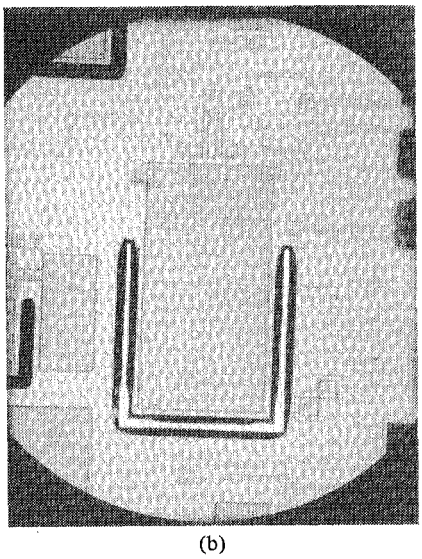
Fig. 8 shows a completed chip containing several accelerometers. On the chip are six sets of beam width/length ratios which have mask dimensions of: 70/235, 200/225, 275/510, 410/505, 500/570, and 950/1240 μm. The range in sizes was taken in order to achieve sensitivities to various g values and to determine processing constraints. The larger beams, processed by two-sided etching, have Si beam thicknesses of 50 μm and a ZnO layer thickness of 1.7 μm.

Results

An Unholtz-Dickie Model 351 Recording Vibration Calibration system was used to investigate the performance of several of the beams. This system consists of a controlled shake table



(a)



(b)

Fig. 8. (a) Chip photograph showing six versions of the accelerometer. Two structures are compensated with pyroelectric compensation capacitors, two are uncompensated, and two structures have no amplifiers on chip. (b) 950/1240 μm beam without temperature compensation.

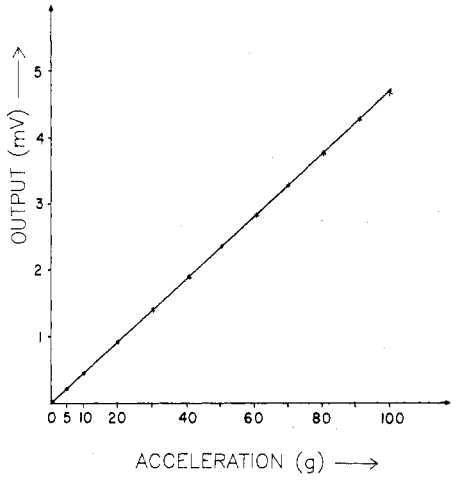


Fig. 9. Measured output (at the FET gate) versus acceleration in g for a 950/1240 μm beam.

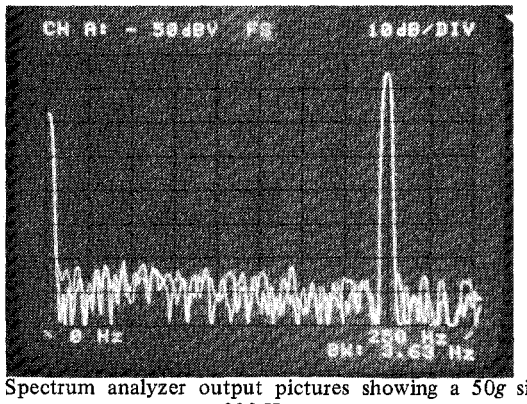


Fig. 10. Spectrum analyzer output pictures showing a 50g signal at 200 Hz.

which incorporates a carefully calibrated reference accelerometer. It can be programmed to test a specimen over a wide range of g values and frequencies. A series of measurements was carried out on the 950/1240 μm beam which had been designed to have a scale factor of 44 μV/g. The depletion-mode, p-channel MOSFET had a threshold voltage of +1.5 V and the load resistance was 1 kΩ. Fig. 9 is a plot of the measured output voltage (at the FET gate) at 200 Hz as the acceleration is increased from 5 to 100g. The indicated scale factor is 47 μV/g, which is very close to the theoretical design value. The response is also seen to be extremely linear—the measured nonlinearity is lower than 0.8 percent. At accelerations less than 50g, the nonlinearity is below 0.2 percent. This extreme linearity is a very useful property of the accelerometer.

A Hewlett-Packard model 3582A spectrum analyzer was used to investigate signal and noise characteristics. The noise spectrum for the device appears to be white. Fig. 10 is an oscilloscope trace showing the spectrum of the output signal with an input acceleration of 50g applied at 200 Hz. The noise at this g value is 60 dB below the signal or equivalent to 0.05g for a 3.63-Hz bandwidth.

The accelerometer was expected to have a nearly flat sensitivity from dc to frequencies that approach the beam resonance. To study the frequency response, the accelerometer was coupled to the spectrum analyzer through a series capacitor (in order to block the dc voltage at the MOS drain). The frequency response was then measured at 50 and 100 Hz, and then in 100-Hz intervals to 1 kHz at 5g input excitation. Fig. 11 is a superposition of the images from the spectrum analyzer obtained during this test. The coupling capacitor introduces a zero at roughly 100 Hz which is responsible for the low-frequency rolloff. The small apparent increase in sensitivity at higher frequencies is thought to be a result of mechanical resonance in a light-tight housing which enclosed the device. From these data, we can see that the equivalent noise at the input over the entire frequency range is 40 dB down from the 5g signal in the 14.5-Hz bandwidth passed by the spectrum analyzer. The beam used for these studies was designed to sense accelerations ranging to 1000g, and, therefore, not to have the highest sensitivity. The observed sensitivity could readily be improved by adding proof mass. The design, construction, and fabrication of beams that make use of added

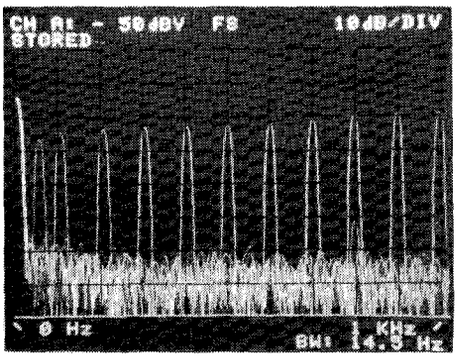


Fig. 11. Spectrum analyzer output showing the frequency response from 50 to 1000 Hz for a 5*g* signal.

proof masses is presently under study and will be reported on at a later time.[1]

As described earlier, several of the accelerometer structures are partially temperature compensated by the addition of an unstrained ZnO capacitor to balance out the voltage produced by pyroelectricity in the ZnO. Earlier research had shown this effect to be the most influential cause of temperature sensitivity [11]. Preliminary studies on the beam accelerometers have shown that the compensating capacitor essentially cancels the pyroelectric effect, and the remaining temperature sensitivity is essentially that of the p-channel MOSFET. The percentage change in $I_D/°C$ has been measured as - 0.16 percent.

An important result of this research is the demonstration that by isolating the ZnO and passivating the overall circuit with deposited SiO_2 layers, there can be an extremely slow decay in the piezoelectric response to a static load. By coupling the output of the piezoelectric film capacitor through a depletion-mode MOS transistor, we have been able to achieve a near-dc response in the integrated accelerometer structure. Measurements of the response to an applied static load on the cantilever have indicated a time constant for the decay of the piezoelectrically induced voltage of seven days.

The results summarized in this section validate the design concepts for the integrated accelerometer, and point the way toward fully integrated systems in which on-chip signal processing can simplify the design of control systems.

[1] Measured results on an accelerometer with the geometry described in this paper except for a proof mass formed by unetched Si at the free end have a sensitivity of 1.5 mV/*g* and a flat response from 3 Hz to 3 kHz.

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