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Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip

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Electronic and photonic technologies have transformed our way of living – from computing and mobile devices, to information technology and the Internet. Our future demands in these fields require innovation in each technology separately, but also depend on our ability to harness their complementary physics through integrated solutions [1, 2]. Today, this goal is hindered by the fact that the majority of silicon nanotechnologies that enable our processors, computer memory, communications chips, and image sensors, utilize bulk silicon substrates, a cost-effective solution with an abundant supply chain, but with significant limitations for the integration of photonic functions. Here, we aim to address this challenge by bringing photonics into bulk silicon complementary metal-oxide-semiconductor or 'bulk CMOS' chips using a deposited layer of poly-crystalline silicon (polysilicon) on silicon oxide (glass) islands fabricated alongside transistors. We have used this single deposited layer to realize optical waveguides and resonators, high-speed optical modulators, and sensitive avalanche photo-detectors. We have integrated this photonic platform with an entire 65 nm bulk CMOS process inside a 300 mm-wafer microelectronics foundry. We have implemented integrated high-speed optical transceivers in this platform operating at 10 Gb/s, composed of millions of transistors, and arrayed on a single optical bus for wavelength division multiplexing (WDM), to address the immediate demand for high-bandwidth optical interconnects in data-centers and high-performance computing [3, 4]. By decoupling the formation of photonic devices from transistors, the demonstrated integration approach can achieve many of the goals of multi-chip solutions [5], with the performance, cost advantage, and scalability of monolithic platforms [1, 6–8]. As transistors are scaled beyond 10 nm in the near future [9], and as new nanotechnologies emerge [10,11], this approach can provide the means for integration of photonics with the state-of-the-art in nanoelectronics.

Sustained innovations in electronics, predominantly in CMOS, have transformed computing, communications, sensing, and imaging. More recently, Silicon Photonics has been leveraging the CMOS infrastructure to address the growing demands for optical communications for Internet and data-center networks [3, 6, 7]. This convergence of photonics with CMOS is very promising to create a new paradigm in electronic-photonic technologies: processor and memory chips with high-bandwidth optical input/output [1, 4], communications chips with high-fidelity optical signal processing [2, 12], and highly parallel optical biochemical sensors for blood analysis [13] and gene sequencing [14]. To make these aspirations a reality, photonic devices need to be integrated with a variety of nanoelectronic functions (digital, analog, memory, storage, etc.) on a single silicon die.

Monolithic integration of photonic devices in close proximity to electronic circuits is crucial for two main reasons: it allows us to simultaneously achieve the required levels of performance, scalability, and complexity for electronic-photonic systems; and significantly accelerates system-level innovation by enabling a cohesive design environment and device ecosystem to realize entire 'systems on a chip' (SoC). In fact, the accelerated progress in recent years in electronics is a direct result of such a SoC approach and the addition of new functions and components to CMOS to create new monolithic device platforms – wireless communications and Radar imaging chips (through the addition of inductors and transmission lines [15]), and image sensors (through silicon photodiodes [16]).

The greatest challenge toward the integration of photonic circuits into CMOS has been the lack of a semiconductor material with suitable optical properties for realizing active and passive photonic functions in bulk CMOS, the dominant manufacturing platform for microelectronic chips (every Intel, Apple, and Nvidia CPU/GPU, all computer memory and Flash storage, etc.). As a result, all of the efforts, to date, for the integration of photonics into CMOS have been limited to silicon-on-insulator (SOI) substrates [1, 6–8]. These processes are cost prohibitive for many

applications (e.g., computer memory) and have a limited supply chain for high volume markets. The same photonic integration challenge also exists for the leading CMOS technologies below 28 nm transistor nodes (FinFET and thin-body fully-depleted SOI [17] (TBFD-SOI)) where the crystalline silicon layers are too thin (less than 20nm) to support photonic structures with sufficient optical confinement. To address these integration challenges, we have developed a photonic platform for high-speed and low-power operation using an optimized polysilicon film that could be deposited on silicon oxide islands that are ubiquitous in CMOS (utilized to isolate transistors) even in the most recent technologies using FinFET and TBFD-SOI [17] (Fig. 1a).

Deposited electronic and photonic devices on glass have already impacted many fields: thin-film transistors (TFT) have enabled today's display technologies, and photonic platforms with thin-film components on glass have seen their commercial deployment in optical communications systems [18]. However, deposited photonic components have been restricted to passive functions (e.g., filters and delay lines) lacking light detection and modulation. A variety of materials including amorphous and polycrystalline silicon [19–21], polymer-based devices [22], and chalcogenides [23] have been investigated for deposition onto glass for realizing active photonic components. Nevertheless, the integration of a fully functional photonic platform (i.e., passive functions, optical modulators and detectors) and its integration with CMOS nanoelectronics is yet to be demonstrated. In this work, we have integrated a fully functional polysilicon photonic platform with a 65 nm bulk CMOS process through the addition of a few extra processing steps without affecting transistors native performance, and demonstrated large-scale monolithic electronic-photonic systems.

Fig. 1a shows transistor structures in today's three dominant deeply-scaled CMOS processes. The silicon oxide shallow trench isolation (STI) for transistors in advanced CMOS nodes is too thin to support low-loss optical waveguides on top of this layer due to light leakage into the substrate.

We address this issue by locally adding a thicker silicon oxide photonic isolation layer (□1.5 μm) with a fabrication process very similar to STI. An optimized polysilicon film (220 nm thick) with low optical propagation loss and high carrier mobility is then deposited on this layer, and is used for passive photonic components, free-carrier plasma dispersion modulators [24, 25], and photodetectors that utilize the absorption by defect states at polysilicon grain boundaries [26, 27]. Photonic isolation layer fabrication and polysilicon film deposition are followed by two etching steps (full and partial, for strip and ridge structures) and two doping implants (N and P for modulators and detectors) to form our photonics process module that is inserted into the CMOS fabrication process flow. Fig. 1b shows the cross-sectional drawing of three representative photonic components in our polysilicon photonic platform next to a transistor in a planar bulk CMOS process.

The photonics process module is inserted in the middle of transistor processing, after gate definition, but before source and drain implants (see numbers in Fig. 1b for the fabrication order). With this approach, all of the high-temperature photonics processing takes place before the definition of the source, drain, and channel of transistors. This eliminates the need for re-optimizing the source and drain implants and anneal processes that would otherwise be needed because of the sensitivity of deeply scaled transistors to the source and drain doping profiles [28]. Also, this approach allows us to reuse some of the frontend processing steps (high-doping implants, and silicide formation) for active photonic components to minimize the number of photolithography masks. In doing so, the entire fabrication development is shifted to the photonics side, as low-loss photonic structures have to be implemented while transistor gate features already exist on the same level. This necessitates careful optimization of the polysilicon film deposition, polishing, and etching steps to achieve low (<1 nm) surface and sidewall roughness for low-loss and high-performance devices (see Methods for process details).

This optimized photonics process was integrated with an entire commercial 65 nm bulk CMOS process with seven metal interconnect layers, featuring transistors with three different threshold voltages and two oxide thickness variants. Fig. 1c shows bird's eye scanning electron micrographs (SEMs) of our monolithic platform with photonic components next to transistors with 60 nm channel length. This platform is fabricated on 300 mm wafers in a CMOS foundry located at the Colleges for Nanoscale Sciences and Engineering (CNSE), State University of New York, Albany, New York. Fig. 2a shows a photo of a fully fabricated wafer, and close-up photos of the entire reticle and one packaged chiplet composed of several WDM photonic transceiver rows. The micrographs of the transceiver chiplet, transmitter and receiver circuit blocks, and individual photonic components are shown in Fig. 2b and Fig. 2c. We were able to build a library of passive and active photonic components (waveguides, microring resonators, vertical grating couplers, high-speed modulators, and avalanche photo-detectors) with a performance similar or better than previous demonstrations on polysilicon [20, 21, 26], next to circuit blocks composed of millions of transistors operating at native CMOS process specifications.

Fig. 3a summarizes the performance of passive components measured on partial-flow (passive photonics only) and full-flow (active and passive photonics with electronics) wafers, at a wavelength of 1300 nm. We achieved approximately 10 dB/cm propagation loss for ridge and strip waveguides, and >20,000 loaded quality factor (Q-factor) for microring resonators on partial-flow wafers. Full-flow wafers exhibit higher loss; however, this issue did not significantly affect the performance of our optical transceivers: the 20 dB/cm waveguide loss results in 3 dB loss across the 10-lambda WDM rows, and the 10,000 loaded Q-factor of microring resonators is close to optimal for 10-20 GHz bandwidth resonant modulators and detectors (see Methods for further discussion). Waveguide loss and resonator Q-factor are two times better at 1550 nm (Extended Data Fig. 1), but all optical transceivers were initially designed at 1300 nm. Grating couplers

(GCs) for coupling light into and out of the chip are designed using both the partial- and full-etch steps to construct a periodic L-shaped geometry (Fig. 3b). The measured grating transmission, shown in Fig. 3b, indicates a peak efficiency of −4.2 dB for the partial flow and −5.2 dB for the full flow, with 1 dB bandwidth of around 40 nm. (See Methods for discussions on further device improvements.).

Depletion-mode resonant modulators and defect-based photodetectors were implemented using ridge microring structures with lateral PN and PIN diode junctions, respectively. Device micrographs and designs are shown in Fig. 2c and Fig. 3c,f. Two mid-level doping implants, P and N with concentrations of 6×10^{18} cm^{-3}, are optimized for active photonics (see Methods for discussion on implants).

The modulator uses a lateral PN junction to modulate light through the modulation of the resonance wavelength using the free-carrier plasma dispersion effect [29] (Fig. 3d). By operating the PN junction under full depletion, a 3 dB bandwidth of 16.8 GHz (Fig. 3e), and digital modulation at 10 Gb/s is achieved with only 2 Vpp modulation signal (Fig. 3e inset).

The defect-based photodetector has a responsivity of 0.11 A/W (quantum efficiency of 10%) near 1300 nm under very low bias voltages (Fig. 3g) using a resonant design that enhances the weak absorption in polysilicon (Fig. 3g inset). We have also observed avalanche gain for the first time in polysilicon photodetectors [30] at bias voltages above 8V (Fig. 3g), leading to a responsivity of 1.3 A/W at 16 V bias with a noise equivalent power (NEP) of 0.27 $pW/\sqrt{Hz}$. This device has a 3 dB bandwidth of more than 8 GHz under reverse bias voltages above 0 V, reaching 11 GHz for 5 V bias (Fig. 3h). More results on photodetectors are given in the Extended Data Fig. 2.

In order to examine the performance of transistors after introducing the photonics module into the CMOS process, electrical ring oscillators composed of 15 equally-sized inverting stages are used inside all electronic-photonic blocks to probe the speed of transistors, as well as the intra- and inter-die variations. The fastest transistors (low-threshold voltage) in the process with gate lengths of 55 nm were used for the ring oscillator design. Fig. 4a shows the histogram of the normalized frequency of ring oscillators relative to the nominal frequency (2.33 GHz, single stage delay of 14.3 ps), simulated with the original process design kit (PDK) provided by the foundry. This distribution is within the standard range of native CMOS processes, confirming that our photonic process module does not degrade the performance of transistors.

As a first demonstration of monolithic electronic-photonic systems in this platform, we have implemented high-bandwidth photonic WDM transceivers. We designed a total of six chiplets, each containing four stand-alone WDM transmitter and receiver rows, each supporting up to 16 channels. Different designs for resonant modulators and detectors were used in WDM rows. The chiplets are diced and wire-bond packaged with 100 pads to provide DC supplies, bias signals, and high-speed clocks for electro-optical testing (Fig. 2a). By integrating all of the analog and digital blocks, signal generation and error estimation of transceivers are performed on the chip.

The transmitter is composed of a full digital backend that generates a pseudo-random binary sequence (PRBS) signal, a serializer with an 8 to 1 ratio, and finally an inverter chain that drives the microring modulator (Fig. 4c). On the receiver side, a transimpedance amplifier (TIA) analog frontend converts and amplifies the received photo-current into a voltage signal, and a pair of double-data-rate (DDR) samplers converts the signal into the digital domain [31] (Fig. 4d). These bits are deserialized and fed into a bit-error-rate (BER) checker on the chip. The generated PRBS signal and BER data are monitored via on-chip scan chains to measure the functionality and performance of the transceivers. Overall, approximately 30,000 logic gates (~0.5 million transistors) from IP

standard cells have been used in each transceiver channel.

The operation of one channel of a 10-lambda WDM transceiver is shown in Fig. 4e,f. Modulators were operated in the depletion mode (0 to -1.5 V voltage swing) at 10 Gb/s data-rate with an extinction ratio of 4.7 dB (Fig. 4e). The receiver achieved a BER better than 10^{-10} with -3 dBm input optical power sensitivity at 7 Gb/s, as shown in Fig. 4f. The speed of receivers is currently limited by the long on-chip clock distribution network and can be further improved by integrating local clock generators [31]. Thermal tuning controllers and heater drivers are also included in the transceivers, to adjust for microring resonance fluctuations due to temperature and process variations [32]. Using the digital-to-analog converters in the thermal tuning controllers and heater drivers, we measured 45 μW/GHz tuning efficiency for integrated microheaters on microring modulators and detectors (Fig. 4g). The total electrical energy consumption of the complete transmitter and receiver was 100 fJ/b and 500 fJ/b, respectively. The transceiver achieved the bandwidth density of 180 Gb/s/mm^2 with 10% of the effective area occupied by photonics, which can be reduced to 5% by optimizing the floorplan. Incorporating this photonics platform in advanced sub-10 nm technology nodes with higher transistor densities [33] would lead to >2 Tb/s/mm^2 bandwidth densities meeting the needs of next-generation SoCs.

The demonstrated optical transceivers in bulk CMOS are an important milestone toward terabyte-scale optical interconnects for direct integration with logic and memory to improve the performance of computing systems, currently limited by the chip input/output bandwidth. Also, the demonstrated photonic platform and integration approach shows a path forward for adding photonic functions on a variety of substrates to enable the next generation of systems on a chip for computing, communications, imaging, and sensing.

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Methods

Chip Implementation. Photonic device layouts were developed and drawn in Cadence Virtuoso (an industry-standard design tool for frontend electronics in conjunction with mixed-signal electronics [34]). Digital electronics were implemented using a combination of digital synthesis and place and route tools from Cadence. All photonic and electronic designs conform to the 65 nm CMOS technology manufacturing rules (more than 5000 rules). New design rules were added to the original CMOS rules for the new photonics masks that were added to the process. The most critical mask rules with the introduction of photonics into the process are density rules. This is important as photonics and electronics occupy separate regions on the chip, but their respective masks have to maintain a certain maximum and minimum density of shapes across the whole design area. These density rules were met by custom fill shapes designed by our team. Density fill shapes can be seen in the SEM images in Fig. 1c. The physical design verification was performed using Mentor Graphics Calibre.

Fabrication. Designs were fabricated on 300 mm wafers in the fabrication facility at Colleges for Nanoscale Sciences and Engineering (CNSE), State University of New York, Albany, New York. The photonics passive-only wafers (partial flow) were fabricated on silicon wafers with 1.5 μm thick SiO_2 under-cladding blankets with the whole CMOS backend dielectric stack as the over-cladding. Partial-flow wafers were fabricated for photonics process optimization before integration with electronics. For full-flow wafers (passive and active photonics with electronics), the deep photonic trench is first fabricated by etching the trench in the silicon substrate and filling it with SiO_2 by chemical vapor deposition followed by a planarization step. At this point, the wafer goes through the CMOS frontend process up to the source and drain formation. Photonic device

fabrication is then followed by the deposition, annealing, and planarization of a 220 nm photonic polysilicon layer. Using two reactive ion etching steps, one full (etching the entire 220 nm depth of polysilicon film) and one partial (120 nm deep), strip and ridge photonic structures are formed. This is followed by the photonic mid-level doping implants. From here, electronics and photonics share the rest of the fabrication process, including the high-doping implants (for the transistor source and drain, and the photonic modulator and detector ohmic contacts), nitride liners (silicide block, and etch-stop for the first via), silicide formation, and metallization. There are a total of 7 metal interconnect layers in this process, with the first 4 having a lithography resolution of less than 100 nm.

Each wafer quadrant on full-flow wafers received a separate mid-level doping implant concentration for photonic active components (modulators and detectors) ([1, 2, 3, 6]$\times 10^{18}$ cm^{-3}). Due to the presence of a large density of defects in polysilicon, the carrier activation occurs only after the majority of defect states are occupied, whose onset occurs for a doping concentration of roughly 10^{18} cm^{-3} [35]. This necessitates careful optimization of photonic mid-level P and N doping concentrations to balance loss, modulator efficiency, and device series resistance, which affects the speed of both modulators and detectors. By using a separate doping concentration in each quadrant of the wafer, we tested the performance of modulators and detectors as a function of doping concentration. From the results of doping splits in an earlier fabrication run for optimizing the photonics process, we expected the optimal doping concentration to be close to 3×10^{18} cm^{-3}. However, in the full flow run, due to an increase in optical loss caused by polishing residues, microring Q-factors dropped by a factor of two. This required larger wavelength shifts in modulators to compensate for the broadened resonance line-shape to achieve the same level of modulation depth. Therefore, we observed the best overall performance for a P and N implant concentration of 6×10^{18} cm^{-3}. The results presented in this

paper are for devices receiving this implant concentration.

Discussion on Fabrication Results. The mask density rules assure that the material density during polishing, etching, and lithography is within an acceptable range over the entire reticle and wafer to eliminate pattern-dependent results and achieve a high fabrication yield. Nevertheless, the maximum density range for each layer (polysilicon, metals, etc.) is desirable for more design flexibility. In this fabrication run, we faced unforeseen issues with photonic trench planarization, due to a large density gradient of photonic trenches across the reticle field. This caused dielectric residues on the wafer after photonic trench planarization. We also experienced metal residues after the fabrication of the first via contact. Both of these issues led to a factor of two degradation in the passive photonic performance in full flow runs (20 dB/cm vs. 10 dB/cm for waveguide loss, and 10,000 vs. 20,000 for microring Q-factor at 1300 nm). Both of these issues are resolved through modified design rules, and optimized fabrication processes for the next fabrication run.

Optical Testing. Tunable lasers from Agilent Technologies and Santec were used for the optical characterization. Standard single-mode fibers (SMF28) were used to couple light into and out of the chip using grating couplers. The width of the grating couplers is matched to the mode size of the SMF28 fiber. We used 3-axis positioner stages (Thorlabs NanoMax) to position and align fibers over the grating couplers of the test sites. Minimum fiber-to-coupler insertion loss was achieved by angling the fibers at 15° off-normal from the surface of the chip. Waveguide losses were estimated by measuring transmitted optical power for four different waveguide lengths (50 μm, 1 mm, 5 mm, and 15 mm), and fitting the propagation loss to the transmission

354 measurements. Microring Q-factors were estimated by fitting a Lorentzian function to microrings
355 with close to critical coupling condition. Fiber-to-chip grating coupler (GC) efficiencies were
356 extracted from the transmission measurement data, by fine tuning the fiber angle at the input and
357 output to achieve minimum transmission loss and subtracting the waveguide loss connecting the
358 two identical GCs at the input and output of the test structure. Electro-optical frequency response
359 (S21) of optical modulators and photodetectors were measured using an Agilent Vector Network
360 Analyzer (VNA, 8722D). For modulator bandwidth testing, the modulator was driven by VNA
361 Channel 1 with the bias voltage applied using a Bias Tee (SHF BT 65), and the modulator output
362 was detected by a high-bandwidth photodiode (Discovery DSC30-3-2010) which was connected
363 to the Channel 2 of the VNA for S21 measurement. For photodetector bandwidth testing, VNA
364 Channel 1 was used to drive an external Lithium Niobate modulator (JDSU 10022054), and the
365 photodetector was biased using a Bias Tee (SHF BT 65) whose RF output was connected to VNA
366 Channel 2 for S21 measurement. We used high-bandwidth RF probes (Cascade Infinity, 50 μm
367 pitch) for high-speed testing. Eye diagrams for the modulators and detectors were obtained using
368 a similar setup, with a PRBS pattern generator (Picosecond Programmable Pattern Generator,
369 SDG Model 12072) and a high-bandwidth oscilloscope (Agilent Technologies 86108B Precision
370 Waveform Analyzer). The microring photodetector responsivity was measured by dividing the
371 device photocurrent by the input optical power, which was estimated by measuring the optical
372 power in the input fiber before entering the chip and accounting for the fiber-to-chip grating
373 coupler, and excess waveguide losses.

374

375 **Electrical Testing.** Chips were assembled in ceramic packages (CPG20809) with 100 wirebond
376 connections. These packages were plugged into a socket on a host board PCB, which delivers

supplies, bias signals, high-speed clock (from an Agilent 81142A pulse generator), and scan control signals from an Opal-Kelly FPGA. Scan commands for each measurement are set in Python scripts on a computer and then sent to the FPGA to configure the chip for each particular experiment. In order to read out the ring-oscillator frequencies, the output of the oscillator is fed into an asynchronous digital divider (divide by 8) and the divided clock runs a digital counter block. Then, the oscillator's frequency was estimated by scanning out the counter's value. The transmitter's eye-diagram was captured via an external Ortel photoreceiver with 10 GHz bandwidth on an electrical DCA scope by running the on-chip PRBS modules at 5 GHz external clock frequency. On-chip clock adjustment circuits composed of a duty-cycle corrector (DCC) and a delay line (DL) have been used to synchronize the timing of different transceivers. The receiver's BER test was performed by first programming a KC705 Xilinx FPGA with the same PRBS coefficients used for our on-chip BER checkers. The output of the FPGA was then amplified using a high-voltage modulator driver (JDSU H301), which then drives an external JDSU MZI optical modulator. Modulated light is amplified using a semiconductor optical amplifier (Thorlab BOA1130) and is coupled into the chip. The BER bathtub curves in Fig. 4f show the measured BER at each time delay point between the clock fed into the chip and the FPGA reference clock.

Device Design and Discussion. The reticle area was divided into two main sections: the test device section with photonic and electrical test structures and the electronic-photonic microsystem section (WDM chiplets). The test area included waveguide loss, microring Q-factor, grating coupler efficiency, and sheet resistance test structures as well as, individual modulators and detectors. A variety of parameters in every device was swept to find optimal designs and to extract information about the quality of the fabrication (e.g., estimating surface

and sidewall roughness, doping activation, etc.). Photonic test devices were designed for both 1300 nm and 1550 nm wavelengths. Overall, approximately 1000 test devices were laid out on the reticle. The microsystems included 6 transceiver chiplets, each 4.8 mm×5 mm. Since the same set of masks were used for process optimization and system implementation, there were some uncertainties about the performance of photonic passives and actives. This required sweeping modulator and detector parameters in the WDM transceiver designs to cover a large enough range of device performance.

All photonic components were designed using two etch steps (partial and full). The thickness of the polysilicon layer (220 nm) and the depth of the partial etch (120 nm) were chosen to optimize the overall performance of the whole platform, including the efficiency of grating couplers, radiation loss of the microring resonators, and series resistance of the modulators and detectors. The optimal width of the single-mode waveguides and diameter of the high-Q microrings were around 450 nm and 15 μm, respectively, for 1300 nm operation. The high doping regions for ohmic contacts were □1 μm away from the center of the ridge waveguides to avoid free-carrier loss. The width of the intrinsic region for the photodiode is 800 nm in the reported device. Microheaters were incorporated in the microring modulators and detectors for tuning their resonances to the desired laser wavelength. We used silicided P+ polysilicon resistors for the microheaters. The fabricated microheaters had a resistance of ~100 Ω.

The thickness of the photonic trench was optimized to maximize the grating coupler efficiency. A thickness of approximately 1.5 μm results in constructive interference of the main beam diffracted upwards with the beam diffracted downward and reflected from the surface of the silicon substrate. This improved the directionality and coupling efficiency of the grating couplers.

Improvement of Photonic Performance. We have already taken the necessary steps to improve

the waveguide loss in our full-flow wafers by fixing the photonic isolation planarization issue on the next fabrication run. Hence, we expect to achieve the same passive photonics performance in our fully integrated wafers as that reported in partial-flow runs in this work. This means a factor of two improvements in waveguide loss (10 dB/cm) and microring Q-factor (20,000) by simply resolving the photonic isolation planarization issue.

The loss improvement will also affect the performance of active photonics. The loss improvement will result in a higher quantum efficiency (QE) for photo-detectors by reducing the fraction of photons lost by scattering and absorption. We expect 50-100% improvement in detector responsivity (0.15-0.2 A/W in the linear mode, and 2-2.6 A/W with avalanche gain). The improvement in the microring modulator Q-factor leads to a sharper resonance feature, which consequently reduces the drive voltage and lowers the transmitter power consumption.

The waveguide loss can be improved even further to about 6 dB/cm across the entire telecom and datacom bands (1250 −1700 nm) by optimizing the polysilicon film. Currently, waveguide loss at shorter wavelengths (1300 nm) is twice as high as at 1550 nm (Fig. 1). The similarity of the detector QE (11%) at 1300 nm and 1550 nm suggests that the scattering and absorption losses are increasing proportionately at shorter wavelengths. As optical modes at shorter wavelengths are more confined in the waveguide core and exhibit less scattering by the sidewall roughness, the dominant mechanism for the increase in scattering loss at shorter wavelengths is most likely the increase in scattering by polysilicon grain boundaries. This source of scattering can be reduced by optimizing polysilicon deposition and anneal conditions such that the scattering correlation length is reduced.

The bandwidth of the modulators and detectors can also be improved by optimizing the doping profiles. In the current run, we employed the same source and drain implants for the low-

resistance regions (P++ and N++) of our modulators and detectors. These implants have concentrations that are designed for the shallow source and drain of deeply scaled transistors and are not high enough to provide low series resistance for the 100 nm-thick polysilicon regions in our photonic devices. By using dedicated implant masks and high implant dosages, and by further optimizing dimensions in all doping profiles, we expect to improve the bandwidth of modulators by 25-50% to 20-24 GHz based on the estimates for the contributions of mid-level (P and N) and high-level doping (P++ and N++) regions to the series resistance. As for the detectors, we also expect an improvement in bandwidth by reducing the width of the intrinsic region from 800 nm to reduce the transit time, which is currently limiting the speed of the device. We expect that 50% reduction of the intrinsic region width to 400 nm would not significantly affect the Q-factor and responsivity of detectors, while reducing the depletion width and transit time. A careful optimization of the intrinsic region width combined with the reduction of RC time constant by adjusting the implant conditions can improve the bandwidth of detectors by 25-50% to 14-16.5 GHz in the linear mode, and to 10-12 GHz in the avalanche mode.

We also expect an improvement in the GC efficiency in the next fabrication run. In the current run, a 30 nm photolithography bias caused the dimensions of the grating couplers to be smaller than the nominal design values. This caused the grating coupler efficiency to drop from −1.8 dB in design to −5 dB in the fabricated devices. We are addressing this issue by optimizing the lithography step and pre-biasing the photolithography mask. Also, by utilizing a nonuniform grating design [36], we expect to improve the mode matching of the grating coupler to the Gaussian mode profile of the optical fiber. This will enable us to improve the coupler efficiency to below −1 dB.

Electronic-Photonic Systems on Glass. The current work was aimed at integrating photonics

into bulk CMOS technologies. However, a fully functional deposited photonic platform on glass transcends any one particular substrate or application. All of our partial-flow photonics-only silicon wafers were covered by a blanket of 1.5 μm-thick plasma-enhanced chemical vapor deposition (PECVD) silicon oxide (glass), on which we have fabricated optical waveguides, resonators, modulators, and photodetectors. These thin-film integrated photonic devices along with TFTs that are currently used in display panels can enable 'electronic-photonic systems on glass'. These systems can be fabricated on low-cost large-area substrates such as metal foils, transparent glass, or even flexible substrates as long as they are covered with roughly 1 μm of glass. Such a platform can enable a variety of new systems and applications which current electronic-photonic technologies cannot address due to substrate size or cost limitations. For example, several space and astrophysics applications, such as laser communications and astronomical spectroscopy, require large-area optics and detectors. Also, many optical phased array applications (lidars, augmented reality headsets, etc.) can benefit greatly from large-area integrated photonic circuits. An electronic- photonic platform on glass, enabled by the deposited polysilicon photonics demonstrated in this work, can address these application areas. The performance of photonics on this platform would be similar to the devices we have reported on partial-flow wafers in this paper.

Data Availability. The authors declare that the main data supporting the findings of this study are available within the article and its Supplementary Information files. Extra data are available from the corresponding author upon request.

Reference for Methods

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Figure 1: Photonic integration with nano-scale transistors. a. Illustration of three major deeply-scaled CMOS processes: planar bulk CMOS, FinFET bulk CMOS, and fully-depleted SOI CMOS. **b.** Integration of photonics process module into planar bulk CMOS with photonic devices implemented in an optimized polysilicon film (220nm) deposited on a photonic trench filled with silicon oxide (□1.5 μm). The numbers indicate major fabrication step/steps in the order appearing in the process: (1) and (2), transistor and photonic isolation fabrication; (3) transistor front-end fabrication up to source/drain implant, including gate definition; (4) deposition, anneal, and polishing of photonic polysilicon film; (5) polysilicon full and partial etching for forming strip and ridge photonic structures; (6) doping implants (P and N) for active photonics; (7) high doping implants (P++ and N++) and salicidation for both electronic and photonic devices; (8) metallization. **c.** SEM of different photonic and electronic blocks in our monolithic platform.

Figure 2: Monolithic electronic-photonic platform in 65 nm bulk CMOS. a. Photograph of a fully fabricated 300 mm wafer with monolithic electronics and photonics, and close-ups of a reticle on this wafer, and a packaged WDM chiplet. **b.** Micrograph of a WDM chiplet with four transmitter (Tx) and receiver (Rx) rows. For this photo, the silicon substrate was entirely removed using XeF_2 gas after mounting the die on a carrier substrate, and the micrograph was taken from the backside of the die. **c.** Close-up of a single transceiver macro and its photonic and electronic circuit components.

Figure 3: Photonics Platform Performance. a. Passive components specifications at 1300 nm for partial- and full-flow wafers. **b.** Transmission spectrum and the longitudinal cross-section of the GC. **c.** Microring modulator 3D layout. **d.** Transmission spectrum of a modulator resonance with loaded Q-factor of 5,000. **e.** Modulator electro-optic frequency response (S21) and the eye-diagram obtained with 2 V_{pp} drive voltage. **f.** Microring photodiode 3D layout. **g.** Responsivity

vs. reverse bias voltage. Avalanche gain is observed at biases above 8 V. **h.** Photodiode frequency response (S21) under 0 V and 5 V reverse bias with 3 dB bandwidths of 8 GHz and 11 GHz, respectively. Inset shows the eye diagram obtained under 5 V bias.

Figure 4: Electro-optical testing of WDM transceiver chips. **a.** Histogram of measured frequencies of 485 test ring oscillators normalized to the frequency obtained from simulation with the native CMOS PDK models. **b.** Block diagram of one WDM transmit-receive row in our test setup. **c.** Block-diagram of a WDM transmitter. **d.** Block-diagram of a WDM receiver. **e.** 10 Gb/s transmit eye diagram using the on-chip PRBS generator. **f.** 7 Gb/s receiver bathtub curve obtained from the on-chip BER tester by sweeping the delay between the clocks for the receiver and external transmitter (sampling clock delay). **g.** Thermal tuning of one WDM channel using the integrated microheater.

Extended Data Figure 1: Passive photonic performance at 1300 nm and 1550 nm. (a) Waveguide propagation loss at 1300 nm. Waveguide loss drops with wavelength because of a combination of lower absorption and scattering by polysilicon. (b) Q-factor of a 15 μm diameter microring resonator. (c) Waveguide propagation loss at 1550 nm. (d) One resonance of a 17 μm diameter microring near 1540 nm with a Q-factor of 38,000.

Extended Data Figure 2: Polysilicon avalanche photo-detector. (a) I-V curve of the microring photo-diode under dark and illumination for input optical power of 20 μW. Dynamic range is □60dB and □10dB at 0 V and 16 V, respectively. (b) One microring photo-detector resonance and the corresponding photo-current as the wavelength is swept across the resonance. (c) NEP (blue curve) of the photo-diode estimated based on the dark-current shot noise, which dominates the detector noise. Avalanche gain is 13 at 16 V bias, with an NEP of 0.27 $pW/\sqrt{Hz}$. Simulated SNR (red curve) at the output of the optical receiver, assuming 1 μW optical signal, and a receiver circuit input-referred noise spectral density of 1 $pA/\sqrt{Hz}$ /(d) The responsivity of the photo-diode vs. input optical power, showing minimal power dependency. (e) and (f) Eye-diagrams at 12.5 Gb/s at 0 V and 14.5V reverse bias.

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Author Contributions A. Atabaki, S. Moazeni, and F. Pavanello have all contributed equally to this work. A. Atabaki designed and tested avalanche photodetectors, tested photonic devices during process development, and designed WDM receiver rows. S. Moazeni designed the mixed-signal electronics for transceiver chiplets, tested optical transceivers and electronics, and performed top-level assembly of electronics and photonics on the chip. F. Pavanello designed and tested optical modulators, designed WDM transmitter rows, and performed the top-level assembly of photonics in the transceiver chips. A. Atabaki, S. Moazeni, and F. Pavanello, all contributed to the chip verification. H. Gevorgyan tested optical modulators and loss test structures on full flow wafers. J. Notaros designed and tested the original version of grating couplers. L. Alloatti developed CAD infrastructure for photonics layout and chip verification, and contributed to the layout of waveguide test structures. M. Wade designed and contributed to the layout of optical passive devices. C. Sun contributed to the design of WDM optical transceivers and thermal tuning circuits. S. Kruger ran process experiments for propagation loss improvement, performed CMOS and photonics fabrication compatibility optimization, fabricated full flow wafers, and performed inline electrical and optical testing. H. Meng contributed to the design of avalanche photodetectors. K. Qubaisi tested grating couplers on full flow wafers. I. Wang performed device metrology and post processing of optical waveguide and resonator loss data. B. Zhang performed grating coupler simulations

and contributed to the new grating coupler designs. A. Khilo analyzed device metrology and measurement data for studying and optimizing photonic performance. C. Baiocco developed the 65nm CMOS-compatible photonics design kit, designed IP for in-line electrical test, metrology and optical photonics testing, worked with the mask house with building the photolithography masks and managed the overall process development and wafer fabrication. M. Popović, V. M. Stojanović, and R. J. Ram supervised the project.

Competing Interests C. Sun, M. Wade, R. J. Ram, M. Popović, and V. M. Stojanović are involved in developing silicon photonic technologies at Ayar Labs.

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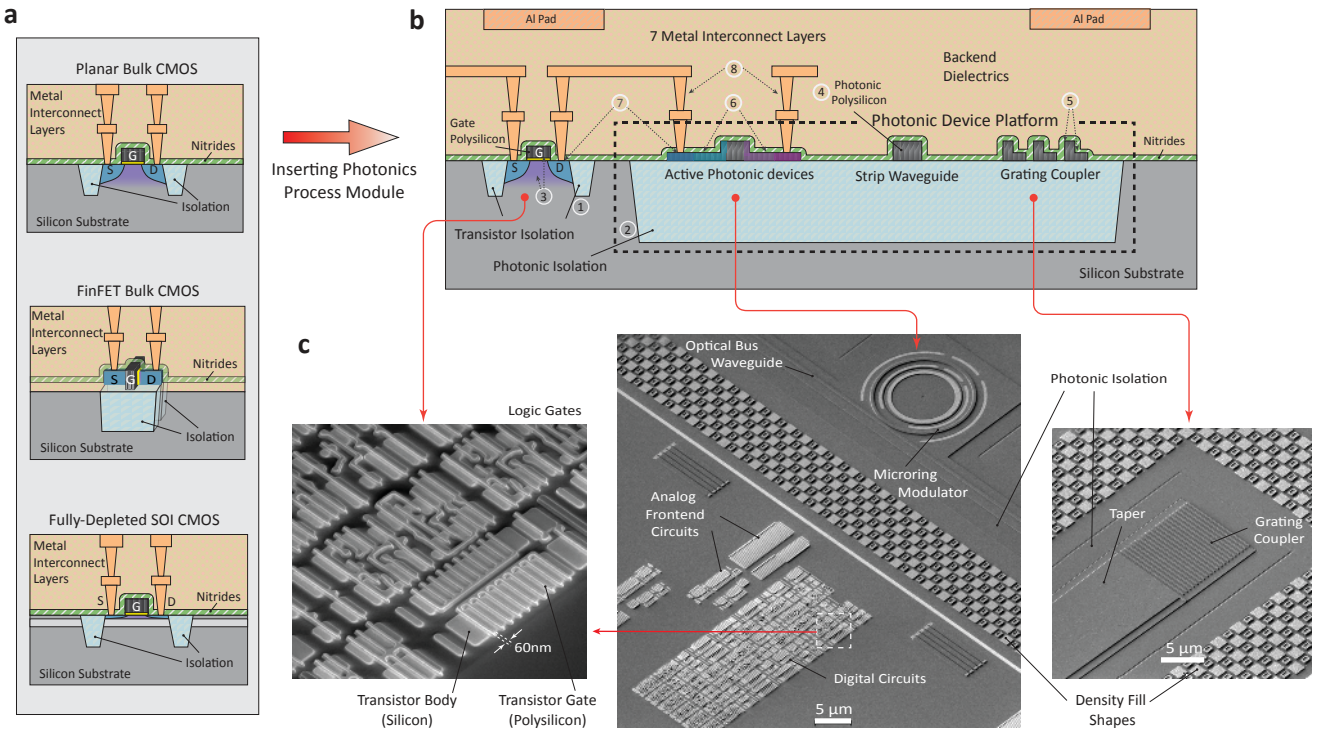
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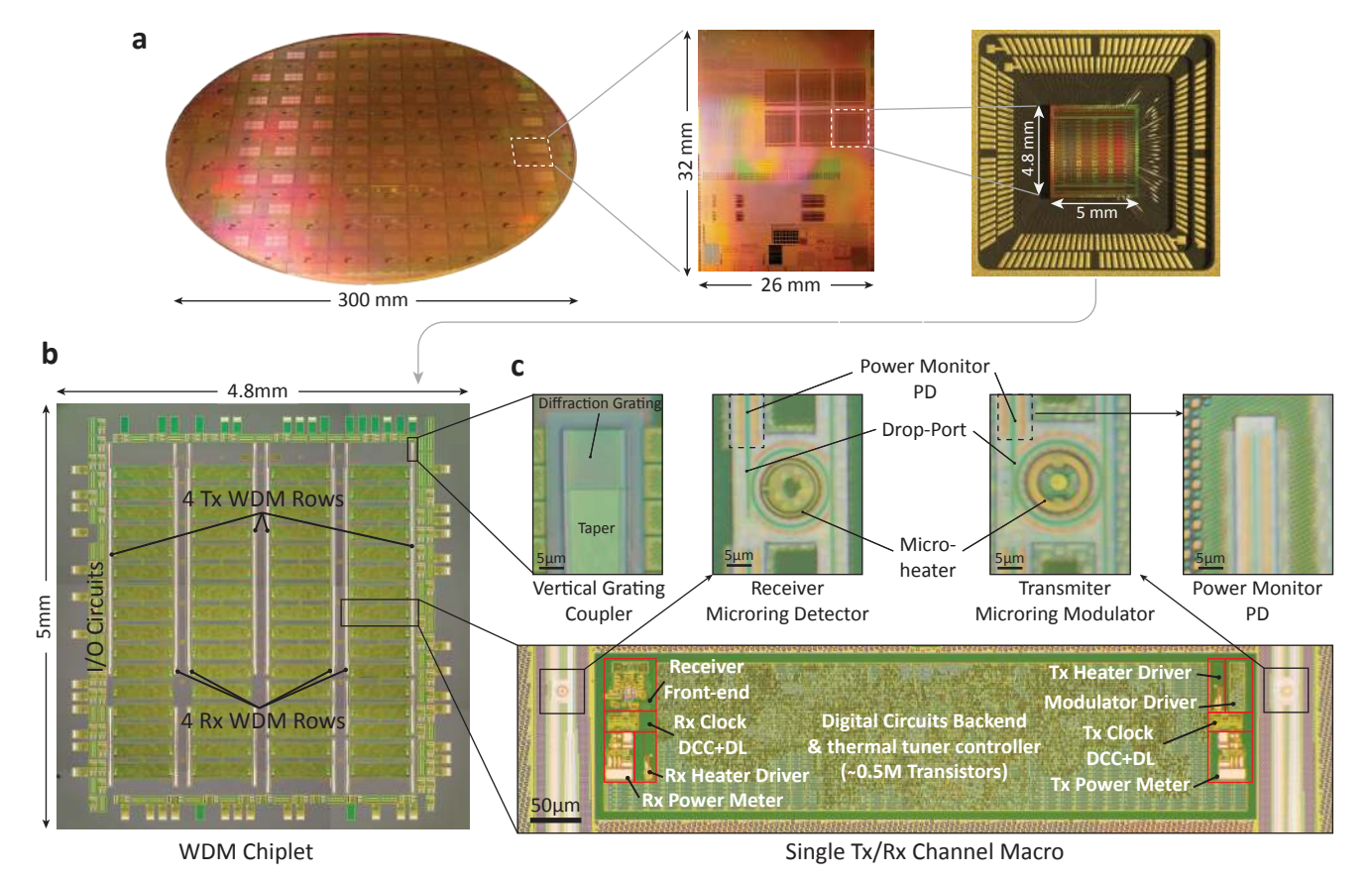
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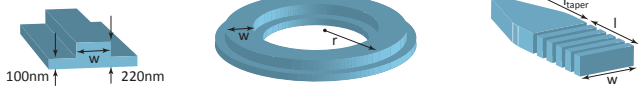
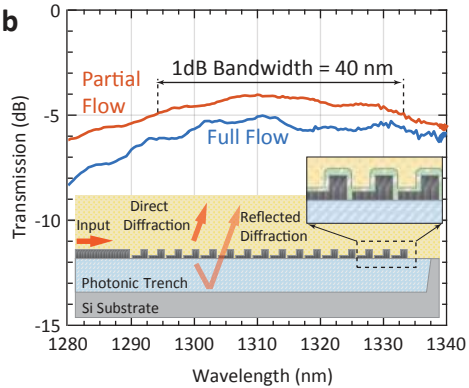
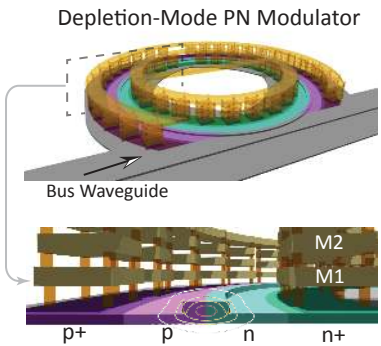
Receiver Microring Detector
Transmiter Microring Modulator
Power Monitor PD
Receiver Front-end
Rx Clock DCC+DL
Rx Heater Driver
Rx Power Meter
Digital Circuits Backend & thermal tuner controller (~0.5M Transistors)
Tx Heater Driver
Modulator Driver
Tx Clock DCC+DL
Tx Power Meter
50μm
Single Tx/Rx Channel Macro

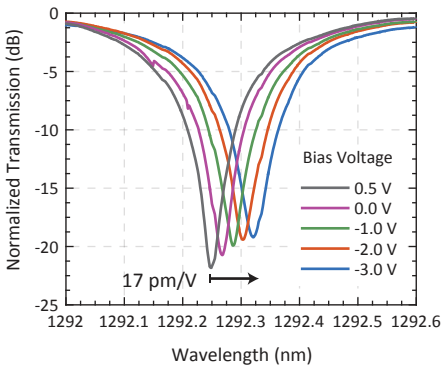
a Passive Components (Specifications at 1300 nm)

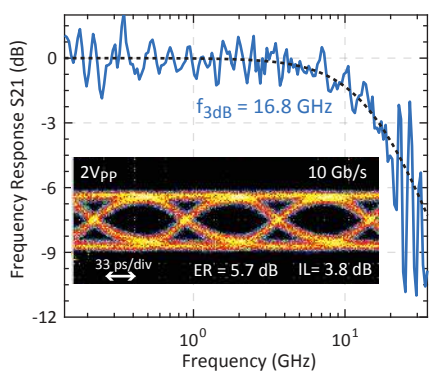


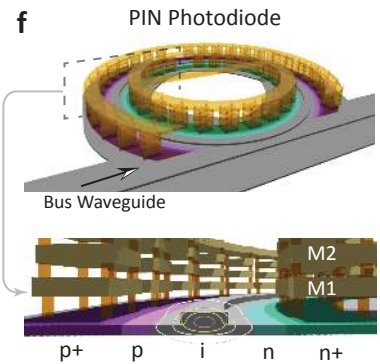
	Propagation Loss	Intrinsic Q	Coupling Loss
Partial Flow	8-15 dB/cm	19-31k	4.2 dB
Full Flow	21-27 dB/cm	10-19k	5.2 dB
Dimensions	w= 400 nm	w = 400 nm r = 7.5 µm	w = l = 8 µm l_{taper}= 250 µm

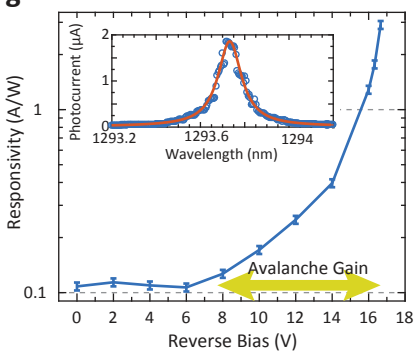


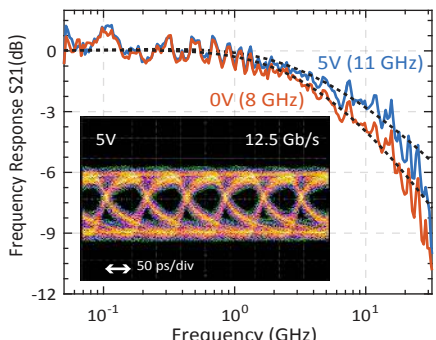


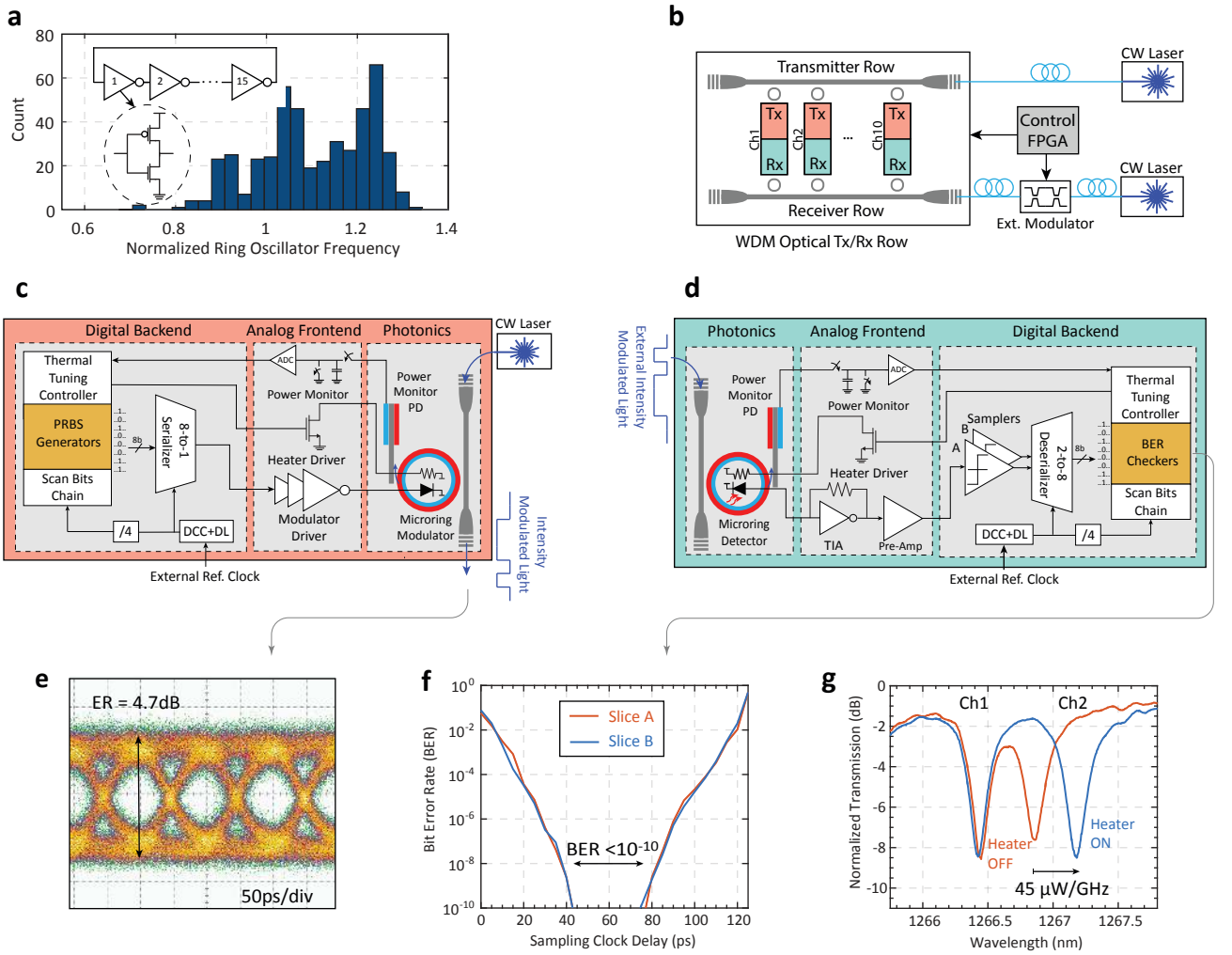








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Digital Backend
Analog Frontend
Photonics
Thermal Tuning Controller
PRBS Generators
Scan Bits Chain
8-to-1 Serializer
Power Monitor
Heater Driver
Modulator Driver
Power Monitor PD
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