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Integration of GaAs, GaN and Si-CMOS on a common 200 mm Si substrate through multi-layer transfer process

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The integration of III-V semiconductors (e.g. GaAs, GaN) and SOI-CMOS on a 200 mm Si substrate is demonstrated. The SOI-CMOS donor wafer is temporarily bonded on a Si handle wafer and thinned down. A second GaAs/Ge/Si substrate is then bonded to the SOI-CMOS containing handle wafer. After that, the Si from GaAs/Ge/Si substrate is removed. The GaN/Si substrate is then bonded to the SOI-GaAs/Ge containing handle wafer. Finally, the handle wafer is released to realize the SOI-GaAs/Ge/GaN/Si hybrid structure on a Si substrate. Through this method, the functionalities of each materials can be combined on a single Si platform.

Scaling of bulk silicon (Si) complementary metal-oxide-semiconductor (CMOS) devices, which is the main enabler for the semiconductor industry to improve device performance, lower power consumption and reduce the cost per transistor, is now reaching fundamental and economic bottlenecks[1,2]. Further shrinking of CMOS devices is expected to result in unreliable, variation-prone and more expensive devices[3,4]. To address this problem, co-integration of Si with other materials such as germanium (Ge) and III-V compounds (e.g., gallium arsenide (GaAs), gallium nitride (GaN)) is a key means to ensure commensurate scaling and functional diversification. For example, III-V materials can be used as a hybrid light source in a silicon photonics platform in order to enhance the performance and design flexibility for optical interconnects[5-10]. Such III-V/Si hybrid devices would compensate for the poor ability of Si to emit light and open up new circuit capabilities and applications beyond communication such as sensing and optical computation. Owing to the fact that III-V compound semiconductors have higher electron mobility than Si, they are also a suitable candidate for fabrication of high electron mobility transistors (HEMTs). HEMTs can be integrated together with Si-CMOS and becomes a promising technology boosters[11,12]. Hence, monolithic integration of high density, and inexpensive Si digital control circuitry with application specific III–V electronic and optical devices opens up new circuit applications and capabilities.

Most importantly, Si foundries work exclusively with large Si substrates for manufacturing efficiency. III-V substrates impose higher risk of cross-contamination and they are never accepted in the Si foundries. In addition, the wafer size of III-V is usually smaller (6 inch or smaller) and this results in a higher cost per-device/-chip during processing/production. This is the primary reason that optoelectronic devices such as those used in telecommunications (InGaAsP/InP-based devices), or GaAs-based wireless devices, or even III-V high efficiency solar cells, are significantly more costly than most "conventional" Si CMOS devices/circuits. Hence the ability to build large, high quality III-V materials on Si substrate is the essential enabler for the further development and adoption of III-V devices and circuits in applications mentioned above.

For III/V-Si hybrid integration, direct epitaxial growth of III-V compounds on Si substrates or CMOS devices would be the most desirable approach, but the high temperature III-V growth would severely degrade the CMOS transistors. The typical

growth temperature of GaN and GaAs/InP is about 1350 ^{o}C and 650 ^{o}C, respectively[13,14].

Wafer bonding, on the other hand, is another promising approach to integrate III-V materials on Si substrate. Although surface-activated bonding (SAB) has attracted a lot of attention recently, it requires a high vacuum system to avoid the oxidation of the semiconductor surface prior to bonding. Fusion bonding (plasma-activated) is chosen in this work because the bonding process can be carried out at room temperature and atmospheric pressure[15,16]. In addition, the bonding has more tolerance to materials with different coefficient of thermal expansion (CTE) mismatch and it is also compatible with CMOS process technology. Through this method, high temperature III-V materials growth can be completed without the presence of the CMOS layer, hence damage to the CMOS layer is avoided. Recently, our group has demonstrated the integration of the Si-CMOS and GaAs/Si or GaN/Si on a common 200 mm Si platform through double bond and layer transfer process[17,18]. In this paper, we take a step further to integrate the Si-CMOS, GaAs and GaN together on a common 200 mm Si platform. Through this method, the functionalities of each materials can be realized on a single Si platform (e.g. GaAs is more suitable for high frequency HEMTs devices, GaN is more suitable on high power devices, and inexpensive Si is for digital control circuitry).

Four sets of wafers were prepared: (i) Si handle, (ii) Silicon-on-insulator (SOI), (iii) GaAs/Ge/Si (001) donor, and (iv) GaN/Si (111) carrier wafers. The SOI that consists of Si (1.3 μm) and buried oxide film (BOX, 0.4 μm by thermal oxidation) is used in this study. The Ge and GaAs epitaxial films were grown directly on Si (001) donor wafer with 6° off-cut toward [110] direction by the metal organic chemical vapour deposition (MOCVD). The details of the growth has been published in the previous reports[19, 20, 21]. The GaN epilayer was grown on a 200 mm Si (111) substrate with resistivity > 3000 ohm-cm by the MOCVD.

The SOI wafer was deposited with a 500 nm oxide by plasma-enhanced chemical vapour deposition (PECVD). Additional densification was carried out to eliminate the residual gas molecules and by-products that are incorporated into the layer during the oxide deposition. The densification process was done at 600 ^{o}C for several hours in N_2 environment. After densification, the oxide surface is planarized by chemical mechanical planarization (CMP). The SOI (after PECVD oxide deposition and CMP-ed) and Si handle

wafers were subjected to O_2 plasma exposure, followed by rinsing them with deionized wafer and then spin dried in a spin rinse dryer (SRD). O_2 plasma exposure could increase the surface hydrophilicity (water droplet surface contact angle <5°) of the dielectric. The rinsing step is necessary to clean the wafers surfaces and to populate the surface with hydroxyl (OH) group at a sufficiently high density to initiate wafer bonding. Post-bonding annealing of the bonded wafer pair was carried out at 300 ^{o}C in an atmospheric N_2 ambient for 3 hr to further enhance the bond strength. The Si substrate from SOI wafer was then removed by a combination of mechanical grinding and wet-etching in the tetramethylammonium hydroxide (TMAH) solution. Prior to wet-etching in TMAH, the backside of the Si handle was protected by a protective film. The details on how to prepare the protective film was mentioned in the previous reports[22,23]. Since the BOX layer acted as an etch-stop layer, the SOI layer was temporarily attached to the Si handle wafer.

Due to the pin-holes and outgassing issues that were discovered previously, the BOX layer was removed and replaced by PECVD oxide (with densification and CMP) and PECVD Si_3N_4 (with densification)[17,18]. The GaAs/Ge/Si donor wafer also received the same PECVD oxide and nitride deposition. After that, the SOI-handle wafer was bonded to the GaAs/Ge/Si donor wafer. The bonding process was similar to the one described above. Similar grinding and wet-etching were carried out to remove the Si donor wafer from the GaAs/Ge/Si substrate to realize the GaAs/Ge-SOI containing handle wafer.

Same PECVD oxide and nitride depositions are then applied on the GaAs/Ge-SOI-handle and GaN/Si carrier substrates. Similar bonding and Si handle removal processes as mentioned previously were carried out. Finally, the SOI-GaAs/Ge/GaN/Si substrate can be realized. The overall process flow is schematically shown in Fig. 1.

An infrared (IR) camera was used to verify the bonding quality of the bonded wafer pair after the first and second bonding. Since Si (E_g = 1.12 ev), SiO_2 (E_g = 8.0 ev), GaAs (E_g = 1.42 ev) and GaN (E_g = 3.4 ev) are transparent to IR, interface voids can be observed by transmitting IR light through one side of the bonded wafer pair and observed from the other side with an IR camera. Transmission electron microscopy (TEM) with operating voltage of 200 kV was used to study the bonding interfaces.

The bonding quality of the first bonding between SOI and Si handle wafers is verified by the IR camera as shown in Fig. 2 (a). The bonding is excellent and no

observable void or particles are found from the IR image.

The BOX layer is then replaced by the PECVD oxide and nitride, followed by the deposition of PECVD oxide and nitride on the GaAs/Ge/Si wafer as mentioned earlier in section 2. The 2nd bonding (between GaAs/Ge/Si to SOI-handle) is then carried out. From the IR image shown in Fig. 2 (b), there are some un-bonded areas, especially on the wafer's edge because of the presence of particles on the wafer surfaces. The overall bonding quality is degraded with some trapped particles between the bonded pair and further improvement is required. The defects that are circled in red are from the backside of the Si handle wafer as it was etched by TMAH during the Si removal process. This is because of the poor adhesion of the protective layer on these particular regions and cause the film to peel off during the prolong TMAH etching (> 2 hours).

After the Si is removed completely from the GaAs/Ge/Si substrate, both the GaAs/Ge-SOI-handle and GaN/Si substrates are deposited with PECVD oxide and nitride. Subsequently, the 3rd bonding is carried out. From Fig. 2 (c), some un-bonded areas are observed in the IR image. This is because of the presence of particles from the GaN/Si surface and the un-bonded areas originated from the 2nd bonding. Again, the defects circled in red are not un-bonded area but are defects from the backside of Si handle wafer. The image of the SOI-GaAs/Ge/GaN/Si substrate after Si handle removal is shown in Fig. 2 (d). Peeling of films is observed mainly on the wafer's edge which is corresponded to the IR images.

Field emission scanning electron microscopy (FESEM) micrograph in Fig. 3 shows the cross-sectional image of the SOI-GaAs/Ge/GaN/Si substrate after the triple bond and layer transfer process. The two white dashed lines are eye guidelines to observe the bonding interfaces between the two PECVD nitride layers.

For a more detailed assessment on the quality of the bonded layers, TEM can be used. The cross-sectional view of TEM image in Fig. 4 shows the SOI-GaAs/Ge/GaN/Si substrate after the triple layer transfer process. No micro-void is observed at the bonding interface between two PECVD Si_3N_4 layers. This indicates that a uniform and flawless bond has been established successfully at the microscale level.

Through multi-layer transfer process, the combination of different group IV and group III-V materials on a single Si platform becomes possible in principle. The main

merit of this method is that the functionalities of different materials can be realized on a single Si platform. Hence, Si-CMOS (on SOI), high frequency devices (e.g. high electron mobility transistors (HEMTs) on GaAs layer) and high power devices (e.g. power amplifier (PA) on GaN layer) can be integrated onto a single piece of wafer forming a hybrid substrate as shown in Fig. 5.

In summary, the integration of Si, GaAs and GaN on a single Si platform can be realized by triple bond and layer transfer process. Through this method, the high frequency GaAs HEMT, PA GaN devices and inexpensive Si digital control circuitry can be combined on a single platform to further shrink the package size at the system level.

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Figure Captions

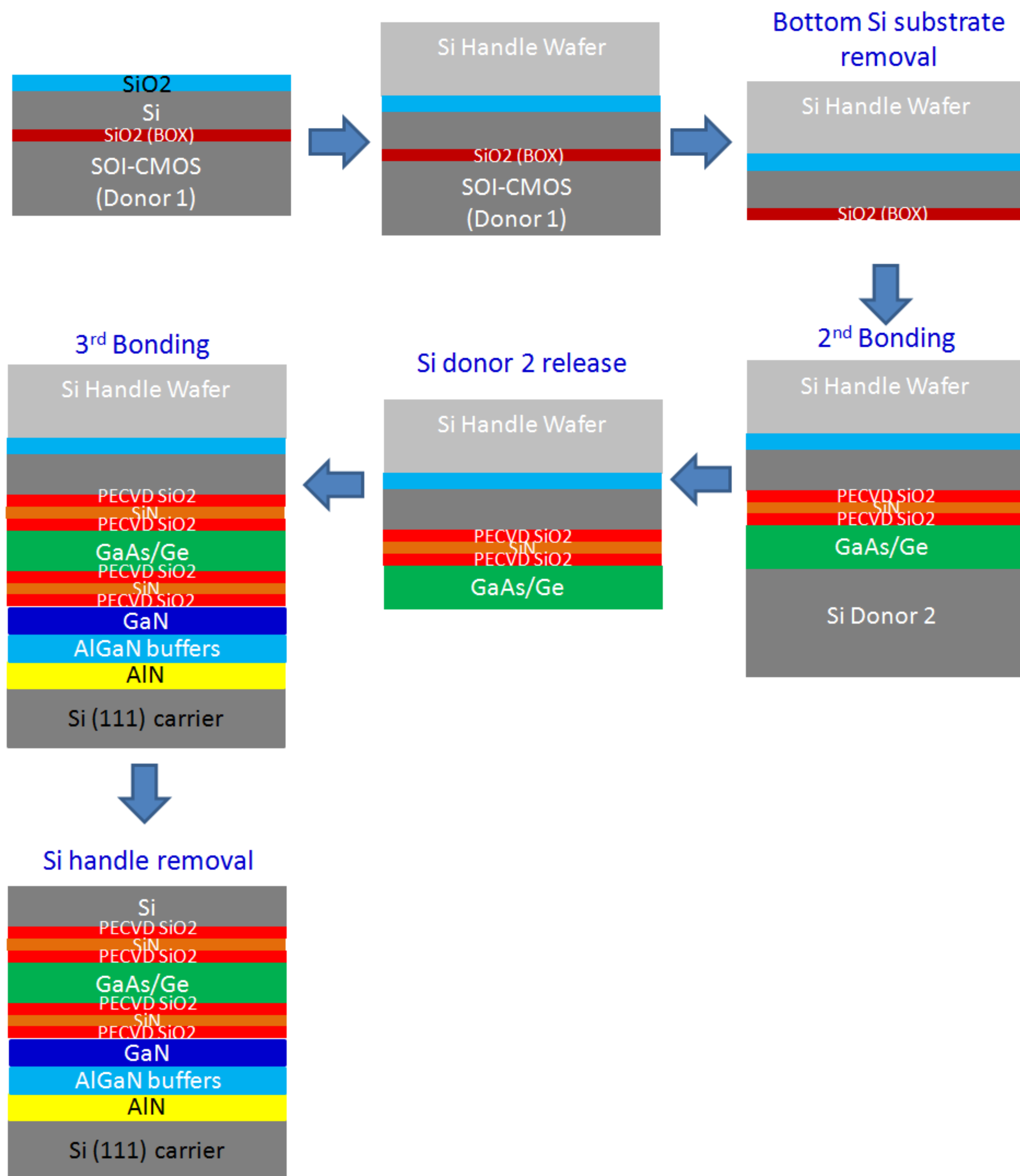
Fig. 1. Schematic shows the process flow chart of the triple bond and layer transfer process.

Fig. 2. Infrared (IR) images show (a) the first bonding SOI and Si handle wafer, (b) the second bonding of bonded wafer pair between handle-SOI to GaAs/Ge/Si substrate, (c) the third bonding of bonded wafer pair between GaAs/Ge-SOI-handle to GaN/Si substrate. No void or particle is observed on the first bonded wafer pair from the IR image. Whereas, some un-bonded areas are observed on the second and third bonded wafer pairs. The red circles show in Fig. (b) & (c) are the defects from the backside of the Si handle wafer during the TMAH etching. (d) Image shows the surface of the SOI-GaAs/Ge/GaN/Si substrate after the triple bond and layer transfer process.

Fig. 3. Cross-sectional view of FESEM micrograph shows the SOI-GaAs/Ge/GaN/Si substrate after the triple bond and layer transfer process. The white dashed line is an eye guideline to observe the bonding interface between the two PECVD nitride layers.

Fig. 4. Cross-sectional view of TEM micrograph shows the SOI-GaAs/Ge/GaN/Si substrate after the triple bond and layer transfer process. The white dashed line is an eye guideline to observe the bonding interface between the two PECVD nitride layers.

Fig. 5. Schematic shows that Si-CMOS (on SOI), high frequency devices (e.g. high electron mobility transistors (HEMTs) on III-As/P layer such as GaAs) and high power devices (e.g. power amplifier (PA) on III-N layer, e.g. GaN) can be integrated on a single piece of wafer forming a hybrid substrate.



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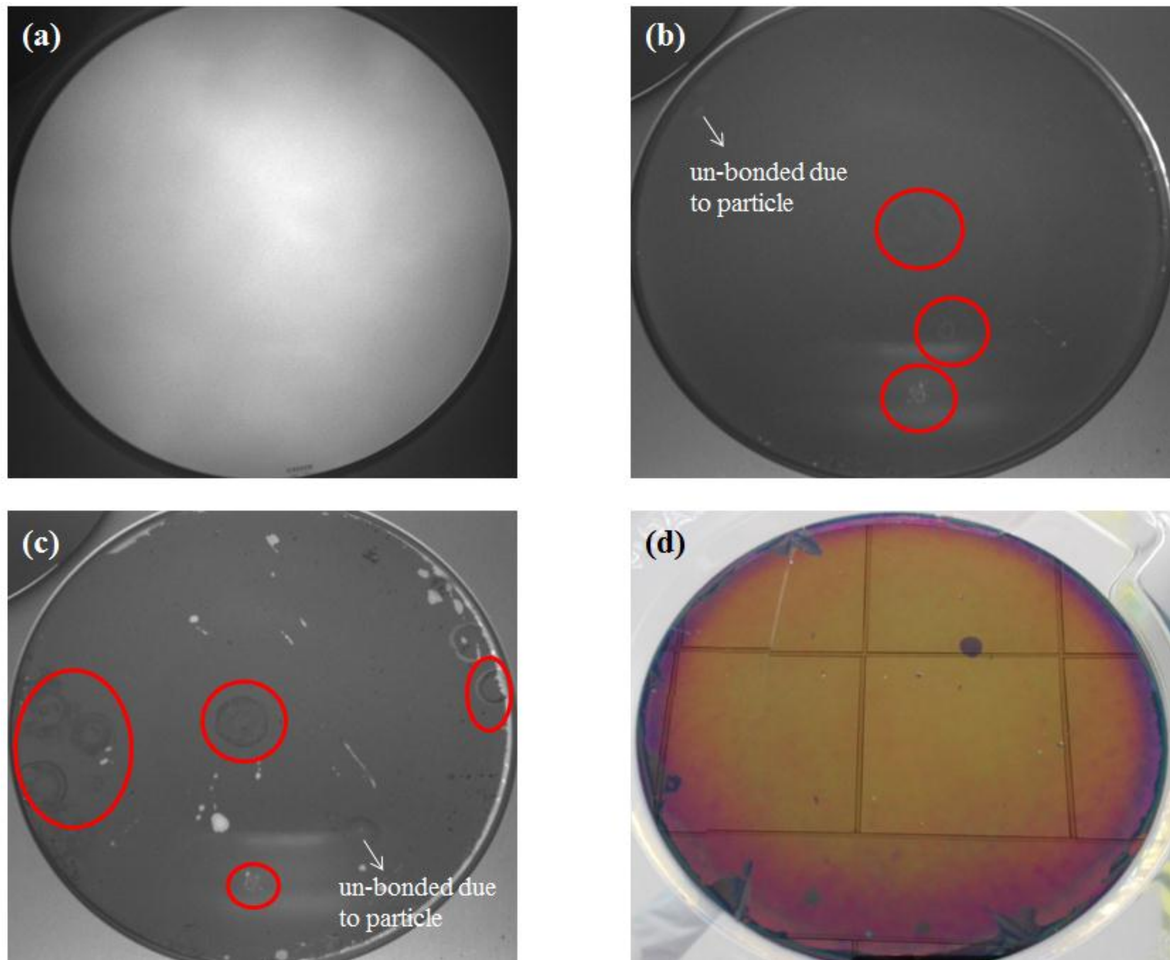

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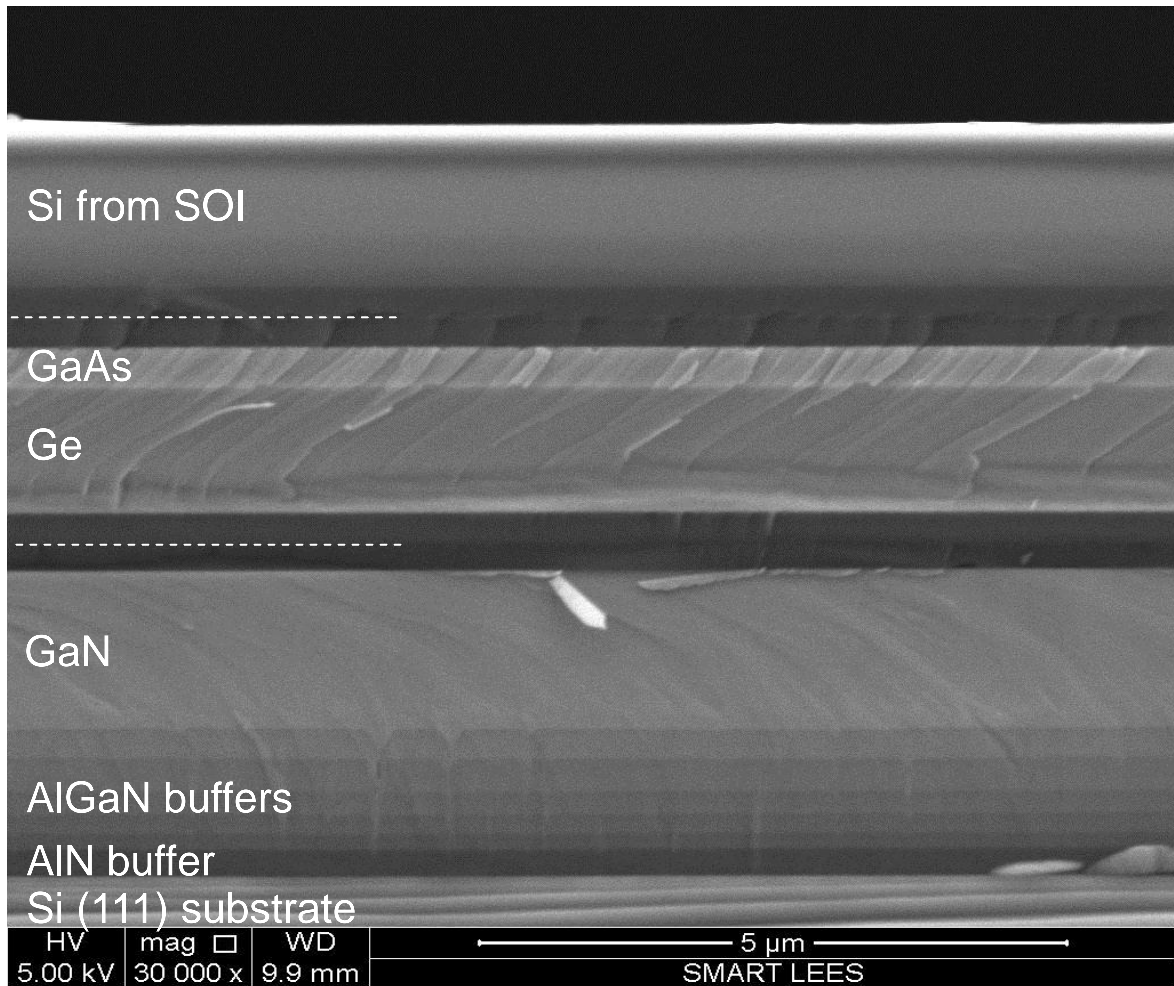

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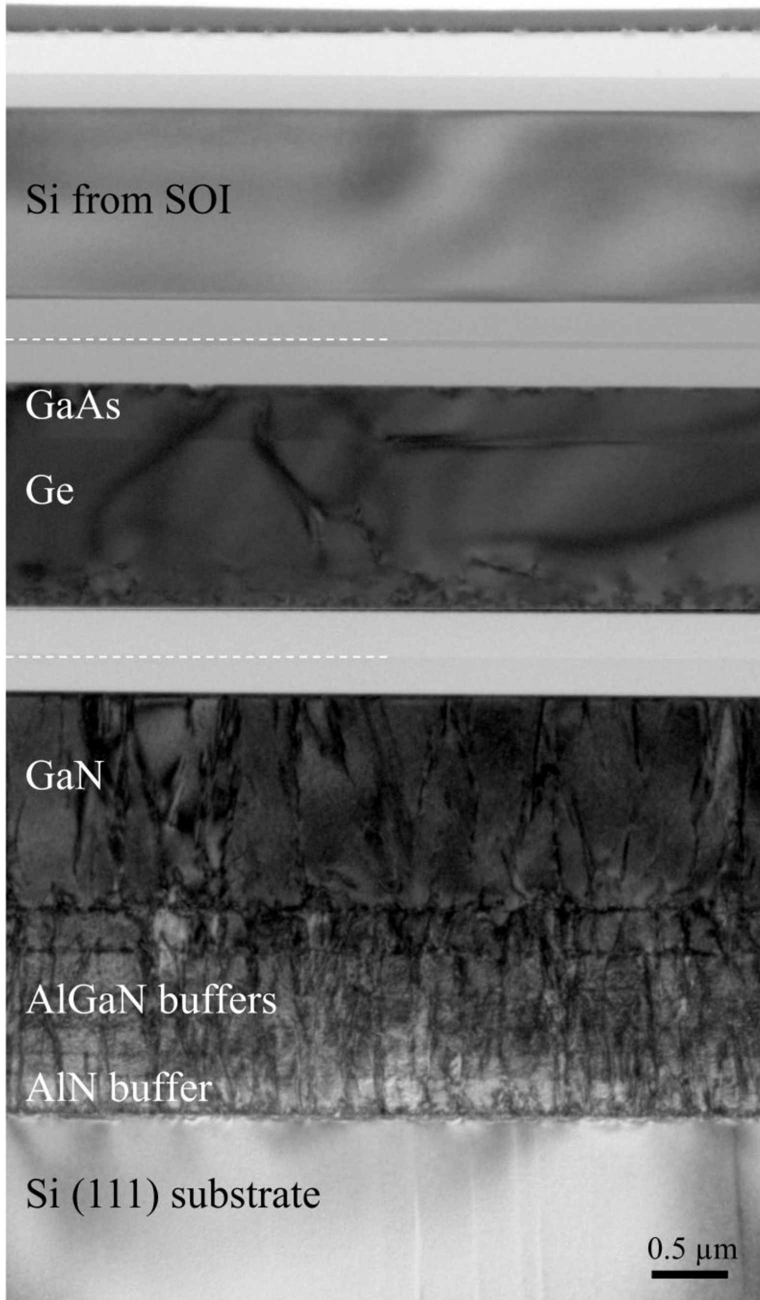

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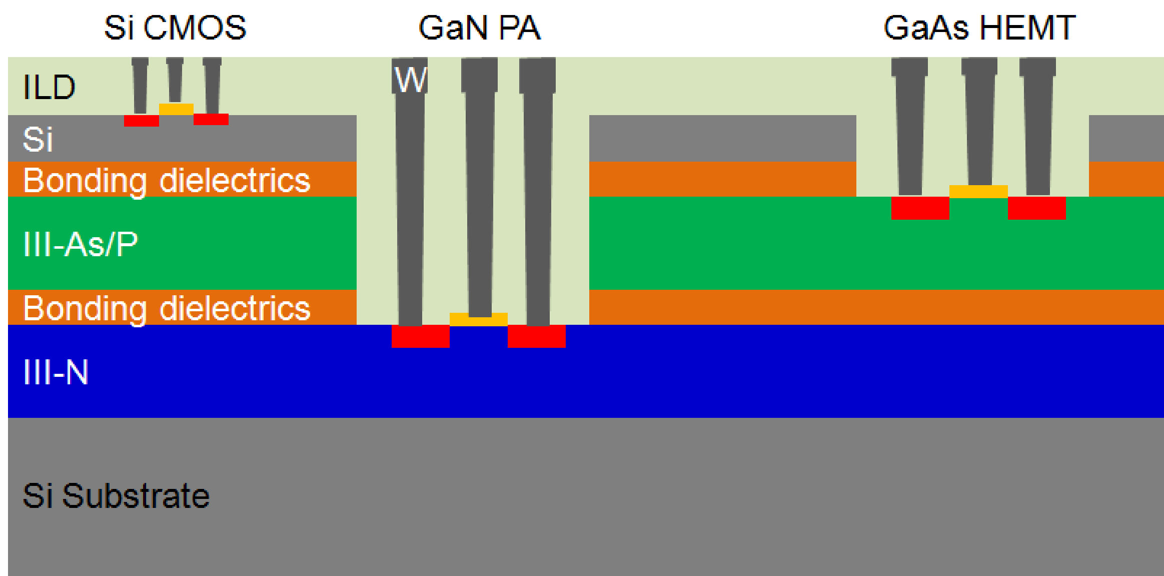

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