Intentionally Carbon Doped AlGaN/GaN HEMTs: Necessity for Vertical Leakage Paths

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***Abstract*— Dynamic ON-resistance (R_{ON}) in heavily carbon doped AlGaN/GaN high electron mobility transistors is shown to be associated with the semi-insulating carbon-doped buffer region. Using transient substrate bias, differences in R_{ON} dispersion between transistors fabricated on nominally identical epilayer structures were found to be due to the band-to-band leakage resistance between the buffer and the 2DEG. Contrary to normal expectations, suppression of dynamic R_{ON} dispersion in these devices requires a high density of active defects to increase reverse leakage current through the depletion region allowing the floating weakly p-type buffer to remain in equilibrium with the 2DEG.**

***Index Terms*—Dynamic ON-resistance, current collapse, HEMT, carbon doping, defects.**

I. Introduction

GaN-based high electron mobility transistors (HEMTs) are of increasing importance in high efficiency power switching applications because of their low capacitance, low on-resistance, and fast switching times. However, they are still subject to many of the same problems which apply to RF devices such as DC-RF dispersion or current-collapse (CC) [1]. A time dependent on-resistance resulting from charge storage in either surface or bulk traps can affect the performance of the device during switching. Surface trapping can be very effectively controlled by the use of field plates [2], but bulk trapping is inherent in all single-heterojunction HEMTs due to the inclusion of deep-level dopants in the GaN buffer to control bulk leakage and short-channel effects [3]. Carbon, which has a complex set of acceptor trap levels in the lower half of the bandgap [4], has been widely used as a GaN dopant for power switching applications due to its excellent breakdown properties, but has also been linked with current-collapse [5, 6]. Simulation suggested that intentional doping with carbon will result in a floating p-type GaN buffer with a consequent bias history dependent, and large, CC [7]. In this letter we experimentally show that low CC can be achieved by defect mediated leakage grounding the floating buffer.

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II. Experiment

Two wafers from a 600V depletion mode GaN-on-Si HEMT technology development were compared; device results are given in [8]. The wafers had nominally identical epitaxy, employing an intentionally carbon doped GaN buffer with an undoped channel region grown on P-type Si. The wafers had a pinch-off voltage V_P=−2V and very similar DC and breakdown properties, however wafer A showed a significant CC whereas wafer B was close to ideal. These wafers represent the extremes in CC observed. Here we seek to identify the electrical, but not the processing, origin of this difference in CC, and its underlying physical root cause.

Conventional dynamic R_{ON} (current collapse) measurements using identical geometry 100 µm width devices were undertaken using a Keithley 4200SCS parameter analyzer. The measurement procedure was to pulse from V_{GS}=0V, V_{DS}=0V to the OFF state at V_{GS}=−3V and V_{DS} of 50V and then wait for 1000s. The device was then pulsed back to the linear region ON state of V_{GS}=0V, V_{DS}= 1V (in about 10ms) and then the drain current, I_D, recorded as a function of time. There was a striking difference in the transient response between the wafers as can be seen in Fig. 1a. Wafer B showed negligible CC, whereas for wafer A I_D showed a serious long-timescale instability representing a >50% change in resistance.

Since it is challenging to distinguish between surface and bulk induced CC, a set of complementary CC measurements were undertaken using pulsed substrate bias [9, 10]. Changes in substrate bias applied to the silicon resulted in a change in the electric field below the 2DEG and hence a change in channel charge and I_D. Any slow change in I_D must be due to changes in buffer charge. This approach has the major advantage that any effect on the channel conductivity cannot be associated with surface effects, and the applied vertical electric field is roughly uniform between source and drain. Pulsed I_D transients were recorded following application of −200V V_{SUB}, with the results also shown in Fig. 1a. For wafer B there was only a relatively small change with time, whereas for wafer A there was a large dispersion of comparable size and time constant to that seen in the dynamic R_{ON} measurement. This strongly suggests a buffer origin and common underlying cause for the CC and the V_{SUB} transients.

Ramping the substrate bias was found to give an indication

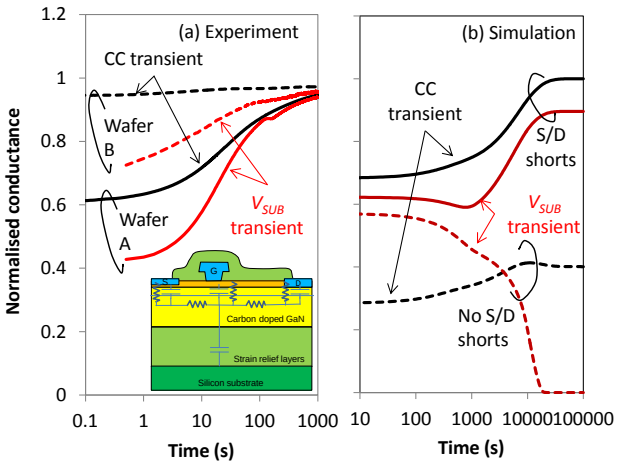

Fig. 1. (a) Black lines show normalized current collapse recovery - device conductance as a function of time following a step from OFF state (V_{DS}=50V, V_{GS} =−3V) to ON state (V_{DS}=1V, V_{GS} =0V). OFF state hold time was 1000s. Red lines show conductance recovery following application of a substrate bias of V_{SUB}=−200V. V_{DS}=1V. Wafer A - full lines, Wafer B - dashed lines. (b) ATLAS simulation of the current collapse and substrate bias transients for the same conditions as in (a). The solid lines have a low resistance short between the source and drain and the buffer. Inset schematic shows the transistor structure overlaid with the leakage paths. All data is normalized to the static conductance at V_{DS}=1, V_{SUB}=0, V_{GS}=0V.

of the location of the responsible defects. V_{SUB} was ramped to −200V and back to 0V for ungated devices with varying source-drain gap as shown in Figs. 2a,b for Wafers A and B. In the figure a ramp rate of 16V/s is shown since it was found to best illustrate the effect. For a 35µm gap, wafer A showed little hysteresis reflecting capacitive coupling between the 2DEG and the Si and little trapping in the buffer, whereas for smaller gaps hysteresis was observed implying that trapping was occurring. By contrast wafer B showed a source-drain gap independent hysteresis. The observation that I_D became independent of V_{SUB} indicates that once the vertical electric field exceeded a critical value, the potential in the GaN buffer ceased to increase. For a negative going ramp where the P-N diode is reverse biased, this implies the presence of a small leakage current between the 2DEG and the buffer which matches the capacitive displacement current. Wafer A showed a much weaker hysteretic effect for large gaps (although hysteresis was still present even for the largest gap), and hysteresis comparable to Wafer B for narrow gaps. The simplest explanation is that there is a reverse leakage path between the buffer and the 2DEG under the contacts in both

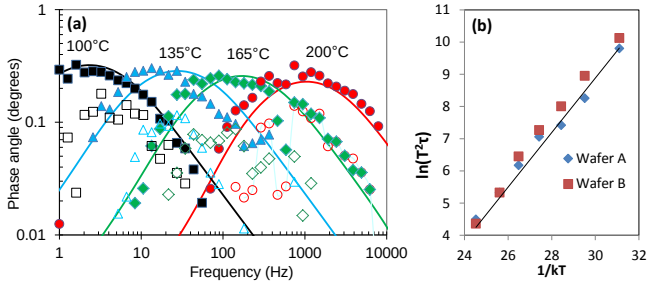

Fig. 3. (a) Transconductance dispersion (phase angle) for wafers A and B (open and solid symbols respectively) at selected temperatures. V_{GS}=~V_P, V_{DS}=50mV. Solid lines are from ATLAS simulation using the parameters given in the text. (b) Arrhenius plot for the two wafers. Solid line is a fit to the ATLAS peaks and has E_A=0.85eV.

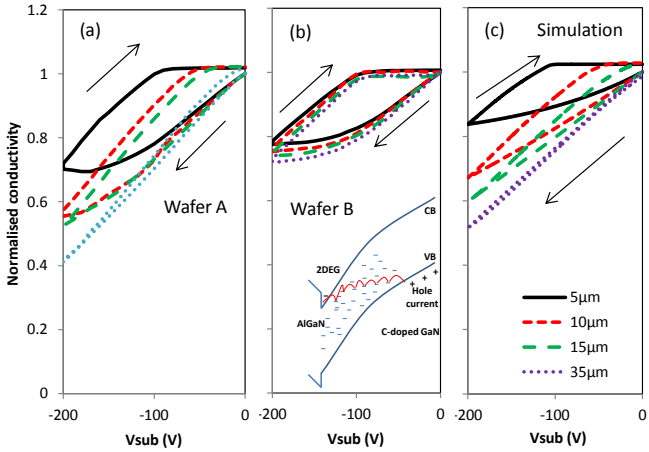

Fig. 2.Sheet conductivity of ungated AlGaN/GaN structures of length 5, 10, 15, 35µm during a ramp of the substrate bias from 0V to -200V and back to 0V. V_{DS}=1V. (a) and (b) show experimental data for Wafers A and B respectively with a ramp rate of 16V/s, and (c) shows a simulation of structures with the same gaps, with source and drain shorts, but at a ramp rate of 0.1V/s. The inset to (b) shows the trap-assisted-tunneling mechanism.

wafers, but the leakage is reduced (but not completely suppressed) in between the contacts for Wafer A and not Wafer B. For wafer A, poor lateral conduction through the semi-insulating buffer to the contacts allows changes in buffer potential to occur in the center of the device.

The ramp rate of 16V/s corresponds to a vertical displacement current of < 1pA for the structures shown in Figs. 2a,b. At the same time the static vertical substrate current was measured to be ≤10pA at -200V for these structures in both wafers. Hence although there are apparently local differences in vertical leakage in the channel region, these were not easily discernible in the substrate currents which may well be dominated by leakage to the contacts.

III. Model and Discussion

To explain these results, we base our model on the fact that carbon doping results in a p-type buffer with a very low density of holes isolated from the 2DEG by a depletion region [7]. GaN on Si is a very defective material with typically >10^9cm^{-2} threading dislocations, so GaN P-N diodes are expected to be leaky. Defect related leakage in such diodes has been reported to be strongly non-Ohmic and linked to multistep trap-assisted-tunneling, probably associated with threading screw and mixed dislocations[11, 12]. The resulting equivalent circuit is shown in the inset to Fig. 1a, and a schematic showing how holes can be injected into the buffer under reverse V_{SUB}, as required to explain the V_{SUB} transients, is shown in Fig. 2b. Since no obvious structural difference in the epilayers after processing was observed using focused ion beam cross-sectioning and SEM analysis, an atomistic origin is most plausible as the underlying root cause. The most logical explanation is that dislocations provide a natural vertical leakage path through the epilayer with different decoration or modification of these defects in the two wafers locally changing the vertical conductivity. These wafers represented the extremes of the processing runs, and although a responsible processing step has not yet been identified,

hydrogen represents a possible cause [13].

The key unknown parameter required to simulate the large-signal behavior is the actual resistivity of the carbon doped buffer. To measure this in the wafers studied and calibrate the model, we used small-signal transconductance (g_m) dispersion. This technique measures the frequency dependence of the loss-angle in the transconductance and is sensitive to trap states located under the gate [14, 15]. The dispersion arose here as a result of a simple *R*-*C* network where *R* was the distributed resistance of the buffer and *C* the capacitance of the depletion region under the gate. As expected the peak frequency was found to be independent of bias, with a magnitude falling above pinch-off. Both wafers showed very similar peak frequency between 100°C and 200°C within the accessible measurement frequency window indicating a similar resistivity, as can be seen in Fig. 3. The small-signal g_m dispersion was then simulated with Silvaco ATLAS using the same approach as [7, 15] with the results shown overlaid in Fig. 3. To achieve the fit as a function of temperature, a hole mobility of $\mu=8(T/373K)^{-1.5}cm^2/Vs$, and an active carbon density of $2x10^{18}cm^{-3}$ 0.92 eV above the valence band (consistent with [16]) compensated with shallow donors was used. Extrapolating to 20°C gave the required resistivity of $5x10^{13}$ Ωcm due to only ~10^4 cm^{-3} free holes. The excellent fit clearly demonstrates the P-type nature of the C doped buffer.

To demonstrate the validity of the experimental conclusion that such vertical conductivity differences result in vastly different CC, large signal device simulations were then performed. As it is non-trivial to simulate the situation of a conducting P-N junction across the entire source-drain gap as for wafer B, a scenario which corresponds closely to that which applies to wafer A was considered. P^{++} shorting regions were placed at the outside edge of the Ohmic contacts between the C doped buffer and the top metal i.e. simulating a conducting dislocation. These shorts had no effect on the simulated static I-V characteristics or the g_m dispersion. Fig. 1b shows that the predicted CC and V_{SUB} transients had a magnitude quantitatively similar to those observed in Wafer A, strongly supporting the model that lateral hole transport to vertical leakage paths through the contacts was present. In the absence of the shorts, and with an ideal junction, the transient charge stored in the buffer never leaked away and the buffer did not come into equilibrium (shown in Fig. 1b and [7]), indicating strongly the critical necessity for including leakage in simulations. Simulating the V_{SUB} ramp with the P++ shorts present gave a gap dependent hysteretic behavior and magnitude comparable to that observed for Wafer A if the ramp rate was reduced to 0.1V/s (see Fig. 2c). In all these large signal simulations, the time constants were about 100 times slower than experiment. This may be a result of error in the extrapolated buffer resistivity, but more likely is a consequence of leakage through non-Ohmic conducting defects present over the entire surface providing a parallel leakage path when biased, resulting in a shorter time constant.

In conclusion, it was demonstrated that GaN HEMTs on carbon doped buffers show small-signal transconductance dispersion characteristic of p-type buffer conduction. By contrast, large signal dispersion showed dramatic variation between wafers due to differences in stored buffer charge, dependent on the band-to-band leakage properties of defects in the channel region. Excellent agreement between 2D models and experiment was obtained. Contrary to what might normally be expected, suppression of the large signal dispersion in on-resistance during pulsed operation appears to require a large density of active conducting defects if the buffer is P-type, as is the case for intentionally C-doped GaN.

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