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Intercell Transformer (ICT) Design Optimization and Interphase Crosstalk Mitigation of a 100-kW SiC Filter-Less Grid-Connected PV String Inverter

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ABSTRACT Increasing the specific power and efficiency of a power converter has been the forever-lasting task for power electronics engineers. With the Wide bandgap (WBG) semiconductor devices, new opportunities and challenges have been found. In this article, a 100-kW SiC grid-connected Photovoltaic (PV) string inverter is proposed. This SiC inverter is free of a grid interface filter, the size, weight, and cost of magnetic components are therefore reduced. In addition, to further achieve high power density high efficiency at 100kW, design aspects including closed-form equation to avoid overdesign passive components, ICT design optimization, and interphase crosstalk mitigation with high switching frequency have been presented. A 100-kW three-phase two-stage prototype has been built in the laboratory, which achieves a specific power of 5 kW/kg, measured peak efficiency of 99.5%, and California Energy Commission (CEC) efficiency of 99.2%.

INDEX TERMS Inverter, power density, silicon carbide MOSFET, filter-less.

I. INTRODUCTION

In the course of a continuous emerging market during the past decades, photovoltaic (PV) industry experienced an unprecedented increase of annual installation from 105 MW in 1992 to 104 GW in 2018 [1], [2]. After several downturns of the global economy and slower growth of the profits in recent years, cost reduction has now become the dominant driver in PV systems development. A recent trend in the PV industry is to use three-phase string inverters for utility applications [3], [4]. Compared with an MW-level central inverter, a string inverter can be directly connected to the low voltage grid without a transformer and can be efficiently designed for outdoor operation without shelters. These features of string inverters will benefit a PV plant with better solar energy yield, lower installation time, and lower operation & maintenance cost. However, string inverters suffered from higher manufacturing cost per watt due to a smaller power rating per unit. The barrier to a higher power rating per unit is the weight issue of a PV string inverter. A commercial string inverter for 1000V PV panels has a specific power of around 1 kW/kg. When the power rating increases over 100-kW level, the weight of the inverter unit will be over 100 kg, which will significantly increase enclosure cost, installation cost, and maintenance cost.

Recently the adoption of the WBG device may reduce the weight of PV inverters. Silicon Carbide (SiC) inverters have increasingly popular in research for 10-kW to MW level power rating [5]–[16]. Although the advantages of SiC over

standard Si devices are the significantly decreased switching and conduction losses, the benefits of increased efficiency and reduced heatsink size can be easily offset by the high cost of SiC devices. Further exploring the benefits of SiC inverters requires increasing the switching frequency to minimize the filter weight and cost. However, it is not easy to reduce the LCL type filter weight by just increasing the switching frequency [5]–[9]. Due to the fact that the inductors of an LCL type filter must withstand high magnetic flux generated by the fundamental frequency current, high-permeability core materials are thereby preferred for their ability to make the same inductance with fewer turns. The inverter side inductor, on the other hand, has to withstand flux caused by switching frequency voltage harmonics. When switching frequency increases, the additional high-frequency loss increases, which limits the weight/cost reduction [10], [11]. For example, a commercial high power SiC inverter is designed to switch only at 8 kHz [13]. In [14], the total filter size of a SiC inverter can be even larger than that of a Si-based counterpart. New design approaches are needed for inverters when SiC devices are adopted.

One approach for filter weight reduction is to increase the switching frequency to several hundreds of kHz so that high-frequency magnetic materials, however low-permeability, can be applied. In the medium to high power applications, hundreds of kHz switching frequency prefer soft switching technologies to further reduce switching loss [15]–[18]. For example, Z. Huang *et al*. designed a 25-kW SiC three-phase inverter operated at critical conduction mode (CRM) to achieve zero-voltage-switching (ZVS) [15]. The switching frequency increased to above 300 kHz, and peak efficiency is close to 99%. The total LCL inductance is 10.3 μH for each phase. A similar approach has also been discussed in [10] where Triangular Current Mode (TCM) is applied for a three-phase inverter. CRM or TCM requires increasing the inverter side inductor current ripple to 100% to achieve zero-voltage turn-on, the cost is the increased turn-off loss and increased Root Mean Square (RMS) current flowing through switches, inverter side inductors, and output capacitors. Therefore this method is beneficial for medium to low power WBG converters as WBG devices usually have much smaller turn-off loss than turn-on loss. It has not been demonstrated for higher power applications that the reduced turn-on switching loss will still be beneficial with increased turn-off loss, conduction loss, and inductor loss caused by high current ripples. Another soft-switching method is to use an auxiliary switch assisted resonant circuit. N. He *et al.* presented a 20-kW ZVS SiC inverter with 98.74% peak efficiency in [18] where the ac side inductance is 33 μH, and auxiliary inductance is 2 μH when switched at 300 kHz. Compared with a hard-switched inverter at 100 kHz switching frequency, the total inductor volume of this ZVS inverter has been reduced from 1.14 liters to about 0.5 liters. Although these high switching frequency based designs have shown effective inductor size reduction, it will lead to a new design issue because the switching frequency will fall into the EMI frequency range (150 kHz to 30 MHz). As EMI standards usually have much higher harmonic suppression requirements than utility code [19], switching faster than 150 kHz will bring more challenges to EMI noise suppression and/or CM chock design [20].

In the authors' previous work [25], a filter-less five-level (5L) SiC inverter was proposed to reduce the weight for a 60-kW three-phase PV string inverter. The basic topology is a three-level T-type ($3LT^2$) circuit, which is well adapted in the PV industry [21]–[24]. Two $3LT^2$ circuits were interleaved with an intercell transformer (ICT) to form a 5L output voltage. A specific power of 3kW/kg and peak efficiency of 99.2% has been achieved for this 60-kW PV string inverter. This paper aims to increase the power rating of the proposed PV inverter to 100-kW without increasing the weight. To further improve the efficiency and specific power, the passive components need to be optimized. Also, the SiC MOSFETs need to be switched faster without false triggering. The paper focuses on solving the above-mentioned design challenges. Section II presents the closed-form equations of high-frequency DM voltage, CM voltage, and dc side current harmonics of proposed 100-kW PV string inverter. These equations are used at the early design stage to prevent the overdesign of passive components. In Section III, the optimization procedure of ICTs is provided with a design case and closed-form equations. The analysis in Section III also presents a new aspect of ICT design: the weight of an ICT is directly related to the accuracy of circulating current control. The analysis shows that the specific core loss of ICT will reduce when switching frequency increases. This feature makes the ICT more preferable for high switching frequency applications over conventional LCL inductors, in which the specific core loss will increase with switching frequency. Section IV focus on how to prevent falsely triggering the SiC MOSFETs. The conventional false triggering issue can be identified at the double pulse testing stage and can be prevented with proper gate driver isolations. However, a different phenomenon has been identified in this paper, which can also lead to false triggering. This phenomenon, named as the inter-phase crosstalk issue, will only happen when there are multiple phase legs switching together. This issue has been analyzed with finite element analysis (FEA) based circuit parasitic extraction and compared with vector network analyzer (VNA) measurements. An improved PCB design is then proposed to solve the new discovered inter-phase crosstalk issue. A 100-kW PV string inverter has been built in the laboratory. The total weight of the 100-kW dc/dc and dc/ac two-stage prototype is less than 20 kg where the total weight of ICTs is less than 2.5 kg. The measured CEC weighted efficiency is 99.2% with a peak efficiency of 99.5% at 720 V input.

II. AN ANALYTICAL BASED PASSIVE COMPONENTS SELECTION METHOD

To achieve high specific power, it is import not to oversize passive components. The passive components that contribute most to system weight and power loss are ac side DM and CM inductors and dc-link capacitors. Selecting these passive

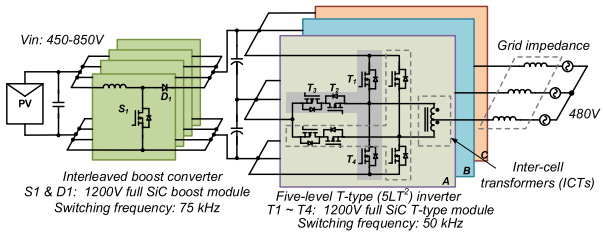

FIGURE 1. The 100-kW two-stage SiC 5LT^2 filter-less PV string inverter.

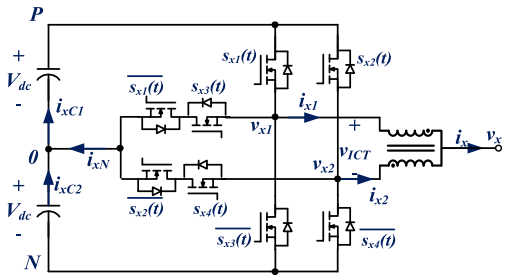

FIGURE 2. One phase schematic of 5LT^2 inverter where s_{x1} , s_{x2}, s_{x3}, s_{x4} are switching functions and $x \in \{a, b, c\}$.

components is usually an iterative task that needs multiple inputs including environmental conditions, operation profile, lifetime requirement, and cost constraint. These inputs vary from design to design. But the common factors for passive components design are the current stress and voltage stress. As the parasitics, power loss, and lifetime of passive components are all frequency-dependent, it is desirable to derive current and voltage stress in the frequency domain. In this section, the spectrums of dc link current and ac side voltage for this three-phase 5LT^2 inverter are derived analytically. As the equations are in closed-form, they can apply to 5LT^2 inverters at any desired operating conditions. The analysis in this section also quantifies the significant reduction of harmonics compare to those of three-level inverters.

A commercial PV string inverter usually includes dc/dc stage and dc/ac stage. The topology of the proposed SiC 100-kW PV string inverter is shown in Fig. 1. The dc/dc stage consists of four SiC interleaved boost circuits. The dc/ac stage is a three-phase 5LT^2 inverter with six 1200 V SiC T-type modules provided by Wolfspeed. Every two modules are parallel-coupled through an ICT to form one phase that has five-level line-to-neutral output voltage [25], [26].

The four switching functions of one phase 5LT^2 inverter are defined as s_{x1}, s_{x2}, s_{x3}, s_{x4}, which are shown in Fig. 2. Switching states corresponding to different voltage levels are listed in Table 1. The redundant switching states in Lv1, Lv2, and Lv3 are used for ICT circulating current control. One way to generate the switching signals for the 5LT^2 inverter is to interleave the carriers of two 3LT^2 inverters. The upper and lower carriers of a 3L carrier-based modulation can be placed in the same direction or in the opposite direction, which are named phase disposition (PD) modulation and phase opposition disposition (POD) modulation, respectively. The key waveforms of the 5LT^2 inverter are presented in Fig. 3.

TABLE 1. Switching States of One Phase of the 5LT^2 Inverter

Level	Switching states $s_{x1}\, s_{x2}\, s_{x3}\, s_{x4}$	$v_x = 0.5(v_{x1}+v_{x2})$	$v_{ICT} = v_{x1} - v_{x2}$
Lv4	1111	V_{dc}	0
Lv3	1011	$V_{dc}/2$	V_{dc}
	0111		$-V_{dc}$
Lv2	1010	0	$2V_{dc}$
	0011		0
	0101		$-2V_{dc}$
Lv1	0010	$-V_{dc}/2$	V_{dc}
	0001		$-V_{dc}$
Lv0	0000	$-V_{dc}$	0

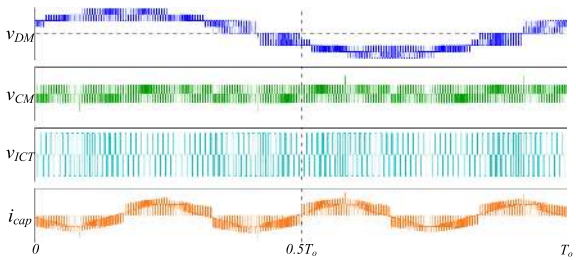

FIGURE 3. Waveforms of v_{DM}, v_{CM}, v_{ICT}, i_{cap} (carrier ratio reduced 10 times for easy observation).

The carrier ratio is reduced by 10 times for easy observation. v_{DM}, v_{CM}, v_{ICT}, i_{cap} are DM voltage, CM voltage, ICT winding voltage, and dc neutral point current, respectively.

Although 3L PD and POD modulation generate different voltage spectrums, with the method from [25], it can be proved that both modulations will generate a voltage spectrum that is the same as 5L alternative phase opposition disposition (APOD). The line-to-neutral voltage spectrum of interleaved modulation is defined as $v_x, x \in \{a, b, c\}$, which can be derived as:

$$\begin{aligned} v_x(t) = {} & V_{dc} M \cos \omega_o t \\ & + \frac{V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \sum_{n=-\infty}^{\infty} J_{2n+1}(2m\pi M) \cos(n\pi) \\ & \times \cos(2m\omega_c t + [2n+1] \cdot [\omega_o t + \theta_x]) \end{aligned} \quad (1)$$

where V_{dc} is the half dc-link voltage, M is the modulation index, ω_o *and* ω_c are the fundamental and carrier angular frequency, respectively, with m, n being the harmonic order for carrier frequency and fundamental frequency. $J_n()$ is the n-th order Bessel function of the first kind where $x \in \{a, b, c\}$, $\theta_a = 0$, $\theta_b = -2\pi/3$, $\theta_c = +2\pi/3$. The harmonics are always odd sidebands around the even carrier multiples, therefore the equivalent switching frequency is twice the actual switching frequency. In (1) and the following equations in this paper, the reference zero potential point for circuit analysis is chosen as the dc capacitor neural, which is the point 0 in Fig. 2.

Derived from (1), the line-to-line voltage spectrum is shown in (2) shown at the bottom of the next page, where

harmonics at $2m\omega_c \pm 3n\omega_0$ are canceled, with m, n being a positive integer:

The voltage spectrum of ICT is derived as:

$$v_{ICT}(t) = \frac{4V_{dc}}{\pi}\sum_{m=0}^{\infty}\frac{1}{2m+1}\sum_{n=-\infty}^{\infty}J_{2n+1}\left[(2m+1)\pi M\right] \cdot \cos(n\pi)\cos\left([2m+1]\omega_c t + [2n+1]\omega_o t\right) \quad (3)$$

From (3) it can be observed that there is no low-frequency harmonics applied on ICT, v_{ICT} only contains odd sidebands around the odd carrier multiples.

The high-frequency CM voltage needs to be derived for ground leakage current suppression or CM voltage reduction purpose, which is shown below:

$$\begin{aligned} v_{CM_HF}(t) &= \frac{V_{dc}}{3}\left[s_a(t) + s_b(t) + s_c(t)\right] \\ &= \frac{V_{dc}}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sum_{n=-\infty}^{\infty}J_{3\cdot(2n+1)}(2m\pi M)\cos(3n+1) \\ &\quad \times \pi\sin\left[2m\omega_c t + 3(2n+1)\omega_0 t\right] \end{aligned} \quad (4)$$

where $s_{a,b,c}(t)$ are the switching functions in the time domain. The dc side current spectrum should also be derived in order to design the dc-link capacitor. Previous efforts to derive the dc-link capacitor current for 5LT^2 inverters only gives simplified results at low frequency [28]. In this paper, the entire spectrum of capacitor current is derived using the method from [29]. In the frequency domain, one phase-leg's contribution to the dc-link current is the superposition of the phase-leg's switching function spectrum with frequency shifts of $\pm\omega_o$, which is described in (5):

$$I_{DC}(\omega) = \frac{I_o}{2}\left[e^{j\emptyset}S_1(\omega-\omega_o) + e^{-j\emptyset}S_1(\omega+\omega_o)\right] \quad (5)$$

where $\emptyset$ is the power factor angle, $I_o$is the amplitude of the fundamental current, and $S_1(\omega \pm \omega_o)$ are the switching functions in the frequency domain. With (5), the harmonic coefficients of the dc-link current can be derived from harmonic coefficients of the switching function.

In a 5LT^2 inverter, the current flowing into the upper and lower dc-link capacitors are the same over a fundamental cycle. The dc neutral point current should be treated as the total dc-link current and the upper and lower capacitors are equally sharing the neutral current. The time-domain expression of the dc-link capacitor voltage is shown in (6):

$$\begin{aligned} i_{cap}(t) &= i_{an}(t) + i_{bN}(t) + i_{c_N}(t) \\ &= \sum_{x\in a,b,c}\left[s_{x1}(t) - s_{x2}(t) + s_{x3}(t) - s_{x4}(t)\right]\cdot i_x(t) \end{aligned} \quad (6)$$

In the frequency domain, (6) is transferred into convolution shown in (7):

$$\begin{aligned} I_{cap}(\omega) &= \sum_{x\in a,b,c}\left[S_{x1}(\omega) - S_{x2}(\omega) + S_{x3}(\omega)\right. \\ &\quad \left. - S_{x4}(\omega)\right] \otimes I_x(\omega) \end{aligned} \quad (7)$$

Equation (8) can then be derived from (5) and (7):

$$\begin{aligned} I_{cap}(\omega) = \frac{I_o}{2}\sum_{x\in a,b,c}\Big[&e^{j\emptyset}S_{x1}(\omega-\omega_o) + e^{-j\emptyset}S_{x1}(\omega+\omega_o) \\ &- e^{j\emptyset}S_{x2}(\omega-\omega_o) - e^{-j\emptyset}S_{x2}(\omega+\omega_o) \\ &+ e^{j\emptyset}S_{x3}(\omega-\omega_o) + e^{-j\emptyset}S_{x3}(\omega+\omega_o) \\ &- e^{j\emptyset}S_{x4}(\omega-\omega_o) - e^{-j\emptyset}S_{x4}(\omega+\omega_o)\Big] \end{aligned} \quad (8)$$

From (8), the coefficient of capacitor current at ω can be calculated by summarizing coefficients of the twelve switching functions at $\omega \pm \omega_o$. It should be noted that in 3L NPC or T-type converters, the spectrum of s_{x1} and s_{x2} are different from the spectrum of one phase leg voltage since the spectrum of s_{x1} and s_{x2} are the results of half sinusoidal waveform compared with the triangular waveform. Therefore, the spectrum of s_{x1} and s_{x2} must be calculated using double-Fourier series [27].

Therefore, the dc neutral point current spectrum of one phase leg can be calculated as:

$$\begin{aligned} i_{xN}(t) = \frac{I_o}{4}\Bigg\{&\left(\frac{10M}{3\pi} - 1\right)\cos(\omega_o t + \theta_x) \\ &- \frac{8M}{\pi}\sum_{n=3}^{\infty}\frac{(1-\cos(n\pi))\sin\left(\frac{n\pi}{2}\right)}{n\left(n^2-4\right)}\cos(n\omega_o t + n\theta_x) \\ &+ \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{2m-1,\,2n}\cos\left([2m-1]\left[\omega_c t + \theta_c\right]\right. \\ &\left. + 2n\left[\omega_o t + \theta_x\right]\right) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{2m,2n+1} \\ &\times\cos(2m\left[\omega_c t + \theta_c\right] + [2n+1]\left[\omega_o t + \theta_x\right])\Bigg\} \end{aligned} \quad (9)$$

$$\begin{aligned} C_{2m-1,2n} = &\frac{2\cos(n\pi)}{(2m-1)\pi} \\ &\times\left\{J_{2n+1}([2m-1]\pi M) - J_{2n-1}([2m-1]\pi M)\right\} \end{aligned} \quad (10)$$

$$v_{ab}(t) = v_a(t) - v_b(t) = \sqrt{3}V_{dc}M\cos\left(\omega_o t + \frac{\pi}{6}\right) + \frac{\sqrt{3}V_{dc}}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sum_{n=-\infty,\,2n+1\neq 3k,\ k\ integer}^{\infty}J_{2n+1}(2m\pi M)\cos(n\pi) \times\cos\left(2m\omega_c t + [2n+1]\cdot\left[\omega_o t + \theta_x + \frac{\pi}{6}\right]\right) = \sqrt{3}v_{DM}(t) \quad (2)$$

$$C_{2m,2n+1} = \frac{4\cos(n\pi)}{m\pi^2}\left\{\sum_{k=1}^{\infty}(2k-1)\cdot J_{2k-1}(2m\pi M)\cdot\left[\frac{1}{(2k+2n-1)(2k-2n-1)} - \frac{1}{(2k+2n+1)(2k-2n-3)}\right]\right\} \quad (11)$$

Equation (9) contains odd-order fundamental harmonics, even- and odd-order switching harmonics and their sidebands. With the interleaved phase legs, the combined dc current harmonics of one phase leg contains odd-order fundamental harmonics, even-order switching harmonics sidebands. With all six phase legs from three phases, the dc current spectrum only contains $3n\omega_o$ and $2m\omega_c \pm 3k\omega_o$ harmonic components, which is derived as:

$$i_{cap}(t) = \frac{3I_o}{2}\left[\frac{16M}{\pi}\sum_{\substack{n=1,\\ n\ is\ odd}}^{\infty}\frac{1}{3n\left(9n^2-4\right)}\cos(3n\omega_o t) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}C_{2m,3(2n+1)}\cdot\cos(2m\omega_c t + 3[2n+1]\omega_o t)\right] \quad (12)$$

$$C_{2m,3(2n+1)} = \frac{4\cos(3n\pi)}{m\pi^2}\left\{\sum_{k=1}^{\infty}(2k-1)J_{2k-1}(2m\pi M)\cdot\left[\frac{1}{(2k+6n+1)(2k-6n-3)} - \frac{1}{(2k+6n+3)(2k-6n-5)}\right]\right\} \quad (13)$$

Equation (12) covers both low frequency and high frequency. It can be used for sizing electrolytic and film capacitors. (12) shows the switching frequency components disappeared, and only part of the sidebands remain at $2\omega_c$.

The above analysis is based on interleaved modulation. The spectrum of interleaved modulation is equivalent to 5L alternative phase opposition disposition (APOD). In some cases, 5L PD modulation is preferred for smaller line-to-line voltage harmonics. To achieve 5L PD or POD, a state-machine based modulation method and its analysis can be found in [30] and [31]. The dc-link current spectrum of 5L PD and POD can be derived following the same procedure from (6) to (12).

The above equations are utilized to find the closed-form spectrum expressions of key circuit waveforms, as they are not currently available from literature for this $5LT^2$ topology and were not derived in the authors' previous work [25], [28]. Equation (1)–(4) and (12) saved the time-consuming task of finding the spectrum of $v_{DM}, v_{CM}, v_{ICT}, i_{cap}$ under different operation conditions through iterations of simulations. Instead, these viable can be quickly calculated via Matlab or python script so that a software design tool can be developed to automatically select the passive components.

Compared with 2L or 3L inverters, $5LT^2$ inverters have smaller voltage harmonics at ac side and smaller current harmonics at dc side. A frequency-weighted RMS value of v_{DM}, v_{CM}, i_{cap} are defined in (14)–(16) to further simplify the design process. This frequency-weighted RMS definition specifies the high order switching harmonics referring to the switching frequency, so it reflects the impedance needed to suppress the RMS value exactly to a required design target. As a result, the passive component is proportional to its frequency-weighted RMS (WRMS) value and will not be overdesigned.

$$V_{DM,WRMS} = \frac{1}{\sqrt{2}}\cdot\sqrt{\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left(\frac{V_{DM,mn}}{m}\right)^2} \quad (14)$$

$$V_{CM,WRMS} = \frac{1}{\sqrt{2}}\cdot\sqrt{\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left(\frac{V_{CM,mn}}{m}\right)^2} \quad (15)$$

$$I_{cap,WRMS} = \frac{1}{\sqrt{2}}\cdot\sqrt{\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\left(\frac{I_{cap,mn}}{m}\right)^2} \quad (16)$$

As an example, the required CM inductance to suppress the ground leakage current, defined as $(i_a + i_b + i_c)/3$, can be calculated using the following steps:

1) Obtain CM RMS current limitation $I_{CM,RMS}$ from utility code or application requirements.
2) Derive the low frequency component of ground leakage current $I_{CM,RMS,LF}$ [28] and calculate the high frequency limitation by $I_{CM,RMS,HF} = \sqrt{I_{CM,RMS}^2 - I_{CM,RMS,LF}^2}$.
3) Calculate the CM inductance using $L_{CM} = \frac{V_{CM,WRMS}}{I_{CM,RMS,HF}\cdot\omega_C}$.

It should be noted that WRMS only contain high frequency components. The low frequency ground leakage current is suppressed through control [28]. In (14)–(16), each of the terms will decrease fast as m and n increases. Therefore only a limited number of m and n need to be calculated. With equation (1)–(4), (12), and (14)–(16), the weighted RMS value can be calculated for DM voltage, CM voltage, and dc-link capacitor current, as shown in Fig. 4. Compared with $3LT^2$ inverters, the frequency-weighted DM voltage switching harmonics of the $5LT^2$ inverter, at 800 V, is reduced to 26.1%, the frequency-weighted CM voltage switching harmonics is reduced to 7.9%, and the frequency-weighted dc-link capacitor current switching harmonics is reduced to 5.6%. Fig. 4 leads to a lightweight design that no DM power filter is needed, CM choke can be designed with a small size and the number of metal film capacitors can be reduced. Therefore, the specific power of 10 kW/kg is achieved for inverter stage only and 5 kW/kg achieved for a 100-kW 2-stage PV string inverter.

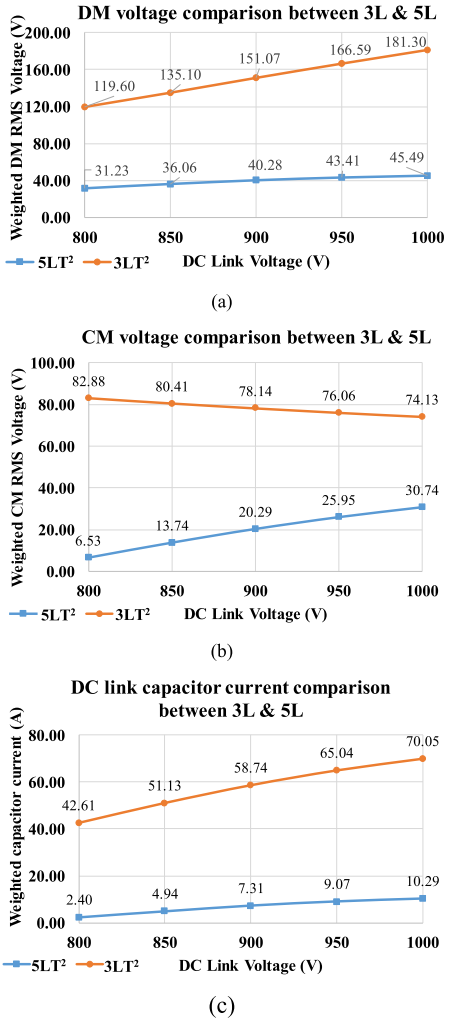

FIGURE 4. **Comparison of switching harmonics between 3LT² and 5LT² inverter. (a) $V_{DM,WRMS}$, (b) $V_{CM,WRMS}$, and (c) $I_{cap,WRMS}$ (condition: 480 Vac 100 kW output, switching frequency 50 kHz).**

III. ICT DESIGN OPTIMIZATION

The operation principles of ICT has been explained in detail in [25]. In this section, the optimized design of ICT to achieve minimum weight and power loss as well as avoid saturation is presented. The optimized design of ICT is divided into a two-step procedures: first, derive the minimum mass of magnetic core based on preventing saturation; second, using the core selected in step one as the initial input, optimize power loss by sweeping the turns number N and dimension of the cores.

A. DERIVING THE MINIMUM MASS OF THE MAGNETIC CORE

To prevent ICT from saturation, (17) must be met.

$$\Delta B\,(\max) + B_{bias} < B_{sat}$$
$$\text{where } \Delta B\,(\max) = \frac{V_{dc}T_s}{4NA_e},\ B_{bias} = \frac{N}{A_eR_m}\cdot I_{bias} \tag{17}$$

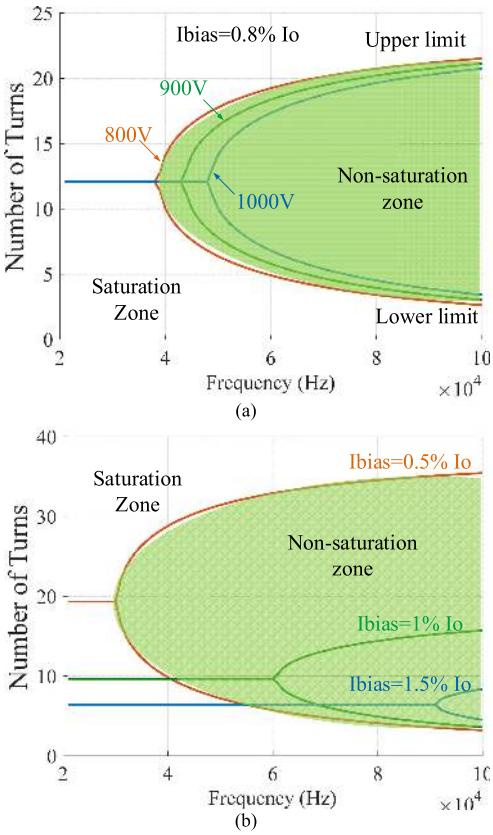

FIGURE 5. **ICT turns number range vs. switching frequency. (a) at different dc-link voltage, and (b) at different circulating current.**

In (17), A_e is the effective cross-section area of the core. R_m is the magnetic reluctance. B_{bias}, I_{bias} are the low frequency component of the core magnetic flux and circulating current, respectively. To meet (17), the turns number N must be large enough to reduce flux fluctuation, while in the meantime it cannot be too large to cause saturation at a small circulating current. The range of N is derived in (18):

$$N \in \left[\frac{B_{sat}A_eR_m - \sqrt{B_{sat}^2A_e^2R_m^2 - V_{dc}I_{bias}T_sR_m}}{2I},\right.$$
$$\left.\times\ \frac{B_{sat}A_eR_m + \sqrt{B_{sat}^2A_e^2R_m^2 - V_{dc}I_{bias}T_sR_m}}{2I}\right] \tag{18}$$

The range of N under different switching frequency, different dc-link voltage and different circulating current is presented in Fig. 5, where a safe-range of N is defined to prevent ICT from saturation. If the range is large, it means there is enough margin from saturation and N can be adjusted to minimize power loss. If the upper limit and lower limit meet each other, it's practically hard to prevent ICT from saturation at this frequency. Fig. 5 is the necessary condition of building a functioned ICT. From Fig. 5(b), it shows the circulating current control is a critical factor of making a small ICT.

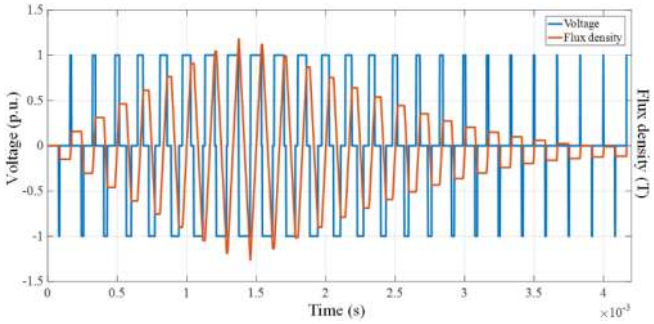

FIGURE 6. The waveforms of magnetic flux density and voltage applied to the ICT in a quarter line cycle, with the carrier ratio reduced for easy observation.

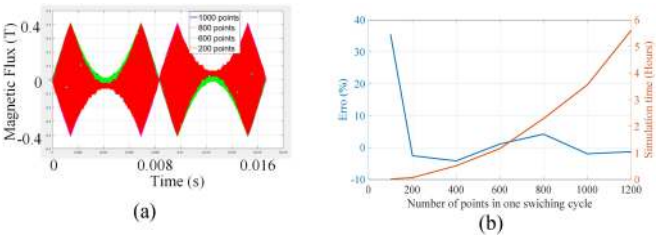

FIGURE 7. ICT Performance under different sample points in each switching cycle. (a) Magnetic flux design plots. (b) Calculation time and error (CPU: i7-4770 RAM: 8 GB).

Based on this principle, the minimum mass of ICT can be derived accordingly.

To make sure there is a positive real number N, the condition $B_{sat}^2 A_e^2 R_m \geq V_{dc} I_{bias} T_s$ must be met, which results in (19).

$$I_{bias} \leq \frac{B_{sat}^2 A_e^2 R_m f_s}{V_{dc}} \tag{19}$$

In this research, I_{bias} of each ICT are sensed by differential current sensors, and controlled by a closed-loop controller in parallel with the output current controller [25]. Therefore, the mass of the ICT core is a function of power rating, switching frequency, core material and the error of I_{bias} control shown in (20).

$$mass \geq e\% \cdot \frac{\mu_{avg} \rho_V}{k_v B_{sat}^2} \cdot \frac{P_o}{3 M f_s} \tag{20}$$

Equation (20) is derived from (19), where $k_v = (A_e \cdot MPL)/Volume$ is the volume correction coefficient. $e\%$ is the percentage of circulating current referred to fundamental current. M is the modulation index. MPL is the magnetic pass length. ρ_V is the volumetric mass density. μ_{avg} is the averaged permeability, it can be replaced with the permeability of the core when the air gap is small enough.

Equation (20) is the scale-law for ICT, it can be used to choose a baseline core size as the starting point of loss optimization. Since (20) is derived from (18), the selected baseline core will meet the non-saturation range defined in Fig. 5. (20) also shows that, increasing switching frequency can directly reduce the mass of ICT. It is equally important to increase the accuracy of circulating current control, as the amount of circulating current is in a linear relationship with the mass of ICT.

B. ICT POWER LOSS OPTIMIZATION

The magnetic flux density waveform of ICT is shown in Fig. 6. It has two unique features: Firstly, unlike inductors in grid-connected voltage source converters (VSC), there is no fundamental frequency flux density in ICT cores. Therefore the trajectory in the BH plane can be treated as a group of closed curves; no minor loop separation is needed [34]. The core loss characteristics of ICT is simpler than that of an ac inductor in VSC. Second, compared with a high-frequency transformer, the ICT is also excited with rectangular voltage, but the duty ratio is different in each switching cycle.

The core loss of ICT can be calculated using iGSE method [34] by (21).

$$\overline{P_{core}} = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{21}$$

The iGSE method can provide enough accuracy under non-sine excitation, and only Steinmetz parameters (k, α, β) are needed. In this application, as the duty ratio of ICT voltage is constantly changing, numerical calculations are required [35]. To achieve enough accuracy, hundreds of data points in each switching cycle is necessary, as shown in Fig. 6. Therefore, the calculation time for high switching frequency application can reach to several hours for one design, which limits its application in ICT design optimization for the proposed 100-kW SiC PV inverter.

Since the converter is controlled in such way that the volt-seconds applied on ICT always returns to zero within one switching cycle, then equation (21) can be further simplified based on the fact of dB/dt being constant. In addition, only a quarter of the line cycle needs to be calculated since the ICT voltage is symmetrical across [0, pi/4, pi/2, 3pi/4] of each line cycle. Thereby a simplified core-loss calculation method is derived as (22):

$$\overline{P_{core}} = 4 k_i f_o \left(\frac{V_{dc}}{N A_e} \right)^{\beta} \sum_{n=1}^{\frac{f_s}{2f_o}} \Delta T_{on}(n)^{\beta - \alpha + 1}$$

$$= 4 k_i f_o f_s^{\alpha - \beta - 1} \left(\frac{V_{dc}}{N A_e} \right)^{\beta} \sum_{n=1}^{\frac{f_s}{2f_o}} d_{ICT}(n)^{\beta - \alpha + 1} \tag{22}$$

where $\overline{P_{core}}$ is the averaged specific core loss. $\Delta T_{on}(n) = T_{inv1}(n) - T_{inv2}(n)$ is the time duration when the voltage applied on ICTs at the n-th switching cycle, which is the difference of on-times of the two interleaved inverter legs. $d_{ICT} = \Delta T_{on}/T_s$, is the duty ratio of ICT voltage waveform. Sum of

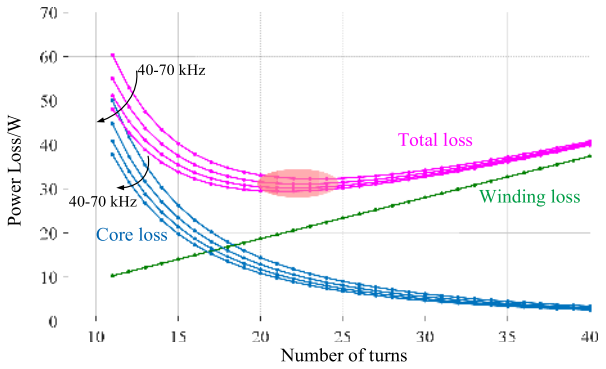

FIGURE 8. ICT power loss calculation with different turns at multiple switching frequencies.

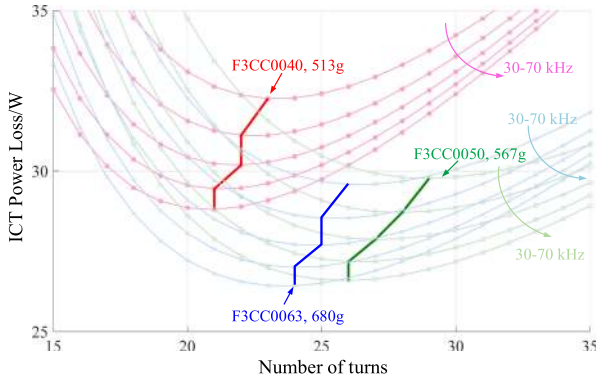

FIGURE 9. ICT power loss vs. turns at different core size.

$d_{ICT}(n)^{\beta-\alpha+1}$ is only affected by switching frequency and modulation index. Since (22) doesn't require calculating flux density, the calculation time has been reduced to 0.2 seconds.

The current flowing through ICT windings is dominated by fundamental frequency current. Thereby the winding loss can be calculated by (23).

$$P_{wire} = 0.25 I_{RMS}^2 R_{wire} = 0.25 I_{RMS}^2 \cdot \rho N \frac{MLT}{CopperHeight \times CopperWidth} \quad (23)$$

where I_{RMS} is the RMS value of output current, R_{wire} is the dc resistance of the windings, ρ is resistivity, N is the number of turns of the two windings, and MLT is the mean length turn of windings.

With (22) and (23), the core loss and winding loss can be calculated. By sweeping the switching frequency and number of turns within the allowable filling factor, the minimal ICT loss can be found, as shown in Fig. 8. Fig. 8 shows the ICT power loss will decrease when switching frequency increases. Fig. 9 presents the power loss of ICT designed with different core sizes. It should be noted that: increasing the size of core doesn't always result in reducing power loss. For example, when increasing core mass from 567 g to 680 g, the total power loss nearly unchanged.

FIGURE 10. The photo of an ICT hardware for the 100-kW PV inverter application.

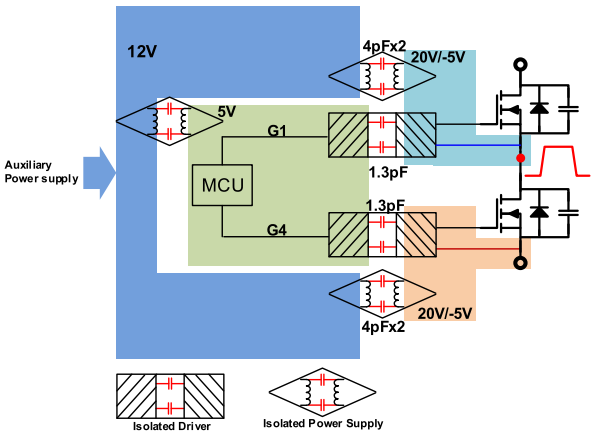

FIGURE 11. Gate driver power and signal path structure.

The photo of the designed ICT hardware is shown in Fig. 10. The measured weight of an ICT is 822 g. The three ICTs amount to 13% of the total weight of the 100-kW prototype, and consumed 8% of total power loss (refer to Fig. 24).

IV. INTER-PHASE CROSSTALK MITIGATION

It is desirable to switch the SiC modules fast to reduce the switching loss. However, a high dv/dt and high di/dt from fast switching can result in crosstalk issues. The crosstalk issues usually happen between the upper and lower switch, or between the switches and the control circuit, which then causes shoot-through and triggers circuit protection. In this research, the conventional crosstalk issues were prevented during the double pulse testing (DPT) and multi-pulse testing (MPT). With the gate driver circuit design shown in Fig. 11, one phase leg of the inverter can be switched at the speed of 17V/ns at rated power condition without causing any crosstalk issue [36]. However, a different crosstalk issue has been observed to happen between phase legs, as shown in Fig. 12.

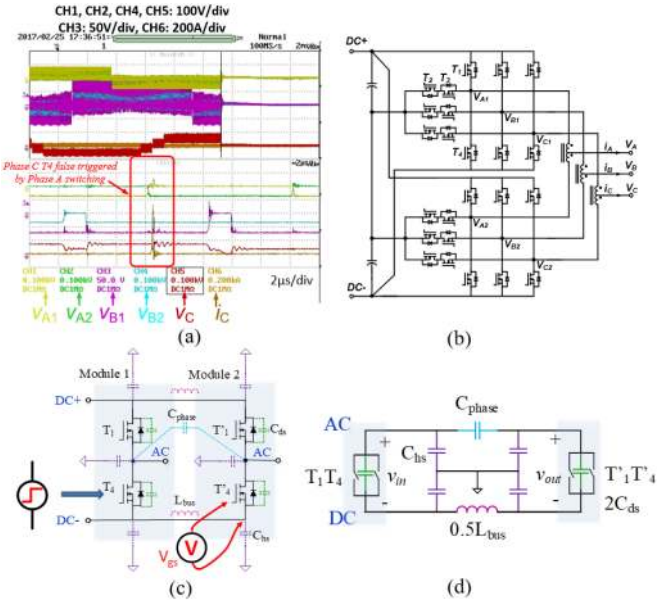

FIGURE 12. The inter-phase crosstalk phenomenon. (a) Experimental waveforms with original PCB design. Failed at 150V input. (b) Schematic. (c) The circuit schematic of two phase legs with parasitic parameters. (d) Equivalent circuit model.

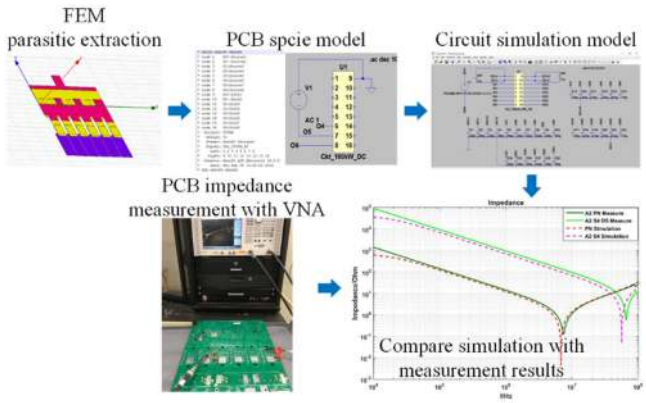

FIGURE 13. Method to extract and verify the PCB parasitic.

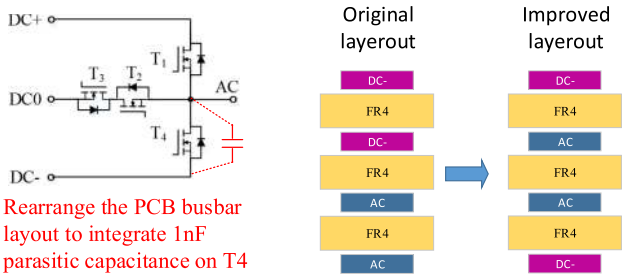

FIGURE 14. Rearrange PCB layout to solve inter-phase crosstalk issue.

Fig. 12(a) is the experiment waveform demonstrating this inter-phase crosstalk issue. When the dc-link voltage increased to 150 Vdc, this crosstalk issue caused shoot-through of a phase leg, and de-sat protection was triggered. In Fig. 12(a), CH1 and CH2 are output voltage waveforms of the two interleaved phase legs from phase A, namely v_{A1} and v_{A2}, respectively. CH3 and CH4 are the phase B voltage waveforms v_{B1} and v_{B2}. CH5 is the 5L voltage of the combined phase C1 and C2 legs (after ICT). CH6 is the current of T4 switch in phase C1. Fig. 12(a) shows that the overcurrent event of phase C1 happened when phase A legs were switching but phase C legs were not switching. Thereby the shoot-through in phase C had time correlation with the switching event from phase A. To rule out other propagation paths, the gate drivers' power supplies of different phase legs were changed to individual batteries that were isolated from each other. In addition, the gating signals were optical isolated. Therefore, the remaining propagation path was through the main power circuit. By cutting the PCB traces to isolate different propagation paths one by one, the signal propagation path was found to be through the ac terminal parasitic capacitance. Fig. 12(b) is the circuit schematic of two phase legs with parasitic parameters showing the propagation path.

To analyze this interphase crosstalk phenomenon, the parasitic parameters of the original PCB board is extracted and an LTspice model is built accordingly. The impedance of the PCB circuit model is simulated and compared with the vector network analyzer (VNA) measurement results to verify the accuracy of extraction. This modeling procedure is shown in Fig. 13. The top three pictures in Fig. 13 show the modeling procedure. The PCB busbar is modeled as a multi-port passive circuit. The impedances of the ports are simulated and then compared with impedance measured by VNA. It can be found from the PCB model that to reduce this interphase crosstalk requires to suppress the transfer gain from one phase leg to another. Although there are multiple solutions to achieve this goal, we choose to re-arrange the PCB layers. In this way, the dimension of PCB will not change, and the locations of the main power components will not change. Fig. 14 shows the improved PCB layout to increase the parasitic capacitance on T4, in turn to reduce the transfer gain from another phase leg. The improved PCB design is shown in Fig. 15. Fig. 15(a) is the simulated gate voltage waveforms using the LTspice model of original PCB and improved PCB. Fig. 15(b) is the experiment waveforms showing the inverter can operate at 830 V dc-link continuously with improved PCB design.

V. PROTOTYPE AND EXPERIMENT RESULTS

The laboratory prototype of the 100-kW PV string inverter is shown in Fig. 16, with key parameters listed in Table 2. The power density of this prototype is 2.8 kW/L (45.4 W/in3) and 5.07 kW/kg. The prototype is tested with a 150-kW DC power supply, a 105-kW resistive load bank for stand-alone operation. In grid-tied operation, the inverter is connected to a 480 V/4.16 kV 1.5 MW distribution transformer, through

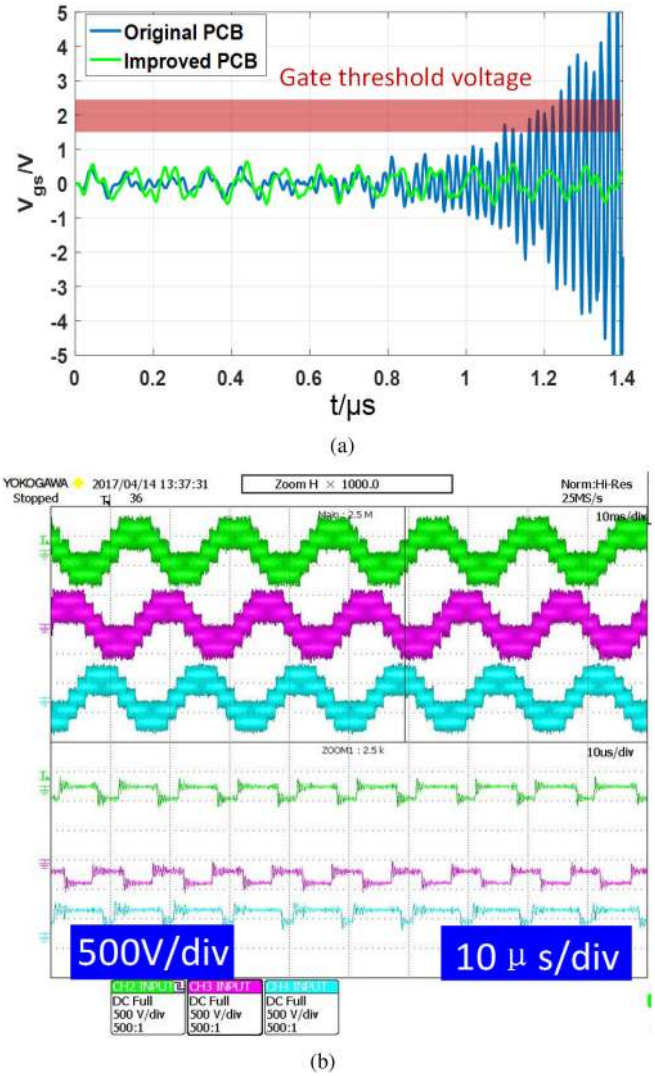

FIGURE 15. Results of improved PCB design. (a) Spice model simulation of gate voltage using extracted PCB parameters. (b) Experimental waveforms of the inverter output voltage at 830 V dc-link voltage.

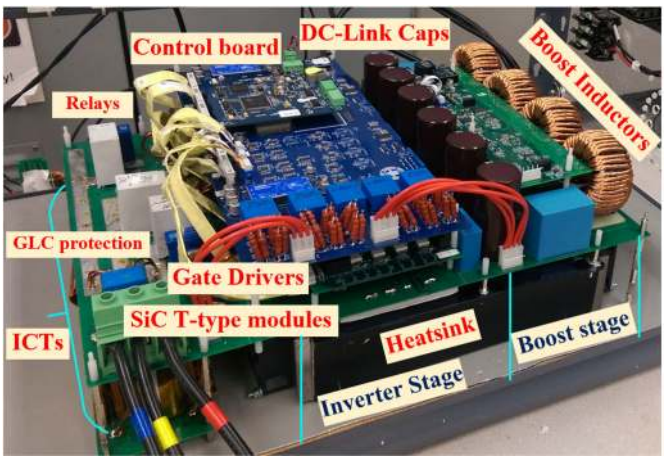

FIGURE 16. The 100-kW 2-stage SiC filter-less PV string inverter prototype.

TABLE 2. 100-kW SiC PV Inverter Specifications

Parameters	Values
Nominal output power	P_o = 100 kW
DC-link voltage	$2V_{dc}$ = 720 V ~ 850 V
Output voltage (line-to-line)	v_g = 480 V rms
Output frequency	f_o = 60 Hz
Boost switching frequency	f_{Boost} = 75 kHz
Inverter switching frequency	f_{Inv} = 50 kHz
Boost inductance	L_{Boost} = 400 μH
ICT magnetizing inductance	L_{ICT} = 9 mH
ICT leakage inductance	L_{DM} = 10 μH
CM inductance	L_{CM} = 240 μH
DC-link capacitance	C_{dc} = 2.1 mF
Cooling	forced air cool
Dimension	18.5" x 17" x 7"
Weight	19.7 kg
Specific power (two-stage)	5.07 kW/kg, 2.3 kW/lb
Power density (two-stage)	2.8 kW/L, 45.4 W/in^3
Boost inductor weight	815g x 4
ICT weight	822g x 3
CM chock weight	229g

about 35 meters of AWG 0 cable. The measured total inductance, including the transformer leakage inductance and the cable inductance, is 120 μH in each phase. The key waveforms of the stand-alone test are shown in Fig. 17, which includes the half dc-link voltage, output line-to-line voltage, output line to neutral voltage, and output current. The stand-alone experiment is performed with the 105-kW resistor load bank directly connected to the three-phase output of the inverter, without any filter in between. The measured dc-link voltage ripple is 53.5 V. It should be noted that the line-to-line voltage is also used in the grid-tied control for grid synchronization and feedforward control. Since there is a significant amount of carrier frequency harmonics, a second-order analog filter is used in the signal conditioning circuit. It can be observed from Fig. 17(b) that the peak-to-peak value of output current ripple is 43 A, which is 25% of the rated output current. The current ripple of grid-tied experiments, shown in Fig. 18, is much smaller than that of the stand-alone mode since there is grid impedance in the distribution transformer and connection cable. In the grid-connected mode, the measured current THD is 2.41% at 85% load ratio, with the grid voltage THD being 3.53%.

The ground leakage current experimental results are obtained in grid-tied mode and presented in Fig. 20. The grid is neutral grounded, and two of 12 μF capacitors are connected to the dc positive and negative inputs to emulate the parasitic capacitance from PV panels. With the CM chock design shown in Fig. 19, the measured ground leakage current is 205 mA at full load current.

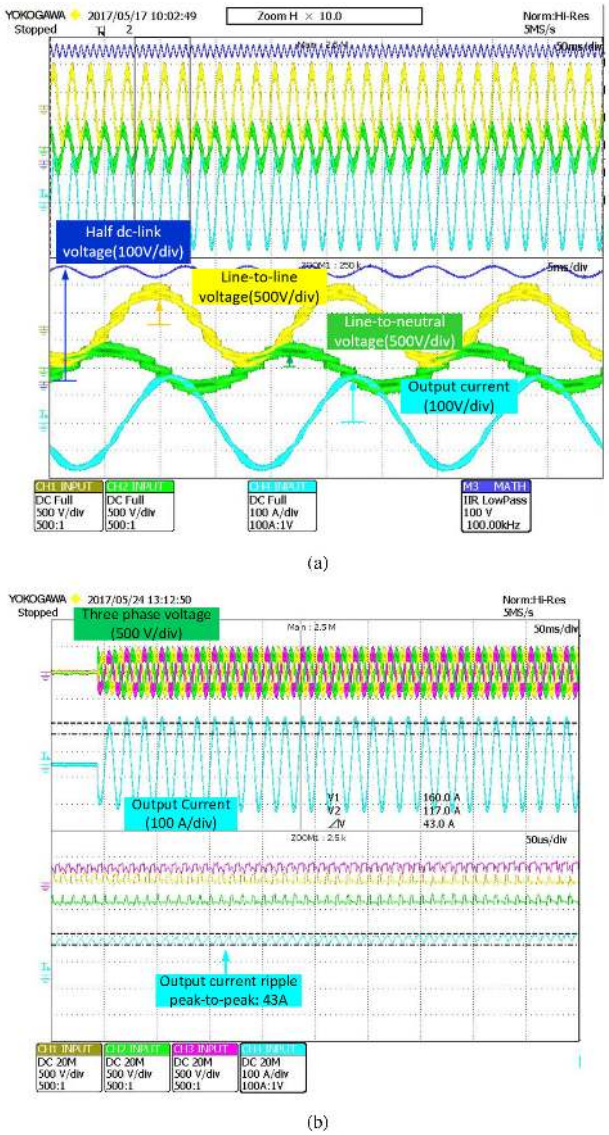

FIGURE 17. Stand-alone experimental waveforms. (a) Half dc-link voltage, output line-to-line voltage, output line-to-neutral voltage, and output current. (b) Three-phase line-to-neutral voltage and output current ripple.

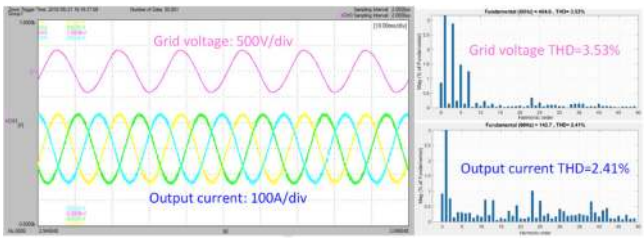

FIGURE 18. Grid-connected experimental waveforms.

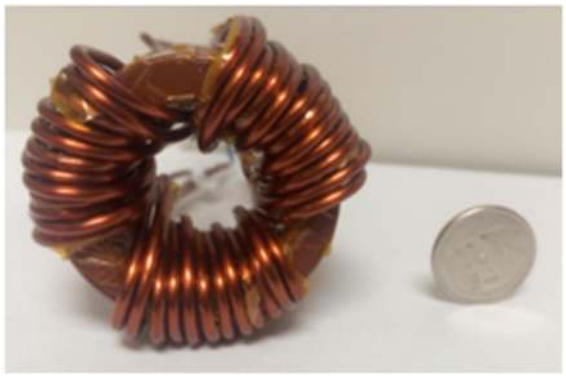

FIGURE 19. CM choke for ground leakage current suppression. 240 μH @100 kHz, 229 g.

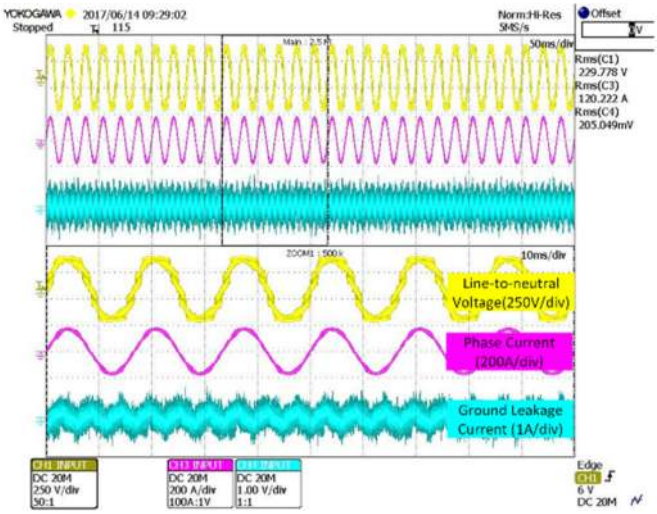

FIGURE 20. Ground leakage current experimental results. PV panel ground capacitance: 12 μF each; CM choke: 240 μH; Ground leakage current: 205 mA.

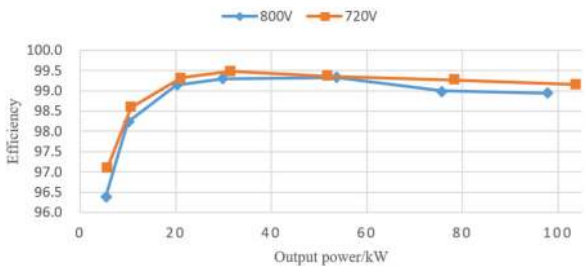

FIGURE 21. Measured efficiency of the 100-kW 5LT^2 inverter.

The measured efficiency curves are presented in Fig. 21. The measurements are performed with WT3000 precision power analyzer and LEM IT 200-S high accuracy current transducer with an accuracy of 0.0001% at 100 Hz, 0.0002% at 1 kHz. A thermal image of the converter running at full load is presented in Fig. 22. The hottest area is where the power module attached to the heatsink, with a temperature reading of 62 degrees Celsius. The weight breakdown and power loss breakdown is illustrated in Fig. 23.

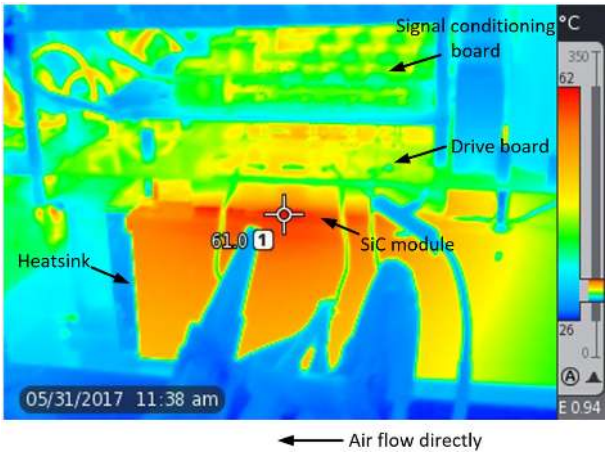

FIGURE 22. Prototype thermal image under 100-kW continuous operation.

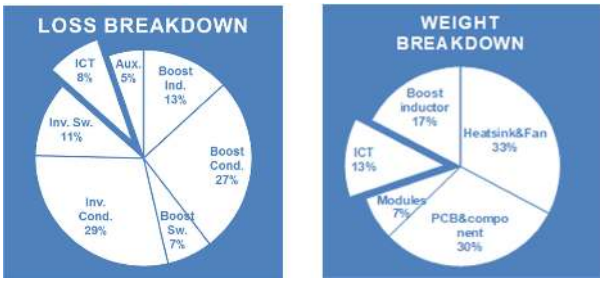

FIGURE 23. Loss breakdown and weight breakdown.

VI. CONCLUSION

This paper has proposed a lightweight high-efficiency design for a three-phase high power string PV inverter adopting SiC MOSFETs. This design is free of the conventional LCL-type power filter. This design is suitable for high power high-frequency inverter applications as the size of passive components will be much smaller than the conventional design. The experimental verifications have been demonstrated on a 100-kW filter-less PV inverter prototype. This 2-stage prototype is built with 1200 V SiC boost and T-type modules from Wolfspeed. The measured weight of this two-stage prototype is less than 20 kg, which includes the weight of the power circuit, switching devices, passive components, sensors, relays, the cooling system, wireless communication, and auxiliary power supply. Therefore the specific power of 10 kW/kg is achieved for inverter stage only and 5 kW/kg achieved for a 100-kW 2-stage PV string inverter. Experimental results have shown a 2.41% current THD measured in a grid with 3.53% voltage THD. The ground leakage current is 205 mA. The measured CEC efficiency under 720 V input voltage is 99.2%, and the peak efficiency is 99.5%.

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