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Interface properties in metal-oxide-semiconductor structures on *n*-type 4H-SiC(03$\bar{3}$8)

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The interface properties of SiO_2/4H-SiC(03$\bar{3}$8) were characterized using *n*-type metal-oxide-semiconductor structures fabricated by wet oxidation. The interface states near the conduction band edge are discussed based on the capacitance and conductance measurements at a low temperature and room temperature. 4H-SiC(03$\bar{3}$8) was found to have different energy distribution of the interface state density from the (0001) face. The shallow interface state density on (03$\bar{3}$8) is lower than on (0001) by a factor of 4 to 8. © *2002 American Institute of Physics.*
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Interface properties are the most important issues to determine the performance of metal-oxide-semiconductor (MOS) devices. As is the case with silicon (Si), silicon carbide (SiC) can be thermally oxidized to form silicon dioxide (SiO_2). In addition to that, SiC has excellent physical properties, such as wide band gap and high breakdown field suitable for high-power and high-temperature devices. Combined with the above features, SiC MOS transistors are expected to have high switching speed and low energy loss at room temperature and even under high-temperature operation. However, poor interface properties of SiC MOS structures, especially in 4H-SiC, processed by standard thermal oxidation hinder the realization of high-performance SiC MOS transistors.

It is well known that the interface properties of MOS structures in Si strongly depend on the surface orientations, that is, Si(100) has the smallest interface state density and Si(111) has the largest one, and the situation of Si(110) sits between the above two faces.[1] This is originated from the interface states of P_b-type dangling bonds. As for SiC, we have experimentally demonstrated that the interface properties of MOS structures also strongly depend on the surface orientations as follows: higher performance of MOS transistors and lower density of shallow interface states were obtained on 4H-SiC(11$\bar{2}$0) compared to those on (0001).[2–5] The (0001) and (11$\bar{2}$0) faces of hexagonal crystal structure correspond to the (111) and (110) faces of cubic structure, respectively. The origin of interface states in SiC MOS structures has not been clarified yet. For example, carbon clusters and near-interface oxide traps are suggested as origins for interface states.[6] The formation of these defects may be different on different surfaces, because Si and C atom arrangements on the surface affect the oxidation kinetics as the oxidation rate depends on the surface orientations.[7]

There may exist surface orientations other than the above two faces in 4H-SiC that can improve MOS transistor performance and MOS interface properties further. Although the origin of interface states is different, we have selected a new surface orientation, 4H-SiC(03$\bar{3}$8),[8] according to the Si analogy. The 4H-SiC(03$\bar{3}$8) is semi-equivalent to 3C(cubic)-SiC(100), tilted by 54.7° toward $\langle 01\bar{1}0 \rangle$ from (0001), as illustrated in Fig. 1. In this letter, the interface properties of MOS structures on 4H-SiC(03$\bar{3}$8) were characterized, based on capacitance and conductance measurements, focusing on the interface states near the conduction band edge.

The starting materials were *n*-type 4H-SiC substrates with surface orientations of (03$\bar{3}$8) and (0001). 4H-SiC(03$\bar{3}$8) substrates were prepared by slicing ingots grown on (000$\bar{1}$) by a modified Lely method at SiXON Ltd. with an angle of 54.7° toward the $\langle 01\bar{1}0 \rangle$ direction. *N*-type epitaxial layers were grown by standard atmospheric-pressure cold-wall chemical vapor deposition (CVD) at 1520 °C using SiH_4 and C_3H_8 as source gases and H_2 as a carrier gas. The net donor concentrations of epilayers were 3.2×10^{17} and 8.7×10^{16} cm^{-3} for the (03$\bar{3}$8) and (0001) faces, respectively. The specular surface was successfully obtained by CVD growth on (03$\bar{3}$8) as well as on (0001). The

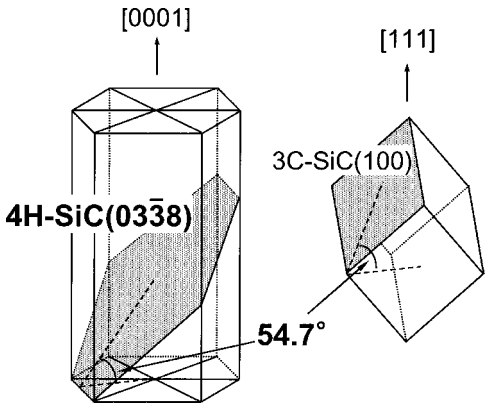

FIG. 1. Schematic illustrations of surface orientations for 4H-SiC(03$\bar{3}$8) and 3C-SiC(100).

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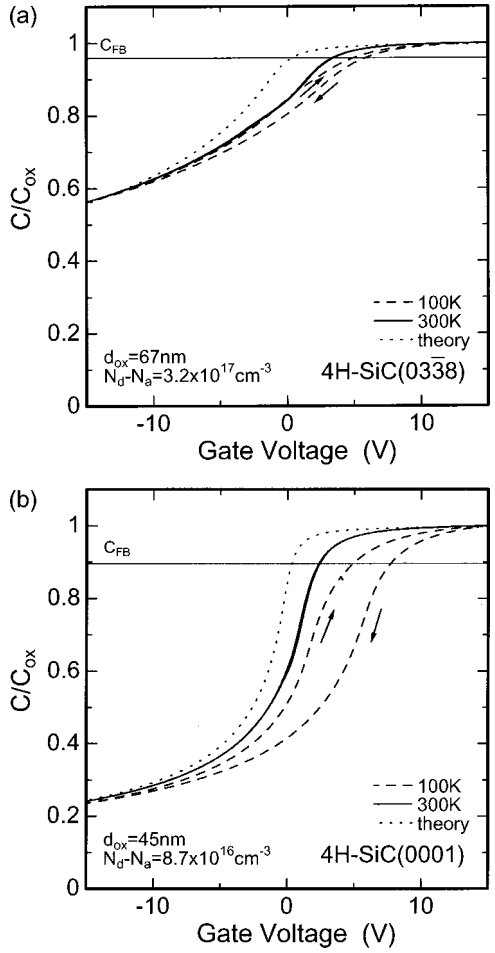

FIG. 2. High-frequency $C-V$ characteristics of n-type 4H-SiC MOS capacitors on (a) $(03\bar{3}8)$ and (b) (0001) faces. Solid and broken curves were taken at 300 and 100 K, respectively. Dotted curves indicate theoretical calculations. Injection-type hysteresis is observed.

samples were cleaned by an RCA method, and then loaded immediately into the oxidation furnace. Wet oxidation was performed at 1150 °C to grow a thermal oxide. The oxidation time/thickness were 25 min/67 nm for $(03\bar{3}8)$ and 120 min/45 nm for (0001), which revealed that the oxidation rate for $(03\bar{3}8)$ was 6–7 times faster than for (0001). After thermal oxidation, *in situ* post-oxidation annealing was carried out at 1150 °C for 30 min in Ar. Al was deposited on the surface as a gate electrode with a diameter of 300 μm and also on the back side for an ohmic contact. Finally, post-metallization annealing was done in a forming gas (10% H_2 in N_2) at 400 °C for 30 min.

To characterize the interface properties, high-frequency (1 MHz) $C-V$ characteristics were measured at room temperature (300 K) and at a low temperature (100 K) with a bias sweep rate of 0.1 V/s. The interface state density was calculated from the peak value of the parallel conductance measured in the frequency range of 1 kHz to 1 MHz at room temperature.[9,10] Both the capacitance and conductance measurements were done using an HP4284A precision LCR meter in an electrically shielded dark box.

Figures 2(a) and 2(b) show high-frequency $C-V$ characteristics of 4H-SiC MOS capacitors on $(03\bar{3}8)$ and (0001), respectively, measured at 300 K and 100 K. Note that the different slopes of the $C-V$ curves are due to the difference of the net donor concentration and the oxide thickness for the two samples. At 300 K (solid curves in Fig. 2), a small hysteresis (<0.1 V) was observed for both samples. The flatband voltage shift is 3.1 V for the $(03\bar{3}8)$ face and 2.0 V for the (0001) face. Although the flatband voltage shift on $(03\bar{3}8)$ looks larger than on (0001), the effective oxide charge density calculated from the multiplication of the flatband voltage shift and the oxide capacitance (51.2 nF/cm^2 for $(03\bar{3}8)$ and 76.2 nF/cm^2 for (0001)) results in the same number of charges (1.0×10^{12} cm^{-2}, negative charges) for both faces. These negative charges originated from both fixed charges and electrons trapped at interface states.

At a low temperature of 100 K (broken curves in Fig. 2), both the flatband voltage shift and hysteresis increased due to the existence of shallow interface states.[5,11,12] Relatively shallow interface states affect the flatband voltage shift, because electrons trapped at the interface states stay, and behave like fixed negative charges. As for quite shallow states, they become the origin of the injection-type hysteresis due to slow emission of electrons from the interface states during the voltage sweep. Neither shallow state has much effect on the $C-V$ curves at room temperature. The flatband voltage shift at 100 K is 4.4 V for $(03\bar{3}8)$ and 7.0 V for (0001), leading to the effective negative charge density (Q_{eff}) of 1.4×10^{12} and 3.3×10^{12} cm^{-2}, respectively. The increased ratio of the effective negative charge density from 300 to 100 K [Q_{eff}(100 K)/Q_{eff}(300 K)] is 1.4 for $(03\bar{3}8)$ and 3.3 for (0001). This indicates that the interface state density on $(03\bar{3}8)$ at relatively shallow energies is smaller than on (0001).

Compared with the change of the flatband voltage shift, the larger difference in the increase of hysteresis is observed for different surface orientations. Although the hysteresis under flatband condition at 300 K is very small for both faces, it increases to 0.9 V for $(03\bar{3}8)$ and 2.9 V for (0001). The increase of hysteresis corresponds to the emitted electron density (Q_{hys}) of 3.1×10^{11} cm^{-2} for $(03\bar{3}8)$ and 1.4×10^{12} cm^{-2} for (0001). In comparison with the value at room temperature [$Q_{\mathrm{hys}}(300\ \mathrm{K})\sim3\times10^{10}$ cm^{-2}], the increased ratio [Q_{hys}(100 K)/Q_{hys}(300 K)] is 9.6 for $(03\bar{3}8)$ and 41 for (0001). This means that the interface state density on (0001) increases toward the conduction band edge drastically, but that on $(03\bar{3}8)$ does not. From the increase of the flatband voltage shift and hysteresis at the measurement temperatures from 300 to 100 K, SiO_2/4H-SiC$(03\bar{3}8)$ is found to have smaller interface state density than (0001) near the conduction band edge.

The distribution of interface state density (D_{it}) as a function of energy from the conduction band edge (E_C) is shown in Fig. 3 for both $(03\bar{3}8)$ and (0001) faces. At deep energies of $E_C-E>0.4$ eV, D_{it} on $(03\bar{3}8)$ tends to be larger than on (0001). However, the slope of the distribution of D_{it} on $(03\bar{3}8)$ is not as steep as that on (0001). Therefore, the $(03\bar{3}8)$ sample has lower D_{it} than the (0001) sample at shallow energies of $E_C-E<0.3$ eV, which verifies the previous argument based on the temperature dependence of the $C-V$ curves shown in Fig. 2. Between the energy range of $E_C-E=0.1-0.2$ eV, D_{it} on $(03\bar{3}8)$ is smaller than on (0001) by a factor of 4 to 8. The data on $(11\bar{2}0)$[13] are also indicated in Fig. 3 for comparison. The $(03\bar{3}8)$ sample gives a half

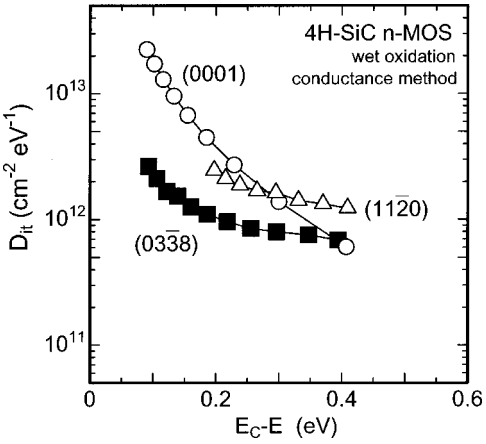

FIG. 3. Distribution of interface state density (D_{it}) evaluated from conductance method.

value of D_{it} on $(11\bar{2}0)$ in the whole energy range monitored in this experiment. The different D_{it} profiles in Fig. 3 for various surface orientations suggest that origins of interface states (for example, carbon clusters, near-interface oxide traps, dangling bonds, and so on) and their numbers are different for these faces. More detailed investigation is needed to clarify the origin of interface states of SiC MOS structures.

Obtaining small D_{it} values near the conduction band edge is important for SiC MOS structures, because the performance of SiC MOS transistor is mainly limited by the interface states at shallow energies.[14] As a matter of fact, we have fabricated 4H-SiC MOS transistors on $(03\bar{3}8)$, $(11\bar{2}0)$, and (0001) faces using the same oxidation process (wet oxidation at 1150 °C) as described in this letter, and obtained higher effective channel mobility on $(03\bar{3}8)(\sim 11\ cm^2/Vs)$ than on $(11\bar{2}0)(\sim 6\ cm^2/Vs)$ and $(0001)(\sim 4\ cm^2/Vs)$.[15] The channel mobilities obtained here on $(03\bar{3}8)$ and $(11\bar{2}0)$ are not so high compared to our previously reported value $(\sim 30\ cm^2/Vs)$ on $(11\bar{2}0)$,[2–4] probably due to immature fabrication processes. We believe that much higher channel mobility could be obtained on $(03\bar{3}8)$ by improving the fabrication process of MOS transistors as well as optimizing the oxidation conditions.

In summary, the interface properties of *n*-type MOS structures with wet oxides on 4H-SiC$(03\bar{3}8)$ were characterized. High-frequency $C-V$ characteristics measured at a low temperature indicated a large flatband voltage shift and hysteresis on (0001), while those on $(03\bar{3}8)$ were small. This implies that MOS structures on $(03\bar{3}8)$ have smaller interface states at shallow energies than on (0001), which was verified by the measurement of interface state density using the conductance method at room temperature. The interface state density on $(03\bar{3}8)$ at shallow energies was 4 to 8 times smaller than on (0001), leading to higher channel mobility on 4H-SiC$(03\bar{3}8)$. Therefore, the $(03\bar{3}8)$ face of 4H-SiC is a promising surface orientation for realizing high-performance MOS devices on 4H-SiC.

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