Interfacial properties of ultrathin pure silicon nitride formed by remote plasma enhanced chemical vapor deposition

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This article addresses the electrical properties of interfaces between *n*- and *p*-type Si and remote plasma-deposited Si_3N_4, which are of interest in aggressively scaled advanced CMOSFETs. The nitride films of this article display excellent electrical properties when implemented into stacked oxide/nitride dielectrics in both NMOSFETs and PMOSFETs with oxide, or nitrided oxide interfaces. The same nitride layers deposited directly onto clean Si surfaces display degraded electrical properties with respect to devices with oxide, or nitrided oxide interfaces. PMOS interfaces are significantly more degraded than *n*-type metal–oxide semiconductors interfaces indicating a relatively high density of donor-like interface traps that inhibit channel formation. [S0734-211X(99)04904-5]

I. INTRODUCTION

Gate dielectric scaling requires new materials with dielectric constants (K) higher than SiO_2 to provide the increased capacitance without compromising gate leakage current.[1,2] One such material is Si_3N_4 that has approximately twice the dielectric constant of SiO_2, and additionally is effective in blocking diffusion of dopants such as boron. Si_3N_4 has also been proposed as an interface layer for high K transition metals oxides since it has a higher K than SiO_2 and is also an excellent diffusion barrier. To date, the interfacial and bulk properties of Si_3N_4 have not been encouraging, and only a few processes have shown promising results.[3–5] One such process is jet vapor deposition (JVD) in which the current transport mechanism in the dielectric films is predominantly electron tunneling similar to what has been observed in SiO_2.[4] However these films contain a relatively high concentration of O ($\sim$20 at %) which reduces the dielectric constant, and additionally, the devices have $Si–SiO_2$ interfaces. Recent studies at NCSU have shown that nitride films formed by RPECVD, and subjected to a postdeposition anneal in an inert ambient at 900 °C produce good quality films with relatively low concentrations of both O ($<$2 at %) and H ($<$14%).[3,6] When used in SiO_2/Si_3N_4 stacks (O/N), in which a thin oxide layer separates the nitride film from the substrate, these films display excellent electrical properties in both NMOS[7] and PMOS devices.[4] The goal of this work is to extend the study of the RPECVD nitride as the gate dielectric, and in particular to determine the electrical properties of $Si–Si_3N_4$ interfaces in both NMOS and PMOS devices.

II. EXPERIMENTAL PROCEDURES

Silicon nitride films were formed in a cluster tool in which the entire gate stack is completed before exposure to atmosphere. Prior to gate stack formation, a 200 nm field oxide was grown on 100 mm substrates followed by patterning of the active areas. A 10 nm sacrificial oxide was then grown and removed with 2% HF solution immediately before insertion into the cluster tool. Nitride layers were formed by RPECVD at 400 W, 300 mTorr and 300 °C using $SiH_4+NH_3(N_2)$.[3,7,8] Single layer nitrides varying in thickness from 1.5 to 3.0 nm were formed on both *n*- and *p*-type substrates. In addition to forming single layer nitride films, nitride/oxide stacks were also formed to study the properties of ultrathin nitride at the interface while using conventional characterization techniques. After deposition, films were annealed at 900 °C in vacuum to reduce the hydrogen content and promote formation of additional Si–N bond.[3,6] Gate dielectrics were then capped by rapid thermally deposited polysilicon in the cluster tool system. Control oxides of varying thickness were also prepared by thermal oxidation. Surface channel NMOS and PMOS devices were formed by conventional techniques, and a forming gas (10%H_2 in N_2) anneal at 400 °C was performed after metallization.

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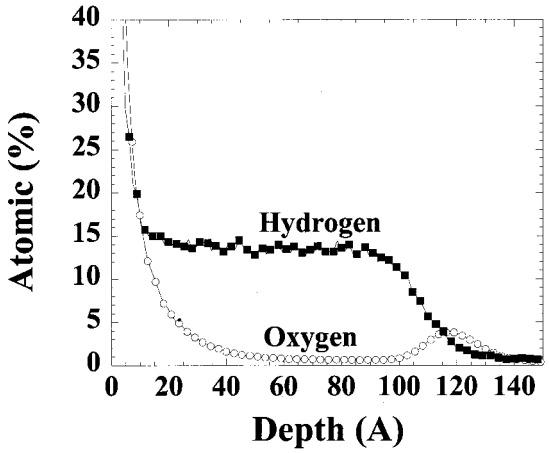

FIG. 1. Secondary ion mass spectroscopy depth profile of RPECVD nitride.

III. RESULTS

Secondary ion mass spectroscopy analysis of RPECVD nitride films is shown in Fig. 1. The hydrogen content is less than 15% throughout the film. The oxygen concentration is also very low (<3%) with a slight increase at the interface. The low hydrogen and oxygen content makes this film very different from the nitrides deposited via LPCVD techniques and is expected to exhibit different electrical characteristics. The slight increase of oxygen at the interface may be related to surface contamination from being exposed to the cleanroom before being loaded in the RPECVD chamber. In order to determine the dielectric constant, the physical thickness was measured by transmission electron microscopy and compared to the electrical oxide equivalent thickness. This gave a dielectric constant of 7.3.

I_{ds} vs V_g measurements were taken on NMOS and PMOS devices. The thickness were extracted from capacitance–voltage data using a least-square fit method.[9] The equivalent oxide thicknesses of the nitride and control oxide were 2.1 and 2.3 nm, respectively. As shown in Fig. 2(a), the data for NMOSFETs with nitride dielectrics had a lower V_t compared to the control devices agreeing with what has been observed for nitrided oxides; this is attributed to the fixed positive charge.[10–12] The nitride devices also displayed an ~50% degraded peak mobility, but an enhanced high-field mobility. The behavior of reduced peak degradation and enhanced high field mobility are consistent what has been observed in heavily nitrided oxides.[10,12] The PMOS data with nitride dielectric, shown in Fig. 2(b), display markedly different characteristics compared to NMOS devices. The channel conduction is significantly reduced, and there is a very large V_t shift, ~1.5 V. The degraded I_{ds} and large V_t shift make these PMOS devices effectively nonfunctional. To better understand the cause of the degraded PMOS behavior, capacitance–voltage (C–V) measurements were performed on transistors to obtain both accumulation and inversion characteristics.

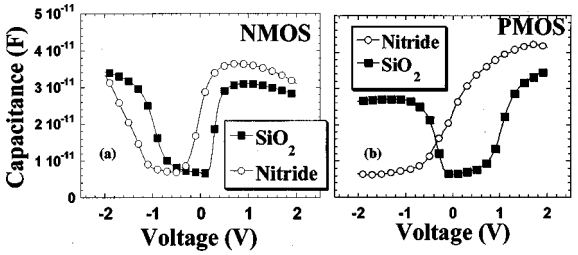

FIG. 3. Capacitance–voltage on $50\times50\ \mu m^2$ (a) NMOSFETs and (b) PMOSFETs taken at 1 MHz. The equivalent oxide thickness for nitride and SiO_2 are 2.1 and 2.3 nm, respectively.

As shown in Fig. 3(b), the C–V measurements on PMOSFET devices did not indicate the presence of an inversion layer which is consistent with the severely degraded drive currents obtained from the IDVG measurements. However, normal characteristics were observed in accumulation suggesting that only holes in the channel were being affected. To see if this behavior was independent of the substrate conductivity, C–V measurements were also made on NMOSFETs. As shown in Fig. 3(a), the NMOS devices showed degraded characteristics near the accumulation region, whereas the inversion C–V curves were normal. Although the degradation in the NMOS devices was lower than in the PMOS, these results demonstrated that the nitride dielectric was affecting channel holes significantly more than channel electrons.

To determine the effect of the interface nitride thickness on the C–V characteristics, the nitride/oxide stacks were also measured on PMOSFETs. As shown in Fig. 4, a nitride thickness of >5 Å can drastically influence the inversion characteristics. This implies that the interfacial nitride dras-

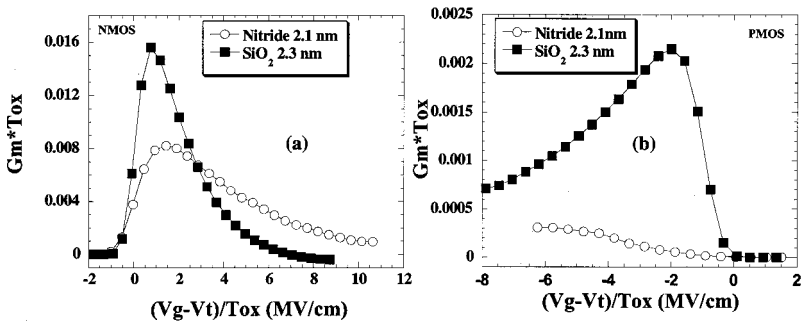

FIG. 2. $G_m{*}T_{ox}$ vs. oxide field for silicon nitride and SiO_2 for 0.6 μm channel length (a) NMOSFETs and (b) PMOSFETs. The oxide field was calculated as $(V_g - V_t)T_{ox}$.

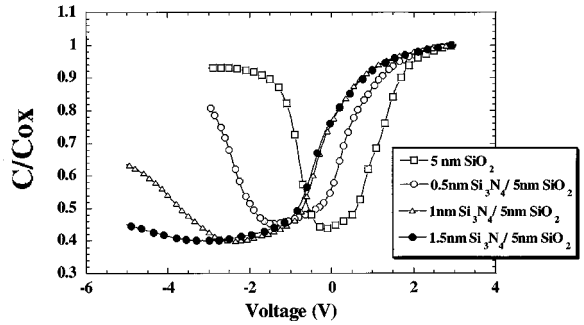

FIG. 4. Capacitance–voltage on 50×50 PMOSFET with varying nitride/oxide stack layers taken at 1 MHz.

tically modulates the hole carriers in the channel region.

Gate tunneling current was measured both in accumulation and inversion for both NMOS and PMOS devices (area=$10\times3\ \mu m^2$) and is shown in Figs. 5(a) and 5(b). The voltage drop across the oxide was obtained using V_g-V_t in inversion and V_g-V_{fb} in accumulation. The nitride shows slightly lower tunneling current than SiO_2 in the positive region for both NMOS [Fig. 5(a)] and PMOS [Fig. 5(b)] devices. However under negative bias conditions, the gate current through the nitride layers is excessive compared to SiO_2 even though the nitride layers are physically thicker.

In an effort to understand the mechanisms responsible for the degraded hole behavior, a carrier separation technique was used to separately measure the hole and electron currents.[13] A positive gate bias was applied to the NMOS devices, and a negative gate bias was applied to the PMOS, with the source, drain, and substrate grounded. The gate bias creates a channel and as carriers tunnel out of the channel into the gate dielectric they are replaced by carriers from the source/drain regions. Measurement of gate, channel, and substrate current provides a measure of the electron and hole current components. The results for SiO_2 for both PMOS and NMOS are shown in Figs. 6(a) and 6(b). For both transistors, the gate current is nearly equal to the channel current for all voltages implying that the majority of the carriers that tunnel to the gate come from the channel, i.e., electron current dominates in the NMOS and hole current dominates in the PMOS. The substrate current is a very small percentage

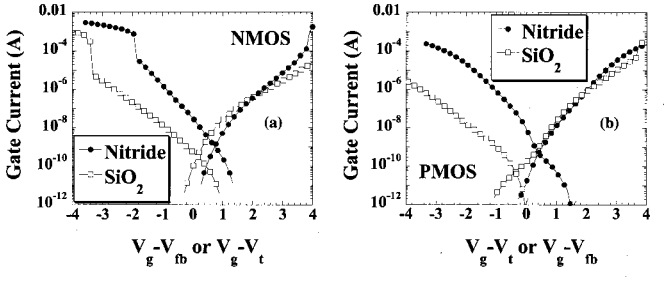

FIG. 5. Gate current measurements for (a) NMOSFET and (b) PMOSFET in inversion and accumulation. The equivalent oxide thickness for nitride and SiO_2 are 2.1 and 2.3 nm, respectively. The voltage across the oxide is taken as V_g-V_t in inversion and V_g-V_{fb} in accumulation.

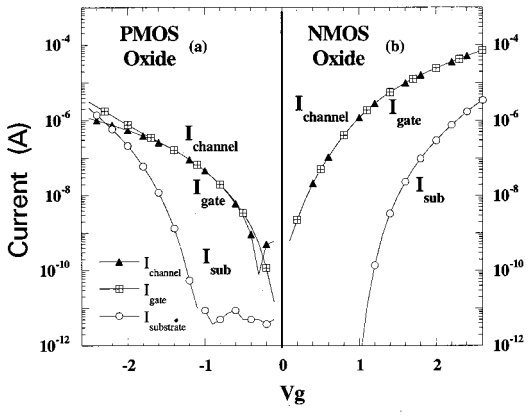

FIG. 6. Carrier separation measurements for silicon nitride on (a) PMOSFET and (b) NMOSFET devices.

of the gate current. The measurements for Si_3N_4 for PMOS and NMOS are shown in Figs. 7(a) and 7(b). The NMOS behavior is similar to the control oxide, i.e., the gate current is dominated by source/drain channel current suggesting that electron current is the dominating process in this regime. However, the PMOSFETs with nitride dielectric display markedly different behavior than their SiO_2 counterparts. First, at smaller gate biases the drain current is very low and is not equal to the gate current suggesting that the channel holes are not participating in the carrier conduction in this regime. Second, the substrate current is very high in this regime and equals the gate current. This implies that the electron conduction from the gate is the dominating process. It should also be noted that after V_g exceeds approximately -1.5 V the channel current starts increasing and becoming equal to the gate current.

IV. DISCUSSION

The proposed explanation for the above results is as follows. The nitride dielectric is believed to have a large density of interface traps below the midgap. These traps remain oc-

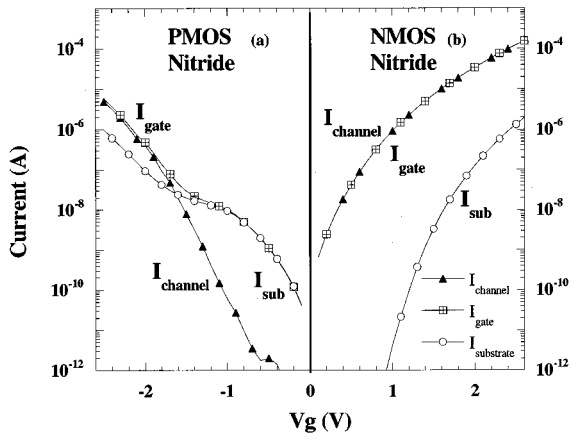

FIG. 7. Carrier separation measurements for silicon nitride on (a) PMOSFET and (b) NMOSFET devices.

cupied and neutral if the Fermi level lies above them as in the case of NMOS inversion. However, as the Fermi level starts moving down towards the Si valence band edge, as in PMOS inversion, these traps get depopulated and become positively charged. The high density of these positive traps in the nitride layers can screen the gate charge until all interface traps become depopulated. This is believed to occur at approximately -1.5 V, which is the same V_t value extracted from the I_d-V_g curves [see Fig. 2(b)]. After this voltage is reached, a surface potential is allowed to drop in the channel resulting in the onset of inversion. This is believed to be the mechanism responsible for the degraded PMOS characteristics in inversion.

As mentioned, the high density of traps below the midgap can effectively screen the gate charge preventing any voltage drop in the semiconductor. This screening process can also explain the high gate tunneling current observed with nitride dielectrics in the negative regime. A much higher electric field is created across the nitride where $V_{\text{nitride}}=V_{\text{applied}}$ as compared to the control oxide where $V_{\text{oxide}}=V_{\text{applied}}-V_{\text{substrate}}$. This higher field assists in large conduction current through the dielectric.

Recently, reports of bonding constraint theory calculations have indicated that the defect formation can be closely related to bonding coordination at the interface of two materials.[14,15] The average bonding coordination per atom of SiO_2–Si interface (including the suboxide region) is 2.9. This is sufficiently low and promotes the formation of low defect density interfaces. On the other hand, the average bonding coordination per atom at the Si_3N_4–Si interface (including the transition region) was calculated to be ~ 3.5 which can promote a high defect density. In this work it is believed that this overcoordination of the Si_3N_4–Si compared to the Si–SiO_2 interface may result in interface trap formation that negatively impacts the electrical properties. To further verify this, a thin layer of oxide (<0.6 nm as measured by *in situ* Auger) was interposed between the nitride and the Si substrate. Transconductance values, shown in Fig. 8, now indicate normal characteristics for *P* and *N* devices suggesting that ~ 0.6 nm of interfacial oxide is sufficient to reduce the interface state density both near the conduction and valence band edges. It should also be noted that the presence of oxygen may assist in reducing the trap density by reducing the average bonding coordination and systematic experiments are being performed to verify this.

V. CONCLUSIONS

Data presented in this article demonstrate that degradation of PMOS and NMOS devices with nitride gate dielectrics derive from interfacial defects. It is believed that a markedly different distribution of interfacial traps near the valence band versus the conduction band edges results in the inability to form a PMOS channel. The observation that these traps are not present in PMOS devices in which an ultrathin oxide layer <0.6 nm is interposed between the Si and the nitride film demonstrates that these defects are a property of the Si–Si_3N_4 interface. Therefore, a pure silicon nitride film cannot be used directly on the silicon surface due to a high density of positively charged, donor-like defects in the lower half of the band-gap near the valence band edge of Si which prevents the formation of a conducting channel. The addition of oxygen as an ultrathin interfacial oxide layer and/or in the bulk of nitride film to form an oxynitride alloy, may be necessary if nitride interface layers are to be integrated into aggressively scaled CMOS devices.

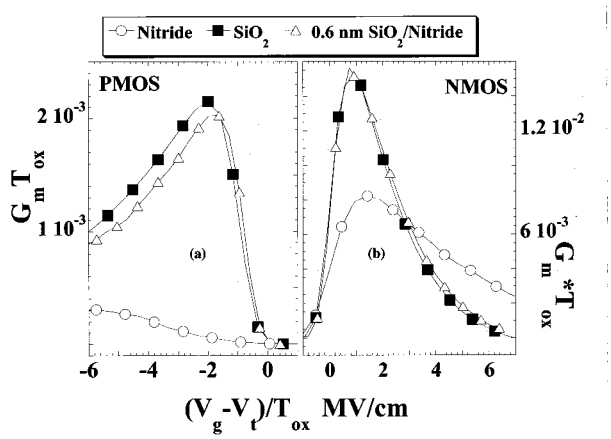

FIG. 8. $G_m{*}T_{ox}$ vs oxide field for silicon nitride, SiO_2 and stacked O/N dielectrics for 0.6 μm channel length (a) PMOSFETs and (b) NMOSFETs. The oxide field was calculated as $(V_g-V_t)/T_{ox}$.

ACKNOWLEDGMENTS

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