Interfacing to Time-Triggered Communication Systems

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Abstract

Time-triggered communication facilitates the construction of multi-component real-time systems whose components are in control of their temporal behavior. However, the interface of a time-triggered communication system has to be accessed with care, to avoid that the temporal independence of components gets lost. This paper shows two interfacing strategies, one for asynchonous interface access (in two variants, one being the new Rate-Bounded Non-Blocking Communication *protocol) and one for time-aware, synchronized interface access, that allow components to maintain temporal independence. The paper describes and compares the interfacing strategies.*

1 Introduction

In many safety- and time-critical applications (e.g., powerplants, medical devices, planes), an increasing number of functions are realized by embedded computer systems. As a consequence, embedded computer systems get more complex. They need more computational resources and are implemented as distributed systems, consisting of an ever-growing number of computer units. Given this growth, we have to ensure that the additional interactions of components do not create interferences that make the system behavior unpredictable, thus infringing the safety of applications.

A composable system design limits the interferences between the components of a distributed embedded system [4]. The components of a composable multi-component system are highly autonomous: the point of control that determines *which* actions a component performs and *when* these actions are triggered resides *within*, not outside the component. Component autonomy ensures that components and multi-component subsystems can be developed independently. Their functionality and timing can be verified and validated in isolation, thus cleanly separating the responsibilies of the suppliers of different subsystems.

Prior work has shown that time-triggered communication allows components of multi-component systems to autonomously control their timing behavior [2]. Reading from or writing to a time-triggered communication interface is similar to reading or writing program variables that are regularly updated. As opposed to event-triggered interfaces, where every received message has to be read and consumed in order to keep the receiving component in a consistent state (i.e., the receiver must read/process every message within a defined time after its arrival), time-triggered communication does not impose control pressure (or variable load) on components whose interface data get updated [3].

While the program-variable semantics of time-triggered interface data does not create an external control pressure on components from the side of the communication system, mutual-exclusion blocking, which must be enforced when the communication system and a component access the interface concurrently, might still lead to external control on the blocked subsystem. In this paper we explore two approaches to avoid external influences on control due to mutual-exclusion blocking when accessing the data-sharing interface of a time-triggered communication system. In the first approach, subsystems access the interface *asynchronously*, without coordination. The software for interface access prohibits external control on subsystems by masking access conflicts (Section 4.1). In the second approach, computing components that access the time-triggered communication interface are *time-aware*. They synchronize to the global time of the communication system and take advantage of the statically available information about the send and receive times of messages to avoid control conflicts when accessing the interface (Section 4.2). After introducing each of these approaches for interface access, Section 5 compares the two strategies in detail.

2 Time-Triggered Communication

A *time-triggered communication system (TTCS)* is an autonomous subsystem of a distributed real-time computer system that transports messages between the nodes of the computer system in a time-predictable way. Time-triggered messages are periodic. The TTCS transports the messages from a sender node to one or more receiver nodes according to a static message-transmission schedule that is constructed at design time. The clock synchronization service of the TTCS provides a global clock to the distributed system. Communication end points of the TTCS, the *linking-interface subsystems (LIFSS)* of the nodes, use this global clock to maintain a uniform view about the progress of time and coordinate their message send and receive operations according to the message schedule. Further, the computational components of the nodes can program the LIFSS to generate (periodic) clock interrupts. This allows computational components to synchronize their operation to the global clock.

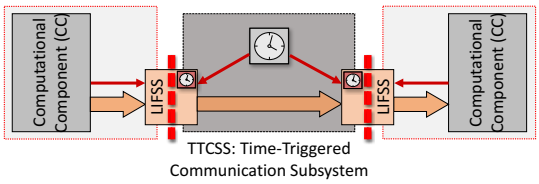

Figure 1. Time-Triggered System Model.

Figure 1 sketches the structure of a time-triggered distributed computer system. The nodes of the distributed system consist of the interacting, autonomous *computational components (CCs)* and the LIFSS. The LIFSS of all nodes taken together constitute the TTCS.

3 Autonomy of Components

In a general distributed computer system, components communicate by the exchange of messages. Besides the data flow, we have to establish appropriate *control flow* relations between communicating components when we aim at constructing systems that guarantee component autonomy. The control flow determines who initiates message transfers and is in command of the individual steps of the transfer. Let us consider the transfer of a message from a sending to a receiving component. If the sender is entirely in control of the message transfer, then the control flow originates at the sender and terminates at the receiver. We call this an *information-push* [2] operation. If the receiver is in control of transferring the message from a sender, then the control-flow direction is from the receiver to the sender, in opposite direction of the data flow. We call this an *information-pull* [2] operation.

Information-push operations are ideal for senders. For an information-push operation, the sender does not have to wait until the receiver is ready, neither does it need buffers for storing messages while waiting. Information-pull operations are ideal for receivers. Following the information-pull policy, receivers can process messages under their own control – message-pull receivers cannot be disturbed by messages that arrive at times that are not under their own control.

In a TTCS, there is no explicit control flow across the communication system. Due to the program-variable semantics of state messages, message arrival does not impose external control on CCs. So, CCs may, in principle, read ports of the LIFSS in information-pull operations and write to ports in informaion-push operations. The only potential control conflicts at a LIFSS can arise due to mutual-exclusion blocking when the LIFSS and a CC try to access a shared data item at the same time. We will show how these mutual-exclusion control conflicts can be resolved by taking advantage of the properties of time-triggered communication respectively by using LIFSS services.

4 Non-blocking Interfaces

In the following we will discuss the two alternative strategies of accessing the LIFSS without control disturbances due to mutual-exclusion blocking. CCs may adopt one of these strategies. The chosen strategy determines how and when CCs access the LIFSS ports and whether they use the clock interrupt service of their LIFSSs. Depending on application requirements, CCs may use the data-sharing interface of the LIFSS either as a

- time-agnostic, asynchronous interface, or as a
- time-aware, time-synchronized interface.

4.1 Time-Agnostic, Asynchronous Interface

Assuming that network communication is time-triggered, but the program activation on the computational component (CC) is event-controlled, a time-agnostic asynchronous communication protocol is required at the LIFSS. In this section we introduce the novel *Rate-bounded Non-Blocking Communication Protocol* (RNBC) as such a protocol.

RNBC allows the parallel write and read of shared data without the need for blocking or waiting, supporting one writer and multiple readers. To facilitate non-blocking, RNBC comes with a schedulability criterion

that bounds the rate of write accesses. Reading via RNBC always provides the latest completely written data. Any pending data write becomes only available for reading, once the write is completed.

RNBC has been inspired by the *Non-blocking Write Protocol* (NBW) [5]. To understand the benefit of RNBC, we first briefly describe NBW, as shown in Figure 2. The data to be communicated is stored in the buffer `buff`. In addition, the writer maintains the concurrency control flag `ccf`, to indicate the writing status. Whenever `ccf` is odd, a writing is in progress, and when `ccf` becomes even again, the writing has completed. Thus, the reader performs a busy waiting during reading to make sure that `ccf` was even and did not change during the whole read operation.

```
1  int buff; // shared msg buffer
2  int ccf = 0;  // 0 means empty buffer
3
4  void nbw_write_msg(int msg) {
5    ccf++;  // becomes odd: write in progress
6    buff = msg;
7    ccf++;  // becomes even: write completed
8  }
9
10 int nbw_read_msg() {
11   int msg;
12   int ccf1,ccf2=0;
13   do {
14     ccf1 = ccf;
15     if (odd(ccf1)) continue;
16     msg = buff;
17     ccf2 = ccf;
18   } while (ccf1 != ccf2);
19   return msg;
20 }
```

Figure 2. NBW: Classical Non-Blocking Write Protocol

While NBW is simple to understand, part of its nature is that it has a variable execution time, depending on whether the read operation overlaps with a write operation or not. To reduce the likelihood of such a read delay, the authors included in the original paper also an extended variant of NBW, which manages a ring buffer [5]. This way, a write operation started during a read does not necessarily cause a delayed reading. Only in case that multiple writes fill up the ring buffer during a pending read, then a delayed read will happen. It has to be noted that this Extended NBW can still suffer from occasional read delays, however, making them more rare. But at the same time the Extended NBW has a significantly higher code overhead than the standard NBW, making read/write clashes more likely. These given limitations of NBW and its extended ring-buffer variant motivated us to develop the Rate-bounded Non-Blocking Communication Protocol (RNBC), a new concurrent read-write protocol that is inspired by the field of lock-free communication data structures, for example, lock-free message queues [1, 6].

4.1.1 RNBC: A Rate-bounded Non-Blocking Communication Protocol

The design strategy for RNBC was, instead of aiming to minimise the likelihood of read/write clashes, to develop a precise schedulability criterion that guarantees absence of read/write clashes. This at the same time allowed us to develop a protocol that has minimal code overhead.

The code of RNBC is shown in Figure 3. The key feature of RNBC is to have two communication buffers, one for the current write operation, and the other one for current read operations. Whenever a write finishes, the roles of these two buffers is swapped. The shared flag `wbuff` indicates which buffer index (0 or 1) is currently allocated for next writing. As we can see from the code, the implementation of both the reader and writer in RNBC became extremely simple, consisting basically just of the access/update of the buffer and the control flag.

```
1  int buff[2];       // shared msg buffer
2  int wbuff = 0;     // buffer index of write
3
4  void rnbc_write_msg(int msg) {
5    buff[wbuff] = msg;
6    wbuff = 1-wbuff; // swap read/write buffer
7  }
8
9  int rnbc_read_msg() {
10   int rbuff = 1-wbuff;
11   return buff[rbuff];
12 }
```

Figure 3. RNBC: Rate-bounded Non-Blocking Communication Protocol

4.1.2 Schedulability Criterion of RNBC

The strong contribution behind RNBC is the precise schedulability criterion that guarantees the absence of read/write clashes regardless of the relative phase between read and write operations. Before introducing this schedulability criterion, we have to first introduce some definitions:

c_r**:** the WCET of the read operation

c_w**:** the WCET of the write operation

*mint***:** the minimum inter-arrival time between two messages, i.e., consecutive write operations

Based on these definitions, we can state the schedulability criterion of RNBC:

Theorem 4.1 *Without any further assumption about the synchrony between read and write, the following is a necessary and sufficient schedulability condition for the RNBC protocol:*

$$c_w + c_r \leq mint$$

This schedulability criterion implies that the maximum execution time available for a read operation $c_{r,max}$ is as follows: $c_{r,max} \leq mint - c_w$. In other words, we have to make sure that the WCET of the read and write operation together is less or equal than the minimum inter-arrival time of messages.

Proof (Theorem 4.1) To prove this, we have to show, both, that the scheduleability criterion is sufficient and also necessary. To do so, we use Figure 4 to visualise some key properties of the behaviour of RNBC. The first row *write* shows in which buffer the individual write operations are writing (with distance *mint* between them). The 2nd row *wbuff* shows the timing diagram of the flag `wbuff`, following directly from the implementation. The row *rbuff* shows the behaviour of a read operation, depending on its starting time in comparison to write operations. This means that the flag `rbuff` at the start of a read operation is always set as the opposite of the current value of the `wbuff` flag. This line shows that after the completion of a write operation to buffer b_i, any read operation started afterwards and before the next writing operation starts, will read from b_i. The lines *rwindow* b_0 and *rwindow* b_1 show the possible reading window for buffer index 0 respectively 1, such that no read/write clash will occur. The reading window for each buffer b_i is from the completion of a write into b_i till the beginning of the next write operation into b_i.

Part 1: Sufficient: As shown in Figure 4, the read access from buffer b_i can only start after completion of its write till the next write completion of buffer b_{1-i}, which is a time span of *mint*. At the same time, the reading window of buffer b_i starts as well directly after the completion of its write and lasts till the beginning of the next write operation to buffer b_i, which is a time span of $2mint - c_w$. Any valid read has to start within $rbuff == b_i$ and has to complete before the end of the reading window *rwindow* b_i, for which the minimum duration is:

$lenth(rwindow) - lenth(rbuff) = (2mint - c_w) - mint = mint - c_w$.

Hence, the minimum guaranteed time available for reading is $mint - c_w$, which implies that $c_r \leq mint - c_w$ is sufficient for non-clashing read/write operations. This proves that the schedulability condition of Theorem 4.1 is sufficient.

Part 2: Necessary: To proof that the schedulability condition is necessary, we use an indirect proof. We start with the assumption that the schedulability condition does not hold and derive from it that the read/write operations can clash.

Assuming that the schedulability condition does not hold, we have the following property:

$$c_w + c_r = mint + \Delta \;\mid\; \Delta > 0$$

To look for the worst case, we assume that the read access to buffer b_i starts just at the end of $rbuff == b_i$, i.e., at *mint*, which is the last possible time before reading is switched to buffer b_{1-i}. In that situation the remaining time of reading window *rwindow* b_i is $mint - c_w$, because $lenth(rwindow) - lenth(rbuff) = (2mint - c_w) - mint = mint - c_w)$.

However, based on the assumed property $c_w + c_r = mint + \Delta \mid \Delta > 0$ it follows that the reading time c_r is $c_r = mint - c_w + \Delta$. Thus, the reading time of buffer b_i is by Δ longer than the remaining length of the reading window, causing a clash of the read/write operations to buffer b_i. This proves that the schedulability condition of Theorem 4.1 is necessary. □

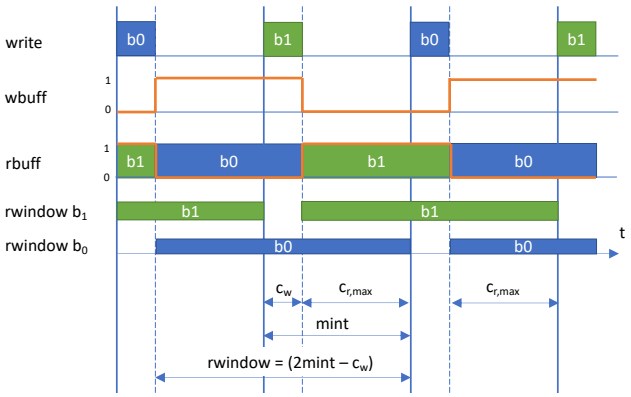

Figure 4. Properties of RNBC Protocol (used in proof of Theorem 4.1)

Corollary 4.2 *If the condition* $(c_w + c_r \leq mint)$ *can be ensured, then there is no benefit in terms of reducing read/write clashes by using more than two communication buffers, e.g., a ring buffer with* $n > 2$ *elements.*

4.1.3 NBW vs RNBC

We have stated that RNBC relies for its correctness on some real-time assumptions, like inter-arrival time and WCETs. NBW does not have any such requirements specified, thus NBW looks easier to be deployed. However, we herewith compare them in further detail.

As stated above, the border-line case where RNBC still works is $c_w + c_r = mint$.

Now lets assume that the WCETs of the read and write operations of NBW are denoted as c'_r and c'_w. Comparing the implementations of NBW in Figure 2 and of RNBC in Figure 3, it is clear that NBW has more overhead for both, read and write, i.e., $c'_w > c_w \wedge c'_r > c_r$. From that follows that $c'_w + c'_r > mint$. This means, while RNBC still just works for this *mint* value, the same *mint* value will cause NBW to be caught in never-ending read-write clashes, regardless of the phase between read and write. Thus, also NBW has to rely on some real-time assumptions, which are actually even more strict than those for RNBC.

Concluding, RNBC is an efficient implementation for the concurrent single-writer multiple-reader communication pattern, using real-time properties like WCET and minimum inter-arrival time to assure correct behaviour. Under the given schedulability condition, RNBC allows a constant access time for both reader and writer.

4.2 Time-Aware Interface

The time-synchronized access strategy solves the mutual-exclusion problem at the LIFSS by avoiding access conflicts from the very beginning. To this end, it carries out the read and write operations of CCs to the LIFSS at times that do not coincide with the accesses by the TTCS — the times when CCs must not access the LIFSS are derived from the TTCS message-transmission schedule that is constructed at system-construction time.

4.2.1 Accessing the LIFSS

When designing the software for a CC with time-synchronized LIFSS access, one will pay particular attention to synchronize the time of read and write operations from the very beginning. On top of conflict avoidance, one can even benefit from the timing information contained in the message schedule and activate the task on a CC tailored to the timing of LIFSS-read and write operations of the TTCS: Such a task schedule will ensure that a task that reads data from the LIFSS will be activated shortly after the message with these data has been received and made available by the LIFSS. In a similar way, the scheduler will activate a task that writes to the LIFSS right before the TTCS will transmit the written data.

To align LIFSS-read and write operations with the actual message transfers, the CC needs (a) a real-time task scheduler and (b) a mechanism for adjusting its local clock to the clock of the TTCS. The alignment can be accomplished by means of a static, table-driven scheduler, where the scheduling table guarantees that the CC accesses the LIFSS in time windows that are guaranteed to be conflict-free. The programmable clock interrupt of the LIFSS can be triggered regularly to synchronize the clock of the CC with the global time-base. This clock synchronization ensures that the task scheduler of the CC and the message schedule of the TTCS stay consistent.

4.2.2 Interface-Timing Constraints

Let us provide a more detailed discussion on when a CC may safely access its LIFSS without running into mutual-exclusion conflicts. We assume that the schedule of TTCS accesses to the LIFSS is given. Further we assume that the CC regularly adjusts its clock to the global clock using master-clock synchronization, i.e., in the clock interrupt routine the clock of the CC is set to the value of the global clock.

In the time intervals between clock synchronization, the clock of the CC drifts away from the global clock. This relative drift has to be taken into account when planning the conflict-free schedule of accesses to the LIFSS. In the following, we will explore how the possible clock drift can be considered when planning the LIFSS access times for CCs. We make the following assumptions.

- The clock of the communication controller that represents the global time of the TTCS acts as the reference clock.
- Tick i of the reference clock happens at time t_i; t_i^j denotes the time of tick c on clock j.
- The drift rate $\hat{\rho}$ denotes the maximum drift rate of a CC clock relative to the reference clock, i.e., $\hat{\rho}$ combines the absolute drift rate of the local representation of the global clock and the maximum absolute drift rate of the clocks of the CCs.

When planning the LIFSS-read and write operations of the CC, we have to ensure that the time intervals of these read and write operations do not overlap with LIFSS-data accesses by the TTCS. The determination of these time intervals has to take the relative drift of the clocks of the CC and the TTCS into account (see Fig. 5).

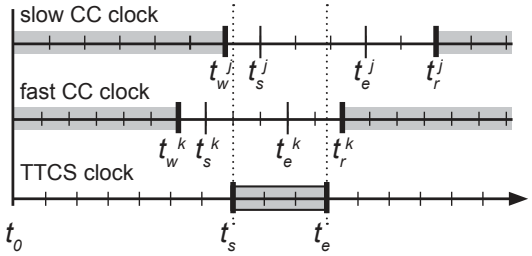

Figure 5. Latest write to and earliest read from LIFSS data.

Let us assume the TTCS accesses some LIFSS data between ticks s and e on its clock, in the time interval $T = [t_s, t_e]$ after the last synchronization point, at time t_0. Now we want to determine the start and end ticks (w and r) of the access interval of the CCs that guarantees mutual exclusion and accounts for the drift of the clocks.

To ensure that all LIFSS accesses by CCs preceding the LIFSS access of the TTCS have completed before T, we must make sure that even the CC with the slowest clock, say CC j, has completed its access at tick w with $t_w^j \leq t_s$, thus

$$w = \left\lfloor \frac{s}{1+\hat{\rho}} \right\rfloor .$$

Analogously, we must guarantee that CCs accessing the LIFSS start only after the TTCS has completed its access. In this case, the CC with the fastest clock, CC k, must not start reading repectively writing the LIFSS before tick r with $t_r^k \geq t_e$ and

$$r = \left\lceil \frac{e}{1-\hat{\rho}} \right\rceil .$$

4.2.3 Scheduling CC Tasks

To maintain mutual exclusion, real-time tasks on the CCs that access LIFSS data must be scheduled such that they do not overlap with the respective $[w, r]$ intervals. These mutual exclusion constraints are added to the application-specific precedence constraints of the scheduler. If tasks are statically scheduled, the pre-runtime scheduler uses those constraints together to build the dispatch tables that the dispatchers running on the CCs will interpret at runtime.

4.2.4 Interface Timing Properties

Synchronizing the LIFSS accesses of the CCs and the TTCS has a positive effect on the timing properties of the interface.

First, synchronizing both LIFSS-write and read operations on all CCs to global time reduces the message-delay jitter in comparison to non-synchronized access. In fact, if we use a synchronized, table-driven scheduler to trigger the LIFSS reads and writes, the jitter can be kept as small as Π, the precision of the global clock.

Second, using table-driven schedules that are aligned to the global clock allows system designers to streamline task executions and message communication. This way, the overall response times of real-time transactions spreading over two or more CCs can be kept short.

Third, if all data manipulations and data transfers via the TTCS follow a global time schedule, then the information about the age of data items is implicitly available at all CCs of the computer systems. As a consequence, the time stamps of real-time observations do not have to be transported via the TTCS. This means, in a time-triggered network with fully time-synchronized CCs, only the *values* of observations have to be handed over to the LIFSS. Both, the *name* and the *time* of the observation are implicitly known.

5 Comparison

Each of the presented access strategies to the interface of a time-triggered communication system aims at the automomy of CCs, to make components time-composable. The different strategies are, however, paired with significant differences in the characteristics of the components that constituate the overall system. We discuss the differences of the component characteristics in the following; see also Table 1.

A CC that accesses the LIFSS as a *time-agnostic interface* acts fully autonomously, i.e., it ignores the message schedule and potential conflicts when interacting with the LIFSS. A *time-aware component*, in contrast, uses its knowledge about the message schedule to synchronize its LIFSS accesses to the operation of the TTCS.

The fact that components with a time-agnostic interface do not synchronize with the message schedule leads to a message-validity jitter of (almost) two times the message period for all data items read from the LIFSS. This is due to the fact that both at the sender

Table 1. Comparison of the Component Characteristics for the Interfacing Methods.

Characteristic	*Interface*		
	Time Agnostic		*Time Synchronized*
	NBW	*RNBC*	
Control paradigm	full autonomy	full autonomy	adaptation to schedule
Message validity jitter	2× message period	2× message period	precision of clock
Jitter of message read	0−2 failed read attempts	0	0
Task-msg. streamlining	no	no	yes
Use of time	value (explicit)	value (explicit)	control (implicit)
Replica determinism	no	no	yes
Build complexity	low	low	medium to high
Example app.	movie streaming, sensor network		flight control, steel mill, drive by wire, film stretching

side and receiver side the duration of the time interval between the LIFSS access of the TTCS and access of the CC may vary between zero and the duration of a message period. This jitter is significantly higher than for time-aware interfaces, for which it is Π, the precision of the global clock.

Write operations to the LIFSS always have a constant execution time. Regarding read operations in NBW, there is an execution-time jitter due to the possibility of retries. Both, RNBC and the time-synchronized reads have no execution-time jitter due to LIFSS-access conflicts. This means that the use of RNBC allows for a construction of components that are fully autonomous, without any external control influences on their temporal behavior.

The lack of synchronization at time-agnostic interfaces inhibits the streamlining (i.e., tight synchronization) of tasks that read from or write to the LIFSS and the messages that transport the respective data items. A time-aware interface with time-synchronized interface access, in contrast, allows for the synchronization of these activities. Thus time-aware interfaces support real-time transactions with much shorter end-to-end delays than asynchronous interfaces.

When all operations of the components and the communication system are time-triggered, controlled by a global execution plan, then the knowledge about the points in time of all data-read and write operations are globally known, i.e., the timestamps of these operations are implicit global knowledge in the system. As a consequence, and in contrast to systems which operate asynchronously, one does not need to transport the times of real-time observations in time-synchronized systems.

Synchronizing the LIFSS-read and write operations of a component with global time is a prerequisite for a clear definition of the state of a CC, which, in turn, is needed for the realization of replica-deterministic components (i.e., components that agree both in the value and time domain within a defined time span). As the provision of replica determinism greatly simplifies the construction of fault-tolerant real-time systems, time-aware LIFSS access of CCs is of essential for implementing fault tolerance, as well.

The central advantage of using interfaces without care about timing is the low build complexity of the components and the overall system. When using time-agnostic interfaces, developers do not need to know about the temporal particularities of the LIFSS or other components. In contrast, to fully exploit the benefits of synchronized interface access, the timing of operations on the components and message transmission on the TTCS have to be tightly coordinated. The complexity and cost for designing such a system-wide coordination may be significant.

Typical example applications for non-synchonized interfaces are entertainment systems, like movie streaming, or monitoring systems (e.g., based on sensor networks). Usually, these applications do not require system-provided fault tolerance, but they greatly benefit from the lower build complexity. Still, they may need to compensate for jitter in the order of message periods during message reception by appropriate buffering or queuing. In the case of monitoring systems, observations can be time-stamped by reading the global time available at the LIFSS after the observation. Applications that use time-synchronized interfaces trade the added build complexity for the realization of deterministic real-time transactions with short end-to-end delays. Typical examples of such applications are related to control (e.g., flight control systems, film stretching systems, ...) which often require highly regular sense-control-act cycles. Some control systems are safety critical and profit from fault

tolerance that is enabled at the architectural level by the use of time-synchronized interfaces.

6 Example: CC Predictability

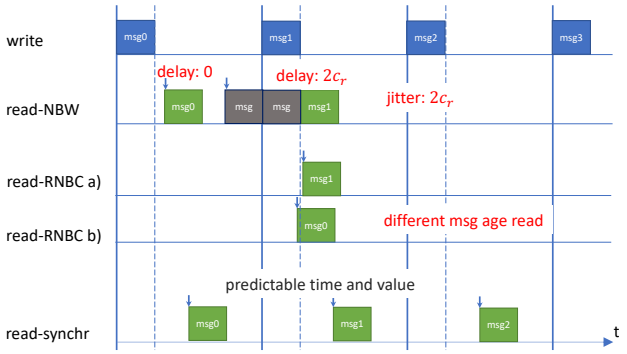

Figure 6. Local behaviour of different interfacing methods

In this section we show the temporal predictability of components using the different access strategies to the interface of a time-triggered communication system. Figure 6 shows the read/write behaviour at a local network node between the CC and the LIFSS:

- The first row shows the time line of the write access to the LIFSS, with different message instances over time.
- The second row "read-NBW" shows examples of asynchronous read access via the NBW protocol. The first read operation happens just after completion of the last write access, and proceeds with zero delay. The second read operation just slightly overlaps with the write operation for message *msg1*. This lead to two read attempts partially overlapped with the write, causing them to fail, and only the third attempt then finally succeds. Thus, NBW causes jitter to the temporal behaviour of a component.
- The rows "read-RNBC a)" and "read-RNBC b)" show examples of the asynchronous read with RNBC. In both cases, the read operation has a constant execution time, as RNBC is free of read-/write conflicts by design. However, what the two different examples also show, is that with RNBC a small difference in the start of a read can cause to read a different message instance. Thus, while RNBC allows components to be time predictable, the predictability in the value domain of messages is not given.
- Finally, the row "read-synchr" shows access patterns with synchronous interfacing. It shows that synchronous interfacing not only gives constant execution time of the read operation, but also provides predictability in the value domain, as read operations are fixed scheduled with some time offset after the completion of each write access.

7 Conclusion

In this paper we discussed different interfacing techniques between a computing component (CC) and a time-triggered communication network. The results show that best predictability in time and value domain is achieved by synchronous interfacing, where the execution of activities at the CC is synchronous with the message communication over the time-triggered network. To achieve this, the local clock of the CC has to be synchronized to the global clock of the time-triggered network. With asynchronous access, no clock synchronisation is required, but it comes at the cost of unpredictability in the value domain, as it is not ensured which message instance is obtained by a read access. We have also developed a new asynchronous access protocol, called *Rate-bounded Non-Blocking Communication* protocol (RNBC), which ensures the temporal predictability and autonomy at the component level for asynchronous access.

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