Interference Assisted Lithography for Patterning of 1D Gridded Design

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ABSTRACT

We present Interference Assisted Lithography (IAL) as a promising and cost-effective solution for extending lithography. IAL achieves a final pattern by combining an interference exposure with a trim exposure. The implementation of IAL requires that today's 2D random layouts be converted to highly regular 1D gridded designs. We show that an IAL-friendly 6T SRAM bitcell can be designed following 1D gridded design rules and that the electrical characteristics is comparable to today's 2D design. Lithography simulations confirm that the proposed bitcell can be successfully imaged with IAL.

Keywords: interference lithography, double exposure, regular design, SRAM

1. INTRODUCTION

The continued scaling to maintain Moore's Law truly challenges lithography. The timely availability of EUV Lithography (EUVL) for mass production is questionable, due to significant challenges with source power and lifetime, mask defect control, suitable resist materials *etc*. The promise of high-index immersion 193nm lithography is also dim due to challenges with absorption of high-index lens materials. Alternative methods that promise higher resolution, such as double patterning and nano-imprinting are being explored. However, double patterning needs to meet the stringent overlay control and new EDA tools for pattern splitting, as well as to address concerns of significantly increased patterning cost. Nano-imprinting faces challenging issues such as overlay and defect control, low throughput etc. No satisfactory cost-effective solutions exist for the patterning of 32nm half pitch features and beyond.

Interference Assisted Lithography (IAL) can be a promising cost-effective lithography solution. IAL achieves a final pattern by combining an interference exposure with a trim exposure [1-3]. The interference exposure generates periodic lines and spaces. The trim exposure then modifies the line/space grating to define the final pattern. IAL promises to reduce the cost of patterning, since it uses a double exposure rather than double patterning process, and can be implemented as a maskless technology if an Electron Beam Direct Write (EBDW) tool is used for the trim exposure. Alternatively, one lower-complexity trim mask with Optical Projection Lithography (OPL) can satisfy the high volume production needs. Highly periodic structures, such as gratings, can be generated cost-effectively through interference, which doesn't require expensive lenses.

IAL offers compelling technical benefits. Since it does not need large expensive lenses, high-index immersion 193nm and even 157nm lithography can be adopted for an interference lithography tool relatively straightforward. This enables the extendibility of IAL beyond the pitch limit of current OPL. IAL is also compatible with Self Aligned Double Patterning (SADP) (a.k.a. spacer lithography) for further extendibility [4]. By using Interference Lithography (IL) to

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define the line/space patterns, almost infinite depth of focus can be achieved. Furthermore, IL provides high contrast, which suggests reduce of line-edge roughness [5].

The implementation of IAL requires that 2D random layouts are converted to highly regular 1D gridded designs. 1D gridded designs are "litho friendly" and allow the k_1 factor to be reduced significantly compared to 2D random layouts. It is possible to realize k_1 of 0.25 with IAL for 1D gridded design, while k_1 for 2D random layout imaged with single-exposure OPL is limited above 0.35. 1D gridded designs have additional benefits, such as reduced Across Chip Linewidth Variation (ACLV) [6]. Tighter distribution of channel length across the process window leads to reduced variation of device characteristics such as subthreshold leakage current and drive current, improving parametric yield. The benefits of increased layout regularity are already causing advanced designs to migrate toward high regularity design. For example, at the 45nm technology node, Intel adopted 1D regular design rules for both SRAM poly layer and random logic poly layer to reduce gate length variation and improve yield [7].

In this work, we show the design of an IAL-friendly 6T SRAM bitcell. SPICE-based studies confirm the functionality and robustness of the IAL-friendly 6T bitcell design. Specifically, through the butterfly curve and N-curve, representing read-stability and write-ability of bitcells, we observe that IAL-friendly 32nm bitcell yields comparable stability and functionality to the scaled 32nm version of an industry standard 90nm bitcell (TSMC 90nm). Lithography simulations are performed to evaluate the printability of these layouts using IAL. The simulation results confirm the applicability of IAL in the patterning of all critical layers (poly, contact, metal, via etc) of these cells.

This paper is organized as follows. Section 2 discusses the concept of Gridded Design Rules and then provides the details of IAL-compatible design of a 6T SRAM bitcell. Section 3 discusses the modeling and simulation results for the SRAM bitcell, including circuit modeling and lithography simulations. Finally, section 4 gives conclusions.

2. 1D GRIDDED DESIGN OF SRAM BITCELL

2.1 Concept of Gridded Design Rules (GDR)

Conventional random logic design has been done for many years using random two dimensional (2D) shapes [8]. These shapes have edges which are placed on a "design grid" which may be ten to twenty times smaller than the technology node feature size. 45nm logic is done with a 1nm grid, for example. This very fine grid means that edges can have a very large number of spacings relative to other edges in the same layer or different layers in the design. As a result, "complex design rules" (CDR) taking hundreds of pages in a design manual are given to the physical design team to follow. Unfortunately, even these complex rules have not been enough and "restricted design rules" (RDR) have been introduced to try to catch "hotspots" and other marginally manufacturable patterns.

One dimensional (1D) "gridded design rules" (GDR) refer to a layout style in which critical layers are drawn with 1D lines on a coarse grid [4, 9-12]. Since the shapes are now straight lines, they can be described with fewer variables such as width, space, and end-gap. The grid is typically the pitch or half-pitch of the layer or a related layer. This can be better understood when compared to "complex design rules" (CDR). Figure 1 shows an example of two functionally equivalent layouts with the left side drawn with 1D GDR and the right side drawn with 2D CDR. Three problem areas are highlighted in the 2D CDR case. Site 1 represents a transistor gate line which is isolated in the x-direction from other lines; it will have a reduced process window as compared to the same gate line in the 1D GDR case. Site 2 indicates a gate line in a denser environment, but it will also have a reduced process window since it is relatively isolated on one side. Finally, site 3 shows gate lines in a congested 2D environment; this site is susceptible to necking and bridging hotspots in addition to showing a reduced process window.

As illustrated by the left side of Figure 1, the vertical gate lines are on a uniform pitch with dummy lines as needed. The horizontal first metal lines are also on a uniform pitch with circuit line segments separated by uniform gaps. Since the gate and first metal lines are on perpendicular grids, the diffusion and gate contacts are automatically located at intersections of the grid lines.

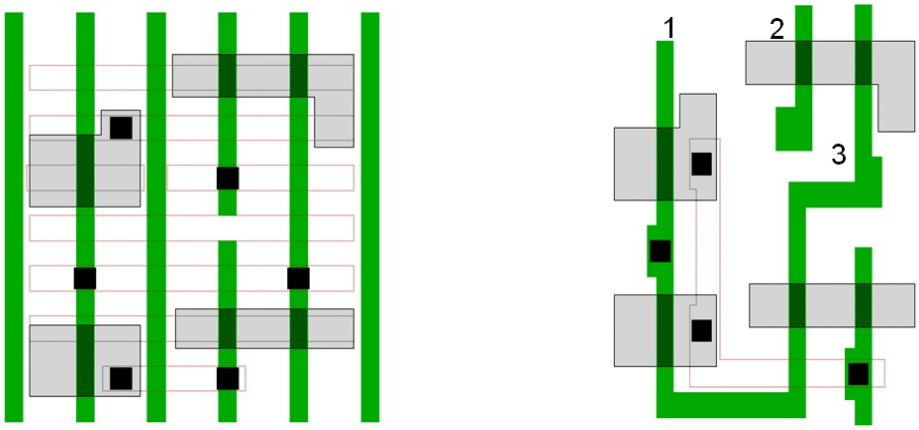


Figure 1. 1D GDR layout (left side) compared to 2D CDR layout (right side).

In a 1D GDR layout, the design rules are greatly simplified because they involve widths, spaces, and end-gaps. Overlap rules, like first metal end-overlap of a contact, are built into the first metal end-gap rule and hence are redundant. Similar logic applies to diffusion-to-contact, gate-to-contact, and metal-to-via overlaps. The Tela Canvas™ implementation of 1D GDR builds these constraints into the logic cell architecture to give "correct by design" layout.

The 1D GDR layout style can allow individual layers to be split into "lines" and "cuts" in a straightforward manner [13]. The lines are essentially a grating pattern and can be imaged using an interferometric technique. The cuts can be patterned by the same technique chosen for other "hole" layers like contacts or vias.

2.2 IAL-compatible SRAM bitcell design

In this subsection, we show the design of a 6T SRAM bitcell following 1D regular-pitch gridded design rules.

We generate an initial grid-based bitcell layout as shown in Figure 2(a). We assume that the feature size and minimum spacing of all layers are each equal to two drawing grids, so that all patterns can have the same linewidth. However, this grid-based bitcell is still not IAL-compatible, as there exist 2-D patterns on the diffusion and Metal1 (M1) layer; furthermore, not all patterns are placed on a 1-D pitch, except for poly patterns. From the initial layout, we can decompose patterns so that they are placed on the 1-D pitch. However, the 'L' shapes on the Metal1 layer cannot be made IAL-compatible through decompaction. To make those 'L' shape geometries 1-D, the 'L' shapes must be split into two rectangles, and then one of the rectangles must be moved to another layer, e.g., Metal2 (M2). We use the vertical direction for Metal1 patterns and the horizontal direction for Metal2 patterns. The new 1-D regular pitch layout is generated as shown in Figure 2(b). Here, we assume that the diffusion layer can be generated by non-IAL process. To make all geometries, including the diffusion layer 1-D, we split the thick width diffusion patterns into two parallel, same-sized patterns as shown in Figure 2(c), though this can lead to larger cell size.

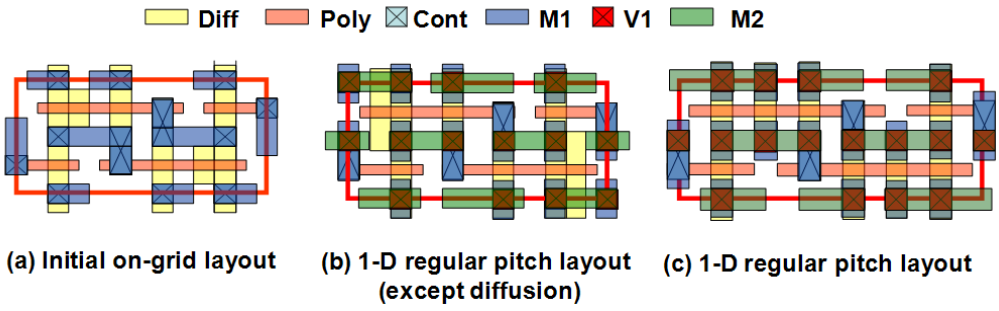


Figure 2. IAL-compatible bitcell layout.

Vertical pitch. In Figure 2, we observe that the IAL-friendly bitcell layout requires at least two poly pitches in the vertical direction. The required size of the pitch in vertical direction is calculated as follows. Vertical pitch is decided by either minimum IL pitch or the minimum distance that embeds all constituent materials. Figure 3 shows a vertical cut-view of the proposed bitcell. From Figure 3, poly pitch must be greater than the sum of poly width, contact width and twice poly-to-contact spaces. Poly-to-contact space is determined by the sum of the thickness of spacer and strain layer. Considering process variations such as overlay and CD error, poly-to-contact space is then calculated as

$$S_{pc} \geq W_{space} + W_{strain\_layer} + E_{overlay} + E_{CD},$$

where S_{pc} is poly-to-contact space, W_{spacer} and $W_{strain\ layer}$ are the widths of the spacer and strain layer, and $E_{overlay}$ and E_{CD} are the amounts of overlay error and CD control error. We assume that W_{spacer} and $W_{strain\ layer}$ are 8nm and 10nm according to Verhaegen et al. [14], and $E_{overlay}$ and E_{CD} are 6.4nm and 2.6nm according to ITRS [15]. Then, the minimum poly-to-contact space is 27nm. The required poly pitch is calculated by summation of poly width, contact width and twice the poly-to-contact space. We also assume that minimum poly width is 32nm and minimum contact width for 32nm technology is 45nm, following [14]. From this, we see that the poly pitch must be greater than 131nm (=27×2+32+45). Since the expected IL pitch for NA = 1.2 and λ = 193nm is much less than 131nm, vertical pitch is determined by the above calculation.

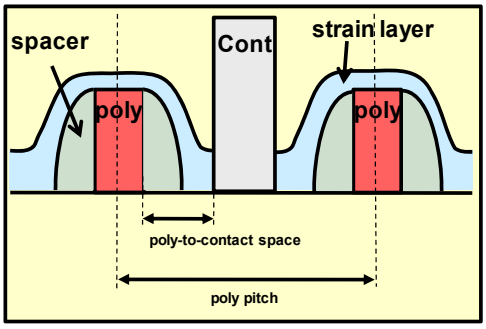


Figure 3. Vertical cut-view of SRAM bitcell.

Horizontal pitch. In the horizontal direction, there are no constraints analogous to those described above for vertical pitch (strain layer, spacer, etc.). Horizontal pitch is constrained by the diffusion-to-nwell spacing, diffusion-to-diffusion spacing, and minimum contact/metal/via pitch (which is in turn determined by IL pitch), etc. Therefore, in the horizontal direction we can use either the same poly pitch size or a reduced pitch size.

Finally, we define the minimum *drawing grid* size. Once we determine the number of grids per pitch, we define the size of a drawing grid by arithmetic division and rounding. In the present study, we consider 6 grids per poly pitch with 22nm per grid. Based on the design rules, we develop 1-D regular pitch bitcell layouts. In Figure 4, (A) is one candidate for 1-D regular pitch layout in which IAL is not applied to the diffusion layer but has smaller size, and (B) is another candidate for a full layer 1-D regular pitch layout where the diffusion layer is also IAL-compatible. The bitcell areas are 0.145 um^2 and 0.163 um^2, respectively. The 28x12 grid design in Figure 4(B) can also be a potential layout for FinFET SRAM by scaling the size of each grid, for example, down to 16nm or 11nm per grid.

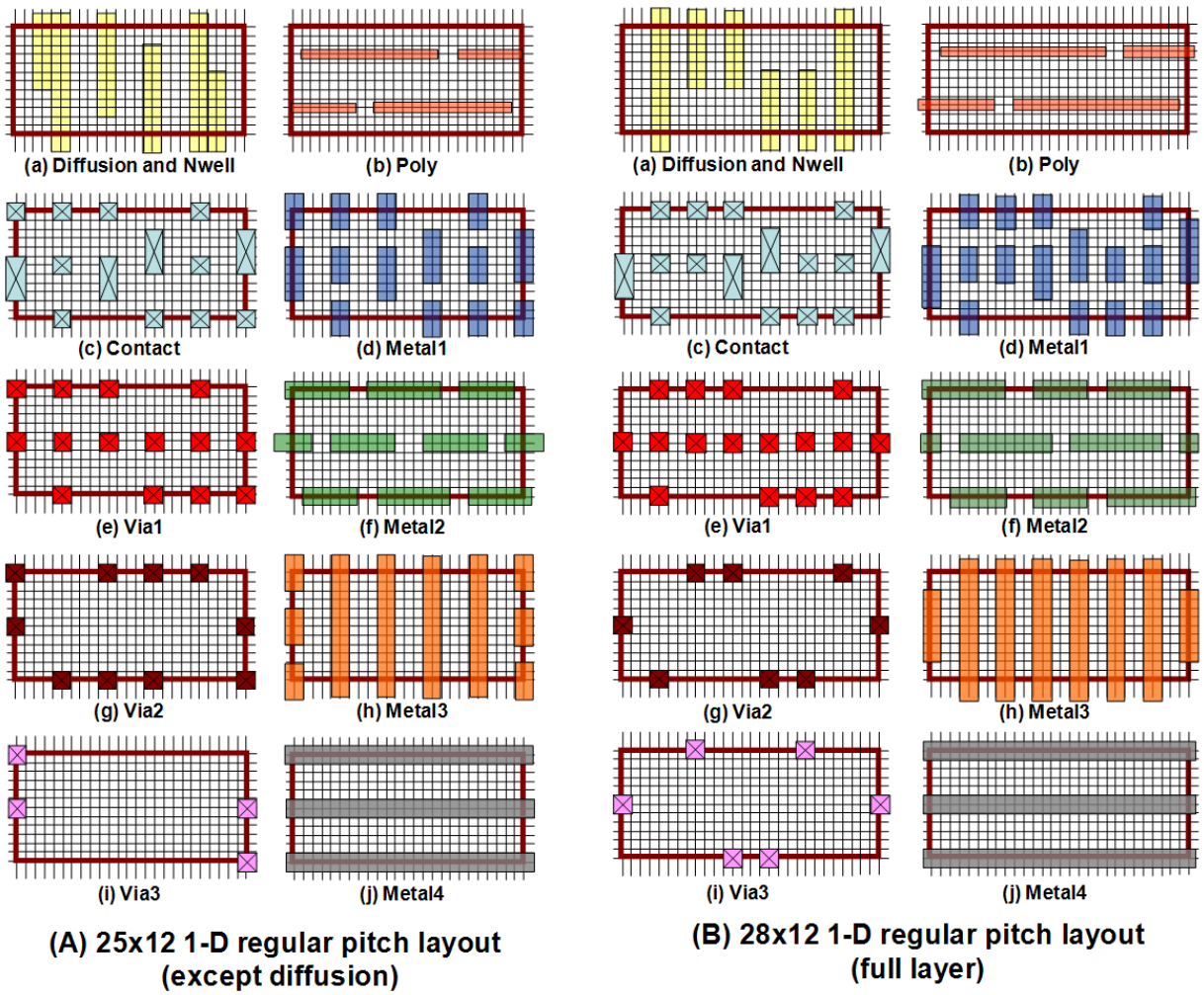


Figure 4. Candidate bitcell layouts.

3. MODELING AND SIMULATION RESULTS

3.1. Electrical characteristics of 1-D regular pitch SRAM bitcells

We verify electrical characteristics of the proposed bitcells according to the following metrics.

- **Butterfly curve.** Butterfly curve is generally used to qualify the static noise margin. To generate the butterfly curve, we measure the voltage transfer curve between internal nodes. Figure 5 left shows the butterfly curves of our proposed bitcells and the reference bitcell for which transistor sizes are shown in Table 1. We observe that the static noise margin of our bitcell is similar to that of the reference.
- **N-Curve.** To obtain more insight into static characteristics, the N-curve can be analyzed. The N-curve is generated by plotting the current consumed by an internal node as the node switches from low to high. SINM (SVNM) is static current (voltage) noise margin, which is strongly related to read stability; WTI (WTV) is write trip current (voltage), which is strongly related to write ability. SINM increases and WTI decreases, when the transistor width increases. Larger SINM means better read ability and smaller WTI means worse write ability. Figure 5 right compares N-curves of the proposed bitcell (SINM_reg and WTI_reg) and the reference bitcell (SINM_TSMC and WTI_TSMC). According to Figure 5, our bitcell has better read stability but worse write ability.

- **I_{read}.** I_{read} is the measured current at a bitline when wordline is switched to high. Large I_{read} means better read stability. We again observe from the second row of Table 2 that our bitcell has better read stability.
- **$I_{leakage}$.** $I_{leakage}$ is the measured current from the supply node when a bitcell is in stable steady state. $I_{leakage}$ is important not only as power consumption itself, but as a metric of stable operation including data retention. Smaller $I_{leakage}$ is preferred. However, we observe that our bitcell has larger $I_{leakage}$, as seen in the third row of Table 2.
- **VDD_{hold}.** VDD_{hold} is the minimum supply voltage required to hold a bit of data, and is measured by lowering supply voltage and monitoring the internal nodes. When the voltage difference between two internal nodes becomes less than the sensing margin, the internal data cannot be captured by the sense amplifier and the data will be lost. Comparison of VDD_{hold} in the fourth row of Table 2 show little difference.

From the simulation results, we observe that our bitcells have better read stability but worse write ability, and there is no significant difference between 25x12 bitcell and 28x12 bitcell, as shown in Figure 6. Therefore, the decision between the proposed bitcells mainly depends on the difficulty in applying IAL to the diffusion layer and the minimum pitch size of IAL in vertical direction.

Table 1. 6-T SRAM bitcell device sizing.

	TSMC 90nm		32nm scaled from TSMC 90nm (Reference)		32nm proposed bitcells (both 25x12 and 28x12)	
	L (nm)	W (nm)	L (nm)	W (nm)	L (nm)	W (nm)
Pull-up	100	100	32	32	32	44
Pull-down	100	175	32	56	32	88
Pass-Gate	115	120	37	38	32	44

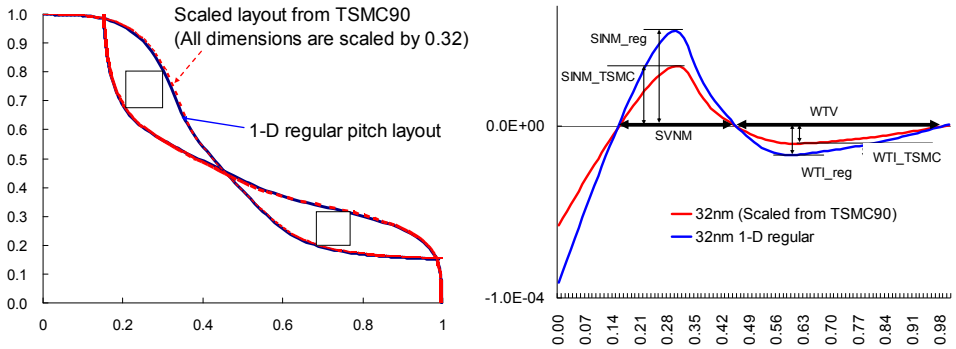


Figure 5. Butterfly and N-curve comparison for reference and proposed bitcells (without parasitics).

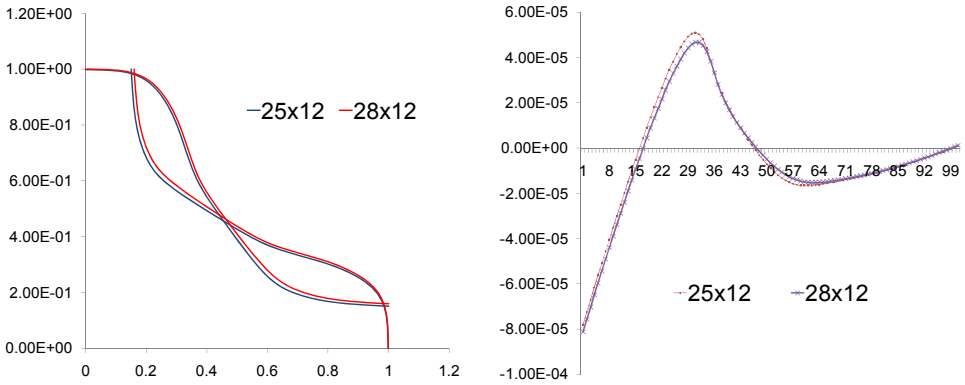


Figure 6. Butterfly and N-curve comparison between 25x12 and 28x12 layout (with parasitics).

Table 2. Comparison of I_{read}, $I_{leakage}$ and VDD_{hold}.

	32nm scaled from TSMC 90nm (Reference)	32nm proposed (1) (25x12)	32nm proposed (2) (28x12)
I_{read}	41.2 uA	66.7 uA	64.4 uA
$I_{leakage}$	85.4 nA	142.7 nA	132.6 nA
VDD_{HOLD}	110 mV	118 mV	119 mV

3.2. Lithography simulations of 1-D regular pitch SRAM bitcells

For the lithography simulation, we use Fraunhofer Institute IISB's Dr. LITHO version 0.12.rc3 with full vector models on thin mask and high contrast positive 50nm resist model parameters for simple acid diffusion and 10% quencher to photo-acid-generator loading. Because of the type of diffusion model used we chose a short post-exposure-bake time of 10 seconds and a develop time of 40 seconds. These process times were chosen after running a full factorial of the poly layer for 90nm-pitch SRAM. The 1D regular-pitch SRAM bitcell used for the lithography simulation here is designed on 30x12 grids with 15nm per grid and has the same pitch for all layers except the diffusion layer, as shown in Figure 7. Electrical modeling shows that this 30x12 grid design has about the same electrical performance as the 25x12 and 28x12 grid design discussed in section 3.1. We apply a simple OPC correction using biasing. As outlined in Table 3, we use an ASML-type cross-quadrupole (XQUAD) shape with x-y Azimuthal-like polarization for the trim exposure with NA=1.2 to trim the 90 nm pitch interference pattern. The interference lithography (IL) was emulated by imaging an alternating phase-shift mask with an on-axis coherent source. We develop solutions for all layers of the SRAM bitcell except the diffusion layer. We use a positive-tone resist for poly layer and negative-tone resist for all other layers. Table 3 summarizes our simulation settings for trim exposure of all layers. Consistent with our previous work [16], chromeless phase assist (CPA) masks provide the best-quality trim exposure.

Table 3. Illumination conditions for trim exposures using ASML-type cross-quadrupole illuminator shape.

Layer	IL pitch	Mask Type				Resist type
		Binary chrome mask		Chromeless phase assist		
		σ_{Center}	σ_{Width} 20˚ Blade Angle	σ_{Center}	σ_{Width} 20˚ Blade Angle	
Poly	90nm	0.65	0.25	-	-	positive
Contact	90nm	0.89	0.2	0.94	0.15	negative
Metal1	90nm	0.89	0.2	0.94	0.15	negative
Via1	90nm	0.41	0.2	-	-	negative
Metal2	90nm	0.94	0.15	0.94	0.15	negative
Via2	90nm	0.41	0.15	-	-	negative
Metal3	90nm	-	-	0.94	0.15	negative
Via3	90nm	0.41	0.15	-	-	negative
Metal4	90nm	-	-	0.94	0.15	negative

3.2.1 Basic Single Focus-Exposure Simulations

We first perform simulations of trim exposure for all layers at a single fixed focus and exposure dosage. The mask pattern and final resist pattern for the poly layer are shown in Figure 8 (a) and (b) respectively. Figure 9 shows the final

resist patterns for contact, Metal-1, Via-1 and Metal-2 layers. We observe that all patterns including rectangular contacts and very high dense hole arrays are successfully printed through the IAL process.

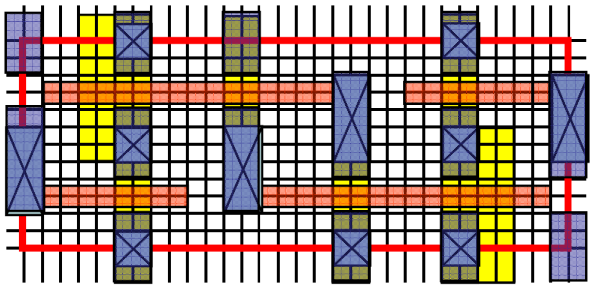


Figure 7. Layout of the 30x12 grids 1D regular pitch SRAM bitcell used for the lithography simulation

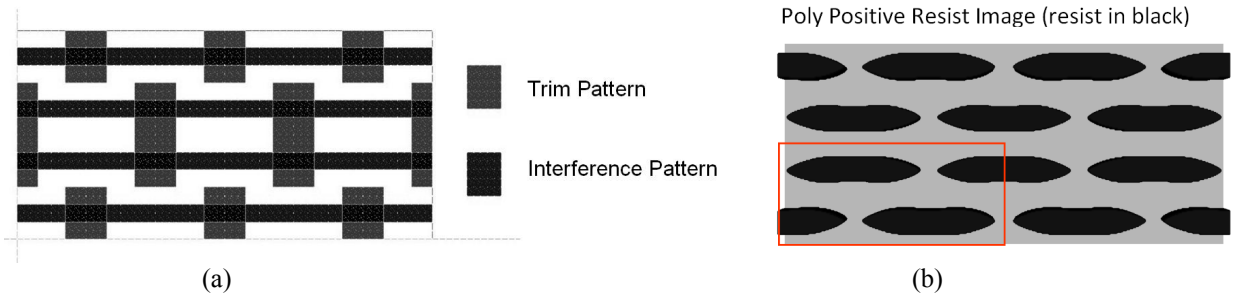


Figure 8. (a) Mask pattern and (b) final resist pattern for the SRAM poly layer. The red box outlines the unit cell.

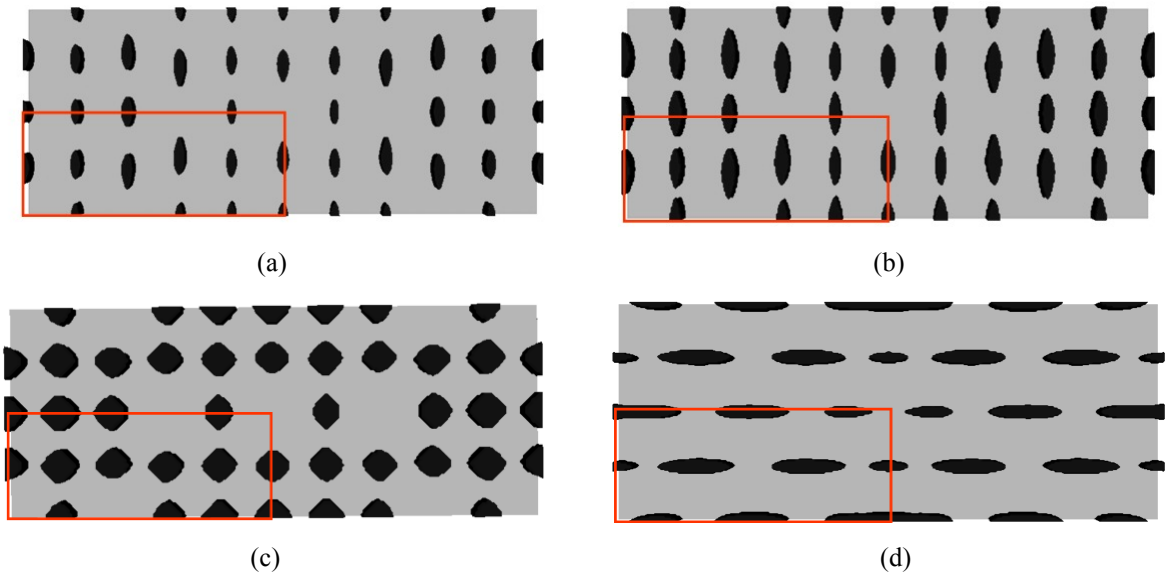


Figure 9. Final resist patterns (negative resist shown in gray) for (a) contact layer, (b) metal-1 layer, (c) via-1 layer, (d) metal-2 layer. The red box outlines the unit cell.

3.2.2 Focus-Exposure Process Window Simulations

We next compare the process window of IAL to a single exposure process for poly layer. In this work the single exposure is made with a 6% attenuated 180˚ phase mask with a numerical aperture of 1.2, and an ASML-type cross-quad illuminator shape is used with x-y Azimuthal-like polarization optimized for the x and y oriented pitches using $\sigma_{xCenter}$=0.27 and $\sigma_{yCenter}$=0.89 with a σ_{Width}=0.15. Typically these studies are made by comparing critical dimension (CD) tolerance for ±10% CD control with no thought of what is actually required to make a functioning. Here, we will look at the problem more globally. Referring to Figure 10 as poly traverses diffusion nearest the end, the CD_{Taper}, is typically narrower than the "inner" poly, the CD_{Inner}, at the other edge of the diffusion area. For this work we allowe the CD_{Inner} to range from 29 nm to 35 nm and then seek to maximize the CD_{Taper} without scumming the resist between the opposing poly ends by setting the CD of the gap between these ends, the CD_{Gap}, to be 45 nm ≥ CD_{Gap} ≥ 10 nm while at the same time maximizing the ratio of the CD_{Taper} to CD_{Inner}. With these criteria for our boundaries we examine the imaging potential of IAL compared to the single exposure imaging process.

Critical Dimension (CD) Target:

CD	Minimum	Maximum
Gap	10 nm	45 nm
Inner	22 nm	27 nm
Middle	22.5 nm	27.5 nm
Taper	10 nm	35 nm

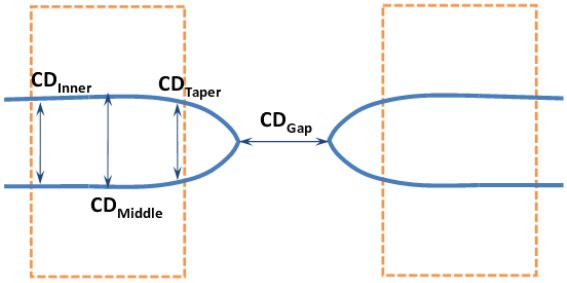
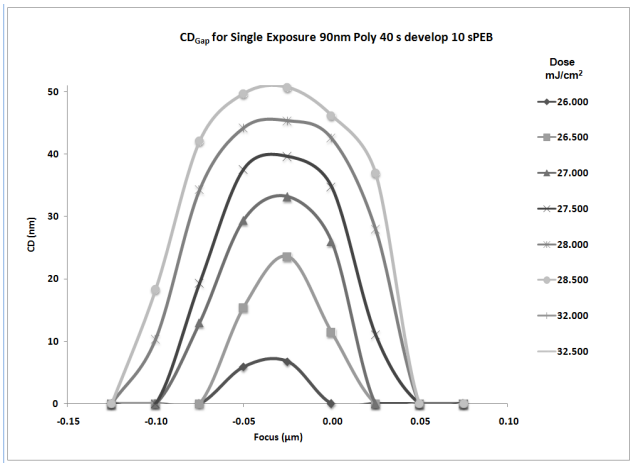


Figure 10. Diagram of critical dimension boundary conditions. Whichever CD boundary is first encountered constrains the overall process window.

The single exposure reference and the IAL CD_{Gap} imaging results are shown in Figure 11 and the CD_{Taper} results are shown in Figure 12. These results are compiled and shown graphically in Figure 13. In the region of a target CD_{Gap} of 30 nm, IAL process has 1.7 times the exposure latitude at 0.10 µm Depth of Focus (DoF) and 2.5 times the maximum DoF compared to the single exposure reference process. As shown in Figure 13, for the same minimum allowed CD_{Taper}, IAL provides significantly overall greater focus and exposure tolerance compared to the single exposure process. Poly line end tapering effect is the most important factor limiting the overall process window of IAL. To mitigate the impact of this tapering effect on device performance, we can increase the poly line-end extension in the SRAM bitcell design, which may result in a somewhat larger bitcell size. Another way to reduce this line-end tapering effect is to implement IAL in a double pattern process, which is the subject of another paper at SPIE Advanced Lithography 2009 [17].



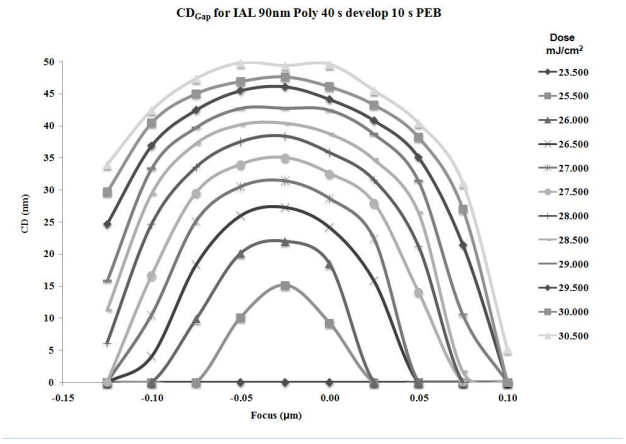


Figure 11: Focus-Exposure results for the reference single exposure process and IAL for CD_{Gap}.

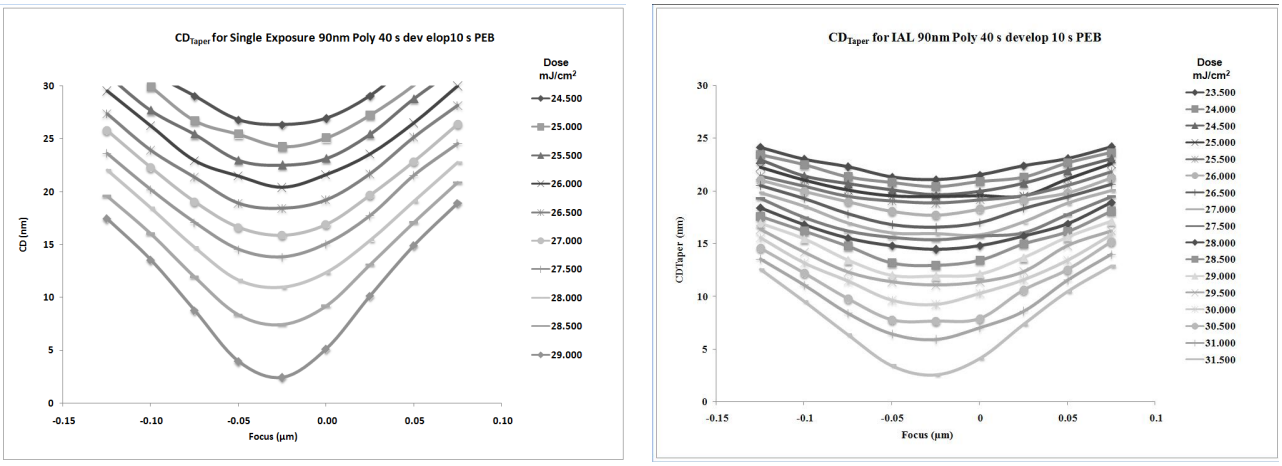


Figure 12: Focus-Exposure results for the reference single exposure process and IAL for CD_{Taper}.

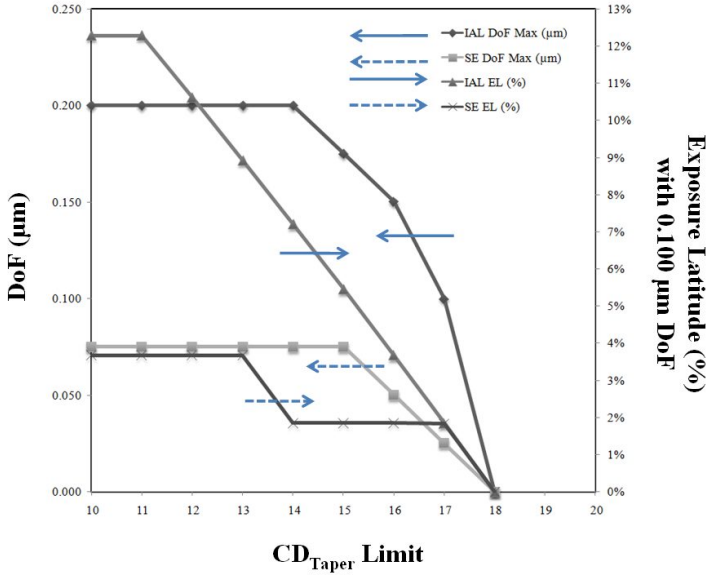


Figure 13: Process window for IAL and the reference single exposure process depending on the minimum allowable CD_{Taper}.

4. CONCLUSIONS

We present Interference Assisted Lithography (IAL) as a promising cost-effective next-generation lithography solution. The implementation of IAL requires the circuit to have 1D regular-pitch gridded design. We propose a family of IAL-friendly SRAM bitcell designs following such 1D regular-pitch gridded design rules. Through circuit and lithography simulations, we confirm that the electrical characteristics of the proposed bitcell design are comparable to existing 2D bitcell design and the proposed bitcell layouts can be successfully printed with IAL. Furthermore, lithography simulations indicate that IAL has a larger process window compared to the single exposure reference process for the patterning of a 90nm-pitch SRAM poly gate layer.

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REFERENCES

1) M. Fritze, T. M. Bloomstein, B. Tyrrell, T. H. Fedynyshyn, N. N. Efremow, D. E. Hardy, S. Cann, D. Lennon, S. Spector and M. Rothschild, "Hybrid Optical Maskless Lithography: Scaling beyond The 45nm Node", *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, **23**(6), 2743–2748 (2005).
2) M. Fritze, B. Tyrrel, T. Fedynyshyn and M. Rothschild, "High-Throughput Hybrid Optical Maskless Lithography: All-Optical 32-nm Node Imaging", *Proc. SPIE Emerging Lithographic Technologies*, **5751**, 1058-1068 (2005).
3) Robert T. Greenway, Kwangok Jeong, Andrew B. Kahng, Chul-Hong Park, John S. Petersen, "32nm 1-D Regular Pitch SRAM Bit-cell Design for Interference Assisted Lithography", *Proc. SPIE*, Vol. **7122**, 71221L (2008)
4) Michael C. Smayling, Christopher Bencher, Hao D. Chen, Huixiong Dai, Michael P. Duane, "APF pitch halving for 22nm logic cells using gridded design rules", *Proc. SPIE*, Vol. **6925**, 69251E (2008)
5) W. Hinsberg, F. A. Houle, J. Hoffnagle, M. Sanchez, G. Wallraff, M. Morrison, and S. Frank, "Deep-ultraviolet interferometric lithography as a tool for assessment of chemically amplified photoresist performance", *Journal of Vacuum Science & Technology B,* Vol. **16**(6), 3689-3694 (1998).
6) Michael C. Smayling, Hua-yu Liu, Lynn Cai, "Low k_1 logic design using gridded design rules", *Proc. SPIE*, Vol. **6925**, 69250B (2008)
7) Clair Webb, "45nm design for manufacturing", *Intel Technology Journal* , Vol. **12** (02), pp. 121-130 (2008)
8) W. Arnold, "Lithography for the 32nm Technology Node," IEDM 32nm Technology Short Course (2006).
9) M. C. Smayling, H. Y. Liu, L. Cai, "Low k_1 logic design using gridded design rules," *Proc. of SPIE*, Vol. **6925** (2008).
10) B.J. Lin, "Immersion lithography and its impact on semiconductor manufacturing," *Proc. of SPIE*, Vol. **5377** (2004).
11) M. C. Smayling, "Gridded Design Rules – 1-D Design Enables Scaling of CMOS Logic," *Nanochip Technology Journal*, Vol. **6**(2), (2008).
12) M. Smayling, "Cell-based aerial image analysis of design styles for 45 nanometer generation logic," *Proc. of SPIE*, Vol. **6521** (2007).
13) T. W. Houston, R. A. Soper, T. J. Aton, "Double pattern and etch of poly with hard mask," US Patent 6,787,469 (2004).
14) S. Verhaegen, S. Cosemans, M. Dusa, P. Marchal, A. Nackaerts, G. Vandenberghe andW. Dehaene, "Litho Variations and Their Impact on the Electrical Yield of a 32nm Node 6T SRAM Cell", *Proc. SPIE Design for Manufacturability through Design-Process Integration II*, **6925** (2008), pp. 69250R-1–69250R-12.
15) *International Technology Roadmap for Semiconductors*, http://public.itrs.net/.
16) J. S. Petersen, M. J. Maslow and R. T. Greenway, "An Integrated Imaging System for the 45-nm Technology Node Contact Holes Using Polarized OAI, Immersion Weak PSM and Negative Resists", *Proc. SPIE Optical Microlithography XVIII*, **5754** (2005), pp. 488-497.
17) J. S. Petersen, R. T. Greenway, T. Fühner, P. Evanschitzky, F. Shao, A. Erdmann, "Exploration of linear and nonlinear double-exposure techniques by simulation," Paper 7274-67 of SPIE Advanced Lithography Conference, February 26th, 2009, 5:30 PM.