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Interference lithographically defined and catalytically etched, large-area silicon nanocones from nanowires

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Abstract
We report a simple and cost effective method for the synthesis of large-area, precisely located silicon nanocones from nanowires. The nanowires were obtained from our interference lithography and catalytic etching (IL-CE) method. We found that porous silicon was formed near the Au catalyst during the fabrication of the nanowires. The porous silicon exhibited enhanced oxidation ability when exposed to atmospheric conditions or in wet oxidation ambient. Very well located nanocones with uniform sharpness resulted when these oxidized nanowires were etched in 10% HF. Nanocones of different heights were obtained by varying the doping concentration of the silicon wafers. We believe this is a novel method of producing large-area, low cost, well defined nanocones from nanowires both in terms of the control of location and shape of the nanocones. A wide range of potential applications of the nanocone array can be found as a master copy for nanoimprinted polymer substrates for possible biomedical research; as a candidate for making sharp probes for scanning probe nanolithography; or as a building block for field emitting tips or photodetectors in electronic/optoelectronic applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

A phenomenal amount of interest has been devoted to the exploration of the potentials of nanostructures for future electronic, optoelectronic, and biomedical devices and systems. For example, silicon nanowires have been successfully implemented in metal–oxide–semiconductor field-effect transistors (MOSFETs) [1], chemical sensors [2], and solar cells [3]. On the other hand, fin-like structures have been suggested to be ideal for sensors as the higher surface-to-volume ratios should result in higher efficiencies for sensing applications. Nanofins are also of great interest for use in MOSFETs since the channel current can be more readily controlled than in planar structures, i.e. fin-FET devices [4, 5]. Most recently, there has been growing interest in synthesizing nanocones and in their application as field emitters [6], electromagnetic sensors [7], fuel cells [8], and probes for scanning probe microscopy [9].

We have recently reported a novel method [10] that makes use of the interference lithography [11] and the catalytic etching (also known as metal-assisted etching) [12] technique, i.e. the IL-CE method, to create precisely shaped nanostructures without resorting to complicated lithography (e.g. e-beam lithography) and etching (e.g. deep reactive ion etching) techniques. We are able to create nanostructures that are perfectly periodic over a very large area (2 cm^2 or more) where the cross-sectional shapes and the array ordering can be varied. We can also readily and independently control the sizes

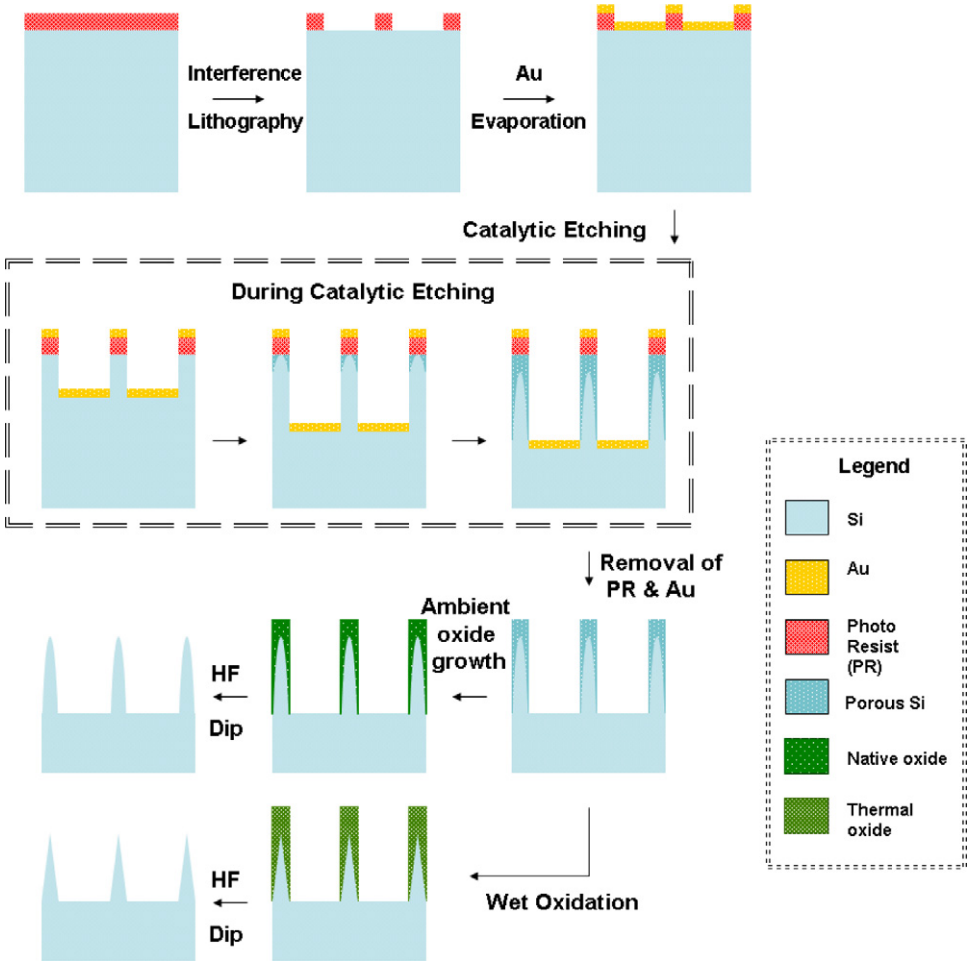

Figure 1. Schematic diagram showing the process flow in obtaining silicon nanocones from nanowires via the IL-CE method. Note that the bending of nanowires is not illustrated in this schematic diagram.

and spacing of the nanostructures down to spacings of 200 nm or less.

In this paper, we describe a novel technique to synthesize a large area of precisely located silicon nanocones with well-controlled geometry on silicon substrate by exploiting the enhanced oxidation characteristics of porous silicon found in silicon nanowires prepared from the IL-CE method.

2. Experimental details

The basic process steps of the IL-CE method can be summarized schematically as shown in figure 1. N-type (100) silicon wafers (resistivity 10 Ω cm) were coated with a layer of photoresist (Ultra-i 123) approximately 400 nm thick, and cured at 90 °C for 90 s. The photoresist was then exposed using a Lloyd's-mirror-type interference lithography set-up [13] with a HeCd laser source ($\lambda = 325$ nm). Exposure of the photoresist with a periodic square array was achieved by two perpendicular exposures of ∼40 s to 1 min each. The unexposed photoresist was then removed using Microposit MF CD-26 developer[4]. Due to the two exposures, circular-shape photoresist dots were left behind on the silicon wafer surface. The samples were subjected to an oxygen plasma etch (power of 30 W, oxygen pressure of 0.5 mbar, etching time of 30–120 s) to remove the residual unexposed photoresist at the silicon interface. Gold was thermally evaporated on the substrate to a thickness of ∼25 nm at a pressure of 10^{-6} Torr. The samples were then etched in a solution of H_2O, HF, and H_2O_2 at room temperature with the concentrations of HF and H_2O_2 fixed at 4.6 and 0.44 M, respectively. The gold was then removed using a standard gold etchant. By carefully controlling the etching duration, straight or bent nanowires can be obtained. Note that figure 1 shows that during catalytic etching, porous silicon will result at the surface of the nanowires. A further oxidation in ambient or by wet oxidation of such nanowires followed by wet etching in 10% HF solution, resulted in a large area, precisely located and of well-controlled geometry and size, of nanocones on the silicon surface. The mechanism and formation of these nanocones will be discussed in detail in the following paragraphs.

[4] Microposit MF CD-26 Developer, Manufactured by Shipley Company, Marlborough, Massachusetts 01752.

3. Results and discussion

Figure 2 shows the scanning electron micrograph (SEM) images of silicon nanowires that had been etched with exactly

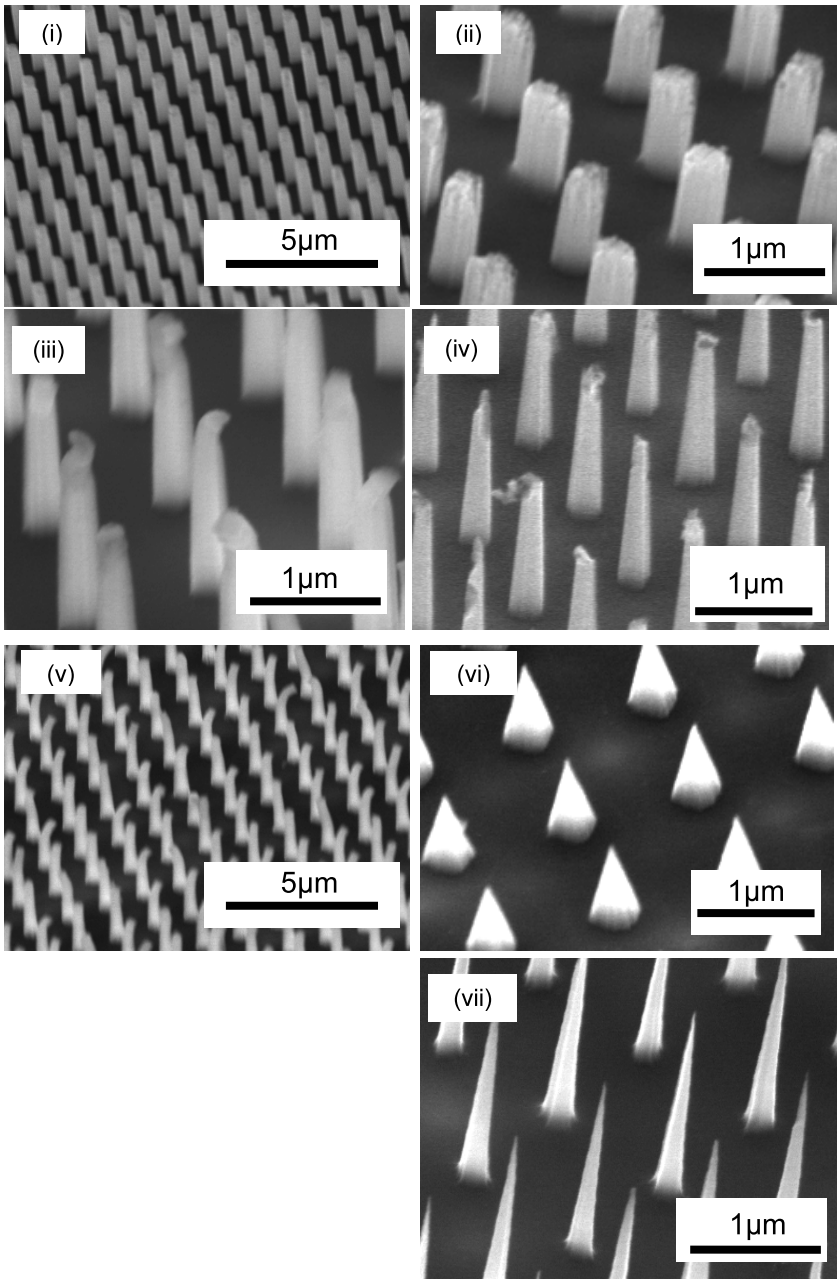

Figure 2. SEM images of large-area, precisely located (i) straight, (iii) top-bent, and (v) severely bent silicon nanowires that were etched in a mixed solution of H_2O, HF, and H_2O_2 at room temperature, respectively. SEM images (ii), (iv), and (vi) show the different shapes of nanostructures after etching silicon nanowires in 10% HF solution for 1 min at room temperature. SEM image (vii) shows silicon nanocones produced by an additional wet thermal oxidation and HF etching of the top-bent nanowires in (iii).

the same etching conditions except with different etching durations that resulted in (i) straight ($\sim$1.70 μm), (iii) top-bent ($\sim$1.80 μm), and (v) severely bent ($\sim$2.00 μm) nanowires. SEM images (ii), (iv), and (iv) show the respective silicon nanowires after being etched again in 10% HF for 1 min. The different degree of bending of nanowires may be linked to the different degree of porosity of these nanowires. This will be further discussed when we examine the oxidation process of the nanowires.

In a similar experiment, a pure silicon wafer and a silicon wafer partially covered with 25 nm of gold (see schematic in figure 3) were etched in the same mixed solution of H_2O, HF, and H_2O_2 at room temperature for 10 min, and the results are shown in figure 3. It can be seen from this figure that for the silicon wafer that is partially covered with a gold layer, the etching process has resulted in silicon with different surface conditions. The silicon underneath the gold layer (located at region (i)) is covered with numerous small pores; followed by a much rougher silicon surface with larger pores located at region (ii) ($\sim$200 μm from the edge of the gold layer). At region (iii) ($\sim$1 mm from the edge of the gold layer), the silicon surface is smoother and resembles that of a pure silicon wafer (see (iv)) that was etched together in the mixed solution of H_2O, HF, and H_2O_2. This shows that the presence of the gold

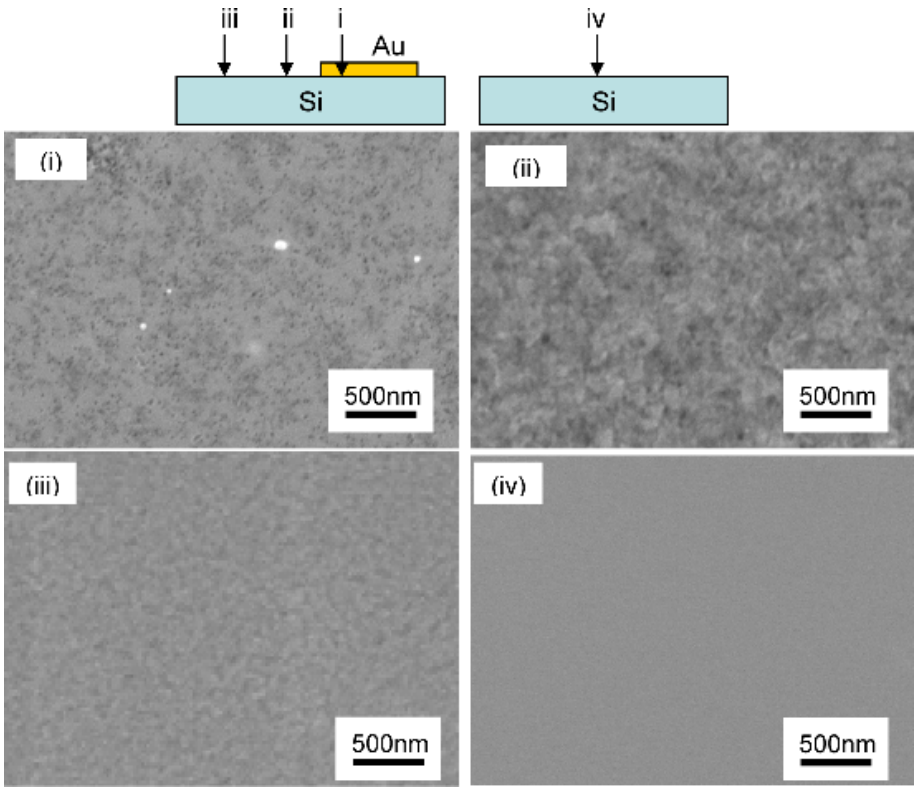

Figure 3. SEM images of a silicon wafer partially covered with an Au layer and a pure silicon wafer that were etched in H_2O, HF, and H_2O_2 at room temperature. Note that images (i)–(iii) refer to results obtained from silicon wafers partially covered with an Au layer and image (iv) is from a pure silicon wafer as defined by the schematic at the top of this figure.

catalyst facilitates an etching process on silicon in the vicinity of the catalyst.

Tsujino and Matsumura [14] have reported the formation of a porous layer at the silicon surface within several hundred nm from the metal catalyst when a silicon wafer was catalytically etched in HF and H_2O_2. Li and Bohn [15] have also reported on the formation of porous silicon adjacent to a gold or platinum metal coating when silicon is etched in a mixed solution of HF and H_2O_2. It was suggested that during catalytic etching, holes are injected into silicon through the metal/silicon interface and the holes are attracted near the catalyst due to the electrostatic force induced by them and this causes the etching of silicon. However, when many positive holes are injected, i.e. etched in high concentration of H_2O_2, some of them escape from the electrostatic force and this leads to lateral transport of charge carriers to silicon in the vicinity of the metal catalyst [14]. This is responsible for the generation of the porous silicon in the vicinity of the catalyst, as shown in region (ii), of figure 3. The smoother surface at region (iii) may be a consequence of the fact that it is not possible for the lateral transport of significant numbers of holes to this region. Based on the results from figure 3 and the mechanism described above, we suggest that during the formation of silicon nanowires by catalytic etching, as the catalytic etching duration increases, the top part of the nanowire would be more porous compared to the lower part because the top part would have been exposed to the etchant for a longer period of time.

Figure 4 shows the corresponding room temperature photoluminescence characteristics of the nanowires described in figure 2. Note that the straight and top-bent nanowires exhibit some photoluminescence signal (at ∼650 nm) as compared to bulk silicon wafer. The severely bent nanowires, however, give rise to a stronger photoluminescence signal than the straight and top-bent nanowires. As mentioned earlier, the surface of the nanowires was porous, and thus the origin of the photoluminescence observed here can be due to the 'porous

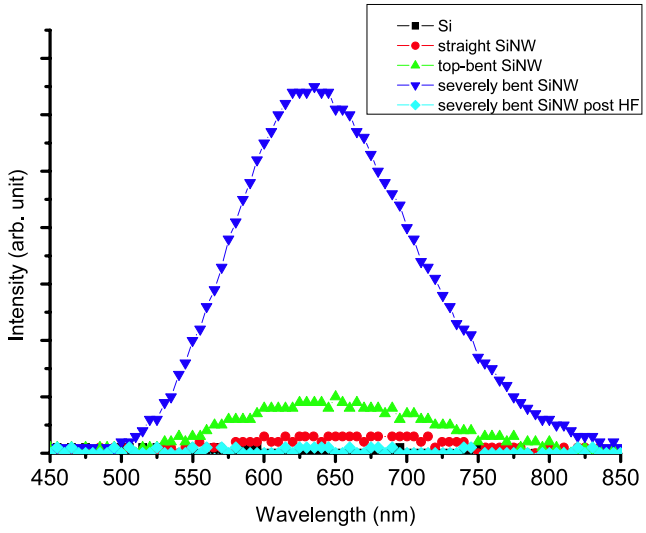

Figure 4. Photoluminescence characteristics of silicon nanowires obtained from the catalytic etching of silicon with Au catalyst in a mixed solution of H_2O, HF, and H_2O_2 at room temperature.

Table 1. The change in nanowire height and the estimated change in nanowire volume after the nanowires were etched in 10% HF solution for 1 min at room temperature.

Type of nanowires	Diameter (nm)	Initial height (μm)	Height after HF etch (μm)	Volume reduction (μm^3)	Change in volume (%)
Straight	400	1.70	1.50	2.51×10^{-2}	10
Top-bent	260	1.80	1.40	7.08×10^{-2}	74
Severely bent	490	2.00	1.00	3.1×10^{-1}	86

silicon' at the nanowire surface. However, one would expect a shift in the photoluminescence peak as the porosity of silicon changes, as pointed out by Wolkin *et al* [16]. As a matter of fact, Wolkin *et al* have shown conclusively that the origin of the photoluminescence (at ∼650 nm) observed from porous silicon samples, prepared by anodic etching of silicon in HF, was due to oxygen-related defects at the porous silicon–silicon oxide interface.

We performed another set of photoluminescence experiments by dipping the silicon nanowires in 10% HF solution for 1 min after the first set of photoluminescence experiments was completed. It is very interesting to note that the photoluminescence peak at ∼650 nm could no longer be observed from all straight, top-bent or severely bent nanowires. Etching the nanowires in HF would have removed all the native oxide present on the nanowire's surface. This convincingly shows us that the origin for the photoluminescence observed in our nanowires was due to oxide-related defects at the silicon nanowire surface, as suggested by Wolkin *et al*.

As mentioned earlier, figures 2(ii), (iv), and (vi) show SEM images of silicon nanowires after being etched again in 10% HF for 1 min. Table 1 summarizes the change in volume of the nanowires as a result of etching in 10% HF solution. The percentage change in volume was arrived at by dividing the change of nanowire volume (i.e. by subtracting the final volume from the initial volume) by the initial volume of the nanowires. Note that the straight nanowires remained straight after etching in 10% HF, and have a reduction of nanowire height from ∼1.7 to 1.5 μm, giving rise to a 10% change in volume with the oxide removed. The top-bent and severely bent nanowires had a reduction of height from 1.80 to 1.4 μm, and 2.00 to 1.00 μm, respectively. This leads to a 74% and 86% volume reduction when the nanowires were etched in 10% HF solution. The top-bent nanowires give rise to silicon nanocones after the oxide at the silicon surface was removed. Note that a large number of these nanocones exhibit 'blunt' tips. The removal of a significant amount of oxide from severely bent nanowires resulted in silicon nanocones with sharp tips.

Figure 2(vii) shows an SEM image of top-bent nanowires that have gone through a further wet thermal oxidation process at 900 °C for 35 min and then etched in 10% HF solution. It can be seen from this figure that significantly sharper nanocones have been obtained by the extra wet thermal oxidation process. Therefore, we are able to vary the geometry of the silicon nanocones by manipulating the amount of silicon oxide grown on the silicon nanowire surface.

The results from figure 2 suggest that all the nanowires obtained from the IL-CE method contained silicon oxide after exposure to atmospheric ambient. Figure 1 schematically illustrates how we obtained sharp silicon nanocones from nanowires. We assume here that the removal of silicon oxide from the silicon nanowires is complete while immersed in the mixed solution of H_2O, HF, and H_2O_2. Therefore, the oxide formed after the nanowires had been exposed to air must be due to a reaction from ambient oxygen to the porous silicon at the surface of the nanowires. The porous silicon will oxidize rapidly as the sponge-like structure [17] consists of a large number of pores resulting in a large surface area for rapid oxidation [16]. It also means that the region with the highest degree of porosity was found to be at the bending portion of the severely bent nanowires, in agreement with our earlier suggestion. The non-uniform distribution of porous silicon along the length of the nanowire and its subsequent oxidation in ambient conditions results in the residual nanocone. By performing a controlled oxidation step for the top-bent nanowires, more silicon is consumed at the top portion of the nanowires, forming even sharper nanocones compared to those obtained from ambient oxidation.

Hochbaum *et al* [18] have recently examined the structure of single crystalline mesoporous silicon nanowires obtained by etching p-type silicon wafers in a solution consisting of $AgNO_3$ and HF. They have observed an increase in the surface roughness of the nanowires as the resistivity of three silicon wafers changed from 10, 0.1 to 0.005 Ω cm. As our results above were all obtained from n-type silicon of resistivity 10 Ω cm, we selected p-type silicon wafers of resistivity of 10, 0.1 Ω cm as well as n-type 0.1 Ω cm silicon to determine the influence of dopant type and concentration for the creation of nanocones. The preparation procedures were exactly the same as shown in figure 1 and the SEM images of the as-prepared nanowires and the nanocones (i.e. after oxidation and HF etch) are shown in figures 5(i), (iii), (v) and (ii), (iv), (vi), respectively. It should be noted that with a lower resistivity silicon wafer, the as-prepared nanowires are of comparable height to those obtained from a silicon wafer of 10 Ω cm (by exploiting a shorter etch duration), but resulted in shorter nanocones when oxidized and etched in HF. This is in agreement with the results of Hochbaum *et al* in that our lower resistivity wafer would have given rise to more porous silicon nanowires and then resulted in shorter nanocones when oxidized and etched in HF. Our results also indicate that obtaining nanocones using our method is independent of doping type.

We have carried out another experiment by thermally evaporating 2 nm of gold on an n-type silicon wafer with a resistivity of 10 Ω cm. As the film is very thin, it is composed of gold islands. We then performed catalytic etching for two different etching durations, 4 and 20 min. Figures 6(i) and (ii) are SEM images of the as-etched silicon surface. Regions covered by gold would be etched and leave behind a network of silicon nanowires with varying sizes. Due to the capillary effect, clumping of the nanowires is observed. Figures 6(iii) and (iv) show the silicon surface after a similar wet oxidation and HF etch mentioned earlier. A shorter etch duration does not

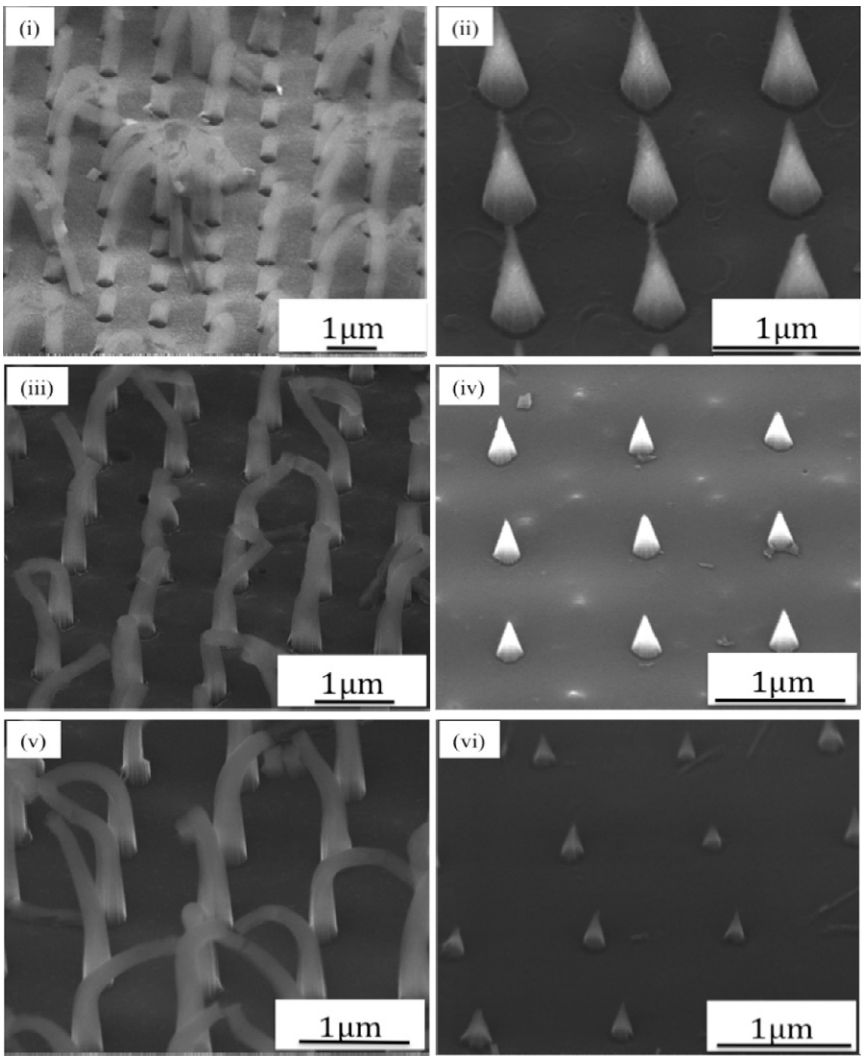

Figure 5. The SEM images of as-etched nanowires with (i) p-type silicon with resistivity 10 Ω cm, (iii) p-type silicon with a lower resistivity of 0.1 Ω cm, and (v) n-type silicon with resistivity 0.1 Ω cm. SEM images of the respective nanocones obtained by wet thermal oxidation and HF etch of the nanowires are shown in (ii), (iv), and (vi) respectively.

result in significant porous silicon formation, therefore only the surface of the nanowires will be oxidized and etched away in HF, causing a thinning in the nanowires.

As observed from figure 6(iv), conical structures were obtained by exploiting a longer etching duration. This is in agreement with our earlier statement that as catalytic etching takes place, the nanowires become more porous. A longer etch duration will result in more porous silicon formation, and leave behind nanocones after oxidation and HF etch. The resulting networks of nanocones have varying heights, and are randomly located. Though nanocones can also be obtained by a simple thin metal deposition followed by catalytic etching, oxidation, and HF etch as mentioned above, there is no control in terms of location and geometry of the nanocones obtained. The above experiment does, however, verify the mechanism in which we obtain our precisely located and geometrically controlled nanocones.

There are a few reports on the synthesis of silicon nanocones using different methods. For examples, Bae *et al* synthesized silicon nanocones via the vapour–liquid–solid method using Ga and Al catalysts [19], Yang *et al* synthesized silicon nanocones on Fe-coated crystalline silicon using radiofrequency (RF) microplasma in air [20], Tsuji *et al* fabricated silicon nanocones using agglomeration in the $Si/CoSi_2/Si$ double heteroepitaxial structure [21]. It should be noted that there is really no evidence of spatially well located nanocones being fabricated in all these reports, and the control of the nanocone size seems to be rather difficult to achieve. Hsu *et al* fabricated silicon nanocones via self-assembly of silica nanoparticles followed by careful control of reactive ion etching [22]. Though they are capable of fabricating nanocones over a wide area, the presence of domains and grains due to the self-assembly process makes it impossible to achieve ordering over a very large area as compared to our results shown in figure 2. Furthermore, the synthesis methods in the above examples are much more complicated and costly compared to our process.

The nanocone array we fabricated, paves the way for a wide variety of interesting applications. Due to the positional control we are capable of achieving, our nanocones are ideal

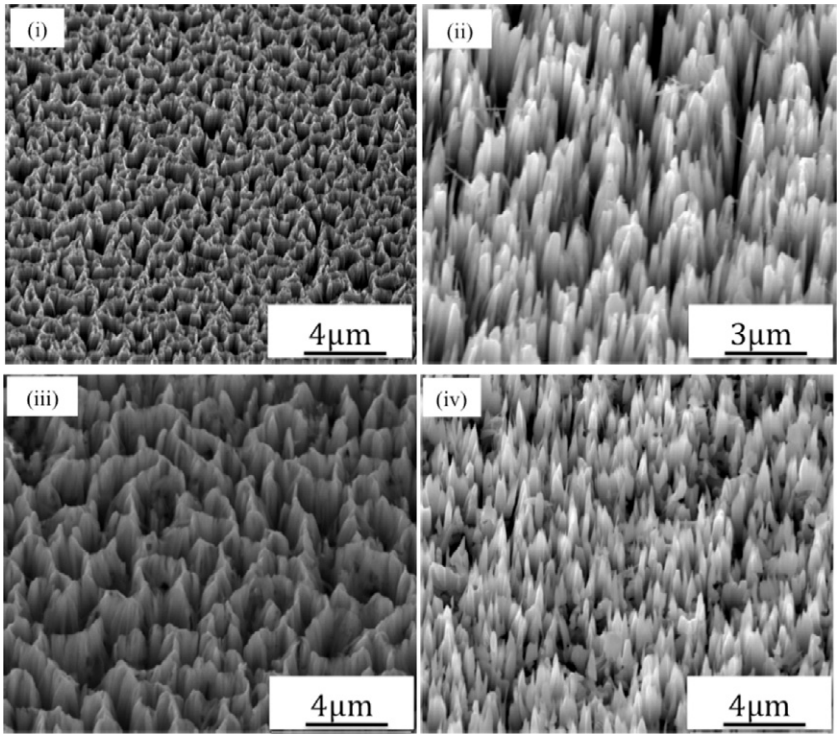

Figure 6. SEM images of 2 nm gold evaporated on silicon and catalytically etched for (i) 4 min and (iii) 20 min. (ii) and (iv) are SEM images of the respective nanowires in (i) and (iii) after a further wet oxidation and HF etch.

in applications where location, position, and uniformity are important. For example, the nanocones can be used as a master for nanoimprinting on polymer substrates. These polymer substrates can then be treated as a platform for biomedical research. Nanocones can also function as probes for scanning probe nanolithography [23]. Finally, our large-area array of nanocones can be exploited in applications that require field emission [6] or as photodetectors as suggested by Zhu *et al* [24].

4. Conclusion

In conclusion, we show that by using our IL-CE method to synthesize Si nanowires using a gold catalyst, significant etching of silicon near the catalyst resulted in porous silicon at the top part of the nanowire surface. The porous silicon resulted in an enhanced oxidation of the nanowires when exposed to atmospheric ambient or in wet oxidation ambient. Very well located nanocones with uniform sharpness resulted when these oxidized nanowires were etched in 10% HF. By varying the resistivity of the silicon wafer, the height of the nanocone can be controlled. Our results show that the formation of nanocones using our method is independent of dopant type. The origin of the photoluminescence observed from such nanowires is due to oxide defects. We believe this is the first report of a novel method of producing large-area, low cost, well defined nanocones from nanowires both in terms of the control of location and shape of the nanocones. The nanocones would be of interest to researchers working in fields ranging from biomedical, nanolithography to electronics or optoelectronics.

Acknowledgments

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