Interleaved High Step-Up Converter With Coupled Inductor and Voltage Multiplier for Renewable Energy System

Xing Liu, Xiao Zhang, Xuefeng Hu, Hao Chen, Lezhu Chen, and Yujia Zhang

***Abstract*—The concepts of dual coupled inductors and voltage multiplier cell are integrated to derive a novel non-isolated interleaved high step-up boost converter in this paper. At the input, due to the interleaved dual coupled inductors and voltage multiplier cell, the converter inhibits current ripple and reduced voltage stress for the power devices; At the output, the secondary sides of the two coupled inductors are connected in series to achieve the purpose of much higher voltage gain and lower voltage stress on the power devices. Therefore, lower voltage rating MOSFETs and diodes can be selected to reduce both switching and conduction losses. In addition, the leakage inductance energy of two coupled inductors can be absorbed and recycled to the output, and the reverse-recovery problem of diodes can be effectively suppressed. Zero current switching (ZCS) turn-on is realized for the power switches to reduce the switching loss. The working principle and steady-state characteristics of the converter are analyzed in detail. The voltage balance of the output capacitors and input current sharing by two interleaved phases are realized through the double closed-loop control of voltage and current. Finally, a 400 W laboratory prototype with 25~30 V input and 400 V output is built to verify the significant improvements of the proposed converter.**

***Index Terms*—Coupled inductor, high voltage gain, interleaved, voltage multiplier cell.**

I. Introduction

In recent years, there are increasing demand of high voltage gain DC-DC converters, which have been widely employed in some fields of industries, such as photovoltaic (PV) generation systems, fuel cells (FC) systems, hybrid electric vehicles, energy storage systems, and DC distribution systems[1]–[17]. Generally, the output voltages of the PV cells and FC cells are low, which need to be stepped up to higher levels by high step-up DC/DC converters for meeting the requirement of potential application. Fig. 1 shows a typical renewable energy system.

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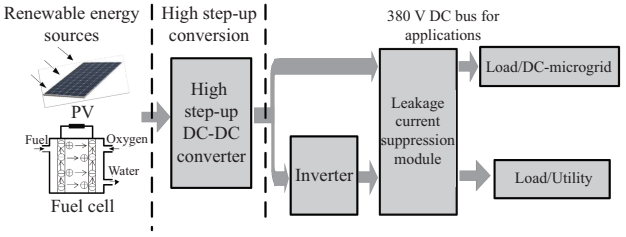


Fig. 1. Typical renewable energy system.

Generally, in some isolated converters such as flyback, half-bridge and full-bridge converters, the high voltage gain can be achieved by increasing turns ratio of the isolated transformer and the duty cycle of active switches. However, this method for high voltage gain will result in disadvantages of high voltage/current stress of power switches, large weight and size, and low efficiency [6]–[9]. So, non-isolated structures are recommended where isolation is not necessary. The traditional boost converter can achieve high voltage gain by increasing the duty cycle of the main switch. In fact, an extremely duty cycle will lead to the reverse recovery of output diode, electro magnetic interference(EMI),large current ripple and low efficiency. Switched-capacitor technology is applied in some converters to achieve high conversion ratio [10]–[13]. However, the switched-capacitor circuit often requires lots of active switches, and the active switches will also suffer instantaneous large current, increasing conduction loss. In the references [14]–[16], the switched-inductor technology has been combined with basic boost converters for obtaining the high voltage gain, but the voltage value across the power switch is still high, causing serious conduction losses. At the same time, the input current ripples are also large, which affects the lifetime of input dc sources.

The basic interleaved boost has advantages of low input current ripple, compact magnetic elements, and high power handling capability. However, the voltage gain of the conventional interleaved boost converter is only determined by the duty ratio. In practical application, the voltage gain is limited to five times due to the influence of parasitic parameters of some components. Some high gain interleaved boost converters were successfully developed by combining the coupled inductors with switched capacitors for renewable energy power system [1]–[7], [15]–[25].

In this paper, a novel interleaved boost converter with high step-up is proposed, in which the primary sides of coupled inductors are connected in parallel and the secondary sides of

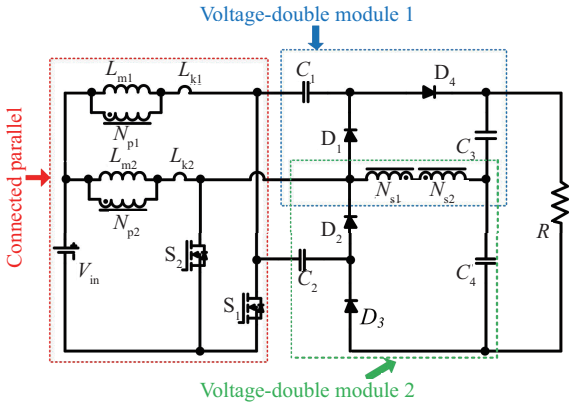


Fig. 2. The topology of the proposed converter.

coupled inductors are connected in series . In addition, voltage multiplier techniques that integrate coupled inductor and diode-capacitor are also used for higher voltage gain and lower voltage stress on power devices. The topology of the proposed converter is shown in Fig. 2.

II. Operating Principles of Proposed Converter

To simplify the circuit analysis, the assumptions are made as follows:

(a) All the power semiconductors and energy storage components are ideal, which means the on-state resistances of power semiconductors, the forward voltage drop of the diodes, and the equivalent series resistances (ESRs) of the inductors and capacitors are ignored.

(b) All the capacitances are large enough, and each capacitor voltage can be treated as constant.

(c) The relationship between d_1 and d_2 can be written as $d_1 = d_2 = d$, where d_1 and d_2 are the duty cycles of S_1 and S_2 respectively.

(d) The phase difference between the gate driving signals of S_1 and S_2 is 180°, and the operating duty cycle is not be lower than 0. 5.

In a switching cycle, when there is always current flowing through L_{m1} and L_{m2}, the proposed converter operates in the continuous conduction mode (CCM), and when the current flowing through L_{m1} and L_{m2} is zero for a period of time, the proposed converter operates in discontinuous conduction mode (DCM).

According to the operation of S_1 and S_2, when the proposed converter operates in CCM, there are eight operated modes. Fig. 3 represents several key theoretical waveforms during a switching period. And Fig. 4 represents the equivalent circuits of the converter in different modes.

Mode I [t_0~t_1] At the time of t_0, the main switch S_1 is switched on, the switch S_2 maintains the state of conducting. The equivalent circuit is shown in Fig. 4(a). Because the current of the inductor can't be changed suddenly, the diode D_4 is still on. The current through the diode D_4 decreases gradually. When the current i_{D4} is reduced to zero, the diode D_4 is turned off under ZCS condition, and this mode ends.

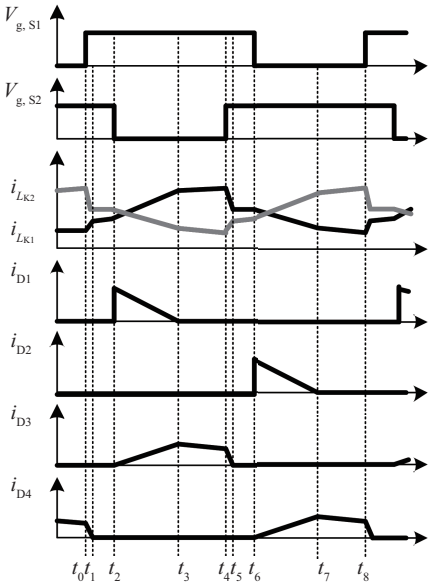


Fig. 3. Key waveforms of one cycle at CCM operation.

Mode II [t_1~t_2] At the time of t_1, the main switches S_1 and S_2 are switched on. All diodes are reverse biased. The equivalent circuit is shown in Fig. 4(b). During this transition, L_{m1}, L_{m2}, L_{k1} and L_{k2} are charged linearly by input power. The energy of load is provided by the two output capacitors.

Mode III [t_2~t_3] At the time of t_2, the main switch S_2 is switched off, the switch S_1 maintains the state of conducting. Diodes D_1 and D_3 are on, and the equivalent circuit is shown in Fig. 4(c).Part of energy stored in L_{k2} is transferred to C_1 via D_1. The voltage stress of switch is clamped to V_{C1}. The input voltage, coupled inductors and V_{C2} are in series connection to charge the output capacitor C_4, extending the voltage gain of this converter. The current i_{Lk2} begins to decrease. At the same time, the current i_{D_1} is decreased gradually. D_1 is turned off under ZCS condition, and this mode ends.

Mode IV [t_3~t_4] At the time of t_3, D_1 is turned off, as shown in Fig. 4(d). L_{m1} and L_{k1} are charged linearly by the input dc source. C_4 is still charged through L_{m2}, L_{k2} and C_2. The load current is provided by C_3.

Mode V [t_4~t_5] At the time of t_4, the main switch S_2 is switched on and the switch S_1 maintains the on-state. The equivalent circuit is shown in Fig. 4(e). Because the current of the inductor can't be changed suddenly, the diode D_3 is still on. When the current i_{D3} of diode D_3 is reduced to zero, the diode D_3 is turned off under ZCS condition, and this mode ends.

Mode VI [t_5~t_6] At the time of t_5, all diodes are switched off, the equivalent circuit shows in Fig. 4(f). In this mode, the main switches S_1 and S_2 are switched on. The energy of load is provided by the capacitors C_3 and C_4.

Mode VII [t_6~t_7] At the time of t_6, the main switch S_1 is switched off and the main switch S_2 continues to be turned on. The diodes D_2 and D_4 are turned on. The equivalent circuit is shown in Fig. 4(g). Part of energy stored in L_{k1} is transferred

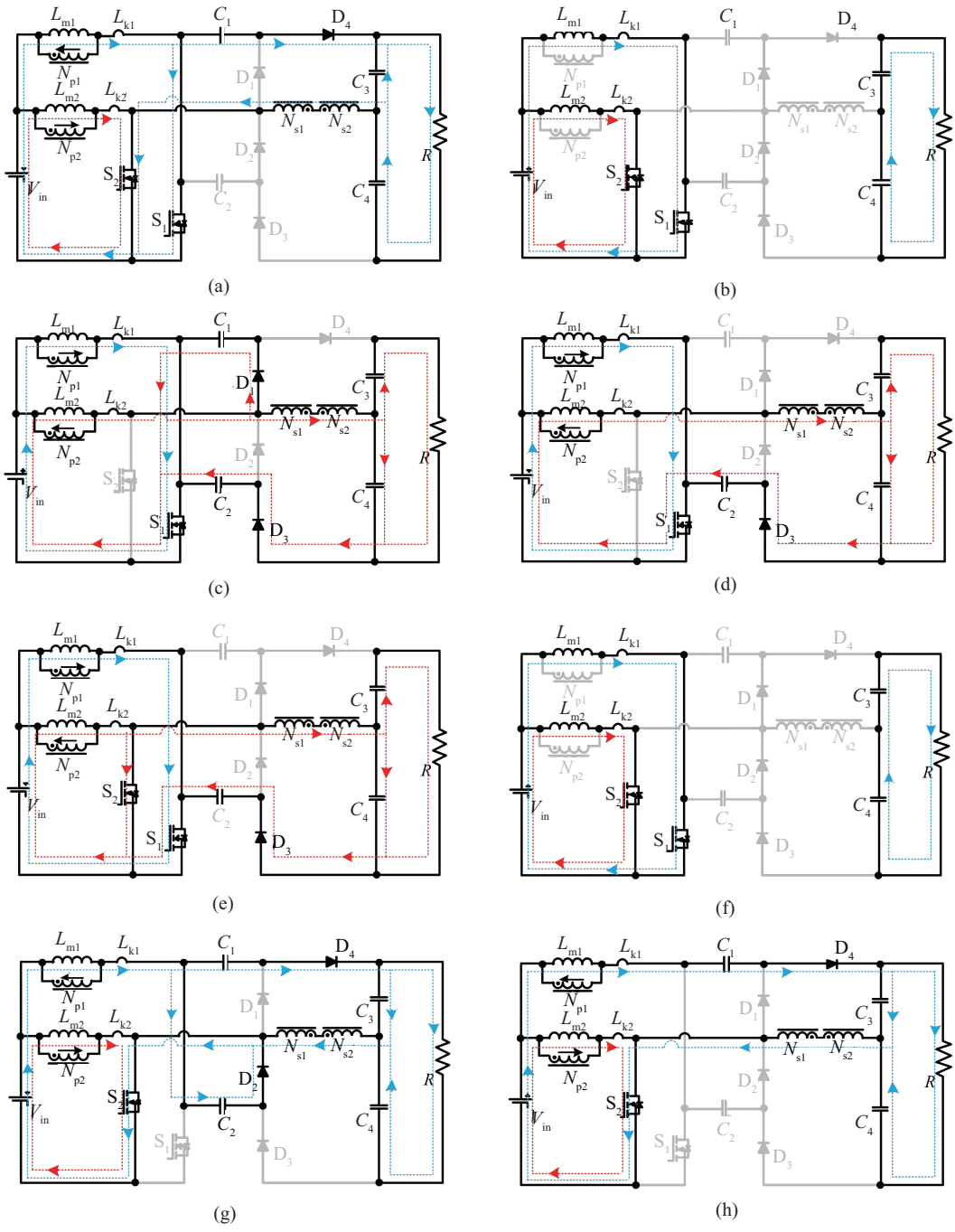


Fig. 4. Equivalent circuits of the proposed converter in different modes.

to C_2 via D_2. The leakage inductor energy is reclaimed by C_2, which can be used to improve the efficiency of the converter. Another part of the energy stored in L_{k1} and the energy stored in C_1 are transferred to C_3 via D_4. The current $i_{L_{k1}}$ begins to decrease. At the same time, the current i_{D_2} is decreased gradually. The current of D_2 drops to zero and it is turned off under ZCS condition, and this mode ends.

Mode VIII [t_7~t_8] At the time of t_7, D_2 is turned off, the equivalent circuit shows in Fig. 4(h). In this mode, L_{m2} and L_{k2} are charged linearly by the input voltage. C_3 is charged by L_{m1}, L_{k1}, and C_1. The load current is provided by C_4.

III. Steady-State Analysis

The characteristics of the proposed converter in CCM operation are analyzed in this section.

A. Voltage Gain

The voltage gain can be obtained by applying the volt-second balance principle of the boost inductor in a switching cycle.

When the switch S_1 is turned on

$$V_{L_{m1}}^{c} \times T_{1_{on}} = V_{L_{m1}}^{disc} \times T_{1_{off}}, \tag{1}$$

where the T_{1on} is the conducting time in one cycle S_1 and the T_{1off} is the turn-off time in one cycle. The $V_{L_{m1}}^{c}$ is the charging voltage of L_{m1} and $V_{L_{m1}}^{disc}$ is the discharging voltage of L_{m1}.

In order to simplify the steady-state analysis, the leakage inductance voltage is neglected. From mode II to mode VI, the voltage of the L_{m1} as in the following equation:

$$V_{L_{m1}}^{c} = V_{in}. \tag{2}$$

By (1) and (2), the voltage of the L_{m1} is

$$V_{L_{m1}}^{disc} = \frac{T_{1on}}{T_{1off}} V_{L_{m1}}^{c} = \frac{d_1}{1-d_1} V_{L_{m1}}^{c} = \frac{d_1}{1-d_1} V_{in}. \tag{3}$$

where d_1 is the duty cycle of switch S_1.

According to the same principle, when the switch S_2 is opened, the voltage of L_{m2} can be obtained as in the following equation:

$$V_{L_{m2}}^{disc} = \frac{T_{2on}}{T_{2off}} V_{L_{m2}}^{c} = \frac{d_2}{1-d_2} V_{L_{m2}}^{c} = \frac{d_2}{1-d_2} V_{in}. \tag{4}$$

The $V_{L_{m2}}^{c}$ is the charging voltage of L_{m2} and $V_{L_{m2}}^{disc}$ is the discharging voltage of L_{m2}.

Where the T_{2on} is the conducting time in one cycle for S_2 and the T_{2off} is the turn-off time in one cycle.

By the mode III, the voltage of the capacitor C_1 can be obtained as in the following equation:

$$V_{C1} = V_{in} + V_{L_{m2}}^{disc} = V_{in} + \frac{d_2}{1-d_2} V_{in} = \frac{1}{1-d_2} V_{in}. \tag{5}$$

Similarly, the expression of the voltage of the capacitor C_2 can be obtained by the mode VII,

$$V_{C2} = V_{in} + V_{L_{m1}}^{disc} = V_{in} + \frac{d_1}{1-d_1} V_{in} = \frac{1}{1-d_1} V_{in}. \tag{6}$$

By mode VIII, the expression of the voltage of the capacitor C_3 can be obtained

$$\begin{aligned} V_{C3} &= V_{in} + V_{L_{m1}}^{disc} + V_{C1} + V_{N_{s1}}^{disc} + V_{N_{s2}}^{c} \\ &= V_{in} + V_{L_{m1}}^{disc} + V_{C1} + nkV_{L_{m1}}^{disc} + nkV_{L_{m2}}^{c}, \end{aligned} \tag{7}$$

where n is the turn ratio, and k is the coupling coefficient of coupled inductor. The $V_{N_{s1}}^{disc}$ is the discharging voltage of N_{s1} and $V_{N_{s2}}^{c}$ is the charging voltage of N_{s2}.

In the same way, the expression of the voltage of the capacitor C_4 can be obtained.

$$\begin{aligned} V_{C4} &= V_{in} + V_{L_{m2}}^{disc} + V_{C2} + V_{N_{s1}}^{c} + V_{N_{s2}}^{disc} \\ &= V_{in} + V_{L_{m2}}^{disc} + V_{C2} + nkV_{L_{m1}}^{c} + nkV_{L_{m2}}^{disc} \end{aligned} \tag{8}$$

Where the $V_{N_{s1}}^{c}$ is the charging voltage of N_{s1} and $V_{N_{s2}}^{disc}$ is the discharging voltage of N_{s2}.

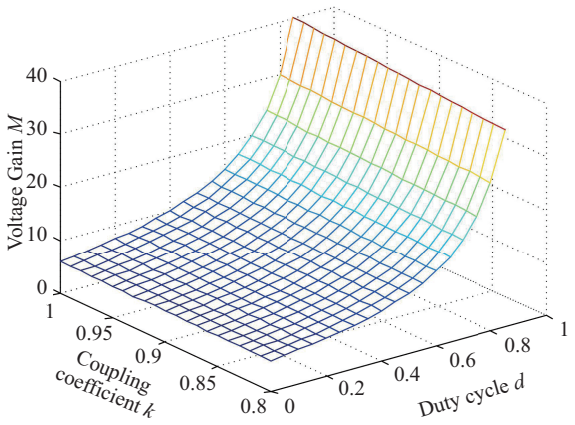


Fig. 5. The relationship between voltage gain, coupled coefficient and duty cycle.

Order $d_1 = d_2 = d$,

$$V_{C3} = V_{C4} = \frac{2+nk}{1-d} V_{in}. \tag{9}$$

According to mode II and mode VI, the expression of the output voltage can be obtained as in the following equations:

$$V_O = V_{C3} + V_{C4} = \frac{4+2nk}{1-d} V_{in}. \tag{10}$$

Therefore, the voltage gain is attained as follow

$$M = \frac{V_O}{V_{in}} = \frac{4+2nk}{1-d}. \tag{11}$$

Fig. 5 shows the relationship between voltage gain, the coupling coefficient, and duty cycle. According to this diagram, it can be seen that the coupled coefficient of the coupling inductor has little effect on the voltage gain. Therefore, in order to simplify the calculation, the coupled coefficient $k = 1$ can be assumed in the theoretical analysis.

B. Voltage Stress of the Semiconductor Devices

In this section, the steady-state analysis of the proposed converter is given. It is assumed that the coupled coefficient k is 1. Based on the operational principle and the results of equals (5)–(11), the voltage stress on the switches S_1, S_2 and diodes D_1~D_4 are derived as

$$V_{S1} = V_{S2} = \frac{1}{1-d} V_{in} = \frac{1}{4+2n} V_O \tag{12}$$

$$V_{D1} = V_{D2} = \frac{2}{1-d} V_{in} = \frac{2}{4+2n} V_O \tag{13}$$

$$V_{D3} = V_{D4} = \frac{2+2n}{1-d} V_{in} = \frac{2+2n}{4+2n} V_O \tag{14}$$

The plot of the normalized diode and switch voltage stress

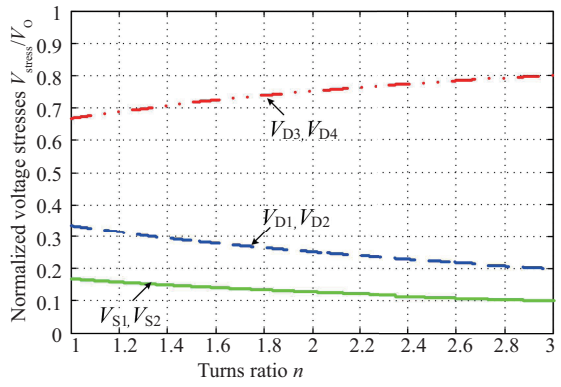


Fig. 6. Normalized power components voltage stress.

with the turns ratio of the coupled inductors is shown in Fig. 6. It can be seen that the voltage stress of diode and main switches is always lower than the output voltage. The voltage stress of switches is no more than two-tenth of output voltage. So the lower voltage rating MOSFETs and diodes can be selected to reduce both switching and conduction losses in high step-up and high output voltage application.

C. Voltage Sharing of Two Branch Output

Assuming that the duty cycle of the main switch S_1 is d_1, the duty cycle of the main switch S_2 is d_2 and $d_1 \neq d_2$. In addition, the power MOSFET and diode usually have some voltage drops (assumed as V_d) which should be considered in practical circuit design. By applying the volt-second balance to the magnetizing inductance, the voltage difference between the two output capacitors C_3 and C_4 is

$$V_{C3} - V_{C4} = \frac{n(d_1 - d_2)}{(1 - d_1)(1 - d_2)}(V_{in} - V_d) \neq 0. \quad (15)$$

It can be seen from (15), there is a voltage difference between the capacitor C_3 and C_4 when the duty cycle d_1 is not equal to d_2. Although it may be small, it still results in unbalanced of the voltage on the C_3 and C_4. To alleviate the above problem of the proposed converter, a voltage-current loop together with a simple voltage-balance loop is presented in Fig. 7.

The voltage-balance loop aims to reduce the voltage difference between C_3 and C_4. In this loop, the different duty cycle Δd is achieved by a simple PI controller through the ΔV between C_3 and C_4. Then the duty cycle d_1 of the switch S_1 can be easily obtained by

$$d_1 = d_2 - \Delta d. \quad (16)$$

By only controlling one of the boost converters, the input current and output voltage of the converter can be easily controlled to be stable. In Fig. 6, the blue block is a voltage balance loop that aims to reduce the unbalance voltage between

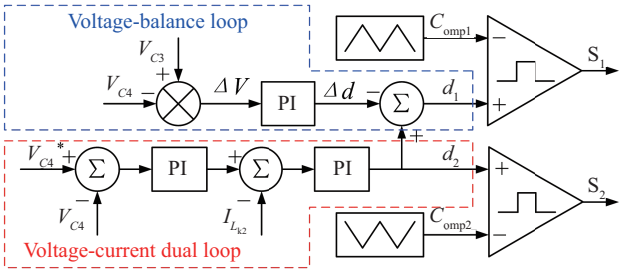


Fig. 7. Loop control of the proposed converter.

C_3 and C_4. The red block is the voltage-current dual loop that aims to ensure the stability of the input current and output voltage.

From (16), the voltage-balance process is: when the voltage of C_3 is higher than C_4, the different duty Δd is positive which makes the d_1 decrease. Then the voltage of C_3 comes to decrease to follow V_{C4}. Conversely, V_{C3} will increase to V_{C4}.

D. Analysis of Input Current Ripple Under CCM Mode

In order to simplify the analysis, the influence of transient mode can be ignored, the leakage current is equivalent to linear variation as shown in Fig. 8(a), at the time of t_1, the leakage inductance current and the input current can be expressed as

$$\begin{aligned} i_{L_{k1}}(t_1) &= I_{L_{k1},avg} - \frac{(1-d)\Delta i_{L_{k1}}}{2d} \\ &= \frac{(2+nk)I_O}{1-d} - \frac{V_{in}(1-d)T_S}{2L_{m1}} \end{aligned} \quad (17)$$

$$i_{L_{k2}}(t_1) = I_{L_{k2},avg} + \frac{\Delta i_{L_{k2}}}{2} = \frac{(2+nk)I_O}{1-d} + \frac{V_{in}dT_S}{2L_{m2}} \quad (18)$$

$$\begin{aligned} i_{in}(t_1) &= i_{L_{k1}}(t_1) + i_{L_{k2}}(t_1) \\ &= \frac{(4+2nk)I_O}{1-d} + \left(\frac{d}{2L_{m2}} - \frac{1-d}{2L_{m1}}\right)V_{in}T_S. \end{aligned} \quad (19)$$

The expression of the input current ripple obtained as

$$\Delta i_{in} = \left|\left(\frac{d}{2L_{m2}} - \frac{1-d}{2L_{m1}}\right)\right| V_{in}T_S \quad (20)$$

Assuming $L_{m2} = NL_{m1}$,

$$\Delta i_{in} = \left|\frac{(N+1)d}{N} - 1\right| \frac{V_{in}T_S}{2L_{m1}}. \quad (21)$$

The relation between the input current ripple and the duty cycle d is given in Fig. 8. It can be seen from Fig. 8(b) that the inductance value of the converter can be designed according to the duty cycle of the converter, and the zero ripples of the input current can be realized theoretically.

E. Performance Comparison

The performance of comparison among interleaved high step-up converters published in [20], [21], [25] and the

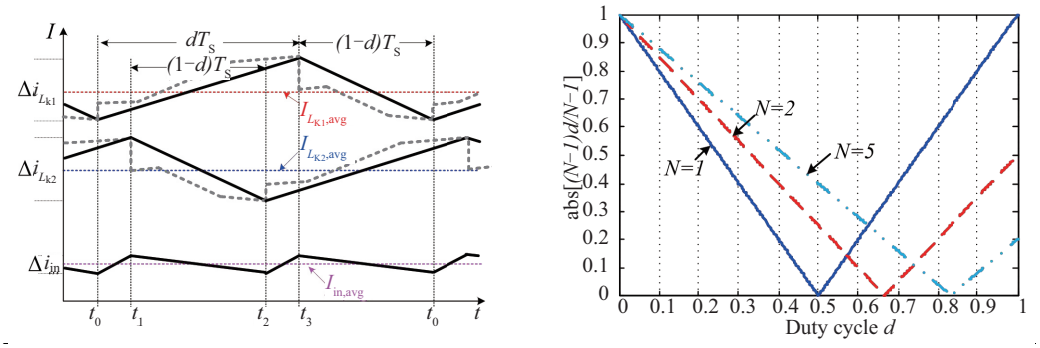


Fig. 8. Diagram of input current ripple analysis. (a) Current analysis. (b) Relation between current ripple and duty cycle.

TABLE I
PERFORMANCE COMPARISON IN DIFFERENT CONVERTERS

Topology	Converter in [20]	Converter in [25]	Converter in [21]	Proposed converter
Numbers of active switches	2	2	2	2
Numbers of diodes	6	8	4	4
Number of capacitors	5	5	3	4
Number of windings	6	6	5	4
Voltage gain	$\frac{2+2nk}{1-d}$	$\frac{1+3nk}{1-d}$	$\frac{2+nk}{1-d}$	$\frac{4+2nk}{1-d}$
Voltage stress of active switches	$\frac{1}{2+2nk}V_O$	$\frac{1}{1+3nk}V_O$	$\frac{1}{2+nk}V_O$	$\frac{1}{4+2nk}V_O$
The maximum voltage stress on diodes	$\frac{1+2nk}{2+2nk}V_O$	$\frac{1+2nk}{1+3nk}V_O$	V_O	$\frac{2+2nk}{4+2nk}V_O$

proposed converter is shown in Table I. One can see that the proposed converter is higher than those of the other topologies and the voltage stress on switches is lower than those of the other. In addition, the number of windings are also minimal in these converters. It is favorable in terms of reliability, circuit volume, and cost. Therefore, the proposed converter is a good alternative for applications that require ultra-step-up voltage gain with high efficiency.

The Fig. 9 clearly shows the value of the voltage stress of each converter under different turns ratio. Comparing with the literatures[20], [21] and [25], the proposed converter has the lower voltage stress on switches and diodes. So switches with lower voltage rating and diodes with lower forward voltage drop can be adapted, reducing the on-state losses.

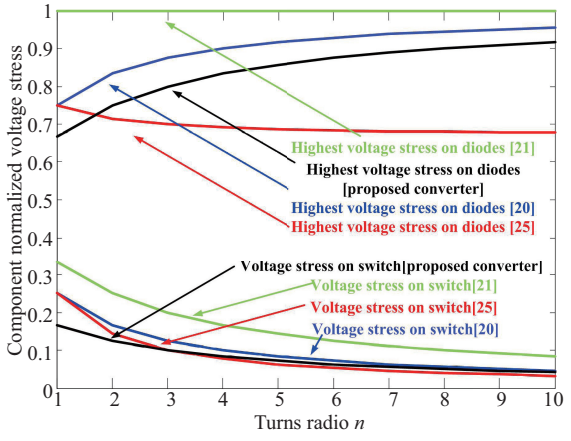


Fig. 9. Comparison of components normalized voltage stress between proposed converter and other converters in the literatures.

F. Analysis of Losses

In order to analyze the loss of the converter, the parasitic parameters of the converter are assumed as follows.

V_{FS} and r_S are forward voltage drop and on-resistance of the switches when the main switches are turned on. V_{FD} and r_D are forward voltage drop and on-resistance of the diodes when the diodes are turned on. The parasitic resistance of coupled inductor and capacitor are r_L and r_C respectively.

The conduction losses equations about the power switches and diodes are as follow:

$$P_{cond,Si} = \frac{1}{T_S}\int_0^{dT_s}(V_{FSi}i_{Si} + r_{Si}i_{Si}^2)dt = (V_{FSi} + r_{Si}I_{Si})I_{Si}d \tag{22}$$

$$P_{cond,Dj} = \frac{1}{T_S}\int_{dT_s}^{T_s}(V_{FD}i_{Dj} + r_D i_{Dj}^2)dt = (V_{FD} + r_D I_{Dj})I_{Dj}(1-d). \tag{23}$$

The average currents of the main switches S_1, S_2 and D_1~D_4 are I_{S1}. I_{S2}. I_{D1}~I_{D4}, respectively.

The switching loss equations about the power switches and diodes are as follows:

$$\begin{aligned} P_{\mathrm{SW,S1}} &= \frac{1}{T_{\mathrm{S}}}\int_0^{t_{\mathrm{on}}} V_{\mathrm{S1}} i_{\mathrm{S1}}\,\mathrm{d}t + \int_0^{t_{\mathrm{off}}} V_{\mathrm{S1}} i_{\mathrm{S1}}\,\mathrm{d}t \\ &= \frac{1}{6} f_{\mathrm{s}} V_{\mathrm{S1}} \frac{I_{\mathrm{S1}}}{d}(t_{\mathrm{on}} + t_{\mathrm{off}}) \end{aligned} \tag{24}$$

$$\begin{aligned} P_{\mathrm{SW,S2}} &= \frac{1}{T_{\mathrm{S}}}\int_0^{t_{\mathrm{on}}} V_{\mathrm{S2}} i_{\mathrm{S2}}\,\mathrm{d}t + \int_0^{t_{\mathrm{off}}} V_{\mathrm{S2}} i_{\mathrm{S2}}\,\mathrm{d}t \\ &= \frac{1}{6} f_{\mathrm{s}} V_{\mathrm{S2}} \frac{I_{\mathrm{S2}}}{d}(t_{\mathrm{on}} + t_{\mathrm{off}}) \end{aligned} \tag{25}$$

$$\begin{aligned} P_{\mathrm{SW,D1}} &= P_{\mathrm{SW,D2}} = \frac{1}{T_{\mathrm{S}}}\int_0^{t_{\mathrm{b}}} P_{D(t)}\,\mathrm{d}t \\ &= \frac{1}{6} f_{\mathrm{s}} V_{\mathrm{Doff}} I_{\mathrm{rr}} t_{\mathrm{b}} = \frac{1}{3} f_{\mathrm{s}} \frac{V_{\mathrm{in}}}{1-D} I_{\mathrm{rr}} t_{\mathrm{b}} \end{aligned} \tag{26}$$

$$\begin{aligned} P_{\mathrm{SW,D3}} &= P_{\mathrm{SW,D4}} = \frac{1}{T_{\mathrm{S}}}\int_0^{t_{\mathrm{b}}} P_{D(t)}\,\mathrm{d}t \\ &= \frac{1}{6} f_{\mathrm{s}} V_{\mathrm{Doff}} I_{\mathrm{rr}} t_{\mathrm{b}} = \frac{1}{3} f_{\mathrm{s}} \frac{(1+n)V_{\mathrm{in}}}{1-D} I_{\mathrm{rr}} t_{\mathrm{b}}. \end{aligned} \tag{27}$$

The total loss of the main switches is as follows:

$$P_{\mathrm{S,Loss}} = P_{\mathrm{cond,S1}} + P_{\mathrm{cond,S2}} + P_{\mathrm{SW,S1}} + P_{\mathrm{SW,S2}}. \tag{28}$$

The total loss of the diodes is:

$$P_{\mathrm{D,Loss}} = P_{\mathrm{cond,D1}} + \cdots + P_{\mathrm{cond,D4}} + P_{\mathrm{SW,D1}} + \cdots + P_{\mathrm{SW,D4}}. \tag{29}$$

The power loss of the coupled inductors T_1, T_2 in the converter is:

$$P_{\mathrm{cond},L_{\mathrm{m1}}} = P_{\mathrm{cond},L_{\mathrm{m2}}} = r_{L_{\mathrm{m1,2}}} I^2_{L_{\mathrm{m1,2}}} \tag{30}$$

$$P_{\mathrm{cond},L_{\mathrm{s1}}} = P_{\mathrm{cond},L_{\mathrm{s2}}} = r_{L_{\mathrm{s1,2}}} I^2_{L_{\mathrm{s1,2}}} \tag{31}$$

The total loss of the coupled inductor is:

$$P_{\mathrm{T,Loss}} = P_{\mathrm{cond},L_{\mathrm{m1}}} + P_{\mathrm{cond},L_{\mathrm{m2}}} + P_{\mathrm{cond},L_{\mathrm{s1}}} + P_{\mathrm{cond},L_{\mathrm{s2}}} \tag{32}$$

The power loss of the capacitor is:

$$P_{\mathrm{cond},C_{\mathrm{m}}} = \frac{1}{T_{\mathrm{S}}}\left(\int_0^{T_{\mathrm{c}}} r_{C_{\mathrm{m}}} i^2_{C_{\mathrm{m\text{-}c}}}\,\mathrm{d}t\right) + \frac{1}{T_{\mathrm{S}}}\left(\int_0^{T_{\mathrm{disc}}} r_{C_{\mathrm{m}}} i^2_{C_{\mathrm{m\text{-}disc}}}\,\mathrm{d}t\right), \tag{33}$$

where T_{c}, T_{disc}, $i_{C_{\mathrm{m\text{-}c}}}$ and $i_{C_{\mathrm{m\text{-}disc}}}$ are the charging time, discharging time, charging current and discharging current of capacitors in a cycle respectively.

The total power of the capacitor loss is:

$$P_{C,\mathrm{Loss}} = P_{\mathrm{cond},C1} + P_{\mathrm{cond},C2} + P_{\mathrm{cond},C3} + P_{\mathrm{cond},C4}. \tag{34}$$

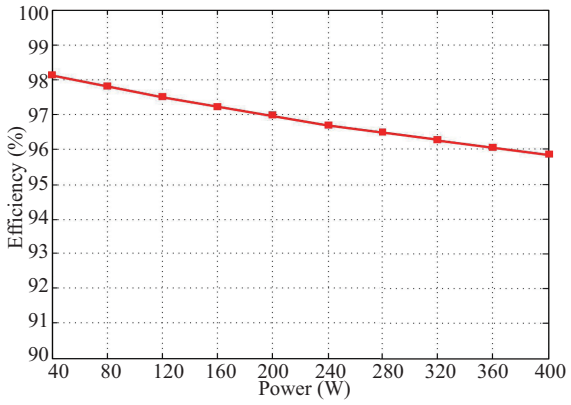


Fig. 10. The waveform of the theoretical efficiency.

In summary, the total power loss of the converter is:

$$P_{\mathrm{Loss}} = P_{\mathrm{S,Loss}} + P_{\mathrm{D,Loss}} + P_{T,\mathrm{Loss}} + P_{C,\mathrm{Loss}}. \tag{35}$$

Therefore, the efficiency of the proposed converter when operating in CCM mode is:

$$\eta = \frac{P_{\mathrm{O}}}{P_{\mathrm{O}} + P_{\mathrm{Loss}}} \times 100\%, \tag{36}$$

where output power: $P_{\mathrm{O}} = V^2_{\mathrm{O}} / R$.

When $V_{\mathrm{in}} = 25$ V, $n = 1$, $d = 0.6$, $V_{\mathrm{FS}} = 0.8$ V, $V_{\mathrm{FD}} = 0.8$ V, $r_{\mathrm{D}} = 1$ mΩ, $r_{\mathrm{S}} = 50$ mΩ, $t_{\mathrm{on}} + t_{\mathrm{off}} = 72$ ns, $t_{\mathrm{b}} = 35$ ns, $I_{\mathrm{rr}} = 10$ μA, $r_{L_{\mathrm{m}}} = r_{L_{\mathrm{s}}} = 50$ mΩ and $r_C = 50$ mΩ. Fig. 10 shows waveform of the theoretical efficiency.

IV. Design Considerations

A. Inductor Selection

The design of the coupled inductors is based on the boundary operating condition of the magnetizing inductance. The turns ratio of the coupled inductors n and the coupled coefficient k are considered unity in the design procedure. Due to the circuit symmetry, the coupled inductors average current is identical, and the input current I_{in} is the summation of $I_{L_{\mathrm{m1}}}$ and $I_{L_{\mathrm{m2}}}$.

$$I_{L_{\mathrm{m1}}} = I_{L_{\mathrm{m2}}} \tag{37}$$

$$I_{\mathrm{in}} = I_{L_{\mathrm{m1}}} + I_{L_{\mathrm{m2}}} \tag{38}$$

Considering the ideal efficiency, the relation between I_{in} and the output current I_{out} could be achieved

$$P_{\mathrm{in}} = P_{\mathrm{out}} \tag{39}$$

$$I_{\mathrm{in}} V_{\mathrm{in}} = I_{\mathrm{out}} V_{\mathrm{out}}, \tag{40}$$

where P_{in} and P_{out} are the input and output power, respectively. By considering the voltage gain (11), and the input current (38) in (40), the relation between $I_{L_{\mathrm{m1}}}$ which is equal to $I_{L_{\mathrm{m2}}}$, and I_{out} is obtained

$$I_{L_{m1}} = I_{L_{m2}} = \frac{2 + nk}{1 - d} I_{out} \tag{41}$$

$$V_{L_m} = L_m \frac{\Delta I_{L_m}}{\Delta t}. \tag{42}$$

So, according to the nominal output power, the magnetizing inductance average current and the desired current ripple ΔI_{L_m} can be calculated from (41) and (42) on the basis of the CCM operation range.

When the switches are turned on, the voltage on the input magnetizing inductor is equal to V_{in}. Based on (42), L_m can be obtained as below:

$$L_m = \frac{V_{in} d}{f \Delta I_{L_m}}, \tag{43}$$

in which f is the switching frequency.

According to the required voltage gain ,the equation of turns ratio can be expressed as:

$$n = \frac{M_{CCM}(1 - D) - 4}{2}. \tag{44}$$

B. Capacitors Selection

The capacitor design mainly considers the voltage stress and the fluctuation of the voltage on the every capacitor to a certain range, and the capacitance value can be selected according to the formula (45).

$$C_{1\sim4} \geqslant \frac{P_{C1\sim4}}{2\, V_{C1\sim4}\, \Delta V_{C1\sim4}\, f} \tag{45}$$

In practical applications, with the increase of the capacitance, the equivalent series impedance of an aluminum electrolytic capacitor will become smaller. Therefore, the capacitance is always selected to be greater than the calculated result for the sake of reducing the power losses.

V. Experimental Results

An experimental prototype circuit of the presented converter is built and tested in the laboratory in order to verify the validity of the theoretical analysis. The components of the converterare shown in Table II.

Fig. 11 (a) and (b) show the waveforms of currents of the leakage inductor L_{k1}, L_{k2} and input current i_{in}. The current $i_{L_{k1}}$ and $i_{L_{k2}}$ are nearly equal, and the input current ripple is lower than the currents of two input branches due to the interleaved operation. It helps to improve the efficiency of the input power supply.

Fig. 12 show the waveforms of currents of main switches S_1, S_2 and diodes D_1~D_4. From the experimental waveform, the diodes D_1 and D_2 are turned off under the ZCS condition and the main switches S_1 and S_2 are turned on under the ZCS condition. Besides, the diodes D_3 and D_4 are switched on and switched off all under the ZCS condition. The switching losses of main switches and diodes are reduced effectively, and the efficiency of the proposed converter can be improved.

TABLE II
Utilized Components and Parameters of the Prototype

Component	Parameter
Input voltage V_{in}	25~30 V
Output voltage V_O	400 V
Maximum output power P	400 W
Switching frequency f_s	40 kHz
Inductor L_{m1}, L_{m2}	100 μH
Power switch S_1,S_2	IRFP260N
Diode D_1~D_4	DSEI-06A
Capacitors C_1 and C_2	47 μF/100 V
Capacitor C_3 and C_4	100 μF/250 V

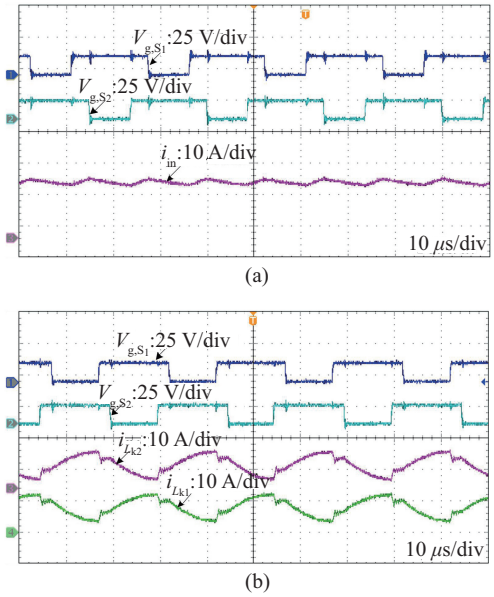


Fig. 11. Waveforms of $i_{L_{k1}}$, $i_{L_{k2}}$, and i_{in}: (a) i_{in}. (b) $i_{L_{k1}}$, $i_{L_{k2}}$.

Fig. 13(a) and (b) shows that the voltage stress on the diodes D_1~D_4. The voltage stress of the diodes D_1 and D_2 are approximately 130 V and that of D_3 and D_4 are only 2/3 of the output voltage. From Fig. 13(c), the voltage stress of main switches are about 67 V, only 1/6 of the output voltage. So, the MOSFET with low on-resistance and low voltage level can be used to reduce the conduction losses and improve the efficiency of the converter. Fig. 13(d) shows the voltage of output capacitors. With the closed-loop control, the voltage of C_3 and C_4 are equal. It defends that the analysis of the voltage balance control is right.

Fig. 14 shows the dynamic response because of the variation of load. It can be seen that the output voltage is maintained at 400 V when the load changes suddenly. It proves that the converter has better dynamic performance and it is consistent with the previous small-signal analysis conclusion.

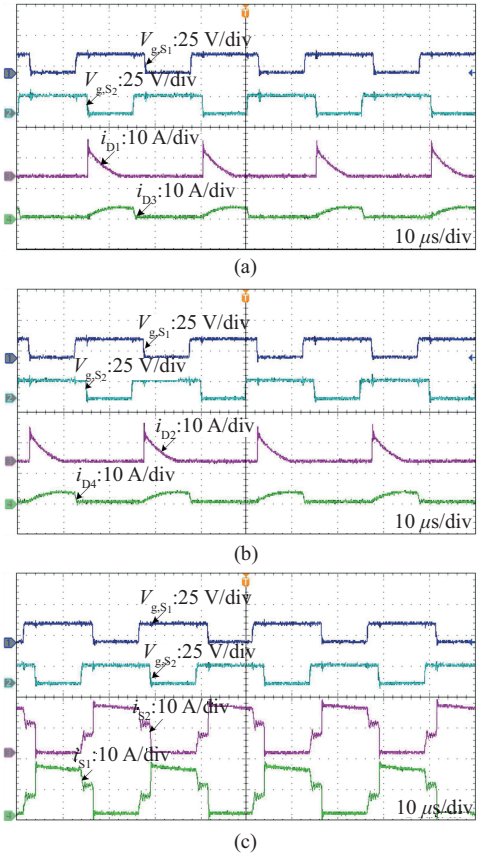
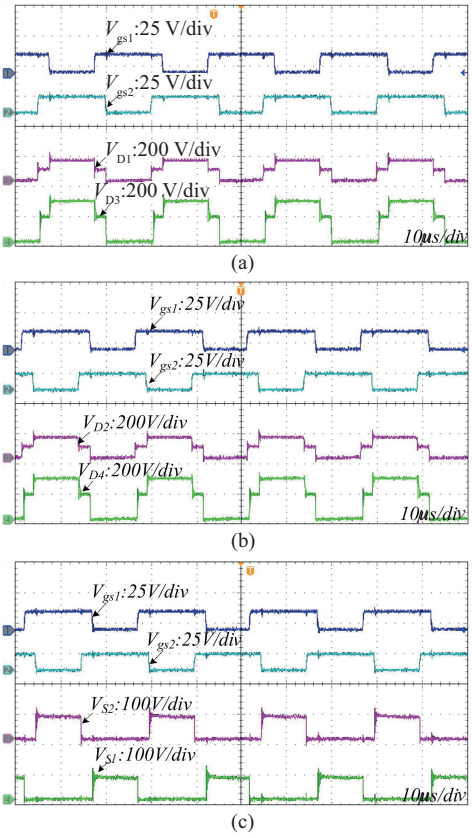


Fig. 12. Waveforms of currents of main switches and diodes. (a) i_{D1}, i_{D3}. (b) i_{D2}, i_{D4}. (c) i_{S1}, i_{S2}.



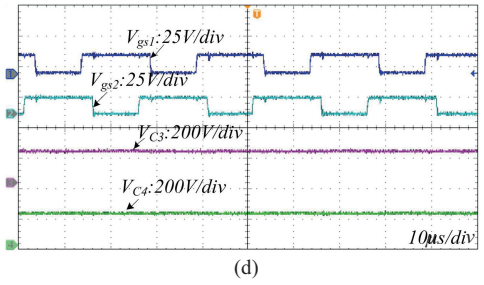


Fig. 13. Voltage stresses of main switches and diodes: (a) V_{D1}, V_{D3}. (b) V_{D2}, V_{D4}. (c) V_{S1}, V_{S2}. (d) V_{C3}, V_{C4}.

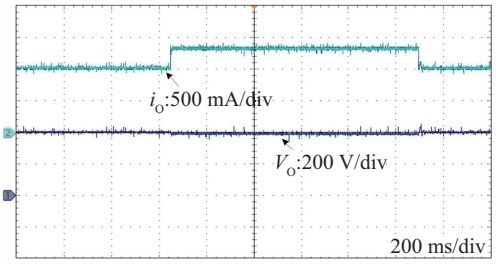


Fig. 14. The experimental waveform of the step load.

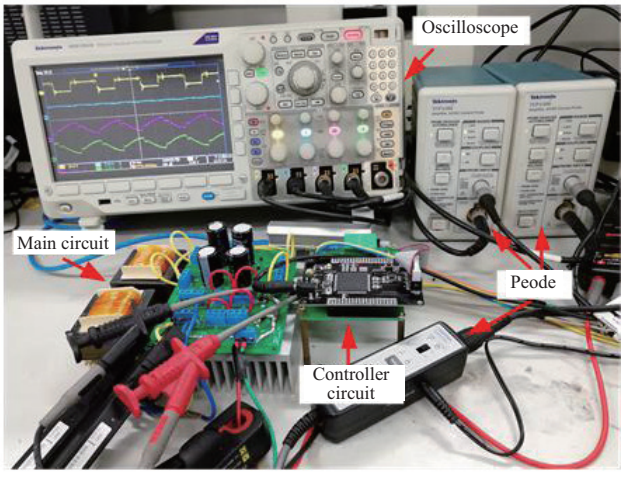


Fig. 15. The picture of experiment testing platform.

Fig. 15 shows the picture of the experimental platform, and some key components are marked. The efficiency curves at different input voltages are shown in Fig. 16. The conversion efficiency of proposed converter at full load can reach 93.2% even the input voltage is reduced to 20 V. The maximum conversion efficiency of the converter is 95.0% when the output power is 280 W and input voltage is 30 V.

VI. Conclusions

This paper has successfully developed a parallel-series interleaved boost converter structure, that the primary sides of the double coupled inductors are connected in parallel at the input, and the secondary sides of the two coupled inductors are connected in series to achieve much higher voltage gain at the output. The working principle and steady-state characteristics

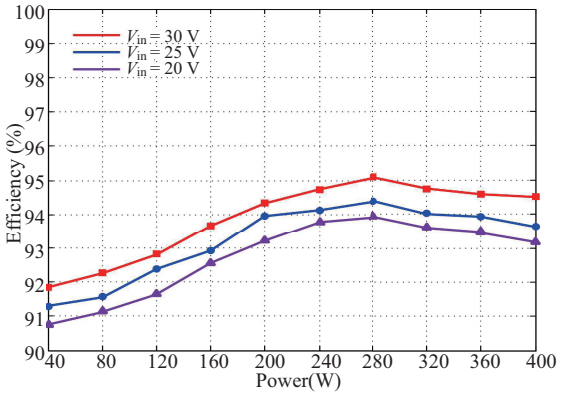


Fig. 16. The experimental efficiency curve of proposed converter.

of the converter are analyzed in detail and verified successfully. By using the technologies of interleaved input-parallel and output-series and voltage multiplier, the proposed converter has been implemented high step up conversion with high efficiency, low input current ripples, low output voltage ripples. The voltage stress of power devices is also very low, which will allow one to choose lower voltage rating MOSFETs and diodes to reduce both switching and conduction losses. In addition, because of the leakage inductance of coupled inductor, the power MOSFETs and output diodes are turned-on under zero current switching that not only reduce the switching losses but also help to conversion efficiency improvement.

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