Interleaved Switched-Capacitor Bidirectional DC-DC Converter with Wide Voltage-Gain Range for Energy Storage Systems

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***Abstract*—**In this paper, an interleaved switched-capacitor bidirectional DC-DC converter with a high step-up/step-down voltage gain is proposed. The interleaved structure is adopted in the low-voltage side of this converter to reduce the ripple of the current through the low-voltage side, and the series-connected structure is adopted in the high-voltage side to achieve the high step-up/step-down voltage gain. In addition, the bidirectional synchronous rectification operations are carried out without requiring any extra hardware, and the efficiency of the converter is improved. Furthermore, the operating principles, voltage and current stresses, and current ripple characteristics of the converter are analyzed. Finally, a 1kW prototype has been developed which verifies a wide voltage-gain range of this converter between the variable low-voltage side (50V-120V) and the constant high-voltage side (400V). The maximum efficiency of the converter is 95.21% in the step-up mode and 95.30% in the step-down mode. The experimental results also validate the feasibility and the effectiveness of the proposed topology.

***Index Terms*—**Bidirectional DC-DC converter, Interleaved, Switched-capacitor, Synchronous rectification, Wide-voltage-gain range

I. INTRODUCTION

With the aggravation of the global energy crisis and the deterioration of the environment pollution, the renewable energy systems become very important in the world [1] , [2] . However, the renewable energy systems, including photo-voltaic systems and wind-power generating systems, cannot provide a stable power and supply enough instantaneous power when the load power suddenly increases. Energy storage systems, which are used to compensate the power fluctuation between the power generation side and the load side, play an important role in renewable energy power systems [3] , [4] . A bidirectional DC–DC converter is a key device for interfacing an energy storage element such as a battery pack or a super-capacitor pack, with a DC bus [5] , [6] . The voltage of a storage battery is typically 48V or lower, while the voltage of a DC bus is 400V or higher [7] . Thus, a bidirectional DC–DC converter with a wide voltage-gain range is desired for energy storage systems to connect a low-voltage battery with a high-voltage DC bus.

There are two different types of bidirectional DC-DC converters in different applications, which include the isolated converters and non-isolated converters. The isolated converters include the Flyback, the Forward-Flyback, the half-bridge and the full-bridge. High voltage-gain is obtained by adjusting the turns ratio of the high frequency transformer. However, the leakage inductance of the transformer results in high voltage spikes on semiconductors. In order to reduce the voltage stress caused by the leakage inductance, a full bridge bidirectional DC-DC converter with a Flyback snubber circuit [8] and a bidirectional DC-DC converter with an active clamp circuit [9] were proposed. Although the energy of the leakage inductor can be recycled, more additional circuits are required. Besides, when the input and the output voltages cannot match the turns ratio of the transformer, the switching loss will increase dramatically [10] .

The non-isolated converters include the Cuk, Sepic/Zeta, coupled-inductor, conventional buck-boost, three-level [11] -[14] , multi-level and switched-capacitor [15] . Due to the cascaded configurations of two power stages, conversion efficiencies of Cuk and Sepic/Zeta are lower [16] , [17] . Coupled-inductor converters can achieve a high voltage gain by adjusting the turns ratio of the coupled inductor [18] , but the problem associated with the leakage inductor is still difficult to be solved and the converter's power converting and transferring capabilities are limited by the capacity of the magnetic core. By utilizing a coupled-inductor**,** the Sepic converter has been modified, and a high efficiency and high voltage-gain bidirectional DC-DC converter with soft-switching was proposed in [19] . But it requires extra active power semiconductors and capacitors. Conventional buck-boost converters are good candidates for low-voltage applications due to its high efficiency and low cost. Unfortunately, the drawbacks including the narrow voltage conversion range, the high voltage stress and extreme duty cycles of semiconductors make them not suitable for energy storage applications. Though the conventional two-phase interleaved bidirectional DC-DC converter in [20] can reduce low-voltage side current ripples, but this converter still has disadvantages including the narrow voltage conversion range and the high voltage stress for power semiconductors. The voltage stress of power semiconductors of the bidirectional three-level DC-DC converters in [11] , [12] is half that of the conventional two-phase interleaved bidirectional DC-DC converter, but its voltage-gain range is still narrow. Besides, the low-voltage and high-voltage side grounds of this converter are connected by a power semiconductor, the potential difference between the two grounds is a high frequency PWM voltage, which may result in more maintenance issues and EMI problems. The low-voltage and high-voltage sides of the bidirectional three-level DC-DC converter in [14] share the common ground, but the voltage-gain of this converter is still limited. In addition, this converter requires the complicated control scheme to balance the flying-capacitor voltage. The converters in [13] , and [21] can achieve a high voltage gain, and the low voltage stress of power semiconductors. However, these converters need more power semiconductors, and require additional hardware circuits and control strategies to maintain the balanced voltage stress of

power semiconductors. The switched-capacitor converter structures and control strategies are simple and easy to expand. Different charging and discharging paths of the capacitors transfer energy to either the low-voltage or the high-voltage side to achieve a high voltage gain. Single capacitor bidirectional switched-capacitor converters were proposed in [22] , [23] , but the converter's efficiency is low. To reduce the input current ripple, interleaved switched-capacitor converters have been proposed in [24] -[27] . However, the converter in [24] needs more components, and the inductor currents of the converter in [25] are unbalanced when D_b is not equal to $2D_a$. Although the bidirectional DC-DC converters in [26] , and [27] just need four semiconductors, the maximum voltage stress of the converter in [26] is that of the high voltage side, and the maximum voltage stress of the converter in [27] is higher than that of the high voltage side. The bidirectional converters in [28] , and [29] only require three semiconductors. But their voltage-gain ranges are still small. In addition, the low-voltage and high-voltage side grounds of these converter are connected by a power semiconductor or an inductor, which will also cause extra EMI problems. Finally, the high voltage-gain converter in [30] needs more power components and fails to achieve bidirectional power flows. In addition, the balanced inductor currents just can be achieved when the number of the voltage multiplier stages is odd. The converter in [31] suffers from the huge current ripple in the low-voltage side.

These non-isolated bidirectional DC-DC converters referred above cannot simultaneously achieve the low current ripple, the low voltage stress of power semiconductors and the wide voltage-gain range. In order to solve this problem, an interleaved switched-capacitor bidirectional DC-DC converter is proposed in this paper. Comparing with the conventional two-phase interleaved bidirectional DC-DC converter and the bidirectional three-level DC-DC converter, the proposed converter has advantages including low current ripple, low voltage-stress of power semiconductors and wide voltage-gain range. In addition, the connection between the low-voltage and the high-voltage side grounds of the proposed converter is a capacitor rather than a power semiconductor. To achieve a high step-up gain, the capacitors are charged in parallel and discharged in series in the step-up mode. Opposite to the step-up mode, the high step-down ratio can also be obtained because two capacitors are charged in series and discharged in parallel. Furthermore, the capacitor voltage of the proposed converter is half of the high-voltage side voltage, and the efficiency is improved by synchronous rectification operation. This paper is organized as follows. In Section II, the topology of the interleaved switched-capacitor bidirectional DC-DC converter is presented. In Section III, the operating principles of the proposed converter are analyzed in detail. The steady-state characteristics of the converter are analyzed in Section IV and experimental results are analyzed in Section V.

II. The Proposed Converter

The proposed interleaved switched-capacitor bidirectional DC-DC Converter is shown in Fig. 1. This converter is composed of four modules. C_{low} is the energy storage/filter capacitor of the low-voltage side. Module 1 includes power semiconductors Q_1, Q_2, and energy storage/filter inductors L_1, L_2. In addition, L_1-Q_1 and L_2-Q_2 form the parallel structure of the low-voltage side. Module 2 is a switched-capacitor network, including switched-capacitor units C_1-Q_3, C_2-Q_4 and C_3-Q_5. The interleaved structure is used in the low-voltage side of this converter. In this case, the duty cycles of Q_1 and Q_2 are the same, and the phase difference between the gate signals S_1 and S_2 is 180°. The low-voltage side, Module 1, Module 2 and the high-voltage side form the bidirectional DC-DC converter with the structure of the low-voltage-side in parallel and the high-voltage-side in series.

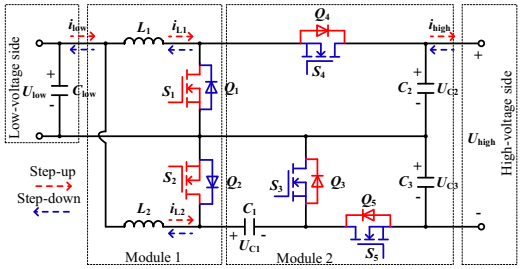


Fig. 1 The proposed topology of the interleaved switched-capacitor bidirectional DC-DC Converter.

III. Operating Principles

To simplify the steady-state characteristics analysis of the proposed converter, several reasonable assumptions about the operating conditions are made as follows: (a) all the power semiconductors and energy storage components of the converter are treated as ideal ones, and the converter operates in the continuous conduction mode (CCM); (b) all the capacitances are large enough that each capacitor voltage is considered as constant in each switching period.

A. Step-Up Mode

When the energy flows from the low-voltage side to the high-voltage side, the output voltage U_{high} is stepped up from U_{low} by controlling the power semiconductors of Q_1, and Q_2, and the anti-parallel diodes of Q_3, Q_4 and Q_5. The relationship between d_1 and d_2 can be written as d_1=d_2=d_{Boost}, where d_1 and d_2 are the duty cycles of Q_1 and Q_2 respectively. Fig. 2 shows the typical waveforms in the step-up mode, and Fig. 3 shows the current flow path of the proposed converter.

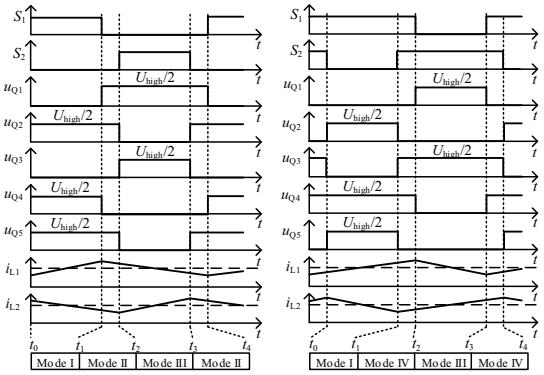
Mode I: The power semiconductor Q_1 is turned on and Q_2 is turned off. The anti-parallel diode of Q_3 is turned on, while the anti-parallel diodes of Q_4 and Q_5 are turned off. The current flow path of the proposed converter is illustrated in Fig. 3(a). The energy is transferred from the DC source U_{low} to the inductor L_1. Meantime, C_1 is being charged by inductor L_2, while C_2 and C_3 are discharging. C_2 and C_3 are connected in series to provide energy for the load in the high voltage side.

Mode II: The power semiconductors Q_1 and Q_2 are turned off. The anti-parallel diodes of Q_3 and Q_4 are turned on, while the anti-parallel diode of Q_5 is turned off. The current flow path of the proposed converter is given in Fig. 3(b). Inductors L_1 and L_2 are discharging. Meantime, C_1 is charging from inductor L_2, while C_3 is discharging. The DC source U_{low}, L_1 and C_3 output energy to the load.

Mode III: The power semiconductor Q_1 is turned off and Q_2

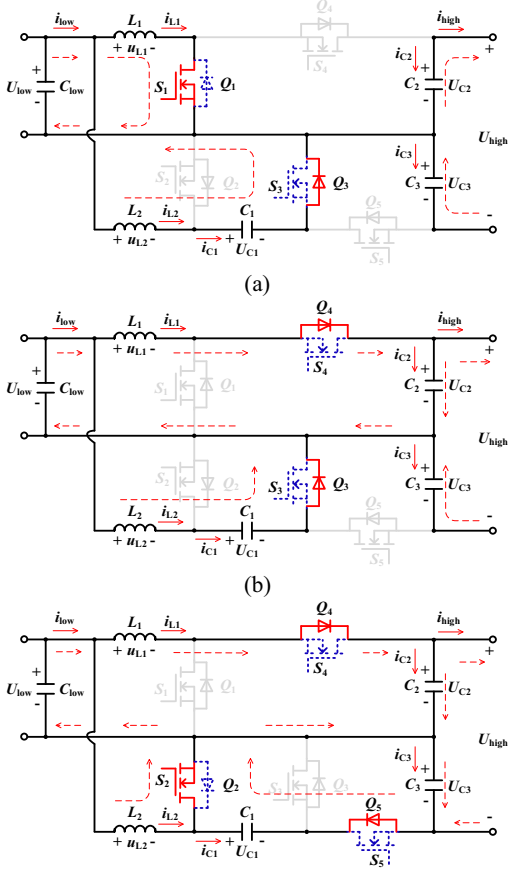
is turned on. The anti-parallel diode of Q_3 is turned off, while the anti-parallel diodes of Q_4 and Q_5 are turned on. The current flow path of the proposed converter is shown in Fig. 3(c). Inductor L_1 is discharging, while L_2 is charged by the DC source. Meantime, C_3 is charged by C_1, while C_2 is charged by inductor L_1. The DC source U_{low}, L_1 and C_1 output energy to the load.

Mode IV: Power semiconductors Q_1 and Q_2 are turned on. The anti-parallel diodes of Q_3 and Q_4 are turned off, while the anti-parallel diode of Q_5 is turned on. The current flow path of the proposed converter is displayed in Fig. 3(d). Inductors L_1 and L_2 are charged by the DC source U_{low} in parallel. Meantime, C_1 and C_2 are discharging in series to provide energy for the load.

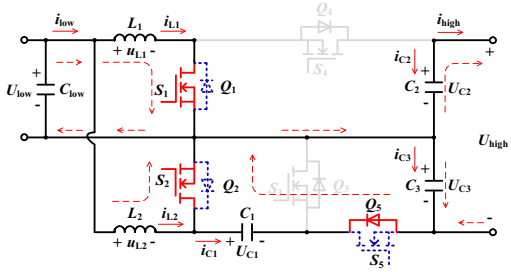


(a) (b)

Fig. 2 Typical waveforms of the proposed converter in the step-up mode. (a) $0<d_{Boost}<0.5$. (b) $0.5\leq d_{Boost}<1$.



(a) (b) (c)



(d)

Fig. 3 Current flow path of the proposed converter in the step-up mode. (a) Mode I S_1S_2=10. (b) Mode II S_1S_2=00. (c) Mode III S_1S_2=01. (d) Mode IV S_1S_2=11.

B. Step-Down Mode

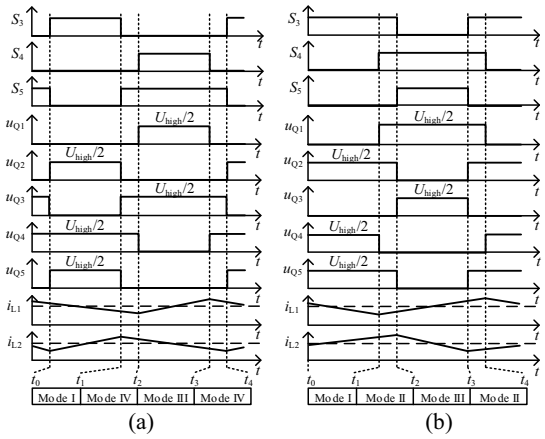
When energy flows from the high-voltage side to the low-voltage side, the output voltage U_{low} is stepped down from U_{high} by controlling the power semiconductors Q_3, Q_4 and Q_5, and the anti-parallel diodes of Q_1 and Q_2. The relationship between d_3 and d_4 can be written as d_3=d_4=d_{Buck}, where d_3 and d_4 are the duty cycles of Q_3 and Q_4 respectively. Fig. 4 shows the typical waveforms in the step-down mode, and Fig. 5 shows the current flow path of the proposed converter.

Mode I: The power semiconductor Q_3 is turned on, while Q_4 and Q_5 are turned off. The anti-parallel diode of Q_1 is turned on, and the anti-parallel diode of Q_2 is turned off. The current flow path of the proposed converter is shown in Fig. 5(a). C_2 and C_3 are charged by the DC source U_{high} in series. Meantime, inductors L_1, L_2 and C_1 are discharging to provide energy for the load in the low voltage side.

Mode II: Power semiconductors Q_3 and Q_4 are turned on, while Q_5 is turned off. The anti-parallel diodes of Q_1 and Q_2 are turned off. The current flow path is shown in Fig. 5(b). C_1 is discharging to transfer energy to inductor L_2, and simultaneously outputting energy to the load. Meantime, the DC source U_{high} charges L_1 and C_3, and simultaneously outputs energy to the load. In addition, C_2 is discharging to supply energy to L_1 and the load.

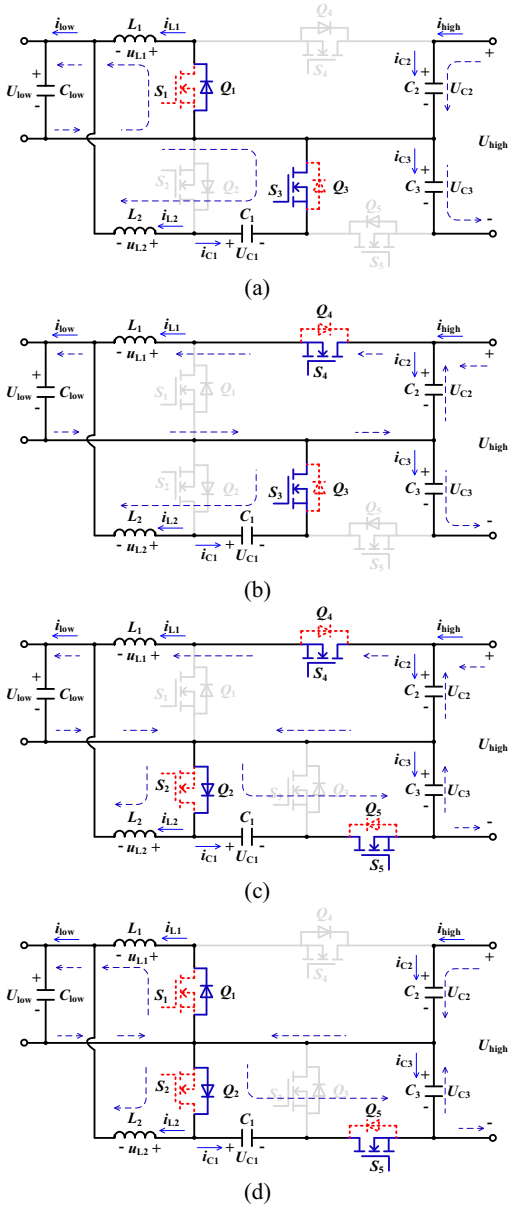
Mode III: The power semiconductor Q_3 is turned off, while Q_4 and Q_5 are turned on. The anti-parallel diode of Q_1 is turned off, and the anti-parallel diode of Q_2 is turned on. The current flow path of the proposed converter is shown in Fig. 5(c). Inductor L_2 is discharging to provide energy for the load. Meantime, the DC source U_{high} charges L_1 and C_1, and simultaneously provide energy for the load. In addition, C_2 is discharging to supply energy to L_1 and the load, and C_3 is discharging to output energy to C_1.

Mode IV: Power semiconductors Q_3 and Q_4 are turned off, while Q_5 is turned on. The anti-parallel diodes of Q_1 and Q_2 are turned on. The current low path of the proposed converter is shown in Fig. 5(d). L_1 and L_2 are discharging to provide energy for the load in parallel. Meantime, the DC source U_{high} charges C_1 and C_2 in series, and C_3 is discharging to supply energy to C_1.



(a) (b)

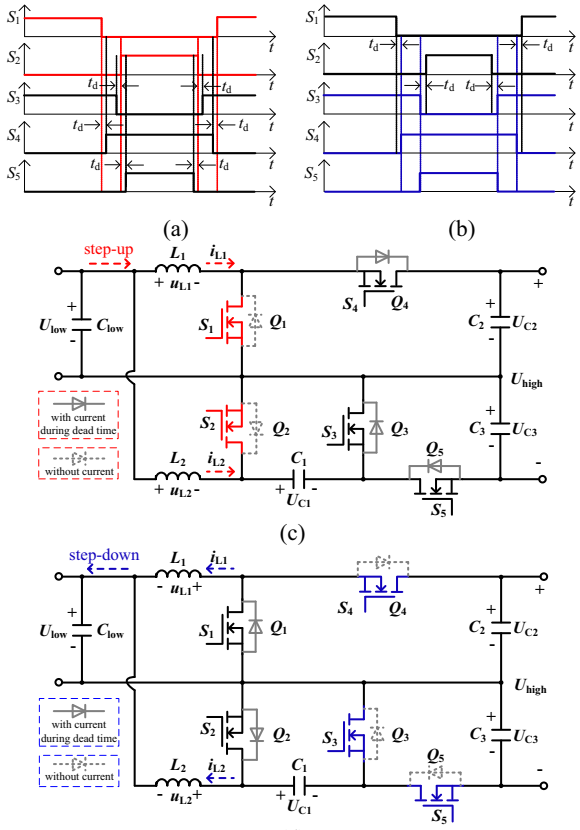
Fig. 4 Typical waveforms of the proposed converter in the step-down mode. (a) $0<d_{\text{Buck}}<0.5$. (b) $0.5\le d_{\text{Buck}}<1$.



(a) (b) (c) (d)

Fig. 5 Current flow path of the proposed converter in the step-down mode. (a) Mode I $S_3S_4S_5$=100. (b) Mode II $S_3S_4S_5$=110. (c) Mode III $S_3S_4S_5$=011. (d) Mode IV $S_3S_4S_5$=001.

C. *Synchronous rectification operation*



(a) (b) (c) (d)

Fig. 6 Synchronous rectification operating principle of the proposed bidirectional converter. (a) Gate signals and the dead time in the step-up mode (left). (b) Gate signals and the dead time in the step-down mode (right). (c) Current flow path in the step-up mode. (d) Current flow path in the step-down mode.

As shown in Fig. 1, if the currents of the proposed interleaved switched-capacitor bidirectional converter flow into the corresponding anti-parallel diodes, it will result in the lower efficiency, as well as lower utilization of the power semiconductors. Therefore, a high step-up/step-down ratio switched-capacitor bidirectional DC-DC converter with synchronous rectification is proposed further in this paper.

The synchronous rectification operating principle of the switched-capacitor bidirectional converter is shown in Fig. 6. In the step-up mode, the main power semiconductors Q_1 and Q_2 switch according to gate signals S_1 and S_2 shown in Fig. 6(a). During the dead time t_d, the current has to fully flow into the corresponding anti-parallel diodes of Q_3, Q_4 and Q_5. Otherwise, the current may flow into the controlled power semiconductors Q_3, Q_4 and Q_5 due to their lower on-resistances and on-state voltage drops, as shown in Fig. 6(c), by means of the gate signals S_3, S_4 and S_5 shown in Fig. 6(a). Similarly, in the step-down mode, the main power semiconductors Q_3, Q_4 and Q_5 switch according to gate signals S_3, S_4 and S_5 shown in Fig. 6(b). During the dead time t_d, the current also has to fully flow into the anti-parallel diodes of Q_1 and Q_2. Otherwise, according to the gate signals S_1 and S_2 shown in Fig. 6(b), the current flows into the controlled power semiconductors Q_1 and Q_2, as shown in Fig. 6(d).

Furthermore, the forward voltage drops of the anti-parallel diodes are close to zero. As a result, the controlled MOSFETs of the slave active power semiconductors can be turned on and turned off with ZVS, and the efficiency of the converter is further improved.

D. Control strategy of bidirectional power flow

Based on the operating principles above, the bidirectional power flow control strategy can be achieved as shown in Fig. 7. The voltages U_{high} and U_{low}, and the current i_{low} are obtained by samplings. The interleaving structure is applied to reduce the current ripples.

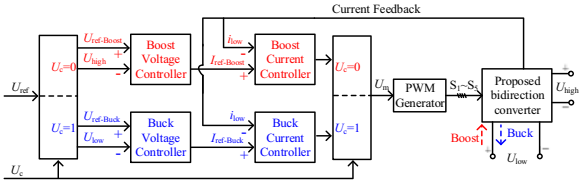


Fig. 7 Control strategy of the bidirectional power flows.

As shown in Fig. 7, the operating modes of the proposed bidirectional DC-DC converter switch between the step-down and the step-up, according to the power flow control signal U_c. It operates in the step-up mode when U_c=0, the voltage U_{high} is controlled by the Boost voltage controller with the reference voltage $U_{ref\text{-}Boost}$ in the voltage-loop. Meantime, the feedback current i_{low} is controlled by the Boost current controller with the reference current $I_{ref\text{-}Boost}$ in the current-loop. The corresponding PWM schemes as shown in Fig. 2 and Fig. 6(a) are selected to generate the gate signals S_1~S_5 in the step-up mode.

Similarly, the converter operates in the step-down mode when U_c=1, the voltage U_{low} is controlled by the Buck voltage controller with the reference voltage $U_{ref\text{-}Buck}$, and the feedback current i_{low} is controlled by the Buck current controller with the reference current $I_{ref\text{-}Buck}$, which is in the opposite direction to the reference current $I_{ref\text{-}Boost}$. The corresponding PWM schemes as shown in Fig. 4 and Fig. 6(b) are also selected to generate the gate signals S_1~S_5 in the step-down mode.

IV. Analysis Of Steady-State Characteristics

A. Voltage-gain in steady-state

(1) Voltage-gain in step-up mode

As shown in Fig. 2(a) and Fig. 3(c), in the range of $0<d_{Boost}<0.5$, C_1 and C_3 are connected in parallel, so that the voltages of C_1 and C_3 are equal. According to Fig. 3(a)-(c) and the voltage-second balance principle on L_1 and L_2, the following equations can be obtained as

$$\begin{cases} d_{Boost}\times U_{low}=(1-d_{Boost})\times(U_{C2}-U_{low}) \\ d_{Boost}\times U_{low}=(1-d_{Boost})\times(U_{C1}-U_{low}) \\ U_{C1}=U_{C3} \end{cases} \tag{1}$$

Therefore, by simplifying (1), the following equations can be written as

$$\begin{cases} U_{C1}=U_{C2}=U_{C3}=\dfrac{1}{1-d_{Boost}}U_{low} \\ U_{high}=\dfrac{2}{1-d_{Boost}}U_{low} \end{cases} \tag{2}$$

According to (2), the voltage-gain of the proposed converter in the step-up mode is $2/(1-d_{Boost})$, which is twice as big as the voltage-gain of the conventional interleaved bidirectional DC-DC converter. In addition, the voltage stress of C_1, C_2 and C_3 can be reduced to half of the voltage U_{high}, and U_{C2}, U_{C3} are self-balanced due to the switched-capacitor technique. Similarly, the corresponding voltage equations of the proposed converter within the range of $0.5\le d_{Boost}<1$ can also be obtained, which are the same as those within the range of $0<d_{Boost}<0.5$.

(2) Voltage-gain in the step-down mode

As shown in Fig. 4(a) and Fig. 5(c), within the range of $0.5\le d_{Buck}<1$, C_1 and C_3 are connected in parallel, so that the voltages of C_1 and C_3 are still equal. According to Fig. 5(a)-(c) and the voltage-second balance principle on L_1 and L_2, the following equations can be obtained as

$$\begin{cases} d_{Buck}\times(U_{C2}-U_{low})=(1-d_{Buck})\times U_{low} \\ d_{Buck}\times(U_{C1}-U_{low})=(1-d_{Buck})\times U_{low} \\ U_{C1}=U_{C3} \end{cases} \tag{3}$$

Therefore, by simplifying (3), the following equations can be written as

$$\begin{cases} U_{C1}=U_{C2}=U_{C3}=\dfrac{1}{2}U_{high} \\ U_{low}=\dfrac{d_{Buck}}{2}U_{high} \end{cases} \tag{4}$$

According to (4), the voltage-gain of the proposed converter in the step-down mode is $d_{Buck}/2$, which is half of the voltage-gain of the conventional interleaved bidirectional DC-DC converter. In addition, the voltage stress of C_1, C_2 and C_3 are still half of the voltage U_{high}, and U_{C2}, U_{C3} are still self-balanced, which are the same as those in the step-up mode. Similarly, the voltage equations of the proposed converter within the range of $0.5\le d_{Buck}<1$ can also be obtained, which are the same as those within the range of $0<d_{Buck}<0.5$.

B. Inductor currents self-balance

(1) Inductor currents self-balance in the step-up mode

According to Fig. 3(a)-(c), the currents of C_1, C_2 and C_3 are as follows, within the duty cycle range $0<d_{Boost}<0.5$ in the step-up mode.

$$\begin{cases} i_{C1}=\begin{cases} I'_{C1} & 0\le t<d_{Boost}T_s \\ I_{L2} & d_{Boost}T_s\le t<T_s \end{cases} \\ i_{C2}=\begin{cases} -I_{high} & 0\le t<d_{Boost}T_s \\ I_{L1}-I_{high} & d_{Boost}T_s\le t<T_s \end{cases} \\ i_{C3}=\begin{cases} -I_{high}-I'_{C1} & 0\le t<d_{Boost}T_s \\ -I_{high} & d_{Boost}T_s\le t<T_s \end{cases} \end{cases} \tag{5}$$

where I_{L1}, I_{L2} and I_{high} are the average currents of i_{L1}, i_{L2} and i_{high}, and I_{C1}, I_{C2} and I_{C3} are the average currents of i_{C1}, i_{C2} and i_{C3} in the step-up mode respectively. In addition, I'_{C1} is the average current of C_1 when Q_2 turns on. By applying the amp-second balance principle on capacitors C_1, C_2 and C_3, the following equations (6)-(8) can be obtained as

$$\langle i_{C1}\rangle=0=\frac{d_{Boost}T_s I'_{C1}+(1-d_{Boost})T_s I_{L2}}{T_s}$$
$$\Rightarrow I_{L2}=-\frac{d_{Boost}}{1-d_{Boost}}I'_{C1} \tag{6}$$

$$\langle i_{C2}\rangle=0=\frac{-d_{Boost}T_s I_{high}+(1-d_{Boost})(I_{L1}-I_{high})}{T_s}$$
$$\Rightarrow I_{L1}=\frac{1}{1-d_{Boost}}I_{high} \tag{7}$$

$$\langle i_{C3}\rangle=0=\frac{d_{Boost}T_s(-I_{high}-I'_{C1})-(1-d_{Boost})T_s I_{high}}{T_s}$$
$$\Rightarrow I'_{C1}=-\frac{1}{d_{Boost}}I_{high} \tag{8}$$

In addition, the relationship $I_{low}=I_{L1}+I_{L2}$ can be drawn in the step-up mode, according to Fig. 3. Then, substituting (8) into (6), I_{low}, I_{L1} and I_{L2} can obtained as

$$\begin{cases} I_{low}=\dfrac{2}{1-d_{Boost}}I_{high} \\ I_{L1}=I_{L2}=\dfrac{1}{1-d_{Boost}}I_{high} \end{cases} \tag{9}$$

In terms of (9), I_{L1} and I_{L2} are both half of the input current I_{low}, i.e. the current self-balance is achieved in the step-up mode. Similarly, the corresponding current equations of the proposed converter within the duty cycle range $0.5\le d_{Boost}<1$ can also be obtained, which are the same as those within the duty cycle range $0<d_{Boost}<0.5$.

(2) Inductor currents self-balance in the step-down mode

The currents of C_1, C_2 and C_3 can be written as follows within the duty cycle range $0<d_{Buck}<0.5$, by means of Fig. 5(a), (c) and (d), in the step-down mode.

$$\begin{cases} i_{C1}=\begin{cases}-I_{L2} & 0\le t<d_{Buck}T_s \\ I'_{C1} & d_{Buck}T_s\le t<T_s\end{cases} \\ i_{C2}=\begin{cases}I_{high}-I_{L1} & 0\le t<d_{Buck}T_s \\ I_{high} & d_{Buck}T_s\le t<T_s\end{cases} \\ i_{C3}=\begin{cases}I_{high} & 0\le t<d_{Buck}T_s \\ I_{high}-I'_{C1} & d_{Buck}T_s\le t<T_s\end{cases} \end{cases} \tag{10}$$

where I_{L1}, I_{L2} and I_{high} are the average currents of i_{L1}, i_{L2} and i_{high}, and I_{C1}, I_{C2} and I_{C3} are the average currents of i_{C1}, i_{C2} and i_{C3} in the step-down mode respectively. In addition, I'_{C1} is the average current of C_1 when Q_3 is turned off. By applying the amp-second balance principle on capacitors C_1, C_2 and C_3, the following equations (11)-(13) can be obtained as

$$\langle i_{C1}\rangle=0=\frac{-d_{Buck}T_s I_{L2}+(1-d_{Buck})T_s I'_{C1}}{T_s}$$
$$\Rightarrow I_{L2}=\frac{1-d_{Buck}}{d_{Buck}}I'_{C1} \tag{11}$$

$$\langle i_{C2}\rangle=0=\frac{d_{Buck}T_s(I_{high}-I_{L1})+(1-d_{Buck})I_{high}}{T_s}$$
$$\Rightarrow I_{L1}=\frac{1}{d_{Buck}}I_{high} \tag{12}$$

$$\langle i_{C3}\rangle=0=\frac{d_{Buck}T_s I_{high}+(1-d_{Buck})T_s(I_{high}-I'_{C1})}{T_s}$$
$$\Rightarrow I'_{C1}=\frac{1}{1-d_{Buck}}I_{high} \tag{13}$$

According to Fig. 5, the current relationship $I_{low}=I_{L1}+I_{L2}$ can also be drawn in the step-down mode. Then, substituting (13) into (11), I_{high}, I_{L1} and I_{L2} can achieved as

$$\begin{cases} I_{high}=\dfrac{d_{Buck}}{2}I_{low} \\ I_{L1}=I_{L2}=\dfrac{1}{2}I_{low} \end{cases} \tag{14}$$

By means of (14), I_{L1} and I_{L2} are also half of the input current I_{low}, i.e. the current self-balance is also obtained in the step-down mode. In a similar way, the corresponding current equations of the proposed converter within the duty cycle range $0.5\le d_{Buck}<1$ can also be obtained, which are the same as those within the duty cycle range $0<d_{Buck}<0.5$.

Based on the analysis previously described, inductor currents self-balance can be achieved within the full duty cycle range for the proposed converter, in both step-up and step-down modes. This contributes to accurate current sensing, and eliminates an extra control loop that may require high performance circuits to balance phase currents.

C. Voltage and current stresses of power semiconductors

(1) Voltage stress

As shown in Fig. 3(b, c) in the step-up mode and Fig. 5(b, c) in the step-down mode, power semiconductor Q_1 is turned off and Q_4 is turned on, so that Q_1 and C_2 are connected in parallel. Therefore the voltages of Q_1 and C_2 are equal. Similarly, the voltages of the other power semiconductors can also be obtained. According to (2) in the step-up mode and (4) in the step-down mode, the voltage stress for the power semiconductors can be written as follows

$$\begin{cases} U_{Q1}=U_{Q4}=U_{C2}=\dfrac{U_{high}}{2} \\ U_{Q2}=U_{Q3}=U_{C1}=\dfrac{U_{high}}{2} \\ U_{Q5}=U_{C3}=\dfrac{U_{high}}{2} \end{cases} \tag{15}$$

Based on (15), all the voltage stresses of the power semiconductors and capacitors are half of the voltage U_{high}.

(2) Current stress

According to Fig. 3 and (9), the current stress of the power semiconductors in the step-up mode can be obtained by applying voltage-balance principle on C_1, C_2 and C_3

$$\begin{cases} I_{Q1} = \dfrac{1}{1-d_{Boost}} I_{high} \\ I_{Q2} = (\dfrac{1}{1-d_{Boost}} + \dfrac{1}{d_{Boost}}) I_{high} \\ I_{Q3} = I_{Q4} = \dfrac{1}{1-d_{Boost}} I_{high} \\ I_{Q5} = \dfrac{1}{d_{Boost}} I_{high} \end{cases} \tag{16}$$

Similarly, according to Fig. 5 and (14), the current stress of the power semiconductors in the step-down mode can be obtained as (17)

$$\begin{cases} I_{Q1} = \dfrac{1}{2} I_{low} \\ I_{Q2} = \dfrac{1}{2(1-d_{Buck})} I_{low} \\ I_{Q3} = I_{Q4} = \dfrac{1}{2} I_{low} \\ I_{Q5} = \dfrac{d_{Buck}}{2(1-d_{Buck})} I_{low} \end{cases} \tag{17}$$

Based on (16) and (17), it can be seen that the current stress of Q_2 is higher than that of Q_1. But it is easier to choose a MOSFET with the high rated current rather than the one with the high rated voltage. Furthermore, the proposed bidirectional converter can obtain a high voltage gain while the duty cycle is in the range of $0.5<d_{Boost}<1$ in the step-up mode or $0<d_{Buck}<0.5$ in the step-down mode. Therefore, the difference of the current stress between Q_1 and Q_2 is limited, and it will not affect the selection of the power semiconductors.

D. Analysis of current ripples

(1) Analysis of current ripples in the step-up mode

In the step-up mode within the range of $0<d_{Boost}<0.5$, it is assumed that $L_1=L_2=L$. According to Fig. 3, the current ripples of i_{L1}, i_{L2} and i_{low} can be derived as follows

$$\begin{cases} \Delta i_{L1} = \Delta i_{L2} = \dfrac{d_{Boost} \times (1-d_{Boost}) \times T_s \times U_{high}}{2L} \\ \Delta i_{low} = \dfrac{d_{Boost} \times (1-2d_{Boost}) \times T_s \times U_{high}}{2L} \end{cases} \tag{18}$$

Where Δi_{L1}, Δi_{L2} and Δi_{low} are the current ripples of i_{L1}, i_{L2} and i_{low}. Similarly, the current ripples of i_{L1}, i_{L2} and i_{low} within the range of $0.5\le d_{Boost}<1$ can be described as follows

$$\begin{cases} \Delta i_{L1} = \Delta i_{L2} = \dfrac{d_{Boost} \times (1-d_{Boost}) \times T_s \times U_{high}}{2L} \\ \Delta i_{low} = \dfrac{(2d_{Boost}-1) \times (1-d_{Boost}) \times T_s \times U_{high}}{2L} \end{cases} \tag{19}$$

(2) Analysis of current ripples in the step-down mode

In the step-down mode within the range of $0<d_{Buck}<0.5$, it is also assumed that $L_1=L_2=L$. According to Fig. 5, the current ripples of i_{L1}, i_{L2} and i_{low} can be derived as follows

$$\begin{cases} \Delta i_{L1} = \Delta i_{L2} = \dfrac{d_{Buck} \times (1-d_{Buck}) \times T_s \times U_{high}}{2L} \\ \Delta i_{low} = \dfrac{d_{Buck} \times (1-2d_{Buck}) \times T_s \times U_{high}}{2L} \end{cases} \tag{20}$$

Where Δi_{L1}, Δi_{L2} and Δi_{low} are the current ripples of i_{L1}, i_{L2} and i_{low}. Similarly, the current ripples of i_{L1}, i_{L2} and i_{low} within the range of $0.5\le d_{Buck}<1$ can be described as follows

$$\begin{cases} \Delta i_{L1} = \Delta i_{L2} = \dfrac{d_{Buck} \times (1-d_{Buck}) \times T_s \times U_{high}}{2L} \\ \Delta i_{low} = \dfrac{(2d_{Buck}-1) \times (1-d_{Buck}) \times T_s \times U_{high}}{2L} \end{cases} \tag{21}$$

Assuming that $L_1=L_2=L=350\mu H$, $f_s=20kHz$, $U_{high}=400V$, $U_{low}=50V\sim120V$, and the rated output power $P_n=1kW$. The current ripple rate of i_{L1}, i_{L2} and i_{low} is shown in Fig. 8, where $\Delta i/I$ is defined as the current ripple rate. According to Fig. 8, the current ripple of the low-voltage side current i_{low} is smaller than those of i_{L1} and i_{L2} in both step-up and step-down modes. When $U_{high}=400V$ and $U_{low}=50V\sim120V$, the duty cycle varies in the range of $0.4<d_{Boost}<0.75$ in the step-up mode according to (2), and varies in the range of $0.25<d_{Buck}<0.6$ in the step-down mode in terms of (4). The current ripple rate of the low-voltage side current i_{low} is further reduced within the corresponding duty cycle range. Taking the step-up operating state as an example, when DC source is in the range of $U_{low}=50V\sim120V$, the minimum ripple rate of the low-voltage side current is 0% when the duty cycle is $d_{Boost}=0.5$. In the range of $0.4\le d_{Boost}<0.5$, the maximum ripple rate of the low-voltage side current arrives at 27.4% when the duty cycle is $d_{Boost}=0.4$. In addition, the maximum current ripple rate of the low-voltage side arrives at 21.1% when the duty cycle is $d_{Boost}=0.67$ within the range of $0.5<d_{Boost}<0.75$.

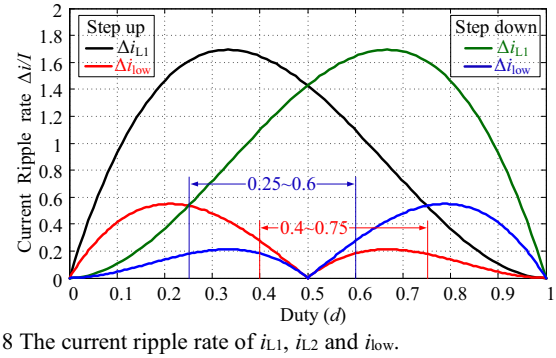


Fig. 8 The current ripple rate of i_{L1}, i_{L2} and i_{low}.

E. Comparisons with other bidirectional solutions

According to the analysis above, the comparisons can be drawn among the proposed and the other bidirectional solutions in the step-up mode, as shown in Tab. 1. The bidirectional DC-DC converter in [14] only needs one inductor, but its ideal voltage-gain 1/(1-d) is limited due to the effects of parasitic resistance and extreme duty cycles. Although the voltage stress across the four semiconductors of this converter is half of the high-side voltage U_{high}, the current stress of the power semiconductors is rather high. In addition, this converter requires a complicate control scheme to balance the flying-capacitor voltage. The interleaved bidirectional DC-DC

Tab. 1 Comparisons among the proposed and the other bidirectional solutions

Bidirectional Solutions	Voltage Gain	Amount of Semiconductors	Amount of Inductors	Maximum Voltage Stress of Semiconductors	Inductor Currents Balancing
Converter in [14]	$U_{low}/(1-d)$	4	1	$U_{high}/2$	-
Converter in [20]	$U_{low}/(1-d)$	4	2	U_{high}	YES
Converter in [25]	$3U_{low}/(1-d)$	5	2	$2U_{high}/3$	When $D_b=2D_a$
Converter in [26]	$2U_{low}/(1-d)$	4	2	U_{high}	YES
Converter in [27]	$U_{low}/(1-d)^2$	4	2	$U_{high}+ U_{high}(1-d)$	When $d=0.5$
Proposed converter	$2U_{low}/(1-d)$	5	2	$U_{high}/2$	YES

converter in [20] can reduce the current ripples in the low-voltage side, but it still has the disadvantages including the small voltage gain range and the high voltage stress across the power semiconductors. The interleaved bidirectional DC-DC converters in [25] -[27] have achieved a high voltage-gain, but the maximum voltage stress across the semiconductors of these converters are $2U_{high}/3$, U_{high} and $U_{high}+ U_{high}(1-d)$ respectively, rather than $U_{high}/2$, which will increase the switching losses and reduce the conversion efficiency. Besides, the converter in [27] can only achieve the inductor currents balance when the duty cycles are $d=0.5$, and the inductor currents of the converter in [25] are unbalanced when D_b is not equal to $2D_a$. Regarding the proposed interleaved bidirectional DC-DC converter, the number of main components is equal to that of the converter in [25] , the voltage stress across all semiconductors and capacitors is $U_{high}/2$, and its voltage gain is higher than that in [14] and [20] . In addition, the inductor currents and the capacitor voltage self-balances can also be obtained within the full duty cycle range, in both step-up and step-down modes.

A. Small-signal modeling

It is assumed that the power semiconductors, the inductors, and the capacitors are all ideal. Then, the average model and the small-signal model can be obtained by using the state-space averaging method. According to Fig. 3(c)-(d) in the step-up mode (or Fig. 5(c)-(d) in the step-down mode), C_1 and C_3 are connected in parallel when Q_2 and Q_5 turn on, and Q_3 turns off. It means the voltages across C_1 and C_3 are equal. So, there is an invalid state variable. By considering the equivalent series resistance (e.g. $r=0.23\Omega$ for C_1), the coupling between the capacitors can be removed to avoid the invalid state variables.

(1) Small-signal modeling in the step-up mode

When the proposed bidirectional converter operates in the step-up mode in the range $0<d_{Boost}<0.5$, the main power semiconductors Q_1 and Q_2 have three effective switching states: S_1S_2=[10, 00, 01]. $u_{low}(t)$, $u_{high}(t)$, and $d_1(t)$, $d_2(t)$ are the input variable, the output variable and the control variables respectively. $i_{L1}(t)$, $i_{L2}(t)$, $u_{C1}(t)$, $u_{C2}(t)$ and $u_{C3}(t)$ are the state variables. When S_1S_2=10, the converter operates in **Mode I** (as shown in Fig. 3(a)), and its operating time is $d_1(t)\times T_s$. So, the state space average model can be obtained as follows

$$\begin{cases}\begin{bmatrix}\frac{di_{L1}(t)}{dt}\\ \frac{di_{L2}(t)}{dt}\\ \frac{du_{C1}(t)}{dt}\\ \frac{du_{C2}(t)}{dt}\\ \frac{du_{C3}(t)}{dt}\end{bmatrix}=\begin{bmatrix}0&0&0&0&0\\0&0&-\frac{1}{L_2}&0&0\\0&\frac{1}{C_1}&0&0&0\\0&0&0&-\frac{1}{C_2R_{L\text{-}Boost}}&-\frac{1}{C_2R_{L\text{-}Boost}}\\0&0&0&-\frac{1}{C_3R_{L\text{-}Boost}}&-\frac{1}{C_3R_{L\text{-}Boost}}\end{bmatrix}\begin{bmatrix}i_{L1}(t)\\ i_{L2}(t)\\ u_{C1}(t)\\ u_{C2}(t)\\ u_{C3}(t)\end{bmatrix}+\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_2}\\0\\0\\0\end{bmatrix}u_{low}(t)\\ u_{high}(t)=\begin{bmatrix}0&0&0&1&1\end{bmatrix}\begin{bmatrix}i_{L1}(t)&i_{L2}(t)&u_{C1}(t)&u_{C2}(t)&u_{C3}(t)\end{bmatrix}^T\end{cases}\tag{22}$$

where $R_{L\text{-}Boost}$ is the equivalent load resistance in the step-up mode. When S_1S_2=00, the converter is operating in **Mode II** (as shown in Fig. 3(b)), and its operating time is $[1-d_1(t)-d_2(t)]\times T_s$. The state space average model can be written as

$$\begin{cases}\begin{bmatrix}\frac{di_{L1}(t)}{dt}\\ \frac{di_{L2}(t)}{dt}\\ \frac{du_{C1}(t)}{dt}\\ \frac{du_{C2}(t)}{dt}\\ \frac{du_{C3}(t)}{dt}\end{bmatrix}=\begin{bmatrix}0&0&0&-\frac{1}{L_1}&0\\0&0&-\frac{1}{L_2}&0&0\\0&\frac{1}{C_1}&0&0&0\\\frac{1}{C_2}&0&0&-\frac{1}{C_2R_{L\text{-}Boost}}&-\frac{1}{C_2R_{L\text{-}Boost}}\\0&0&0&-\frac{1}{C_3R_{L\text{-}Boost}}&-\frac{1}{C_3R_{L\text{-}Boost}}\end{bmatrix}\begin{bmatrix}i_{L1}(t)\\ i_{L2}(t)\\ u_{C1}(t)\\ u_{C2}(t)\\ u_{C3}(t)\end{bmatrix}+\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_2}\\0\\0\\0\end{bmatrix}u_{low}(t)\\ u_{high}(t)=\begin{bmatrix}0&0&0&1&1\end{bmatrix}\begin{bmatrix}i_{L1}(t)&i_{L2}(t)&u_{C1}(t)&u_{C2}(t)&u_{C3}(t)\end{bmatrix}^T\end{cases}\tag{23}$$

When S_1S_2=01, the converter operates in **Mode III** (as shown in Fig. 3(c)), and its operating time is $d_2(t)\times T_s$. The state space average model can be achieved as

$$\begin{cases}\begin{bmatrix}\frac{di_{L1}(t)}{dt}\\ \frac{di_{L2}(t)}{dt}\\ \frac{du_{C1}(t)}{dt}\\ \frac{du_{C2}(t)}{dt}\\ \frac{du_{C3}(t)}{dt}\end{bmatrix}=\begin{bmatrix}0&0&0&-\frac{1}{L_1}&0\\0&0&0&0&0\\0&0&-\frac{1}{C_1r}&0&\frac{1}{C_1r}\\\frac{1}{C_2}&0&0&-\frac{1}{C_2R_{L\text{-}Boost}}&-\frac{1}{C_2R_{L\text{-}Boost}}\\0&0&\frac{1}{C_3r}&-\frac{1}{C_3R_{L\text{-}Boost}}&-\frac{1}{C_3r}-\frac{1}{C_3R_{L\text{-}Boost}}\end{bmatrix}\begin{bmatrix}i_{L1}(t)\\ i_{L2}(t)\\ u_{C1}(t)\\ u_{C2}(t)\\ u_{C3}(t)\end{bmatrix}+\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_2}\\0\\0\\0\end{bmatrix}u_{low}(t)\\ u_{high}(t)=\begin{bmatrix}0&0&0&1&1\end{bmatrix}\begin{bmatrix}i_{L1}(t)&i_{L2}(t)&u_{C1}(t)&u_{C2}(t)&u_{C3}(t)\end{bmatrix}^T\end{cases}\tag{24}$$

Combining (22) and (23) with (24), the average model of the converter can be obtained as:

$$\begin{cases}\begin{bmatrix}\frac{di_{L1}(t)}{dt}\\ \frac{di_{L2}(t)}{dt}\\ \frac{du_{C1}(t)}{dt}\\ \frac{du_{C2}(t)}{dt}\\ \frac{du_{C3}(t)}{dt}\end{bmatrix}=\begin{bmatrix}0&0&0&-\frac{1-d_1(t)}{L_1}&0\\0&0&-\frac{1-d_2(t)}{L_2}&0&0\\0&\frac{1-d_2(t)}{C_1}&-\frac{d_2(t)}{C_1r}&0&\frac{d_2(t)}{C_1r}\\\frac{1-d_1(t)}{C_2}&0&0&-\frac{1}{C_2R_{L\text{-}Boost}}&-\frac{1}{C_2R_{L\text{-}Boost}}\\0&0&\frac{d_2(t)}{C_3r}&-\frac{1}{C_3R_{L\text{-}Boost}}&-\frac{d_2(t)}{C_3r}-\frac{1}{C_3R_{L\text{-}Boost}}\end{bmatrix}\begin{bmatrix}i_{L1}(t)\\ i_{L2}(t)\\ u_{C1}(t)\\ u_{C2}(t)\\ u_{C3}(t)\end{bmatrix}+\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_2}\\0\\0\\0\end{bmatrix}u_{low}(t)\\ u_{high}(t)=\begin{bmatrix}0&0&0&1&1\end{bmatrix}\begin{bmatrix}i_{L1}(t)&i_{L2}(t)&u_{C1}(t)&u_{C2}(t)&u_{C3}(t)\end{bmatrix}^T\end{cases}\tag{25}$$

In the duty cycle range $0.5<d_{Boost}<1$, the main power semiconductors Q_1 and Q_2 also have three effective switching

states: S_1S_2=[10, 11, 01], and the converter is operating in **Mode I**, **Mode IV** and **Mode III** (as shown in Fig. 3). Their corresponding operating times are $[1\text{-}d_2(t)] \times T_s$, $[d_1(t)+d_2(t)\text{-}1] \times T_s$ and $[1\text{-}d_1(t)] \times T_s$, respectively. Similarly, the corresponding average model of the proposed converter within the duty cycle range $0.5 \le d_{Boost} < 1$ can also be obtained, which is the same as that within the duty cycle range $0 < d_{Boost} < 0.5$. Assuming that $d_1=d_2=d_{Boost}$, the state variables, the input variable, the output variable and the control variable can be described by using the small-signal disturbance variables as:

$$\begin{cases} i_{L1}(t)=I_{L1}+\hat{i}_{L1}(t) \\ i_{L2}(t)=I_{L2}+\hat{i}_{L2}(t) \\ u_{C1}(t)=U_{C1}+\hat{u}_{C1}(t) \\ u_{C2}(t)=U_{C2}+\hat{u}_{C2}(t) \\ u_{C3}(t)=U_{C3}+\hat{u}_{C3}(t) \\ u_{low}(t)=U_{low}+\hat{u}_{low}(t) \\ u_{high}(t)=U_{high}+\hat{u}_{high}(t) \\ d_1(t)=d_2(t)=d_{Boost}(t)=D_{Boost}+\hat{d}_{Boost}(t) \end{cases} \tag{26}$$

where I_{L1}, I_{L2}, U_{C1}, U_{C2}, U_{C3}, U_{low}, U_{high} and D_{Boost} are the steady state components, $\hat{i}_{L1}(t)$, $\hat{i}_{L2}(t)$, $\hat{u}_{C1}(t)$, $\hat{u}_{C2}(t)$, $\hat{u}_{C3}(t)$, $\hat{u}_{low}(t)$, $\hat{u}_{high}(t)$ and $\hat{d}_{Boost}(t)$ are the corresponding small-signal disturbance variables. As a result, the small-signal model of the converter can be written as

$$\begin{cases} \begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{u}_{C1}(t)}{dt} \\ \frac{d\hat{u}_{C2}(t)}{dt} \\ \frac{d\hat{u}_{C3}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -\frac{1-D_{Boost}}{L_1} & 0 \\ 0 & 0 & -\frac{1-D_{Boost}}{L_2} & 0 & 0 \\ 0 & \frac{1-D_{Boost}}{C_1} & -\frac{D_{Boost}}{C_1 r} & 0 & \frac{D_{Boost}}{C_1 r} \\ \frac{1-D_{Boost}}{C_2} & 0 & 0 & -\frac{1}{C_2 R_{L\text{-}Boost}} & -\frac{1}{C_2 R_{L\text{-}Boost}} \\ 0 & 0 & \frac{D_{Boost}}{C_3 r} & -\frac{1}{C_3 R_{L\text{-}Boost}} & -\frac{D_{Boost}}{C_3 r}-\frac{1}{C_3 R_{L\text{-}Boost}} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{u}_{low}(t) \\ \quad + \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & -\frac{1}{C_1} & -\frac{1}{C_1 r} & 0 & \frac{1}{C_1 r} \\ -\frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_3 r} & 0 & -\frac{1}{C_3 r} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ U_{C1} \\ U_{C2} \\ U_{C3} \end{bmatrix} \hat{d}_{Boost}(t) \\ \hat{u}_{high}(t)=\begin{bmatrix} 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) & \hat{i}_{L2}(t) & \hat{u}_{C1}(t) & \hat{u}_{C2}(t) & \hat{u}_{C3}(t) \end{bmatrix}^T \end{cases} \tag{27}$$

According to (27) and the experimental parameters in Tab. 2, when the input voltage is U_{low}=50V, the control-to-output transfer function in the step-up mode can be achieved from the time domain to the complex frequency domain as

$$G_{u_{high}d_{Boost}}(s)=\left.\frac{\hat{u}_{high}(s)}{\hat{d}_{Boost}(s)}\right|_{\hat{u}_{low}(s)=0} = \frac{-2.6\times10^{-11}s^4-1.2\times10^{-7}s^3+7\times10^{-3}s^2+1.5\times10^{-2}s+1597}{1.3\times10^{-15}s^5+1.7\times10^{-11}s^4+1.2\times10^{-9}s^3+8.7\times10^{-6}s^2+2.3\times10^{-4}s+1} \tag{28}$$

(2) Small-signal modeling in the step-down mode

When the proposed bidirectional converter operates in the step-down mode in the duty cycle range $0 < d_{Buck} < 0.5$, the main power semiconductors Q_3, Q_4 and Q_5 have three effective switching states: $S_3S_4S_5$=[100, 001, 011]. $u_{high}(t)$, $u_{low}(t)$, and $d_3(t)$, $d_4(t)$, $d_5(t)$ are the input variable, the output variable and the control variables respectively. $i_{L1}(t)$, $i_{L2}(t)$, $u_{C1}(t)$, $u_{C2}(t)$ and $u_{C3}(t)$ are the state variables. In addition, C_2 and C_3 are connected in series, then connected with the DC source U_{high} in parallel. So, the equivalent series resistance (e.g. r_1=0.1Ω for the DC source U_{high}) is considered to avoid the invalid state variables. When $S_3S_4S_5$=100, the converter is operating in **Mode I** (as shown in Fig. 5(a)), and its operating time is $d_3(t) \times T_s$. The state space average model can be obtained as follows

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{low}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 & -\frac{1}{L_2} \\ 0 & -\frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_2 r_1} & -\frac{1}{C_2 r_1} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_3 r_1} & -\frac{1}{C_3 r_1} & 0 \\ \frac{1}{C_{low}} & \frac{1}{C_{low}} & 0 & 0 & 0 & -\frac{1}{R_{L\text{-}Buck} C_{low}} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{low}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{C_2 r_1} \\ \frac{1}{C_3 r_1} \\ 0 \end{bmatrix} u_{high}(t) \tag{29}$$

where $R_{L\text{-}Buck}$ is the equivalent load resistance in the step-down mode. When $S_3S_4S_5$=011, the converter operates in **Mode III** (as shown in Fig. 5(c)), and its operating time is $d_4(t) \times T_s$. So, the state space average model can be written as

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{low}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & -\frac{1}{C_1 r} & 0 & \frac{1}{C_1 r} & 0 \\ -\frac{1}{C_2} & 0 & 0 & -\frac{1}{C_2 r_1} & -\frac{1}{C_2 r_1} & 0 \\ 0 & 0 & \frac{1}{C_3 r} & -\frac{1}{C_3 r_1} & -\frac{1}{C_3 r}-\frac{1}{C_3 r_1} & 0 \\ \frac{1}{C_{low}} & \frac{1}{C_{low}} & 0 & 0 & 0 & -\frac{1}{R_{L\text{-}Buck} C_{low}} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{low}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{C_2 r_1} \\ \frac{1}{C_3 r_1} \\ 0 \end{bmatrix} u_{high}(t) \tag{30}$$

When $S_3S_4S_5$=001, the converter is operating in **Mode IV** (as shown in Fig. 5(d)), and its operating time is $[1\text{-}d_3(t)\text{-}d_4(t)] \times T_s$. The state space average model can be achieved as

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{low}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & -\frac{1}{C_1 r} & 0 & \frac{1}{C_1 r} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_2 r_1} & -\frac{1}{C_2 r_1} & 0 \\ 0 & 0 & \frac{1}{C_3 r} & -\frac{1}{C_3 r_1} & -\frac{1}{C_3 r}-\frac{1}{C_3 r_1} & 0 \\ \frac{1}{C_{low}} & \frac{1}{C_{low}} & 0 & 0 & 0 & -\frac{1}{R_{L\text{-}Buck} C_{low}} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{low}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{C_2 r_1} \\ \frac{1}{C_3 r_1} \\ 0 \end{bmatrix} u_{high}(t) \tag{31}$$

Combining (29), and (30) with (31), the average model of the converter can be obtained as:

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{du_{C1}(t)}{dt} \\ \frac{du_{C2}(t)}{dt} \\ \frac{du_{C3}(t)}{dt} \\ \frac{du_{low}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{d_4(t)}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & 0 & \frac{d_3(t)}{L_2} & 0 & 0 & -\frac{1}{L_2} \\ 0 & -\frac{d_3(t)}{C_1} & -\frac{1-d_3(t)}{C_1 r} & 0 & \frac{1-d_3(t)}{C_1 r} & 0 \\ -\frac{d_4(t)}{C_2} & 0 & 0 & -\frac{1}{C_2 r_1} & -\frac{1}{C_2 r_1} & 0 \\ 0 & 0 & \frac{1-d_3(t)}{C_3 r} & -\frac{1}{C_3 r_1} & -\frac{1-d_3(t)}{C_3 r}-\frac{1}{C_3 r_1} & 0 \\ \frac{1}{C_{low}} & \frac{1}{C_{low}} & 0 & 0 & 0 & -\frac{1}{R_{L\text{-}Buck} C_{low}} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ u_{C1}(t) \\ u_{C2}(t) \\ u_{C3}(t) \\ u_{low}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{C_2 r_1} \\ \frac{1}{C_3 r_1} \\ 0 \end{bmatrix} u_{high}(t) \tag{32}$$

In the duty cycle range $0.5 < d_{Buck} < 1$, the main power semiconductors Q_3, Q_4 and Q_5 also have three effective switching states: $S_3S_4S_5$=[100, 110, 011], the converter is operating in **Mode I**, **Mode II** and **Mode III** (as shown in Fig.

5), and their operating times are $[1-d_4(t)] \times T_s$, $[d_3(t)+d_4(t)-1] \times T_s$ and $[1-d_3(t)] \times T_s$, respectively. In a similar way, the corresponding average models of the proposed converter within the duty cycle range $0.5 \le d_{Buck} < 1$ can also be obtained, which are the same as those within the duty cycle range $0 < d_{Buck} < 0.5$. Assuming that $d_3=d_4=d_{Buck}$, the state variables, the input variable, the output variable and the control variables can be described by using the small-signal disturbance variables as:

$$\begin{cases} i_{L1}(t)=I_{L1}+\hat{i}_{L1}(t) \\ i_{L2}(t)=I_{L2}+\hat{i}_{L2}(t) \\ u_{C1}(t)=U_{C1}+\hat{u}_{C1}(t) \\ u_{C2}(t)=U_{C2}+\hat{u}_{C2}(t) \\ u_{C3}(t)=U_{C3}+\hat{u}_{C3}(t) \\ u_{high}(t)=U_{high}+\hat{u}_{high}(t) \\ u_{low}(t)=U_{low}+\hat{u}_{low}(t) \\ d_3(t)=d_4(t)=d_{Buck}(t)=D_{Buck}+\hat{d}_{Buck}(t) \end{cases} \tag{33}$$

where I_{L1}, I_{L2}, U_{C1}, U_{C2}, U_{C3}, U_{high}, U_{low} and D_{Buck} are the steady state components, $\hat{i}_{L1}(t)$, $\hat{i}_{L2}(t)$, $\hat{u}_{C1}(t)$, $\hat{u}_{C2}(t)$, $\hat{u}_{C3}(t)$, $\hat{u}_{high}(t)$ $\hat{u}_{low}(t)$ and $\hat{d}_{Buck}(t)$ are the corresponding small-signal disturbance variables. As a result, the small-signal model of the converter can be written as

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{u}_{C1}(t)}{dt} \\ \frac{d\hat{u}_{C2}(t)}{dt} \\ \frac{d\hat{u}_{C3}(t)}{dt} \\ \frac{d\hat{u}_{low}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{D_{Buck}}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & 0 & \frac{D_{Buck}}{L_2} & 0 & 0 & -\frac{1}{L_2} \\ 0 & -\frac{D_{Buck}}{C_1} & -\frac{1-D_{Buck}}{C_1 r} & 0 & \frac{1-D_{Buck}}{C_1 r} & 0 \\ -\frac{D_{Buck}}{C_2} & 0 & 0 & -\frac{1}{C_2 r_1} & -\frac{1}{C_2 r_1} & 0 \\ 0 & 0 & \frac{1-D_{Buck}}{C_3 r} & -\frac{1}{C_3 r_1} & -\frac{1-D_{Buck}}{C_3 r}-\frac{1}{C_3 r_1} & 0 \\ \frac{1}{C_{low}} & \frac{1}{C_{low}} & 0 & 0 & 0 & -\frac{1}{R_{L\text{-}Buck} C_{low}} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) \\ \hat{u}_{low}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{C_2 r_1} \\ \frac{1}{C_3 r_1} \\ 0 \end{bmatrix} \hat{u}_{high}(t) + \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & \frac{1}{C_1 r} & 0 & -\frac{1}{C_1 r} & 0 \\ -\frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_3 r} & 0 & \frac{1}{C_3 r} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L1}(t) \\ I_{L2}(t) \\ U_{C1}(t) \\ U_{C2}(t) \\ U_{C3}(t) \\ U_{low}(t) \end{bmatrix} \hat{d}_{Buck}(t) \tag{34}$$

In terms of (34) and the experimental parameters in Tab. 2, when the output voltage is U_{low}=50V, the control-to-output transfer function in the step-down mode can be achieved from the time domain to the complex frequency domain as

$$G_{u_{low} d_{Buck}}(s) = \left. \frac{\hat{u}_{low}(s)}{\hat{d}_{Buck}(s)} \right|_{u_{high}(s)=0} = \frac{2.4\times10^{-12}s^4+1.2\times10^{-7}s^3+8.7\times10^{-4}s^2+3.1\times10^{-2}s+199}{1.1\times10^{-21}s^6+5.7\times10^{-17}s^5+4.5\times10^{-13}s^4+9.5\times10^{-10}s^3+4.5\times10^{-6}s^2+2.3\times10^{-4}s+1} \tag{35}$$

V. Experimental Results and Ayalysis

In order to verify the feasibility of the proposed converter, a 1kW experimental prototype of the interleaved switched-capacitor bidirectional DC-DC converter is developed, which is shown in Fig. 9. The experiment parameters are shown in Tab. 2.

Fig. 9 The experimental prototype of the interleaved switched-capacitor bidirectional DC-DC converter.

Tab. 2 Experiment parameters.

Parameters	Values
Rated power P_n	1 kW
Storage/filter capacitor C_{low}	520 μF
Switched-capacitors C_1, C_2 and C_3	520 μF
Storage/filter inductor L_1	353 μH
Storage/filter inductor L_2	347 μH
High voltage side U_{high}	400 V
Low voltage side U_{low}	50~120 V
Switching frequency f_s	20 kHz
Power semiconductors Q_1~Q_5	IXTK 102N30P

A. *Experimental results in the step-up mode*

The voltage waveforms of the main and slave power semiconductors of the proposed converter in the step-up operation mode are shown in Fig. 10 and Fig. 11, respectively. The PWM voltage of each power semiconductors is 200V, namely half of U_{high}, which validates the analysis in Section IV. In addition, the current flows through the anti-parallel diodes of Q_3, Q_4 and Q_5 during the dead time, and the blocking voltages of Q_3, Q_4 and Q_5 are around zero. Otherwise, the controlled MOSFETs Q_3, Q_4 and Q_5 are turned on and turned off with ZVS by the synchronous rectification, e.g. the gate signal S_4 and the voltage stress of Q_4 as shown in Fig. 11.

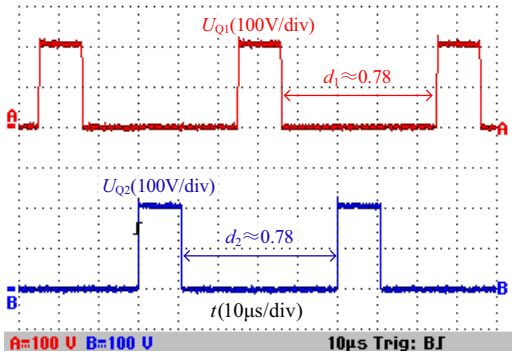


Fig. 10 The PWM voltages of power semiconductors Q_1 and Q_2.

When the input voltage is U_{low}=50V, the output voltage U_{high} and the voltage across C_3 are shown in Fig. 12. According to Fig. 12, the voltage across C_3 is 200V (i.e. half of the output voltage). In addition, the potential difference between the input and output side grounds of this converter is just the voltage across C_3 (i.e. the constant voltage 200V with very small ripple), rather than the PWM voltage.

The input and inductor currents of the proposed converter in the step-up operation mode are shown in Fig. 13. The inductor currents i_{L1} and i_{L2} are shown in Fig. 13(a). Fig. 13(b) shows the

input current i_{low} and the inductor current i_{L1}. According to Fig. 13, the current ripple rates of i_{L1} and i_{L2} are about 49%, and the current ripple rate of the input current is only 17.6%. According to (19), the ripple rate of i_{L1} and i_{L2} is 53.57%, and the current ripple rate of i_{low} is 17.86% theoretically, which agree with the experimental results. The conclusion that the current ripple of i_{low} is much lower than the current ripple of i_{L1} and i_{L2} can be obtained.

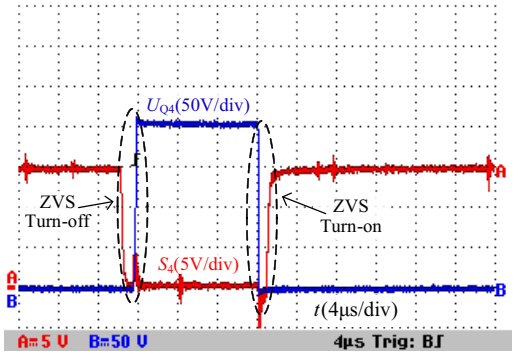


Fig. 11 Gate signal and voltage stress across synchronous rectification power switch Q_4.

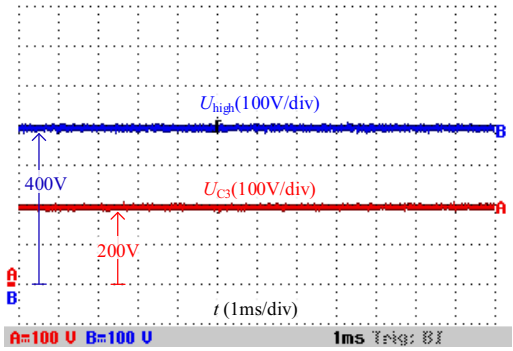
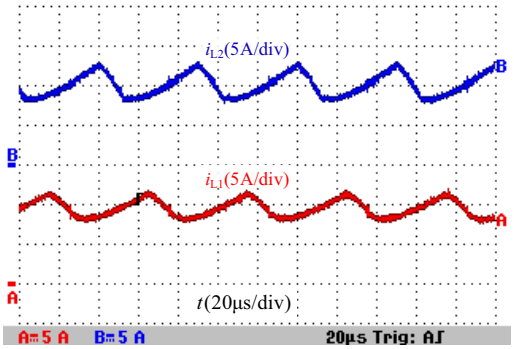


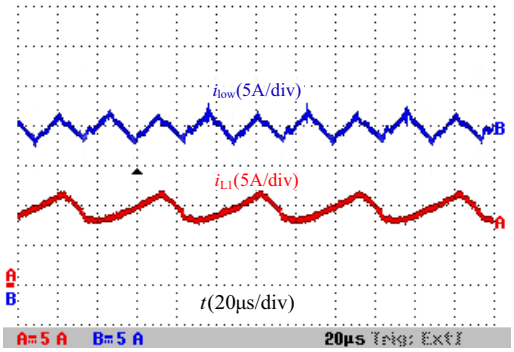
Fig. 12 Voltages U_{high} and U_{C3} when the input voltage is U_{low}=50V.

The input and capacitor current waveforms of the proposed converter operating in the step-up mode are shown in Fig. 14, when the input voltage is U_{low}=50V and the output voltage is U_{high}=400V. From Fig. 14, it can be observed that the amplitude of i_{C1} is higher than those of i_{C2} and i_{C3}, and the maximum charge current of C_1 is nearly equal to half of that of i_{low}. According to Fig. 3(a), the current flowing through Q_3 is the charging current of C_1. Thus, the conclusion that the current stress of Q_3 is reduced to half of the input current can be obtained, which agrees with the theoretical analysis previously mentioned in (16). Besides, the average amplitude of the charging or the discharging current of C_3 is the smallest one (less than 2A), which is conducive to reduce the voltage fluctuations between the input and output side grounds of this converter.

In the step-up mode, the output voltage can stay constant around the reference voltage 400V with the action of the voltage control loop. Fig. 15 illustrates the dynamical responses of the output voltage and the input voltage when the input voltage is changed from 120V to 50V continuously. According to Fig. 15, when the input voltage U_{low} varies continuously from 120V to 50V, the output voltage still stays around 400V, which means the proposed converter can obtain a wide voltage-gain range varying from 3.3 to 8.

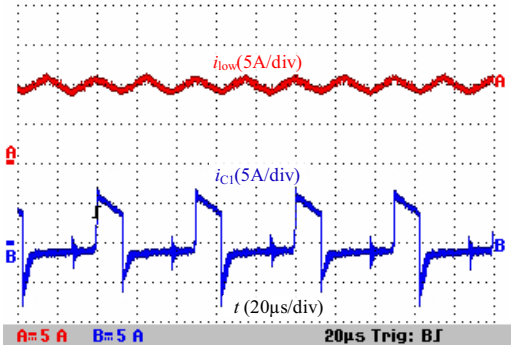


(a)

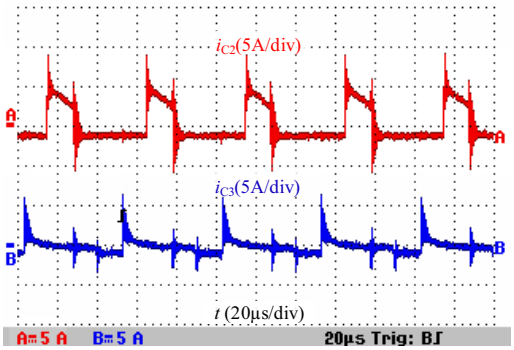


(b)

Fig. 13 The input current i_{low}, inductor currents i_{L1} and i_{L2} when the input voltage is U_{low}=50V and the output voltage is U_{high}=400V. (a) Inductor currents i_{L1} and i_{L2}. (b) The input current i_{low} and the inductor current i_{L1}.



(a)



(b)

Fig. 14 The input current i_{low}, capacitor currents i_{C1}, i_{C2} and i_{C3} in the step-up mode. (a) The input current i_{low} and the capacitor current i_{C1}. (b) Capacitor currents i_{C2} and i_{C3}.

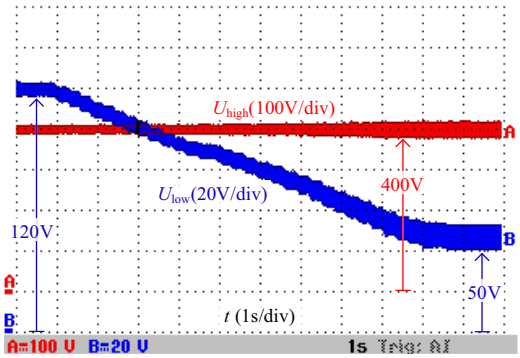


Fig. 15 The output voltage and the wide-range changed input voltage from 120V to 50V in the step-up mode.

B. Experimental results in the step-down mode

The voltage waveforms of the main and slave power semiconductors of the proposed converter in the step-down operation mode are shown in Fig. 16 and Fig. 17 respectively. Similar to the experimental results in the step-up mode, the PWM voltage of each power semiconductors is 200V, which is half of the high-voltage side U_{high}. In addition, the slave power semiconductors Q_1 and Q_2 are also turned on and turned off with ZVS in the synchronous rectification operation, and the gate signal S_1 and the voltage stress of Q_1 are shown in Fig. 17.

When the output voltage is U_{low}=50V, the input voltage U_{high} and the voltage across C_3 are shown in Fig. 18. According to Fig. 18, the voltage across C_3 is also at constant 200V (i.e. half of the output voltage). In addition, the potential difference U_{C3} between the input and output side grounds of this converter also has a very small ripple and dv/dt, which is the same as that in the step-up mode.

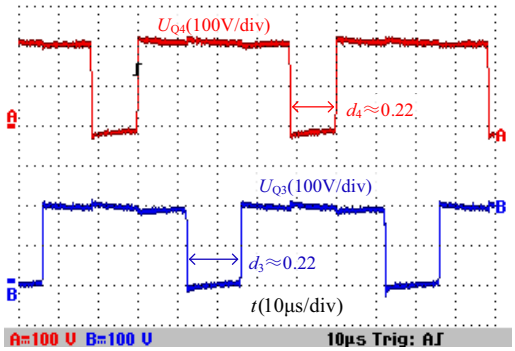


Fig. 16 The PWM voltages of power semiconductors Q_3 and Q_4.

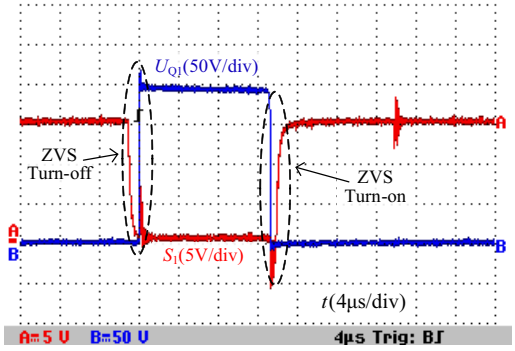


Fig. 17 Gate signal and voltage stress of synchronous rectification power semiconductor Q_1.

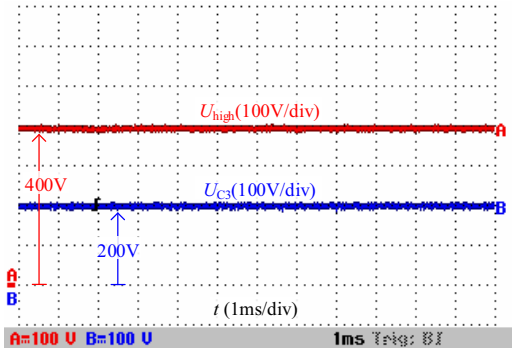
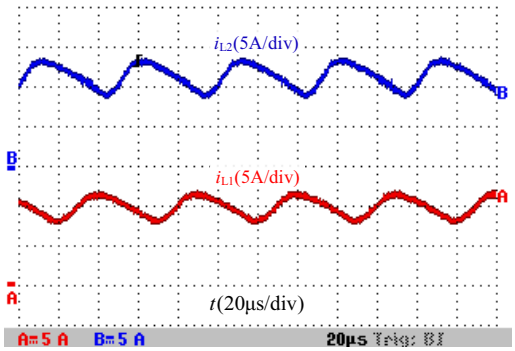
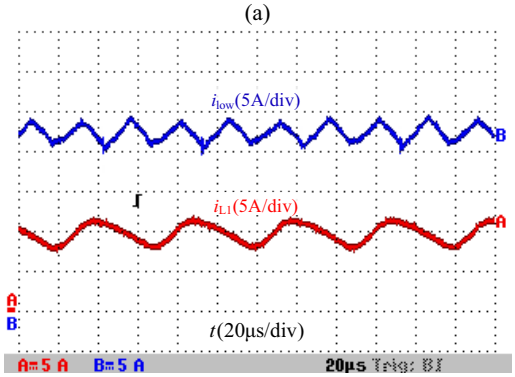


Fig. 18 Voltages U_{high} and U_{C3} when the output voltage is U_{low}=50V.

The output and inductor current waveforms of the proposed converter in the step-down operation mode are shown in Fig. 19. The inductor currents i_{L1} and i_{L2} are shown in Fig. 19(a). Fig. 19(b) shows the output current i_{low} and the inductor current i_{L1}. According to Fig. 19, the current ripple rate of i_{L1} is 46%, and the current ripple rate of i_{L2} is 50.6%. In addition, the current ripple rate of the output current is 17.65%. According to (20), the ripple rate of i_{L1} and i_{L2} is 53.57%, and the ripple rate of i_{low} is 17.86% theoretically, which are in accordance with the experimental results. The conclusion that the current ripple of i_{low} is much lower than the current ripple of i_{L1} and i_{L2} can be obtained.



(a)

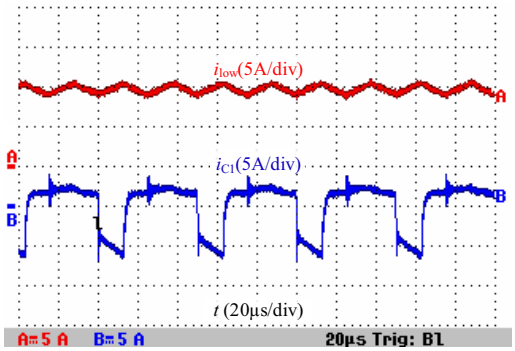


(b)

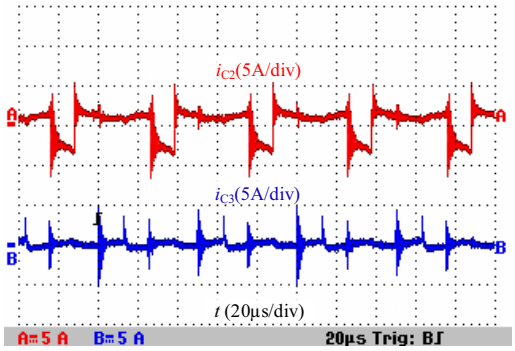
Fig. 19 The output current i_{low}, inductor currents i_{L1} and i_{L2} when the output voltage is U_{low}=50V and the input voltage is U_{high}=400V. (a) Inductor currents i_{L1} and i_{L2}. (b) The output current i_{low} and the inductor current i_{L1}.

Fig. 20 shows the output and capacitor current waveforms of the proposed converter in the step-down mode, when the input voltage is U_{high}=400V and the output voltage is U_{low}=50V. From Fig. 20, it can be seen that the amplitude of i_{C1} is also higher than those of i_{C2} and i_{C3}, and the maximum discharging current of C_1

is also nearly equal to half of that of i_{low}. According to Fig. 5(a), the current flowing through Q_3 is the discharging current of C_1. Thus, the conclusion that the current stress of Q_3 is also reduced to half of the output current can be achieved, which also agrees with the theoretical analysis previously mentioned in (17). Besides, the average amplitude of the charging or the discharging current of C_3 is also the smallest one (less than 2A), which is the same as that in the step-up mode.



(a)



(b)

Fig. 20 The output current i_{low}, capacitor currents i_{C1}, i_{C2} and i_{C3} in the step-down mode. (a) The output current i_{low} and the capacitor current i_{C1}. (b) Capacitor currents i_{C2} and i_{C3}.

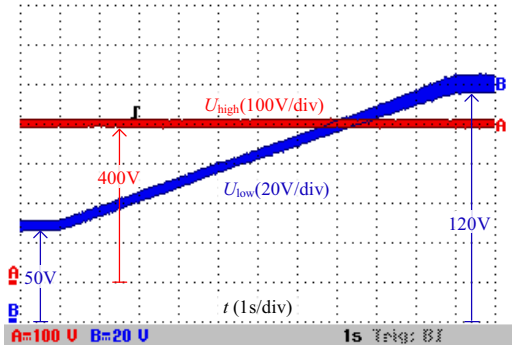


Fig. 21 The input voltage and the wide-range changed output voltage from 50V to 120V in the step-down mode.

Fig. 21 can be used to validate the converter's function of charging the super-capacitors or the batteries. According to Fig. 21, when the input voltage stays around 400V, the output voltage U_{low} varies continuously from 50V to 120V under the control of the voltage loop (i.e. a PI controller), in which the reference voltage is adjusted from 50V to 120V over 10 seconds, while the input voltage keeps at 400V. Therefore, it means the proposed converter can obtain a wide voltage-gain range varying from 1/8 to 1/3.3, and it can charge the super-capacitors or the batteries in a wide terminal voltage range.

C. Bidirectional power flow experiment

Fig. 22 shows the hybrid energy sources storage system, where the super-capacitor bank adopts the super-capacitor of CSDWELL's model MODWJ001PM031Z2. In addition, the battery in the hybrid energy sources is a lithium iron phosphate battery with the rated voltage of 48V. The experimental results of the bidirectional power flow control are shown in Fig. 23.

In the hybrid energy storage sources system shown in Fig. 22, U_{dc} is the DC bus voltage, U_{bat} and I_{bat} are the output voltage and output current of the battery, U_{sc} and I_{sc} are the output voltage and output current of the super-capacitor, and I_{dc} is the load current. In the experiment of the bidirectional power flow control, the output voltage of the battery is about 50V, the output voltage of the super-capacitor is around 40V, and the DC bus power varies with the step changes from 400W to 650W. The interleaved switched-capacitor bidirectional DC-DC converter proposed in this paper is applied to interface the super-capacitor and the DC bus, and it operates according to the control strategy shown in Fig. 7.

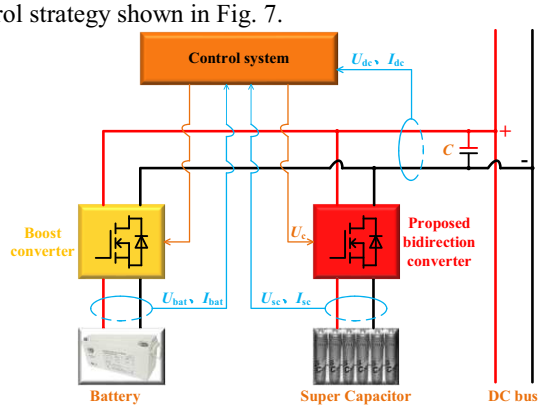


Fig. 22 Hybrid energy sources storage system.

Fig. 23 shows the variations of i_{bat} and i_{sc} during the sudden increase and decrease in the loads of the proposed bidirectional converter, when super-capacitors are operating. According to Fig. 23, when the power required by the DC bus is changed from 400W to 650W with a step change, the control system sets the control signal U_c to "zero". At the same time, the proposed switched-capacitor bidirectional converter responds quickly and operates in the step-up mode. The current I_{sc} increases from zero to 6A in 20ms approximately, and the instantaneous power provided by the super-capacitor is nearly equal to the required power change of the DC bus, avoiding the step change current from the battery, which may shorten the life of the battery. As a result, the current of the battery rises from 8A to 13A gradually, and the current of the super-capacitor falls to zero from I_{sc}=6A. Similarly, when the power required by the DC bus is changed from 650W to 400W with a step change, the control system sets the control signal U_c to "1". At the same time, the proposed switched-capacitor bidirectional converter responds quickly and operates in the step-down mode. The current I_{sc} increases from zero to 6A with the opposite direction in 20ms approximately. As a result, the current from the battery falls from 13A to 8A gradually, and the current of the super-capacitor falls to zero from I_{sc}=-6A.

Fig. 24 shows the variations of i_{bat} and i_{sc} with the same load step change, when super-capacitors are not operating. According to Fig. 24, when the DC bus demand power is changed from 400W to 650W with a step change, the current I_{bat} quickly increases from 8A to 13A with a step change. When the DC bus demand power is changed from 650W to 400W with a step change, the current I_{bat} quickly decreases from 13A to 8A with a step change. It is seen that when the load power varies with a step change, the battery has to tolerate the step change current, and this is easy to cause the impact on the battery itself during the process of the electric vehicle's acceleration and deceleration, and then shorten its service life.

Comparing the experimental results of Fig. 23 and Fig. 24, it is seen that when the DC bus demand power quickly increases or decreases, the proposed switched-capacitor bidirectional converter can respond quickly according to the control signal U_c, and the super-capacitor can compensate (take in and send out) the power gap between the battery and the DC bus side to ensure that the current output from the battery changes more slowly and therefore, avoid reduction of the battery life.

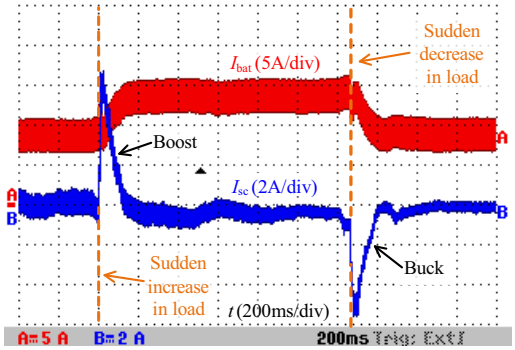


Fig. 23 Experimental results of bidirectional power flow control (super-capacitors are operating).

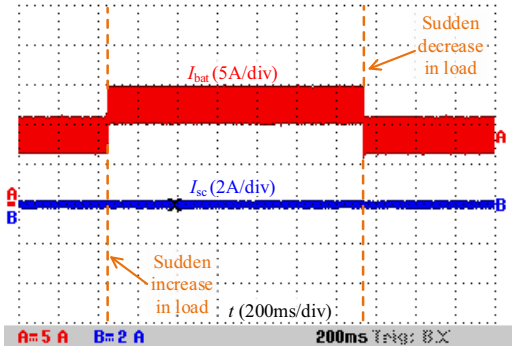


Fig. 24 Experimental results of bidirectional power flow control (super-capacitors are not operating).

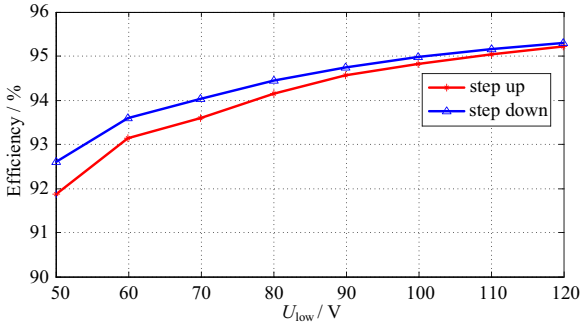


Fig. 25 Efficiencies of the proposed switched-capacitor bidirectional converter in step-up and step-down modes (U_{high}=400V, U_{low}=50V~120 V, P_n=1kW).

The efficiencies of the proposed bidirectional DC-DC converter in the step-up and step-down modes are shown in Fig. 25 when the high-voltage side U_{high} is 400V and the low-voltage side U_{low} varies from 50V to 120V or 120V to 50V continuously. The efficiencies are measured by the power analyzer YOKOGAWA/WT3000. According to Fig. 25, the measured efficiencies are from 91.88% (U_{low}=50V) to 95.21% (U_{low}=120V) in the step-up mode, and from 92.60% (U_{low}=50V) to 95.30% (U_{low}=120V) in the step-down mode. With the constant load P_n=1kW and U_{high}=400V in the step-up/down modes, the effective values of the low side currents increase due to the decrease of the low side voltages (i.e. the increase of the voltage-gain). Therefore, the turn-on/off losses, and the conduction losses of the power semiconductors will raise, as well as the conduction losses of the equivalent series resistors of the circuit. Moreover, the maximum efficiency arrives at 95.21% and 95.30% in the step-up and step-down modes respectively when the low-voltage side U_{low} is 120V, and the efficiency in the step-down mode is slightly higher than that in the step-up mode.

VI. Conclusions

In this paper, an interleaved switched-capacitor bidirectional DC-DC converter has been introduced. The proposed topology can benefit from high step-up/step-down ratio, a wide voltage-gain range and avoiding of the extreme duty cycles. In addition, this converter has the advantages of the low voltage stress of power semiconductors and capacitors, and low current ripples in the low-voltage side. Besides, the slave active power semiconductors allow ZVS turn-on and turn-off, and the efficiency of the converter is improved. The capacitor voltages and the inductor currents can be easily balanced due to the self-balance function. The proposed bidirectional DC-DC converter has good dynamic and steady-state performance and is suitable for the power interface between the low-voltage battery pack and the high-voltage DC bus for various new energy storage systems.

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